Session C4:   **Architectural Synthesis**

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Logic synthesis has been a major research issue in the past decade. Module generators, structural compilers, and a wealth of CAD tools have given sense and real content to the very much sought framework of a Silicon compiler. Plenty of tools are now commercial yet in this Conference one more of them (Frenchip) is being demostrated in world premiere. However still much work needs to be done in assisting and optimizing early phases in the conception of a circuit and at higher levels in the design process. Final performances of the circuit (especially of complex circuits dealing with systems) rely more in these stages than in the logic design and implementation ones. So it pays to devote plenty of attention and effort to them. Above Logic synthesis, High Level synthesis and in particular the very beginning of this process the architectural synthesis from a particular description (behavioral graph, language or schematic), seem to be a key research topic for the nineties. The perception of this reality has been one of the reasons for choosing for this years Conference "Hardware and Software Design Automation" the subtitle "From Specification to Implementation". All authors in this session are very much working in this direction.

Among quite a few papers accepted this year devoted to architectural synthesis, we have gathered in this session four papers related enough as to open the door to a lively discussion among authors and attendees (including the session chairman). Readers interested should be aware that Euromicro 91 features other papers on closely related topics in sessions A4 B4 D4 E4 and F4.

The first paper "A Design Concept for Verified Concurrent Controllers" (M. Schaefer, G. Klein-Hessling, Siemens Corporate R&D) focuses on the subject of specifying, verifying and

implementing controller architectures for those tasks which must be distributed among several cooperating processes in complex systems. Their approach is based on describing a control task with the aid of structured flowcharts.

The second paper "A Prolog Based Design Environment for the High- Level Synthesis of Application-Specific Architectures" (P. Tsanakas, G. Papakonstantinou, S. Kaxiras, National Technical University of Athens) presents a new approach for the systematic design of application-specific architectures. The behavioral specifications are given in an extended version of Prolog that allows the high-level description of algorithms to be implemented in special-purpose VLSI circuits.

The third paper "An Architectural Design Support Environment for High-Performance Digital Systems" (S. Antoniazzi, M. Mastretti, Italtel Central Research Labs) reports on the present status of the Architectural Design Support Environment ADSE, a design tool for application-specific digital systems supporting a quick exploration of alternative architectural styles starting from uncommitted behavioral specifications. Digital systems are described by means of an object-based language called MetaScript.

The fourth paper "Task Level Behavioral Hardware Description" (L. Benders, M. Stevens, Eindhoven University of Technology) defines a synthesizable VHDL subset with constructs focusing on synchronization and communication. With this aim, the VHDL signal concept is replaced by new object types representing mutual exclusion data, communication data and events. At this point the description can be mapped on architecture moduls (and eventually synthesized). A standard IEEE VHDL description is then restored.