# A Low-Power Fully Integrated CMOS RF Receiver for 2.4-GHz-band IEEE 802.15.4 Standard

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***Abstract*—This paper presents a low power 2.4 GHz receiver front-end for 2.4-GHz-band IEEE 802.15.4 standard in 0.18 µm CMOS technology. This receiver adopts a low-IF architecture and comprises a variable gain single-ended low-noise amplifier (LNA), a quadrature passive mixer, a variable gain transimpedance amplifier (TIA) and a complex filter for image rejection. The receiver front-end achieves 42 dB voltage conversion gain, 10.3 dB noise figure (NF), 28 dBc image rejection and -5 dBm input third-order intercept point (IIP3). It only consumes 5.5 mW.**

**Index terms: RF front end, CMOS RFIC, IEEE 802.15.4 receiver, low-noise amplifier (LNA), passive quadrature mixer, complex filter.**

## I. INTRODUCTION

The last decade has seen the rise of CMOS as the choice technology in consumer-based wireless applications. Full system integration continues to be a topic of interest in this research field in order to minimize both the cost and the form-factor of wireless transceivers. In the interests of longer battery life, ultra-low power design has recently become a hot topic for applications such as wireless personal area networks (WPAN), and wireless sensor nodes. The IEEE 802.15.4 standard has been specifically designed to cater to this demand. This standard operates in the 868 MHz/915 MHz/2.4 GHz Industrial, Scientific and Medical (ISM) bands with a data rate varying from 20 to 250 kb/s depending on the operating frequency band.

This paper describes the design and implementation of a low-power fully integrated CMOS RF receiver for 2.4-GHz-band IEEE 802.15.4 standard. The receiver architecture is discussed in Section II. The RF receiver circuit designs are explained in Section III. Section IV summarizes the experimental results of the implemented receiver and, finally, some conclusions are given in Section V.

## II. RECEIVER ARCHITECTURE

Direct conversion architectures (Zero-IF and Low-IF) are known for their suitability for making radios in a single chip. Zero-IF receivers directly down-convert the RF input signal to baseband thus needing only a few components. However, some drawbacks appear: dc offset, 1/f noise, I/Q mismatch, even order distortion and local oscillator (LO) leakage. Alternatively, the low-IF architecture does not exhibit either a severe dc offset or 1/f noise but still possesses the drawback of a restricted image rejection which is carried out by a complex filter. The order of this filter depends on the blocking profile imposed to the receiver.

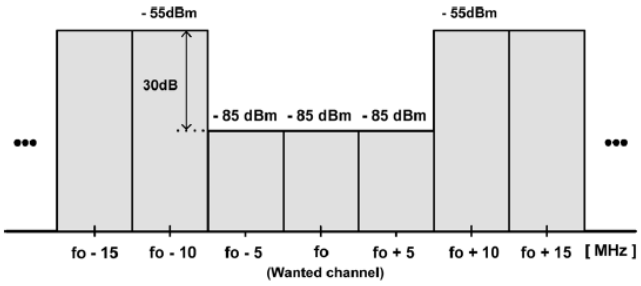


**Figure 1.** Blocking profile in the 2.4-GHz band for ZigBee radio.

Figure 1 shows the blocking profile in the 2.4-GHz band for the IEEE 802.15.4 standard. In this case, the interferers surrounding the desired signal are relatively weak compared with the environment of other radio technologies, (WLAN, GSM, WCDMA, etc.) and the specifications of the image rejection filter are very loose. As a consequence, a number of IEEE 802.15.4 receivers in the literature use a low-IF receiver architecture [1]-[4].

The proposed receiver architecture is shown in Figure 2. The RF input signal is amplified by a LNA and down-converted by a current-mode I/Q mixer. Then, the output current signal is converted to voltage by a transimpedance amplifier (TIA) and filtered by a complex filter to improve the image rejection performance and sensitivity.

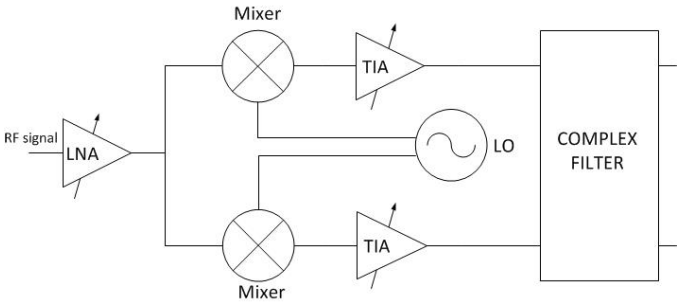


**Figure 2.** System architecture of the proposed receiver.

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## III. CIRCUITS DESIGNS

### A. Low Noise Amplifier

The main goals of the LNA are low noise figure (NF), high gain to sufficiently reduce the NF contribution of the subsequent stages, and high linearity to accommodate high input signal and strong interferences. In addition, the LNA should have a 50-Ω input impedance to match with the output impedance of the off-chip components such as RF bandpass filter or T/R switch.

Figure 3 shows the schematic of the LNA. A single-ended topology has been chosen because it dissipates lower dc current than a differential one and the required input second-order intercept point (IIP2) performance of the IEEE 802.15.4 standard is not as high compared with other wireless communications standards [4].

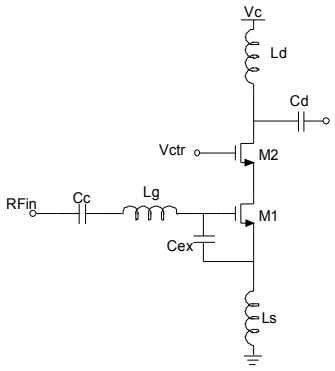


**Figure 3.** Schematic of the Low-Noise Amplifier.

As shown in Figure 3, an inductive degenerated cascode LNA topology is used. This topology is known to provide high gain, low noise and high input/output isolation. In order to achieve simultaneously low noise and input matching, the inductive degeneration technique is used. The addition of $L_s$ generates a real part at the input impedance which reduces the discrepancy between the optimum noise impedance and the LNA input impedance. This is due to the fact that the optimum noise impedance has a real part while without degeneration there is no real part at the input impedance. However, under low power consumption the value needed of this inductance to obtain both noise and input matching is very large. This results in a minimum achievable noise figure of the LNA significantly higher than its $NF_{min}$. This can be solved by including the capacitor $C_{ex}$ as it is shown in Figure 3. By adding this capacitance, one can use lower values of the inductance $L_s$ to achieve simultaneous noise and input matching.

The input impedance of the LNA is given by:

$$Z_{in} = s\cdot\left(L_s + L_g\right) + \frac{1}{s\cdot C_t} + \frac{g_M \cdot L_s}{C_t} \qquad (1)$$

where $C_t$ is the total capacitance between the gate and the source of M1, i.e. $C_{gs} + C_{ex}$. From (1) it can be seen that by including the capacitor $C_{ex}$ the imaginary part of the input impedance changes, allowing smaller values for $L_s$ and $L_g$. This also reduces the parasitic resistance, thus improving the noise figure of the LNA.

In this design, the inductors $L_s$, $L_g$ and $L_d$ are implemented on-chip in order to reduce the off-chip components. This can be done because the noise figure required by the standard is relaxed.

In this topology, the gain control function is implemented by adjusting the bias voltage $V_{ctr}$.

### B. Downconversion Mixer

Figure 4 shows the schematic of the downconversion mixer. A passive double-balanced mixer has been chosen because it dissipates no dc current, provides high linearity and reduces the LO leakage. Also, as no dc current flows through the transistors, the *1/f* noise contribution from the mixers is minimized [5].

The output of the LNA is connected to one terminal of the differential input of the mixer via the coupling capacitor $C_d$, while the second input terminal of the mixer is connected to ac ground through the bypass capacitor $C_{bp}$. This approach maintains most of the advantages of the differential circuitry such as the second-order distortion and the LO leakage, with a negligible gain penalty [1].

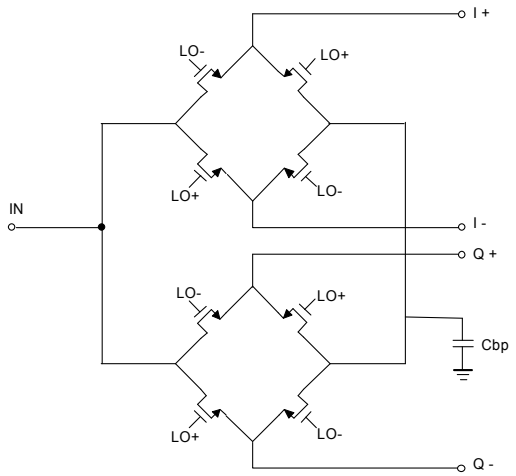


**Figure 4.** Schematic of the downconversion mixer.

There are two parameters that can be modified in this mixer to obtain the best possible performance: the device size and the LO signal characteristics. When low noise performance is desired, the width of the transistors should be large enough to provide a low on-resistance. Also, there is a tradeoff between the mixer noise performance and the gain of the LNA, which has to be considered when sizing the switches. The LNA has a load impedance which is a parallel resonance circuit that consists of a parasitic capacitance and an output inductor. In this case, the inductance must be decreased if the switch capacitance incresases. This has to be done so that the resonance frequency doesn't change. However, this will decrease the gain of the LNA due to the lower load impedance. Also, the dc level of the LO signal will affect the mixer performance because it controls the switching performance.

*C. Transimpedance Amplifier*

The current signal from the mixer is converted to voltage by a TIA. As it can be seen in Figure 5, this amplifier consists of two inverters in parallel (Figure 6) and resistive feedback loops. In order to maintain common-mode voltage stability, the resistors R1 and R2 are used. These resistors produce an effective resistance for differential signals of $R_1R_2/(R_2\text{-}R_1)$. The elimination of the dc offsets produced by the mixer is carried out by a high pass filter formed by this effective resistance and the capacitor C. The increased value of this effective resistance allows the input blocking capacitor to be smaller and, as a consequence, both the noise and area are reduced. In (2) the voltage gain of the amplifier is shown.

$$A_v = \frac{v_{out}}{v_{in}} = 1 - (g_{MN} + g_{MP}) \frac{R_1 \cdot R_2}{(R_2 - R_1)} \qquad (2)$$

As it can be seen, by adjusting the $g_M$ of the inverters the voltage gain can be changed.

To allow the TIA to operate at high and low gain modes, the switches SW1 and SW2 are used in the inverters.

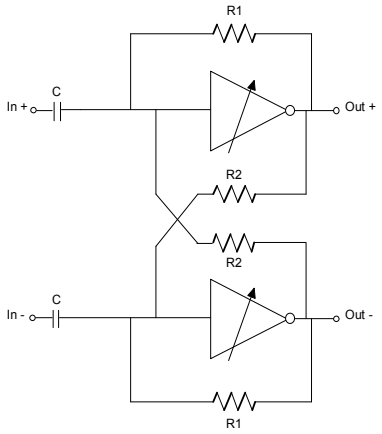


**Figure 5.** Schematic of the TIA.

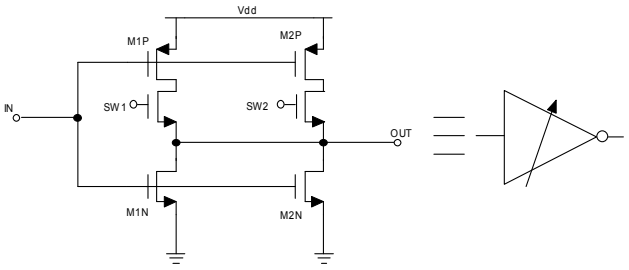


**Figure 6.** Inverter used in the TIA.

*D.* Balanced third-order complex filter

The IEEE 802.15.4 standard requires 0 dB rejection at the adjacent channel (5 MHz) and 30 dB rejection at the alternate channel (10 MHz). This can be accomplished by a Butterworth third order gm-C complex filter. The main advantage of this topology is that the inherent insertion loss of passive filters can be compensated by the transconductance of the input stage. Also, a good trade-off in terms of power, operating frequency and noise can be achieved [6][7].

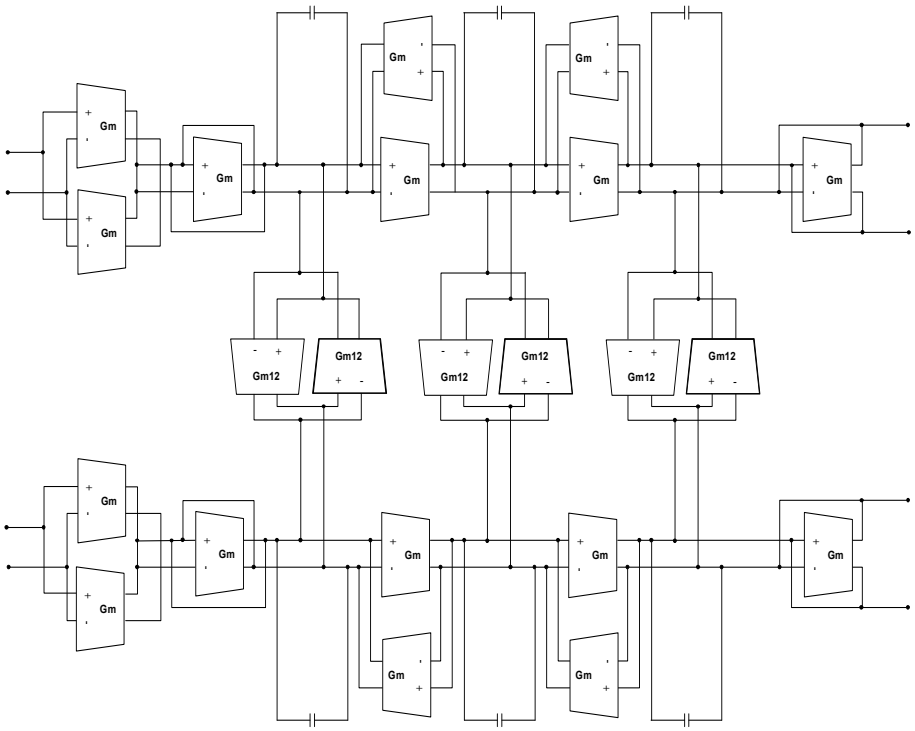


**Figure 7.** Schematic of the complex filter.

The topology of the complex filter is shown in Figure 7. It consist of two Butterworth third order gm-C low-pass filters for the I and Q paths and two crossing extra signal paths per integrator to transform the low-pass prototypes to their band-pass complex counterparts.

In order to reduce the power consumption, inverter based transconductors have been used in the I and Q paths (Figure 8.b). The main issue with this kind of transconductors is the difficulty of setting the dc levels. To maintain the output common mode voltage stability, Nautas' transconductors (Figure 8.a) have been used in the crossing signal paths that connects the I and Q branches [8]. In this type of transconductors, inverters Inv3, Inv4, inv5 and Inv6 are used to maintain common-mode stability and enhance dc gain. Common-mode stability follows if the common-mode gain ($A_{CM}$) is less than unity. On the other hand, if the width of the transistors in Inv4 and Inv5 are designed slightly smaller than those of Inv3 and Inv6 the differential mode gain ($A_{DM}$) is boosted [9].

The frequency response of this filter is shown in Figure 9. As a consequence of both, dispersions in the process of fabrication and variations of the voltage power supply, this frequency response may suffer variations. These deviations can be compensated by controlling the voltage supply of the transconductors with a tuning circuit that controls the voltage supply of both the TIAs and the complex filter transconductors. For this reason those circuits have been designed to work with a 1.4 V voltage supply instead of 1.8 V, which is the voltage supply for the rest of the receiver. In the Nautas' transconductors the voltages Vdd and Vdd' are used for F-tuning and Q-tuning, respectively.

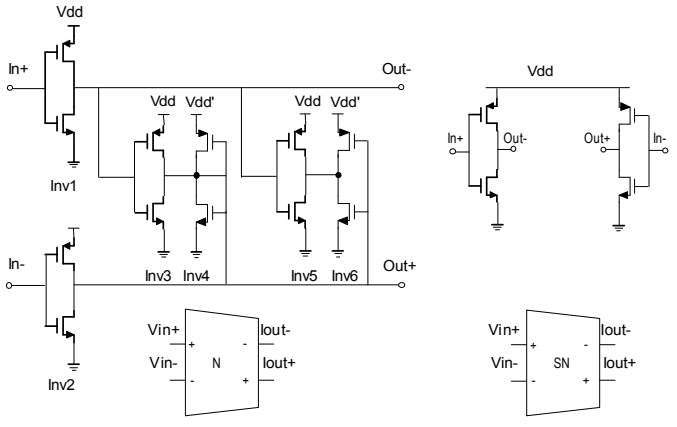


**Figure 8.** (a) Nauta's Transconductor (b) Simplified Nauta's transconductor.

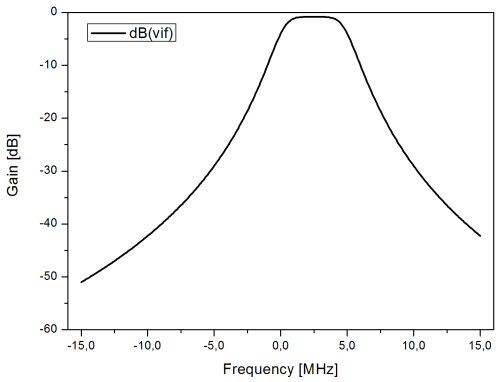


**Figure 9.** Complex filter frequency response

## IV. Simulation Results

The proposed receiver is implemented in a standard 0.18 µm CMOS technology and simulated using Advanced Design System (ADS) software. The total power consumption of the receiver is 5.5 mW – 2.39 mA at 1.8V for the LNA, 60 µA at 1.4 V for the mixer&TIA, and 0.8 mA at 1.4 V for the complex filter.

The input matching of the receiver is shown in Figure 10. It can be observed that for 2.4 GHz the input matching is below -10 dB.

The gain and NF for the entire IEEE 802.15.4 standard band are shown in Figure 11. The noise figure varies from 10.3 dB to 12 dB over the whole band while the gain is almost constant with a value around 42 dB.

The simulated value of the receiver's NF for one channel is shown in Figure 12. The simulation shows a constant value of 10.3 dB approximately, with a high rise at low frequencies due to the 1/f noise. On the other hand, Figure 13 shows the frequency response of the receiver. As can be seen, the maximum gain is over 42 dB and the image rejection of the adjacent channel is 28 dB.

The LNA has a maximum gain of 18 dB and a minimum gain of 4 dB. This is controlled by the LNA's control voltage $V_{ctr}$. As shown in Figure 14, as $V_{ctr}$ increases, the gain also increases, while the NF decreases. In addition, the TIA has a high gain mode of 24 dB and a low gain mode of 1 dB. This is achieved thanks to the switches included in each inverter. In Table I, the total gain and NF of the receiver are shown depending on the gains of the LNA and the TIA. The total gain can be varied from 5 to 42 dB while the NF changes between 10.3 and 43 dB. This increase of the NF at low gains is acceptable because, as the input power increases, so does the tolerable NF. This can be seen in Figure 15, where the tolerable system NF of an IEEE 802.15.4 receiver versus the received signal power is shown [10]. According to the standard, the input signal ranges from a minimum value of -85 dBm (sensitivity) and a maximum value of -20 dBm, which imposes a maximum NF ranging from 15.5 to 78 dB.

*Table I Receiver Gain and Noise Figure for different gain setups*

| LNA gain [dB] | TIA gain [dB] | Receiver Gain [dB] | Receiver NF [dB] |
|---|---|---|---|
| 4 | 1 | 5 | 43 |
| 18 | 1 | 19 | 28 |
| 4 | 24 | 28 | 25 |
| 18 | 24 | 42 | 10.3 |

Finally, the simulated value of the third-order input intercept point ($IIP_3$) at high gain mode is shown in Figure 16. A -5 dBm $IIP_3$ is obtained when two tones at 500 kHz offset from the center of the designed channel are applied at the input.

Table II compares the presented receiver to previously reported IEEE 802.15.4 receivers. It shows that our results are in line with the state-of-the-art of low-power/low-cost front-end receivers.

## V. CONCLUSIONS

A 802.15.4 receiver front-end for 2.4-GHz-band consuming a dc power of 5.5 mW is reported in 0.18-µm CMOS. The receiver adopts a low-IF architecture and comprises a variable gain single-ended LNA, a quadrature passive mixer, a variable gain TIA and a complex filter for image rejection. The receiver shows 42 dB conversion gain with 37 dB gain variation, 10.3 dB NF, 28 dBc image rejection and -5 dBm input (IIP3). The achieved performance exceeds the requirements of 802.15.4, yet performs favorably in terms of high level of integration and low power consumption.

## ACKNOWLEDGMENT

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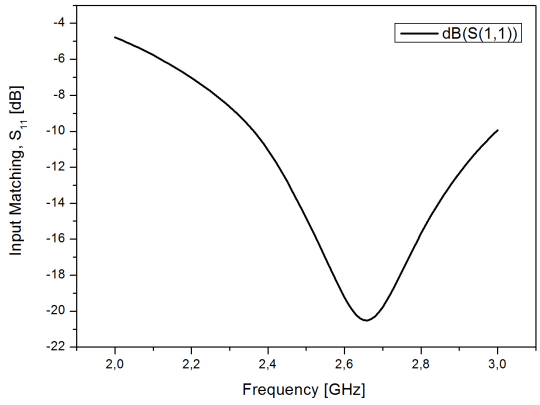


**Figure 10.** Input matching for the receiver

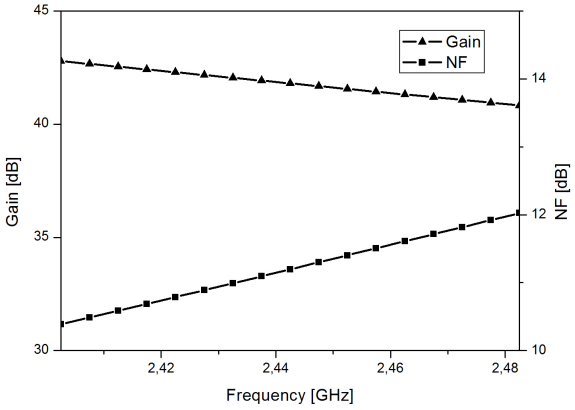


**Figure 11.** Simulated Gain and NF of the receiver over the entire ISM-band

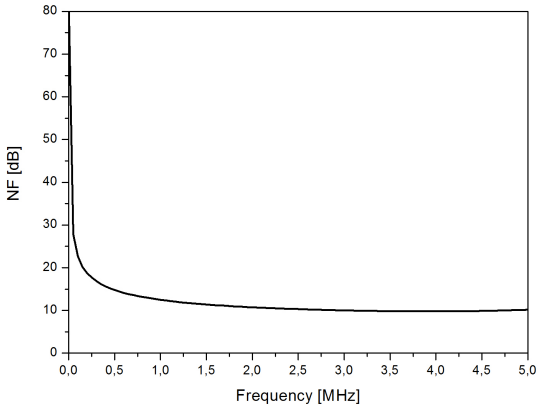


**Figure 12.** Simulated NF of the receiver

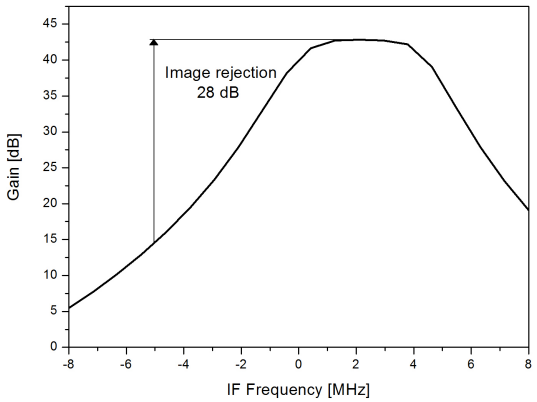


**Figure 13.** Simulated frequency response of the receiver

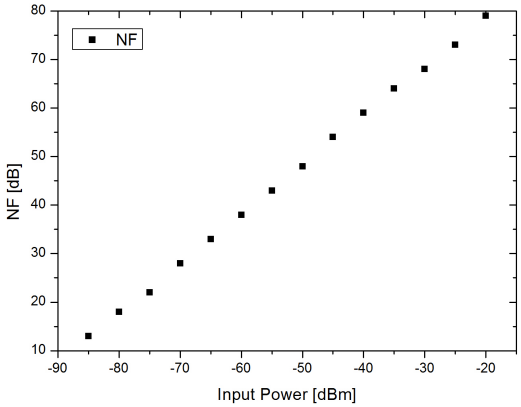


**Figure 15.** Tolerable NF versus receive input power for the IEEE 802.15.4 standard

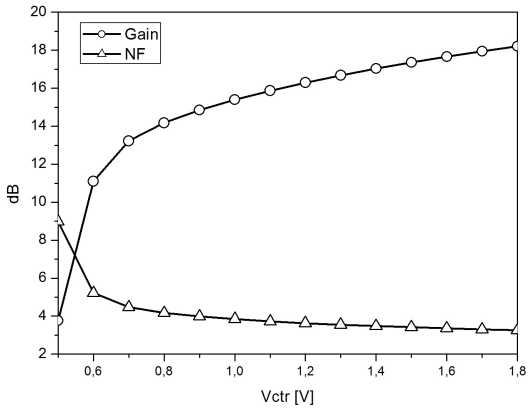


**Figure 14.** Simulated Gain and NF depending on $V_{ctr}$

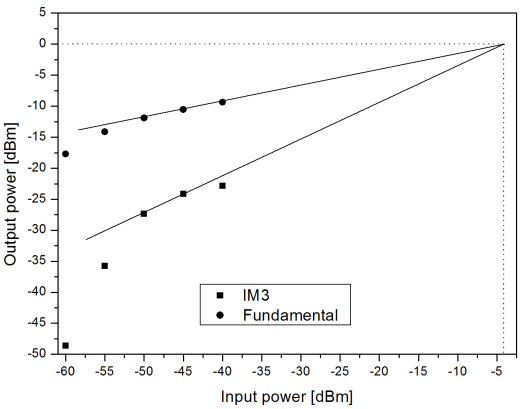


**Figure 16.** Simulated $IIP_3$ of the receiver

*Table II Performance Comparison of 2.4 GHz IEEE 802.15.4 Front-End Receivers*

| | [1] | [2] | [3] | [4] | This Work |
|---|---|---|---|---|---|
| Technology CMOS [nm] | 180 | 180 | 90 | 180 | 180 |
| Voltage Gain [dB] | 86 | 30 | 67 | - | 42 |
| NF [dB] | 8.5 | 7.3 | 16 | <10 | 10.3 |
| IIP3 [dB] | -8 | -8 | -10.5 | >-15 | -5 |
| Power dissipation [mW] | 12.63 | 6.3 | 10 | 10.8 | 5.5 |
| Architecture | Low-IF: LNA+MIX +FIL+PGA | Low-IF: LNA+MIX | Low-IF: LNA+MIX +FIL+PGA | Low-IF: LNA+MIX+FI L+PGA | Low-IF: LNA+MIX +FIL |

LNA: Low Noise Amplifier
MIX: Mixer
FIL: Complex Filter
PGA: Programmable Gain Amplifier