A CMOS latched driver using bootstrap technique for low–voltage applications

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ABSTRACT

In this paper, we propose a high performance direct bootstrapped CMOS latched driver circuit (J–driver). It is a 28% faster and occupies a 58% less active area as compared to a counterpart circuit (L–driver) using indirect bootstrap technique. In addition, our driver J–driver reduces the power consumption by a 2% in driving capacitive loads from $1pF$ to $6pF$. The challenge in designing this latched driver is to appropriately trade–off performance against the active area.

Keywords: CMOS, latch, bootstrap, driver, low–voltage, full–swing

1. INTRODUCTION

As performance of drivers increases, resulting in higher frequency of operation, smaller output and faster output slews, the output load can no longer be treated as a lumped RLC load but as a transmission line. An impedance mismatch causes reflections, resulting in noise and increased delays.

The design of high performance drivers requires a circuit topology that meets the constraints of load, noise margin, while keeping the power consumption and area requirement low. Such drivers are required to drive high capacitive load $(1–10pF)$ in a very short time. On the other hand, the logical circuits are very sensitive to noise effects on the driver interconnect lines. Deployment of bootstrapping techniques have been proposed as an efficient and practical way of implementing driver circuits.[1, 2] Bootstrap drivers can operate with lower power supplies and smaller transistors, therefore, minimizing energy and area, while operate reliably in the presence of noise.

Bootstrapping is based on charge pumps to provide voltages higher than the regular supply voltage in low–supply–voltage systems. A high voltage can be required to drive the analog switches. The output power in energy–limited systems is often in the milliwatt range.

The purpose of this work is to design a latched driver circuit in standard CMOS technology that improves Figure of Merit (area–delay–power product) of the topology shown in Fig. 1, termed *L–driver*.[3]

The paper is organized as follows. Section 2 describes the new proposed bootstrap structure. In Sect. 3, the operation principle of our driver is explained in detail, and in Sect. 4 a comparative evaluation of the two drivers is presented. Finally, in Sect. 5, some conclusions are given and future work is presented.

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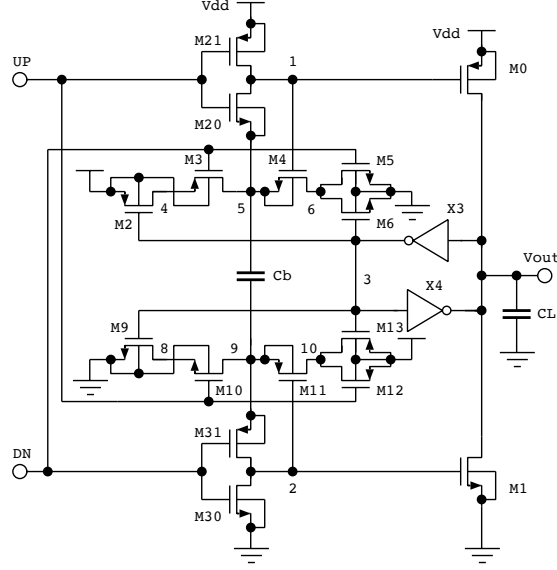S.N.: E-mail: saeid@unsw.edu.au

Figure 1. L–driver.

2. LATCHED DRIVER CIRCUIT STRUCTURE

In order to outperform the limitation factors of *L–driver*, while retaining the advantages of simplicity and reliability, we introduce the configuration illustrated in Fig. 2, termed *J–driver*. Similarly, in this latched driver there is a single bootstrap capacitor `Cb` for speed enhancement and on–demand bootstrapping for power reduction. As a key improvement, we have enhanced the driving capability of the circuit by connection the driver output to the bootstrap capacitor via two complementary pass transistors (`M7` and `M8`). Such technique is called direct bootstrap.[1]

In the circuit of Fig. 2 the upper and the lower halves of the circuit are configured symmetrically with each corresponding pair of devices of opposite polarity. The inputs `UP` and `DN` are similar to R–S latch inputs and should not be asserted simultaneously. `UP` is set to high logic state for a fast output pull–up transition. Similarly, `DN` is set to low logic state for a fast output pull–down transition.

Table 1 shows the channel widths and types of transistors used to design and simulate *L–driver*. We used a CMOS technological process of $0.18\mu m$ from UMC — mix mode/RFCMOS and 1.8V supply voltage. The channel length of all transistors in *L–driver* and *J–driver* is $0.18\mu m$. The active area of *J–driver* is a 58% lower than *L–driver*. Both drivers were loaded with $1pF$ and switching to $142MHz$. The results shown that *J–driver*, outperforms the speed of *L–driver* with less active area and power consumption.

3. CIRCUIT OPERATION

The operation of CMOS latched driver in Fig. 2 can be divided into the following three parts: controlling signal circuit, positive and negative pumping circuit, and driving circuit.

The controlling signal circuit is composed of four inverters `X1` to `X4`. `X1` and `X2` are used to generate inverted signals from input ports `UP` and `DN`, respectively. `X3` and `X4` are used to enable the bootstrapping only if the output transition is required.

The second part is the positive and negative pumping circuit, it consists of twelve transistors `M2` to `M13` and the bootstrap capacitor `Cb`.

And finally, the last part is the driving circuit, it is composed of two transistors `M0` and `M1`. They are used to enhance the driving capability for large capacitive load and increase the speed of the output port.
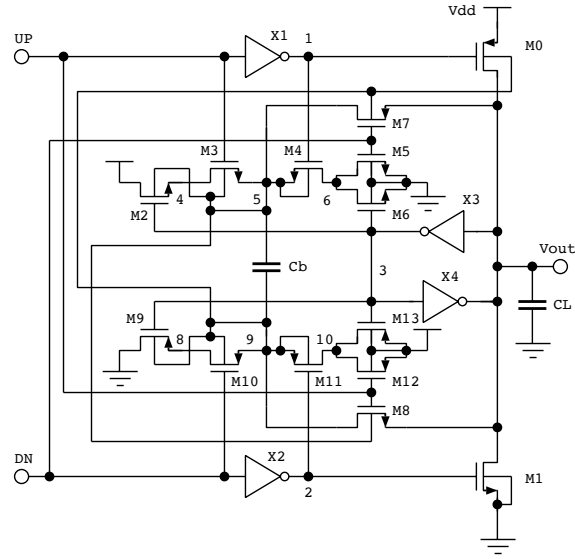
Figure 2. J–driver.

Table 1. Channel widths for L–driver and J–driver.

L–driver			J–driver		
Transistor(s)	Type	Width [μm]	Transistor(s)	Type	Width [μm]
$M0$	PMOS	95	$M0$	PMOS	60
$M1$	NMOS	95	$M1$	NMOS	50
$M2$, $M3$	PMOS	95	$M2$, $M3$	NMOS	1
$M4$, $M5$	NMOS	2	$M4$, $M5$	NMOS	1
$M6$	NMOS	2	$M6$	NMOS	1
—	—	—	$M7$	PMOS	10
—	—	—	$M8$	NMOS	25
$M9$, $M10$	NMOS	95	$M9$, $M10$	PMOS	1
$M11$, $M12$	PMOS	2	$M11$, $M12$	PMOS	1
$M13$	PMOS	2	$M13$	PMOS	1
$M20$	NMOS	40	$NX1$	NMOS	60
$M21$	PMOS	2	$PX1$	PMOS	20
$M30$	NMOS	2	$NX2$	NMOS	30
$M31$	PMOS	40	$PX2$	PMOS	30
$NX3$, $NX4$	NMOS	1	$NX3$, $NX4$	NMOS	1
$PX3$, $PX4$	PMOS	2	$PX3$, $PX4$	PMOS	2

J–driver requires a lower bootstrap capacitor than *L–driver*. Bootstrapping only occurs during the output transition.
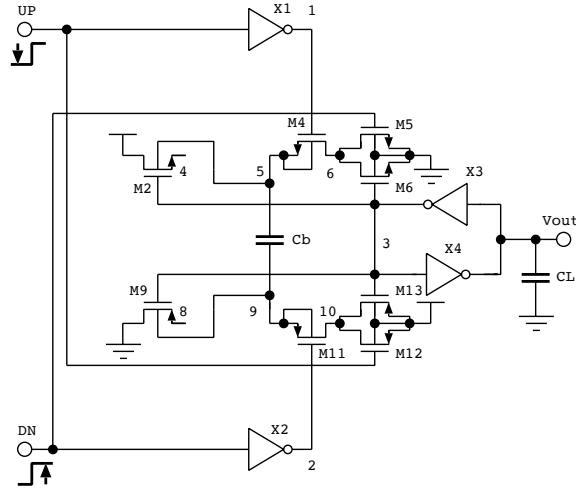

Figure 3. J-driver when UP has a low logic state and DN a high logic state.
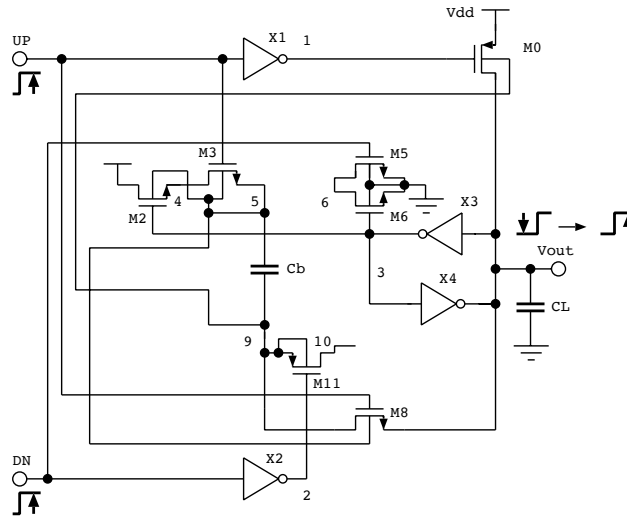

Figure 4. J-driver when UP and DN have high logic states and out has a low logic state.

As can be seen in Fig. 3, when input UP is a low logic state and DN is a high logic state node 1 and node 2 are set to high and low logic states, respectively. Then M0 and M1 turn off, and inverters X3 and X4 preserve their output value. Also, because M4, M5, M11 and M12 turn on, a voltage equal to that of the power supply is induced across Cb as nodes 5 and 9 are set to low and high voltages, respectively.

As is shown in Fig. 4, when UP and DN are set to high logic states and output port has a low logic state, node 3 is set to a high logic state, nodes 1 and 2 are set to low logic states, transistors M0, M2, M3, M5, M6, M8 and M11 are turned on, and transistors M4, M7, M9, M10, M12 and M13 are turned off. After the output of inverter
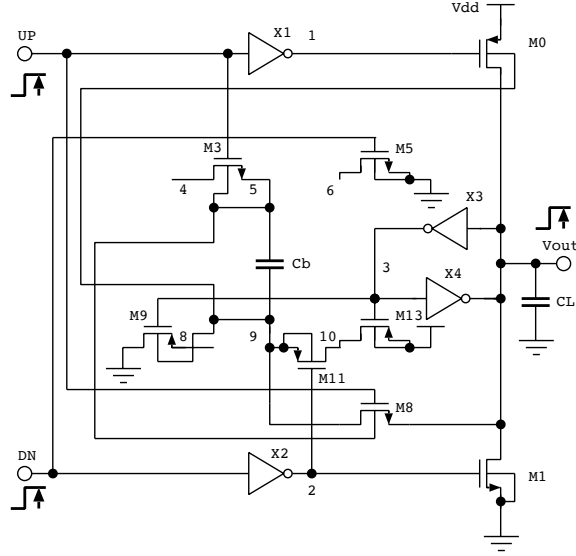
Figure 5. J-driver when UP and DN have high logic states and out has a high logic state.

`X1` changes to a low logic state, transistor `M0` provides a fast output pull–up transition helped from the active positive pumping circuit: `M2`, `M3`, `Cb` and `M8`. This active positive pumping circuit therefore enhances the driving capability of output port in high logic state.

When the output is completely charged to a high logic state, node `3` is then set to a low logic state, transistors `M2` and `M6` are turned off, and transistors `M9` and `M13` are turned on. In that case, node `9` will be to a high logic state across transistors `M11` and `M13`, and bootstrapping will be disabled. On the other hand, if input port `UP` returns to a low logic state, transistor `M0` turns off and *J–driver* again enters the latched state. It is depicted in Fig. 5.

Additionally, if the output port is a high logic state when `UP` becomes a high logic state, node `5` cannot be set to a high logic state because transistor `M2` will be turned off. Hence, the driving capability of transistor `M0` will be not enhanced. This is of no importance on the circuit performance.

Figure 6 depicts a similar situation, when the voltage in the input ports `UP` and `DN` are set to low logic states and output port has a high logic state, node `3` is set to a low logic state, nodes `1` and `2` are set to high logic states, transistors `M0`, `M2`, `M3`, `M5`, `M6`, `M8` and `M11` are turned off, and transistors `M4`, `M7`, `M9`, `M10`, `M12` and `M13` are turned on. While the output of inverter `X2` changes to a high logic state, transistor `M1` provides to a fast output pull–down transition helped from the active negative pumping circuit: `M7`, `Cb`, `M9` and `M10`. This active negative pumping circuit therefore enhances the driving capability of output port in low logic state.

During the output is completely discharged to a low logic state, node `3` is then set to a high logic state, transistors `M2` and `M6` are turned on, and transistors `M9` and `M13` are turned off. In that case, node `5` will be to a low logic state across transistors `M4` and `M6`, and bootstrapping will be disabled. This situation is depicted in Fig. 7. However, if `DN` returns to a high logic state, transistors `M1` will turn off and *J–driver* again will enter the latched state.

Furthermore, if the output port is a low logic state when `DN` becomes a low logic state, node `9` cannot be set to a low logic state because transistor `M9` will be turned off. Hence, the driving capability of transistor `M1` will be not enhanced. That has no effect on the circuit.

In *J–driver*, the body of all PMOS transistors except for `PX1`, `PX2`, `M12` and `M13` are connected to node `9` instead of `Vdd`, while the body of all NMOS transistors except for `NX1`, `NX2`, `M1`, `M5` and `M6` are connected to node `5` instead of ground.
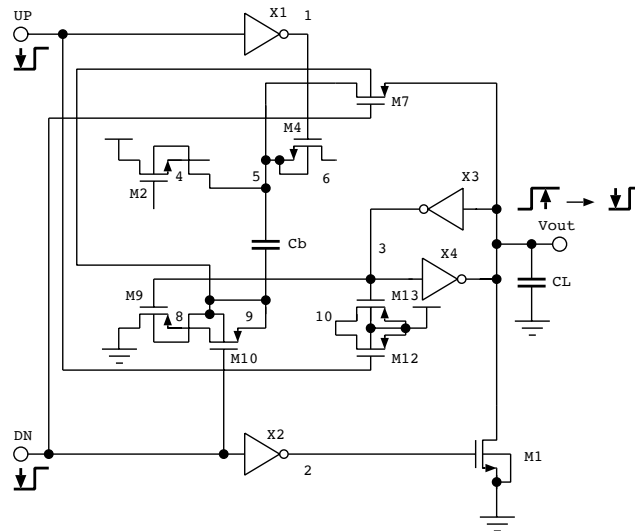
Figure 6. J-driver when UP and DN have low logic states and out has a high logic state.
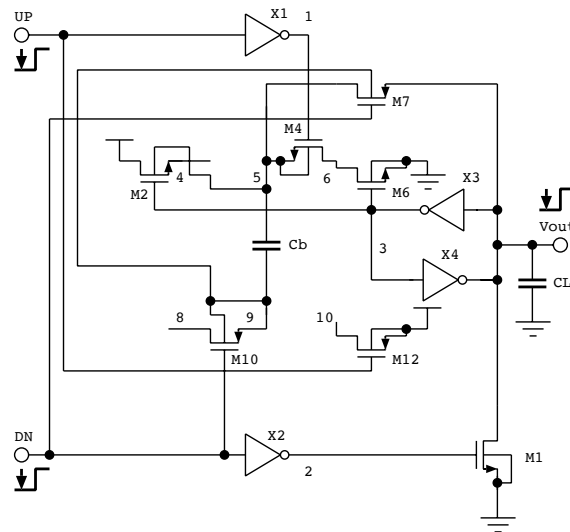

Figure 7. J-driver when UP, DN and out have low logic states.

Figure 8 illustrates the voltages at nodes 5 and 9 — bootstrap nodes — loading with $1pF$. Please note that nodes 5 and 9 are gradually recovered once the output transition completes. Thus, the full swing operation is accomplished.
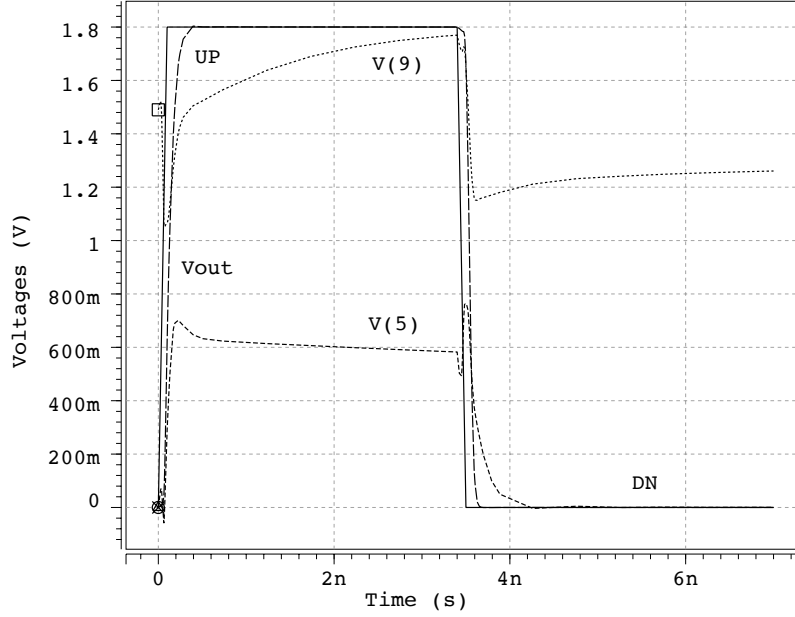

Figure 8. Voltage waveforms of J-driver.

Cb can be realized using NMOSFET, with its drain, source and body terminals connected together, it will have a channel width of $95\mu m$ for *L–driver*, but in the case of *J–driver* Cb will have a channel width of $15\mu m$. In the simulation we have considered a value of $1pF$ and $20fF$ for then, respectively.

4. COMPARATIVE EVALUATION

A set of optimization steps have to be embedded into *J–driver* to satisfy minimum area, maximum speed and minimum power consumption. Simulation results are provided to verify the desired operation of the latched driver circuit.

Bootstrapping techniques can substantially reduce the area of drivers. Such techniques use a small capacitor to transfer excess charge to (or from) the output node during the switching and, therefore, do not consume power continuously. In our design, we have further enhanced the bootstrapping effect by a simple modification. This allows us to trade–off area for speed.

Active areas for *L–driver* and *J–driver* are $138.06\mu m^2$, and $56.88\mu m^2$, respectively. Lower area corresponds lower parasitic capacitance, lower delay and energy consumption.

Table 2 shows the simulation results for the two types of latched drivers considered.

The circuits were simulated at $1.8V$ supply voltage, $142MHz$ frequency, $100ps$ rise and fall times, and different capacitive loads — from $1pF$ to $10pF$.

Figure 9 and 10 show the propagation delay for low to high transition, and high to low transition, respectively. They define how quickly the output responds to a change at the input.

Table 2. Performance and comparison.

| CL [pF]	L−driver			J−driver		
	t_{plh} [ps]	t_{phl} [ps]	Power [mW]	t_{plh} [ps]	t_{phl} [ps]	Power [mW]
1	88.86	135.11	4.86	68.54	92.81	4.76
2	133.06	164.93	6.25	108.08	124.08	6.09
3	181.86	192.25	7.41	145.24	153.97	7.21
4	231.98	221.87	8.41	187.5	184.5	8.22
5	284.17	252.67	9.22	225.88	214.83	9.09
6	339.46	281.73	10.18	263.63	245.02	9.91
7	390.08	313.23	10.51	300.07	275.63	10.65
8	449.81	348.78	11.05	340.14	307.22	11.37
9	514.21	390	11.59	380.29	337.77	12.01
10	586.02	439.68	11.89	418.59	368.62	12.65
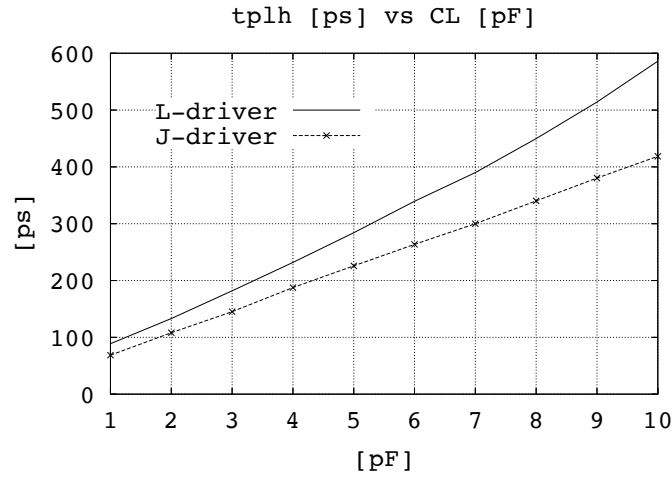
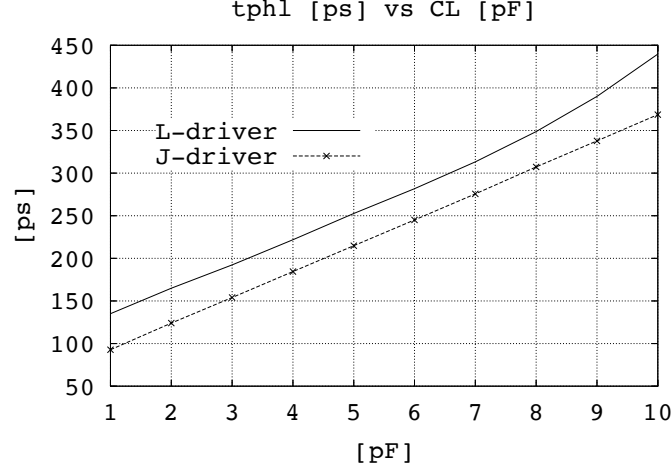**Figure 9.** Pull–up delay time versus output load capacitance.

Figure 10. Pull–down delay time versus output load capacitance.

Figure 11 provides a comparison between the power dissipation levels (@ $142MHz$) in *L–driver* and *J–driver* for various load conditions. It can be seen that for most parts the *J–driver* has a better power dissipation profile. On the average, it has 2% lower power dissipation. On the other hand, *J–driver* has an active area that is 58% less than *L–driver*.
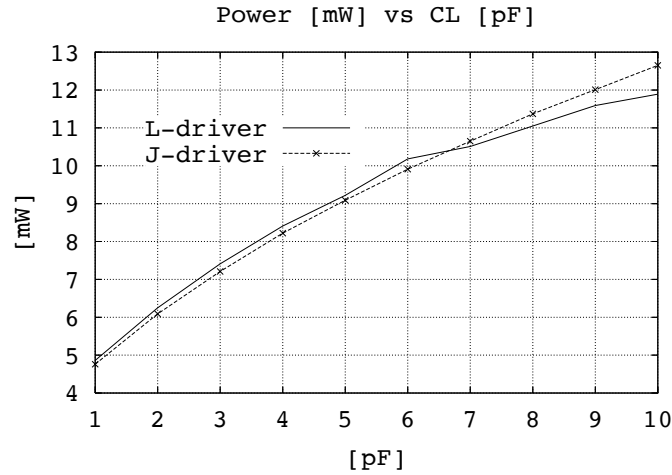

Figure 11. Power dissipation versus output load capacitance.

Comparing the two drivers based on their area–delay–power product Figure of Merit, the *J–driver* circuit, outperforms the *L–driver* circuit for all the output load conditions, as seen in Fig. 12.

5. CONCLUSIONS

The objective of this work is optimising the speed of the final latched driver. The approach consists of modifying the structure of *L–driver* while improving its behavior. In our case, we designed a latched driver termed *J–driver*,
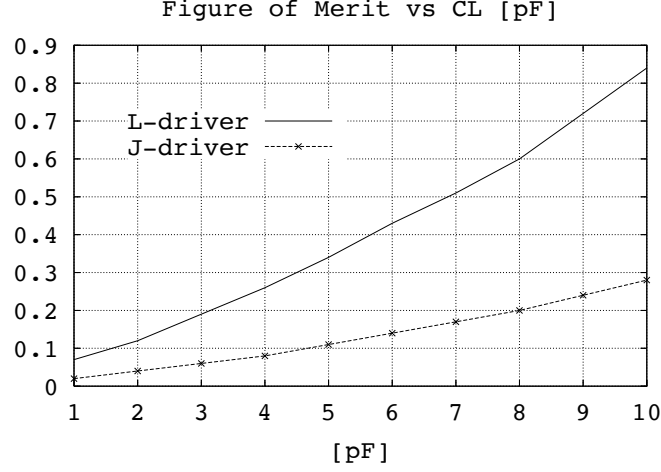
Figure 12. Active area × delay × power versus output load capacitance.

using a $0.18\mu m$, mix–mode/RF CMOS $1.8V$ technology process from UMC. It was simulated at a $142MHz$ frequency with $100ps$ rise and fall times, a supply voltage of $1.8V$, and variable output capacitive load between $1pF$ to $10pF$ respect to L–$driver$. Our proposal use only two additional transistors to L–$driver$.

We have designed J–$driver$ as latched driver that is faster, with lower power dissipation and active area when compared with other similar drivers.

Our future work being to deal with multiple threshold design technique, multiple supply voltage design technique and standby leakage control using transistor stacks to achieve high performance for low voltage and low power CMOS latched drivers.

ACKNOWLEDGMENTS

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