Empirical model of the metal losses in integrated inductors

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ABSTRACT

Integrated inductors are key components in Radio Frequency Integrated Circuits (RFICs) because they are needed in several building blocks, such as voltage-controlled oscillators, low-noise amplifiers, mixers, or filters. The cost reduction, achieved in the circuit assemblage, makes them preferable to Surface Mounted Devices in spite of the different sources of losses that limits the use of integrated inductors; the substrate losses, and the metal losses. We report, in this work, our research in modeling integrated inductors, particularly the losses in the metals. The model is derived from measurements taken from integrated spiral inductors designed and fabricated in a standard silicon process. The measurements reveal that the widely accepted lumped equivalent model does not properly predict the integrated inductor behavior at frequencies above 3 GHz for our technology. We propose a simple modification in the lumped equivalent circuit model: the introduction of an empirical resistor in the port 1-to-port 2 branch of the equivalent circuit. As a result, it will be demonstrated that the integrated inductor behavior is adequately predicted in a wider frequency range than does the conventional model. In addition, the new model is used to build-up an integrated inductor library containing optimized integrated inductors.

Keywords: Integrated Inductors. Silicon RF Circuits. Inductors Wide Band Model.

1. INTRODUCTION

The design and modeling of high quality factor (Q) inductors at high frequencies (around 1 or 2 GHz), is a key factor that determines the performance of RF integrated circuits (RFICs).
Inductors' quality factor is limited by substrate losses and strip metal losses. Due to the low resistivity of Silicon substrate, the resistive losses in the substrate are significant and, as a result, integrated inductors exhibiting high quality factors are not available in such technologies.
Circuit simulation of integrated inductors relies on the availability of an equivalent circuit model. The widely used equivalent model [1], [2], that we call here conventional model, accurately fits the substrate losses in the integrated inductor. This is because the substrate modeling has received a great attention in recent years since it is the main contributor to the inductor behavior at high frequencies. However, we have verified that the conventional model does not take into account some physical characteristics appearing at high frequencies. Therefore, there is a need to develop models representing the metal strip losses in order to optimize the inductor layout. Also, the availability of post-processing techniques like the silicon micro-machining or the use of SoI substrates that overcome the substrate problem [5] require an improvement in the metal modeling.
We report here a new model for the metals in the integrated spiral inductors that improves their wide band modeling. Section 2 presents the conventional model showing the drawbacks at the specified frequencies and the proposed modification, with enhanced frequency response. Section 3 is devoted to validate our modified model for integrated inductors. In section 4 we are presenting an automatic tool, embedded into Cadence™, that helps the circuit designer to

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select the integrated inductor that best fulfill the circuit constraints and automatically generates its lay-out. Finally some conclusions are given.

2. EQUIVALENT CIRCUIT OF AN INTEGRATED INDUCTOR

The most common way to implement an integrated inductor consists in laying-out a metallic spiral directlyabove the substrate (see Fig. 1). Making the spiral as circular as possible can yield significant benefits in inductor performance [6], [9]. At least two metal layers must be available in order to give access to the inner end of the inductor by means of an underpass.

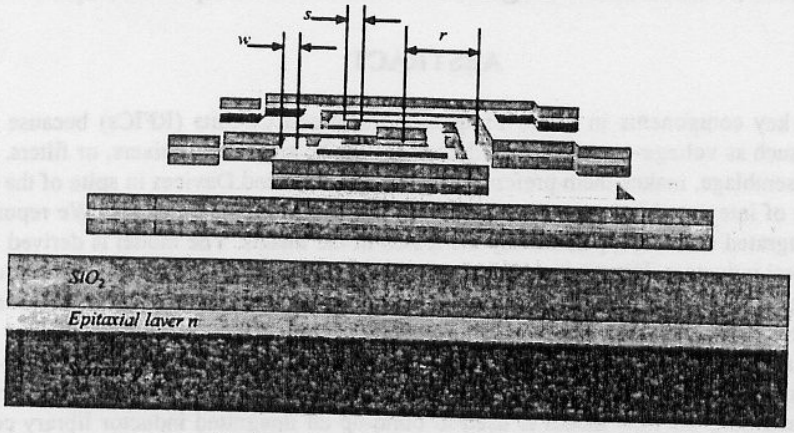

Fig. 1. Square spiral inductor layout

The conventional two-port model for an integrated spiral inductor is shown in Fig. 2 [1]. The schematic is split into three subcircuits whose admittances are Y_L, Y_{SUB1} and Y_{SUB2}. We call the main branch to the subcircuit labeled by Y_L. There Ls accounts for the magnetic effects caused by the ac current flowing in the metal traces, the resistor Rs models the ohmic losses in the metal traces, and the capacitor Cp models the tracks-to-crossunder capacitive couplings. The ground branches, Y_{SUB1} and Y_{SUB2}, incorporate the substrate effects. Thus, capacitors C_{OX1} and C_{OX2} model the oxide capacitance between the coil and the substrate, while C_{SUB1} and C_{SUB2} are the substrate capacitance. R_{SUB1} and R_{SUB2} account for the losses associated to the electrical coupling with the substrate.

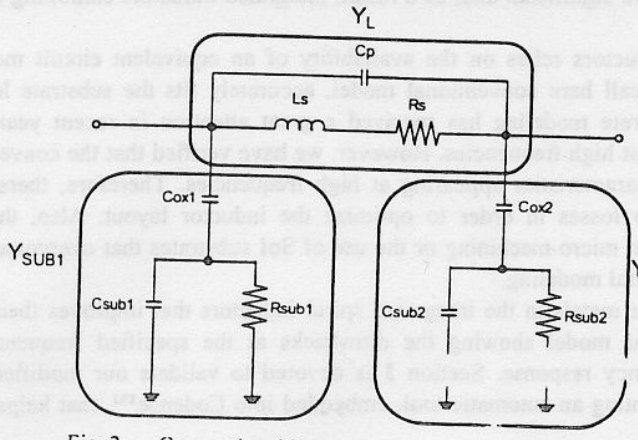

Fig. 2. Conventional integrated inductor two-port model.

We will plot in the following section experimental curves showing that the ground branches (Y_{SUB1}, Y_{SUB2}) adequately model the substrate influence in the behavior of the device at our whole frequency range (from 0.5GHz to 10GHz). However, there is some deviation between the modeled and measured real parts of Y_L. While the conventional model in Fig. 2 agrees with the measurements at the lower frequencies, at the higher ones it can be observed discrepancies for this magnitude (the real part of Y_L).

We propose the modified equivalent circuit shown in Fig. 3 to model the main branch in an increased frequency range. There is a new resistor Rp in series with the capacitor Cp that models resistive losses not accounted for by Rs.

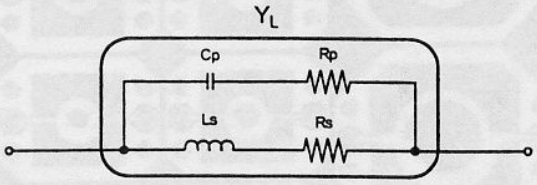

Fig. 3. Modified integrated inductor two port model.

3. EXPERIMENTS DESCRIPTION

More than 100 integrated spiral inductors were designed and fabricated in a standard two metal silicon technology. All of them share some common characteristics in order to make the measurement and characterization procedure easy, and to improve its behavior. In this manner, all the inductors have a semi-integer number of turns (1.5 turns, 2.5 turns, 3.5 turns, etc). As a result, the connection to the pads is straightforward; otherwise this connection would require an extra piece of metal strip parallel to the main inductor strips producing a magnetic coupling between them. This would cause an increase in the inductance and the model predictions would be erroneous.

On the other hand, it is well known that the circular shape is preferred for spiral inductors [6], [9]. This is the reason why all our fabricated inductors have 20 sides.

Metal losses decrease if the inductors are fabricated with different metal levels connected by means of vias; in this manner the effective section is increased and, as a result, their associated resistances decrease [10]. For this reason, the inductors were fabricated with the two available metal levels connected in parallel throughout the whole metal length.

Finally, the spacing between the metal lines should be as smaller as possible; increasing the spacing decreases the total inductance, because of the decreasing of the mutual inductance, and increases the series resistance and the total area.

Fig. 4 shows a photograph of the whole chip and Fig. 5 shows a detailed view of some of the circular spiral inductors.

Fig. 4. Photograph of the chip (more than 100 integrated inductors were fabricated).

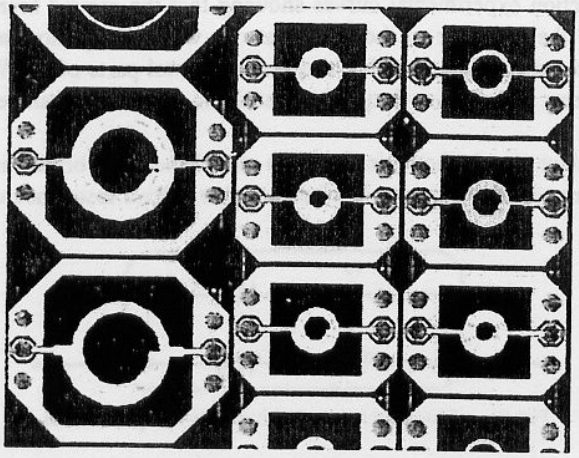

Fig. 5. Detaled view of some fabricated inductors

S-parameter ($S(\omega_i)$) measurements were performed using an on-wafer microwave probing station connected to an automatic network analyzer. The measurements were taken at 201 points in the 0.5-10 GHz frequency band. The influence of the pads and the probes were de-embedded using the four-step de-embedding technique [11].

In characterizing the integrated inductors the $S(\omega_i)$ parameters are transformed into the $Y(\omega_i)$ parameters. This simplify the computation because the equivalent circuit shown in Fig. 2 can be considered as the cascade interconnection of three two-port networks defined by their admittances: Y_L, Y_{SUB1}, and Y_{SUB2}. The element values of the model can be easily computed by a fitting procedure applied to the admittances Y_L, Y_{SUB1} and Y_{SUB2} [3].

Fig. 6 shows the measured and modeled real and imaginary parts of the admittance between the input port and ground (Y_{SUB1}). Note how the network C_{OX1}, C_{SUB1} and R_{SUB1} correctly predicts the behavior of the input-to-ground branch for the entire frequency range. The same can be observed for the admittance between the output port and ground.

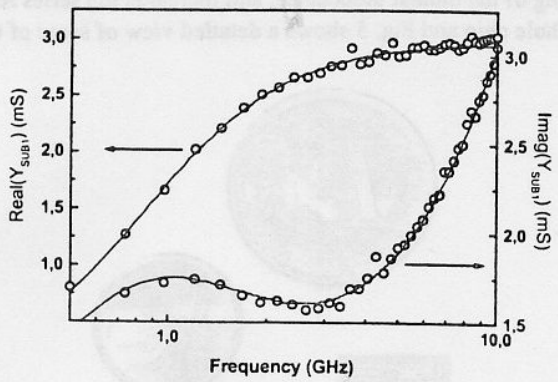

Fig. 6. Real and imaginary parts of the input ground branch admittance against frequency. Measurements: open circles, model: lines

Fig. 7 and Fig. 8 show the imaginary and real parts of the main branch admittance and the result obtained with the

conventional model as a function of the frequency, respectively. Regarding to the imaginary part, the model correctly predicts the inductor behavior, but the same does not occur for the real part. The model fits well at low frequencies but, at high frequencies the real part of the main branch admittance begins to grow and the model does not follow this behavior.

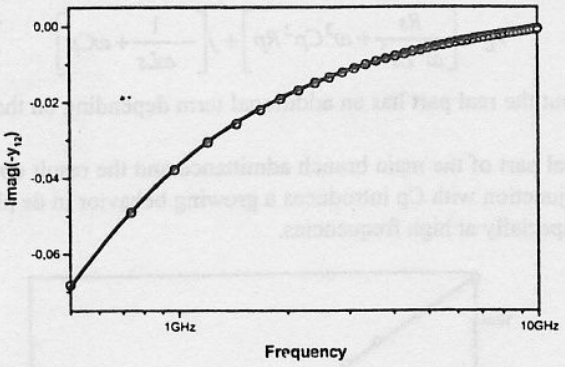

Fig. 7. Imaginary part of the main branch admittance (dots) *vs.* frequency and the result obtained with the conventional model (line).

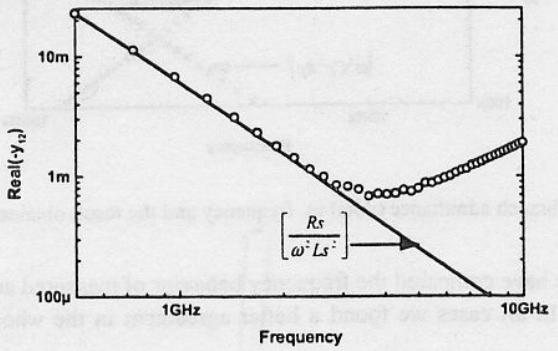

Fig. 8. Real part of the main branch admittance (dots) *vs.* frequency and the result obtained with the conventional model (line).

One of the problems arriving when using a fitting procedure is that the modeler does not have any physical insight about how the circuit elements (Ls, Rs and Cp) affect the inductor behavior. In order to clarify this, let us study the admittance of the main branch of the conventional model:

$$Y_L = \frac{1}{j\omega L + Rs} + j\omega Cp \tag{1}$$

Splitting expression (1) into its real and imaginary parts, we obtain:

$$Y_L = \left[\frac{Rs}{Rs^2 + \omega^2 Ls^2}\right] + j\left[-\frac{\omega Ls}{Rs^2 + \omega^2 Ls^2} + \omega Cp\right] \tag{2}$$

Typical values for Rs, and Ls are units of ohms and a few nH respectively, so equation (2) can be simplified assuming that $Rs^2 << \omega^2 Ls^2$:

$$Y_L \approx \left[\frac{Rs}{\omega^2 Ls^2}\right] + j\left[-\frac{1}{\omega Ls} + \omega Cp\right] \tag{3}$$

This result implies a real part decreasing as frequency increases and an imaginary part depending on Ls and Cp. As stated above, this model does not work because the real part of Y_L begins to grow from a particular frequency. Making the same manipulation in our modified model, the resulting equation is:

$$Y_L \approx \left[\frac{Rs}{\omega^2 Ls^2} + \omega^2 Cp^2 Rp\right] + j\left[-\frac{1}{\omega Ls} + \omega Cp\right] \quad (4)$$

The imaginary part is the same but the real part has an additional term depending on the series resistance of the capacitor, which grows with frequency.

As in Fig. 8, Fig. 9 shows the real part of the main branch admittance and the result obtained with the modified model as function of frequency. Rp in conjunction with Cp introduces a growing behavior in de plot that makes the overall model to fit better to the measurements, especially at high frequencies.

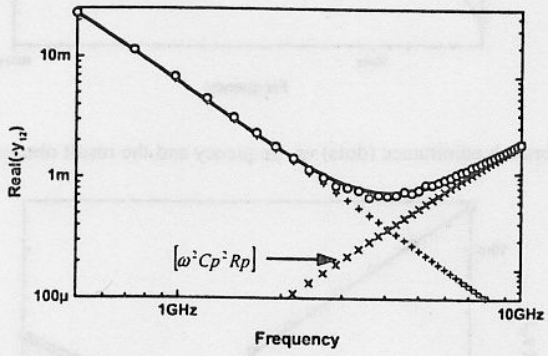

Fig. 9. Real part of the main branch admittance (dots) *vs.* frequency and the result obtained with the modified model (line).

To further validate the model, we have compared the frequency behavior of measured and modeled Y_L, Y_{SUB1} and Y_{SUB2} for all the fabricated inductors. In all cases we found a better agreement in the whole frequency range than using the conventional model.

4. DESIGN TOOLS

In spite of the good modeling attained with the modified model, in a number of cases the broad band behavior can not be represented with a simple lumped element model.

A possible methodology to produce wide band models is to force the equivalent circuit elements to depend on frequency (frequency-dependent model). In this case, the problem is that usual simulators do not permit us to introduce frequency dependent model parameters. This problem can be avoided by using narrow band models where the element values are extracted from the frequency–dependent model in the particular frequency of interest. We report in this section an automatic tool, embedded into Cadence™ that automates this task. This tool helps the circuit designer to select the integrated inductor that best fulfill the circuit constraints and also provides the model that best account its behavior. The lay-out of the selected inductor is also provided.

4.1 Automatic Selector Tool

The set of models already presented completely characterizes every inductor at every frequency, but designers require the best model in every case, and not a set of models. We have developed software embedded into Cadence in Skill language making this task transparent to them.

Fig. 10 shows the Component Description Format (CDF) for the developed Automatic Selector. The designer only needs to introduce the frequency of operation and the desired inductance. The program looks for inductors with the appropriate inductance and chooses the appropriate model. So the program compare the measurements with the modified model and the model with variable components at the specified frequency. It also search for that model presenting a greater useful band. Finally the Automatic Selector give us a set of inductors besides the quality factor, the external radii and the useful band.
Our proposed Automatic Selector facilitates the inductor selection because it reduces the amount of visible cells, give information about the useful band of the used model and allows the use of circuit optimizers.
The program chooses the best-integrated inductor that can be fabricated with the technology being used which fulfill the constraints. Also, the layout of this integrated inductor is automatically generated.
The component description format is very simple. The properties of the inductor are introduced in CADENCE by filling in the first three boxes shown on the right in Fig. 10: inductance, frequency, and number of ports needed (one or two). Once this information is processed the routine returns the already mentioned card in Fig. 10 including the quality factor (Q), the external inductance (L) and resistance (R) and minimum and maximum frequency (fmin and fmax) were the error between the model and the measurements is always smaller than 10%.
The symbol of this inductor to be used in the schematic for the electrical simulations can be observed on the left in Fig. 10. The generated lay-out is presented in Fig. 11 (details are given in the following section).
Our tool greatly reduces the time spent in the inductor selection. Also it solves the problem of selecting the best element geometry, and the designer can easily re-simulate the circuit.
This tool allows the use of circuit optimizers because the inductor is a parametric cell whose defining parameters (f and L) can be variables.

4.2 Automatic Layout Generator

Laying-out a spiral inductor by hand is a slow and error prone process. We have developed a user friendly Automatic Layout Generator Tool which automatically generates the layout. The program is almost independent of the technology (except for a technology file) and has a lot of layout options.
Fig. 11 shows the CDF for the developed Automatic Layout Generator, as seen in the former section it can be linked to the Automatic Selector but it can also be used independently. It is a parametric cell with the following main parameters: number of turns (multiples of 0.25), outer radii, metal width, metal tracks separation and which metals will form the spiral and the output. These parameters cannot have arbitrary values, the tool will correct any non permitted value introduced.
The other parameters are the number of sides per turn (allows squared, octagonal and any other form), and the length of the output path. This permit the user to elongate the spiral in the horizontal or vertical direction. The program also allows to place multilevel spiral inductors, [12], and multiple spirals arranged in the same metal level. Some other features not commented here for simplicity are implemented in our tool.

5. CONCLUSIONS

In this paper, a new wide band model with enhanced frequency response for integrated inductors on silicon is presented. The novelty of the model is a resistor that takes into account resistive losses not accounted for the series resistor, Rs. We also report a set of CAD tools to manage the developed library and to cover all the design aspects of integrated inductors. These tools greatly reduce the time-to-market of circuits incorporating integrated inductors.

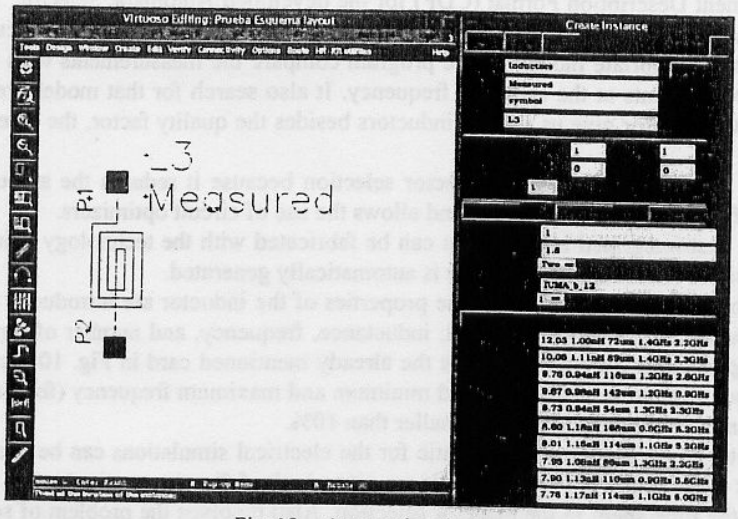

Fig. 10. Automatic selector

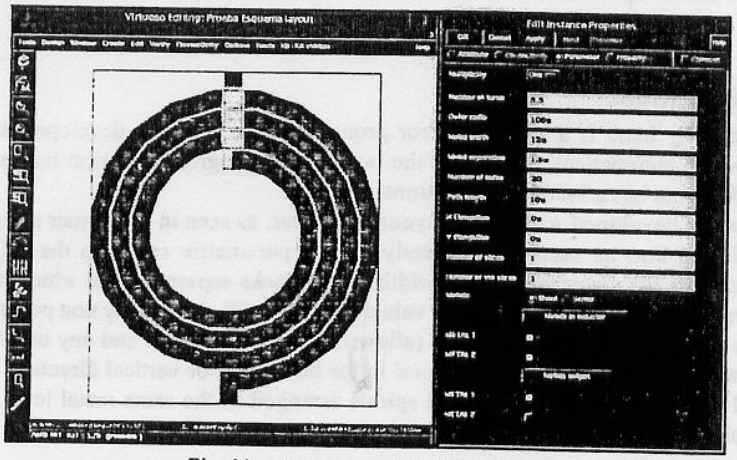

Fig. 11. Automatic layout generator

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