A study of stacked and miniature 3-D inductor performance for radio frequency integrated circuit design

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ABSTRACT

The performance of stacked and miniature three-dimensional spiral inductors is analyzed and compared to standard planar coils. For this purpose, nine of these new structures have been fabricated in a 0.35-µm four-metal SiGe process. According to the measurement results, some of the proposed stacked inductors occupy only 48% of the area of a conventional planar inductor with the same inductance value and work frequency. The area reduction is even more significant with the miniature 3-D structures, which occupy only 22% in some cases, and translate the inductor self-resonance frequency to higher values than the conventional stacked inductors. In spite of this area reduction, these new structures employ metal levels close to the substrate, which significantly degrades the quality factor. So the standard planar coils continue to be the best choice if the designer requires high-quality inductors. However, stacked and 3-D miniature structures could be a better solution if the area saving is the circuit major priority.

Keywords: On-chip spiral inductor, quality factor, self-resonance frequency, stacked spirals, 3-D miniatures inductors.

1. INTRODUCTION

At the present time, the efforts of RF designers are encouraged to reduce the cost and the power consumption of wireless access devices, extended to every facet of modern life. One of the most effective proposals to this issue is increasing the level of integration, so silicon-based processes are preferred. However, silicon is a low resistive substrate, and obtaining high-quality integrated inductors becomes a challenge.

The final performance of voltage controlled oscillators (VCOs) [1] [2], low noise amplifiers (LNAs) [3], matching networks and distributed amplifiers depends strongly on the inductor behavior [4]. Besides this, new appearing standards tend to use higher frequency range.

However, inductor performance at high frequency is seriously degraded by several phenomena such as the skin effect and the eddy currents in substrate and metal traces. Therefore, as the required inductance value and work frequency for radio frequency integrated circuits (RFIC) increase, the design of standard high-quality factor inductors becomes more and more difficult.

Many studies have tried to solve this problem and improve the inductor quality by employing toroidal [5] [6] and solenoidal [7] structures or removing the silicon under the spiral [8] [9] for example. However, all of them make use of unconventional processing or post-processing techniques not suitable for large-volume production.

On the other hand, there are a number of recent applications where the most important requirement is the area saving, more than the inductor quality [10]-[15]. Hence, new on-chip structures with small area, high performance and no additional processing steps would greatly benefit RFIC design.

In this paper, some of these new structures are analyzed. Section 2 revises the basics concepts of the on-chip spiral inductors. Recently appearing inductive structures are then presented and evaluated. Section 3 is devoted to stacked inductors and Section 4 to miniature 3-D structures. Finally, results are discussed in Section 4, where some conclusions are exposed.

2. STANDARD ON-CHIP SPIRAL INDUCTORS

The conventional approach to design an integrated inductor on silicon is to layout a simple metallic spiral directly on the substrate (see Fig. 1). At least two metal levels must be available, because an underpass is required to give access to one of the inductor's port. The challenge is to choose, for a given technology with fixed metal properties, the optimum combination of the number of turns (n), the metal width (w), the spacing between tracks (s) and the external radio (r) to provide a specific inductance and optimum quality factor at the work frequency.
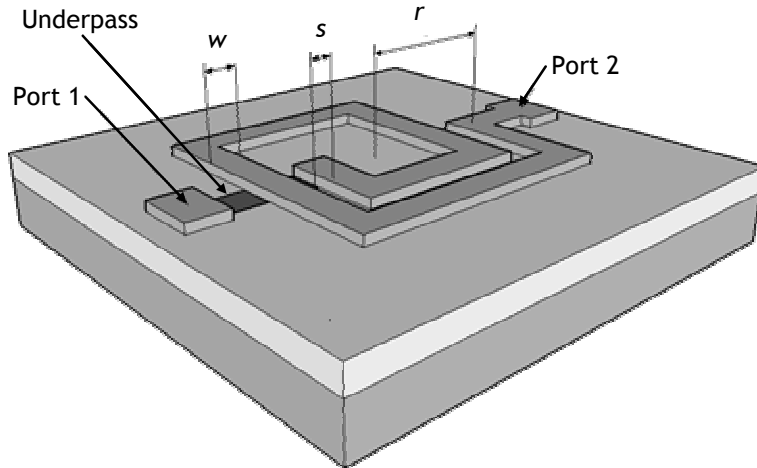

Fig. 1. Layout and geometric parameters on an on-chip spiral inductor.

As said in the introduction, this task is disturbed at high frequencies by the eddy current effects in substrate and metal turns and skin effect in the metal conductor. However, an optimized inductor can be quickly obtained with the aid of a selector tool. We presented in previous works a parametric model that predicts accurately the inductor performance from the geometric and technological coil parameters [16]. Also, an inductor selection tool named IMODEL was implemented based on this model [17]. The algorithm runs a sweep of all inductor geometrical parameters and the best n, w, s and r combination to maximize the quality factor is provided for an inductance value and a work frequency. The tool is technologically scalable, and the foundry process parameters are configured by a text file.

The inductors studied in this work are designed using a 0.35 μm SiGe Austrian Mikro Systems (AMS) process [18]. It provides four metal levels, three of them are similar, with equal thickness and conductivity, and the top metal level is thicker and more conductive. Inductors are designed with this metal, thick and conductive enough to present a low coil resistance, and far from substrate enough to work at high frequencies.

After analyzing carefully the inductors given by IMODEL, it can be concluded that the quality factor of the provided coil decreases and the occupied area grows up as the required inductance and frequency increase. Therefore, some authors recommend stacked [19] and 3-D [20] inductors as a solution to reduce the inductor area and increase the resonant frequency and quality factor.

3. STACKED INDUCTORS

Stacked inductors were originally introduced in GaAs technologies by Geen [21], and later used in CMOS processes by Soyuer [22] and Merrill [23]. As it can be seen in Fig. 2 (a), consists of series-connected spiral inductors in different metal layers. Since the spirals are identical, the inductance value of each spiral separately will be the same. Spiral inductor segments in different layers, close to each other, have positive mutual inductance between them because current flows to the same direction. So, the total inductance value of the structure will increase due to the strong mutual coupling between them, and it can be achieved high inductance in small area. However, the use of more metal layers makes the capacitive parasitic effects amplify, because of the metal-to-metal new capacitance and the increase of the metal-to-substrate oxide capacitance. Thus, the stacked inductor suffers from the low self-resonance frequency.

In order to reduce the equivalent capacitance of conventional stacked inductor, modified stacked inductors are proposed (see Fig. 2 (b)) [19]. The structure is similar to conventional stacked inductor, but it is implemented by using non-

sequent metal layers. Studies about the influence of the oxide thickness between metal layers on stacked inductor performance conclude that the quality factor improves slightly and is shifted to higher frequencies by increasing the thickness [24].
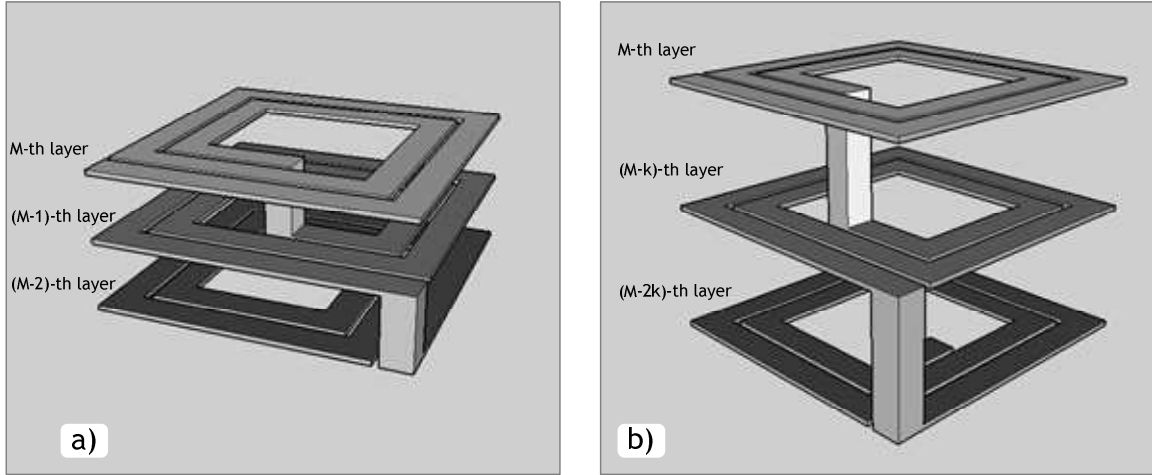

Fig. 2. Structures of stacked inductors: conventional (a) and modified (b).

Five square stacked inductors ($d_{EXT} \times d_{EXT}$) were fabricated in the 0.35 μm SiGe AMS process to test its performance. The main geometric parameters are summarized in Table 1. The measurement system used for the inductor characterization consists of the HP8720ES Vector Network Analyzer and the Summit 9000 Probe Station. To calibrate the measurement system, the short-open-load-through (SOLT) method was applied. Finally, the four-steps de-embedding method [25] was followed to remove the parasitic effects introduced by the measurement structures.

Table 1. Main geometrical parameters of the fabricated stacked inductors.

Inductor	d_{EXT}	w	s	n	Metal layers
SI1	90 μm	6 μm	2 μm	3	M4 and M2
SI2	90 μm	12 μm	2 μm	2	M4 and M2
SI3	90 μm	12 μm	2 μm	2	M4 and M3
SI4	100 μm	6 μm	2 μm	2	M4 and M2
SI5	100 μm	6 μm	2 μm	3	M4 and M2

Fig. 3 compares SI2 and SI3 performance, only differenced by the employed metals. We can see that the inductance value is the same because the lateral dimensions are nearly two orders of magnitude greater than the vertical dimensions. Unfortunately, the employed VNA provides measured data up to 10 GHz, and the SI2 quality factor displacement to higher frequencies cannot be noted. Nevertheless, we can infer from inductance curves that the resonant frequency is lower for SI3 inductor. Momentum simulations predict that it is nearly 10 GHz higher for SI2.

Table 2 recaps the performance of the fabricated inductors: the inductance value (L), the maximum quality factor (Q_{MAX}), and the frequency at which it is reached (f_{QMAX}). In order to compare stacked and standard inductors, these measured data are used to look for the optimal standard inductor for the same application as the stacked inductor is suitable. The values of L and f_{QMAX} in Table 2 are the input data for the inductor selection tool IMODEL.
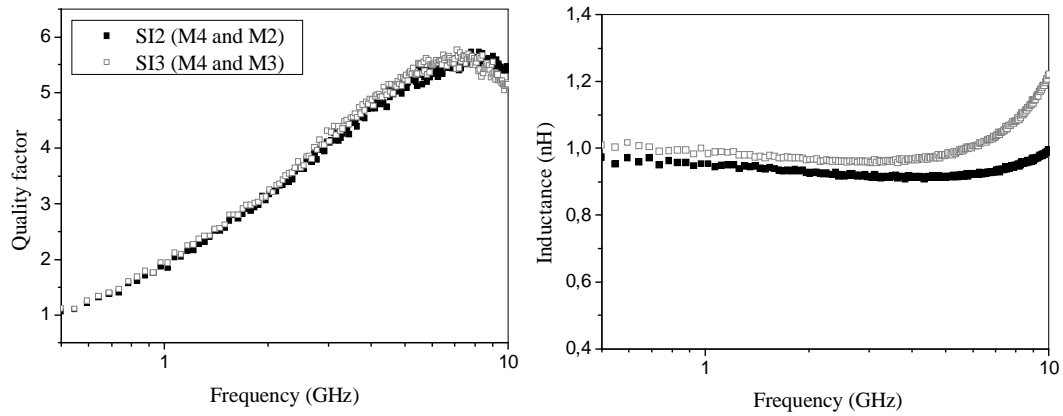
Fig. 3. Measured quality factor and inductance for stacked inductors SI2 and SI3.

Table 2. Performance of the fabricated stacked inductors.

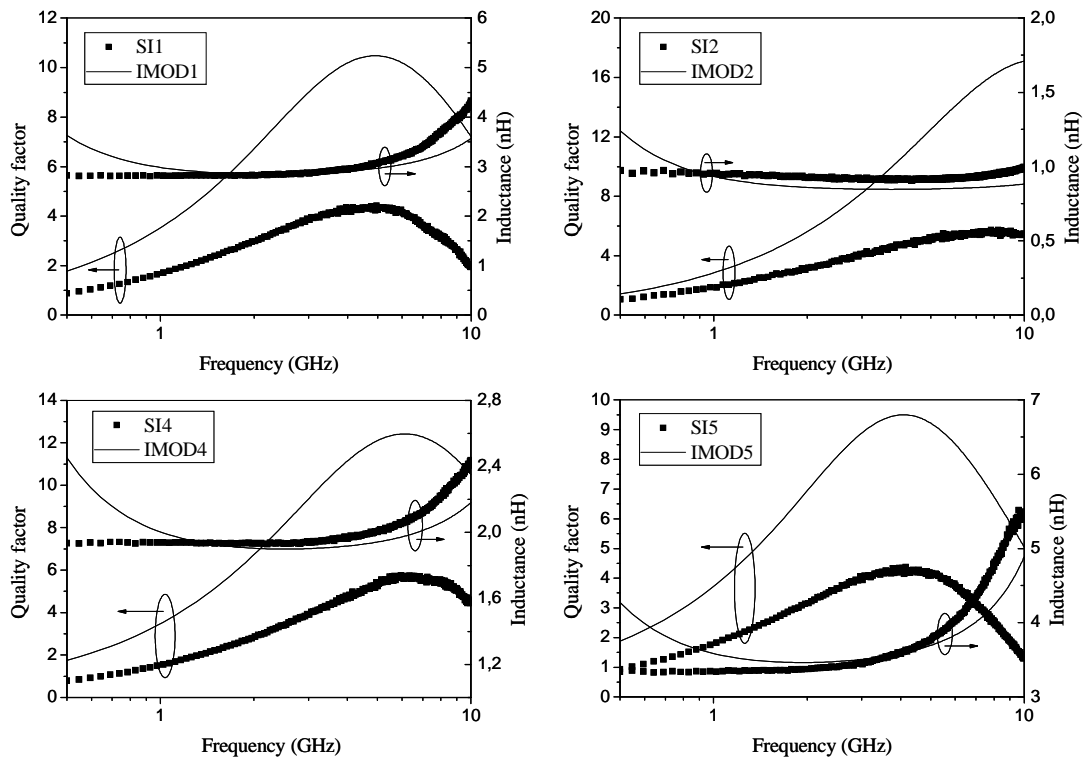| Inductor	L (nH)	Q_{MAX}	f_{QMAX} (GHz)
SI1	3.0	4.4	4.9
SI2	0.9	5.7	7.8
SI4	2.0	5.7	5.9
SI5	3.6	4.4	4.1

Fig. 4. Quality factor and inductance for fabricated stacked coils and provided by IMODEL standard coils.

Fig. 4 compares the main parameters of the measured stacked inductors (SI) and the standard inductors (IMOD) provided by the software IMODEL. It can be seen that the quality factor is considerably higher for the standard inductors. This improvement is less significant as the inductance value goes up (see Table 3). In the same manner, the area saving in stacked inductors is also smaller for low inductances. In the case of the 0.9 nH inductors (SI2 and IMOD2), the quality factor in the standard structure is 10 points better than the stacked one, and the occupied area is 49% higher (4000 μm^2 silicon saving). However, in the case of the 3.6 nH inductors (SI5 and IMOD5), the quality factor of the standard coil improves 5 points and the occupied area is 69% higher (6900 μm^2 silicon saving).

Table 3. Main parameters of stacked (SI) and standard (IMOD) inductors in Fig. 4.

Inductor	Q_{MAX}	area (μm^2)	Inductor	Q_{MAX}	area (μm^2)
SI1	4.4	90x90	IMOD1	10.5	130x130
SI2	5.7	90x90	IMOD2	16	110x110
SI4	5.7	100x100	IMOD4	12.4	130x130
SI5	4.4	100x100	IMOD5	9.5	130x130

4. MINIATURE 3-D INDUCTORS

In an attempt to preserve the advantages of stacked inductor, and at the same time to increase the resonant frequency and the quality factor, Tang et al. proposed in 2002 the miniature 3-D inductors [20]. This structure consists of at least two or more stacked inductors by series connections, and every stacked inductor has only one turn in every metal layer. For example, if there are two stacked inductors with different diameters, and one of them is a one-turn stacked inductor from the metal layer 4 to the metal layer 1, and the other is a one-turn stacked inductor from the metal layer 1 to the metal layer 3, then the miniature 3-D inductor is formed by connecting two stacked inductors at the metal 1, as Fig. 5 shows.
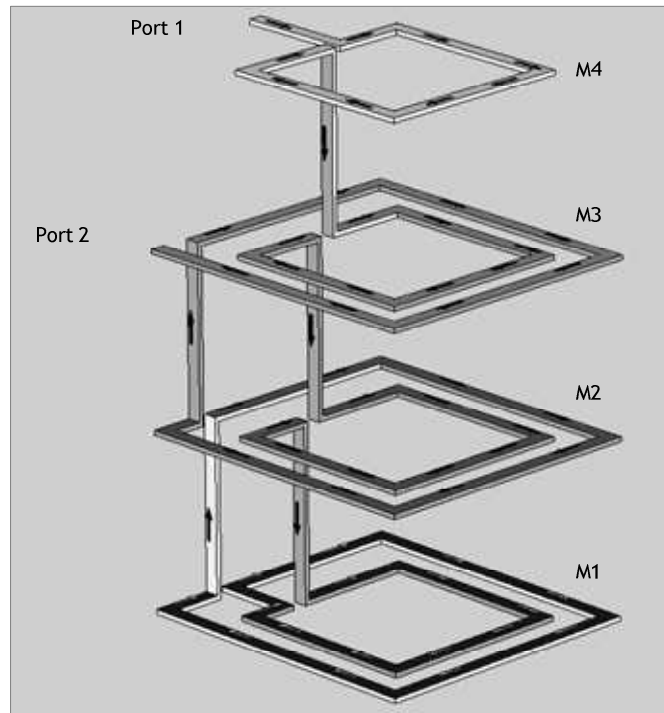

Fig. 5. Structure of the miniature 3-D inductor.

Four square 3-D inductors were fabricated to verify its performance. Table 4 summarizes the main geometrical parameters and the number of stacked inductors each structure is formed by.

Table 4. Main geometrical parameters of the fabricated miniature 3-D inductors.

Inductor	d_{EXT}	w	s	stacked nº
3DI1	80 μm	6 μm	2 μm	2
3DI2	100 μm	6 μm	2 μm	2
3DI3	100 μm	6 μm	2 μm	3
3DI4	100 μm	10 μm	2 μm	2

In the same way we proceed for the stacked inductors, miniature inductors are compared to standard inductors obtained from IMODEL. For this purpose, measured inductance and f_{QMAX} of 3-D inductors, shown in Table 5, are employed as input data in the inductor selection tool. Note that miniature 3-D structures were carefully designed to obtain higher inductance values than the provided by the fabricated stacked inductors.

Comparison results are summarized in Table 6 and shown in Fig. 6. We can see that standard inductors provided by IMODEL do not reach quality factors as high as those in Fig. 4. This is due to the input inductance values, which are higher than in the case of stacked inductors. As said in the introduction, the more inductance is required for a conventional coil, the lower is the quality factor. Nevertheless, the quality of standard inductors continues to be significantly better than in the case of 3-D structures. On the other hand, the latter occupy only between 22% and 39% of the area occupied by the conventional coils, which involves silicon saving up to 22500 μm^2.

Table 5. Performance of the fabricated miniature 3-D inductors.

Inductor	L (nH)	Q_{MAX}	f_{QMAX} (GHz)
3DI1	4.4	3.5	3.9
3DI2	6.6	3.0	2.9
3DI3	10.2	2.5	2.0
3DI4	4.6	3.6	3.0

Table 6. Main parameters of 3-D (3DI) and standard (IMOD) inductors in Fig. 6.

Inductor	Q_{MAX}	area (μm^2)	Inductor	Q_{MAX}	area (μm^2)
3DI1	3.5	80x80	IMOD1	8.3	170x170
3DI2	3.0	100x100	IMOD2	7.1	180x180
3DI3	2.5	100x100	IMOD4	6	180x180
3DI4	3.6	100x100	IMOD5	8.4	160x160

Tang et al. compare in [20] conventional planar and 3-D inductors with the same inductance value and the same quality factor at the work frequency. In this case the area saving would be more than usually higher by using 3-D structures. However, this comparison may not be suitable because if we make the quality of both structures agree, the standard coil is forced to diminish the quality factor by occupying a bigger area. Authors state in the same paper that their proposed miniature structure has the advantages of not only small area but also better quality factor. This work proves that this assertion is not true, provided that standard inductors are designed carefully to be optimum for each application.
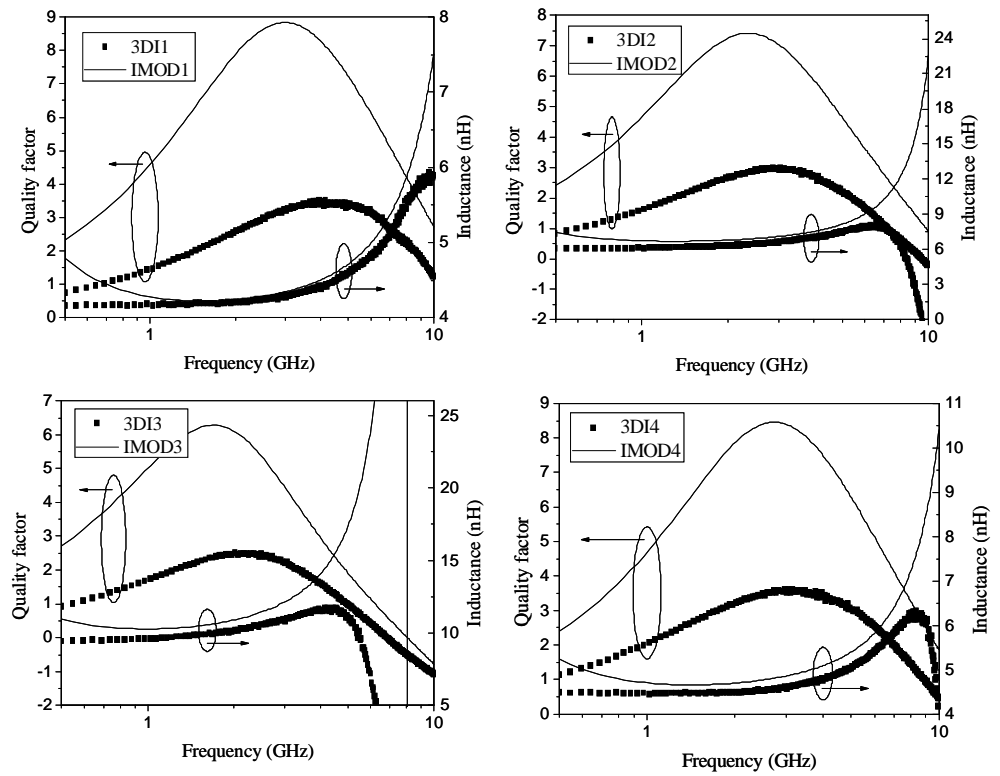

Fig. 6. Quality factor and inductance for fabricated stacked coils and provided by IMODEL standard coils.

5. DISCUSSION AND CONCLUSION

It can be derived from results that inductor goodness depends on the requirements of the circuit where it is going to be employed. Designers should analyze the tradeoff between quality and occupied area.

Table 7. Suitable inductor depending on the requirements.

Main requirement	Suggested structure
Maximum quality factor	Standard planar inductor
Area saving	Stacked/3-D
Very high inductance value or frequency	Stacked/3-D
Maximum self-resonant frequency	3-D

As said in the introduction, there are applications where the most important constraint is the area saving, more than the high quality factor. In these cases stacked and 3-D inductors are a good choice. Selecting the former or the latter depends on the required self-resonant frequency, which is always higher in 3-D structures.

However, when the most important requirement is the quality and the needed inductance value and frequency are not very high, it is possible to find a suitable standard coil with the help of a reliable selector tool as IMODEL.

On the other hand, the quality factor of the optimum conventional inductor goes down for applications with high inductance value and work frequencies (higher than 6 nH and 6 GHz for inductors designed in the employed foundry process). Again, new inductive structures would be a good solution for these requirements. Table 7 summarized these conclusions.

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