Low cost system for transistor modeling

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1 Abstract

If we were to teach a group of students the characteristics of device modeling, we could miss a practical process to obtain the different elements of the model. However, the instruments we would need to get our aim could reach a quite high price. Besides, there is a high risk of break down due to students lack of experience. That is why it has been designed a measurement system which will not reach a very high cost and will, on the other hand, increase its own safety.

2 Introduction

One of the main problems that we face when we want to carry out a device modeling is the high cost of the instruments we need to obtain the starting data. For educational reasons, we thought about the development of a measurement system which could combine a cost as low as possible and protect devices from an inadequate use of the operators.

The basic instruments we need to achieve any modeling consist of a *Curve Tracer* and a *Network Analyzer*. The first one is used to get the DC parameters of the transistor to be modeled, while the second one offers us the S parameters matrix.

Considering how hard designing and constructing a *Network Analyzer* is, a model existing in the market, which can be controlled with IEEE488, was used as starting point. As we can manage it from a computer, we avoid its direct handling. Besides, the risk of failure is reduced.

To achieve one of the two main targets that we have planned, the cost reduction, a *Curve Tracer* was designed and constructed. It was able to get the most important DC data of the transistor to be modeled, and an acceptable precision for the comparative studies of the different models. This device is connected to the computer using a Centronics parallel port.

Finally, a couple of Microsoft Windows™ applications were developed which control the designed *Curve Tracer*, and obtain the DC parameter and the equivalent circuit for the chosen model. The used tool to develop these application is *Borland™ Pascal With Objects 7.0.*

3 Curve Tracer

To implement the *Curve Tracer*, the different margins of voltage and currents needed were studied thanks to the information provided by several medium and low power transistors vendors. In figure 1, it is shown the block diagram of the circuit designed from these data. As you can see, it consists of the following elements: *Output stages, Current/Voltage converters, Selector, ADC, Electronic switches, Calibration Memory* and *Control.*

The blocks named *Gate Output, Drain Output* and *Source Output* are used to bias the transistor from which we want to get the characteristic curves. Its construction was made with 12 bits resolution DAC's, getting a variation margin of (10V with a maximum current of 100mA at the output of *drain* and *source* terminals, and 30mA at the one of the *gate* (Table 1). The output resolution is 4.88 mV ($20/2^{12}$) and are current limited to the above mentioned values, so they are able to stand, for an unlimited period of time, a short-circuit between any output and ground.

The blocks labeled *C/V CONV* are engaged of measuring the current along each terminal, and turn them into voltage using four scales. In figure 2, the block diagram of this stage and the above mentioned electronic switches is shown. The way it works is very simple: the current that flows along the sensor resistor R_1, R_2 or R_3 provokes a voltage drop which is applied to the input of a programmable gain instrumentation amplifier. The output of this device is a voltage proportional to the current flowing along the matching terminal. Each one of its gains represents a different measurement scale. In the case of the gate pin, these scales are: ±58 µA, ±470 µA, ±3.7 mA and ±30 mA. The practical resolution obtained in the smallest scale is 146 nA. The ranges chosen for the drain and source terminals are: ±0.2 mA, ±1.6 mA, ±13.25 mA and ±106 mA. (Tables 2 and 3). The resolution for the smallest scale in these terminals is 303 nA.

The voltage sampling is done on the output terminals, with the range and precisions shown in table 4.

Once we have the different voltages and currents available, the following step consists in time multiplexing them and fixing their variation range so they are suitable for the following stage (ADC).

The analog-digital conversion is carried out by a 12 bit resolution Crystal Semiconductor™integrated circuit. This device is based on the successive approximations method and delivers a shifted binary code. Its conversion rate is 7.2µs and includes a sample and hold circuit which needs just 2.8µs to sample the signal. This is way, the maximum sampling rate is 100,000 samples per second.

To minimize the errors as much as possible, a circuit which makes an autocalibration of the amplifiers and tests the gain precision and the possible derives of the offset, has been included. The operation is carried out using a high precision voltage reference. The calibration results are stored in a RAM. This way, they can be used later, during the measurement.

The last element in the block diagram in figure 1 is the control. It is used as an interface between the computer and the circuits that build the curve tracer. All this block has been made in just one EPLD by Altera™: EPM5128JC-2.

4 Tracer Handling Software

The program that controls the *Curve Tracer* lets a calibration and a data acquisition of the input (I_D-V_{GS}) and output (I_D-V_{DS}) curves of a FET. The possibility to measure any diode (I_D-V_D) has also been included if its curve is inside the current margins which the device is able to handle. Finally, the program lets us export the obtained data to several mathematics analysis programs.

In figure 3, the curves of one of the measured transistors (2N5485), obtained with this program, are shown.

5 Device Modeling

From the data we got with the measurement instruments above mentioned, the non-linear model elements as well as the ones of the low signal circuit are obtained by optimization, using the Levenberg-Marquardt algorithm. The non-linear equivalent circuit that has been used is shown in figure 4. The low signal model is obtained eliminating the current sources I_{GS} e I_{DG}, making the values C_{gs} and R_i constant and making I_{DS} equal to the product of the transconductance and the voltage drop at the Cgs terminals.

As a sample of the program, in figure 5 the initial dialog for the low signal modeling is shown. That is where we can fix the initial values for different parameters, their variation range, and some other variables used for the optimization. The results obtained at the end of the process are shown in figure 6.

6 Conclusion

It has been explained a way to build a completely automated measurement system, using a compatible PC which lets us obtain all the necessary data for the equivalent circuits as well as device modeling. So, we avoid the risk of a bad use in the measurement devices at the time we simplify the process.

Another remarkable point is that, though we have designed the algorithms taking the shown equivalent circuit as reference, it would be very easy to apply it to any other circuit due to the software modularity.

7 Bibliography

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Terminal	Voltage Ranges	Resolution	Current Ranges
Gate	-10V to 9.9997V	4.8828mV	30mA
Drain	-10V to 9.9997V	4.8828mV	100mA
Source	-10V to 9.9997V	4.8828mV	100mA

Table 1. Output stages characteristics.

Scale	Resolution	Precision
±58 μA	29nA	1% Measurement ± 146 nA
±470 μA	232nA	1% Measurement ± 232 nA
±3.71mA	1.86 μA	1% Measurement ± 1.86μA
±30.48 mA	14.8 μA	1% Measurement ± 14.8μA

Table 2. Gate current measurement characteristics.

Scale	Resolution	Precision
±200 μA	101 nA	1% Measurement ± 303 nA
±1.6mA	811 nA	1% Measurement ± 811 nA
±13.25 mA	6.5 μA	1% Measurement ± 6.5 μA
±106 mA	52 μA	1% Measurement ± 52 μA

Table 3. Drain and source measurement characteristics.

Terminal	Range	Resolution	Precision
Gate	-10V to +10V	4.8828 mV	2% Measurement ± 9.7656 mV
Drain	-10V to +10V	4.8828 mV	2% Measurement ± 9.7656 mV
Source	-10V to +10V	4.8828 mV	2% Measurement ± 9.7656 mV

Table 4. Voltage measurement characteristics.

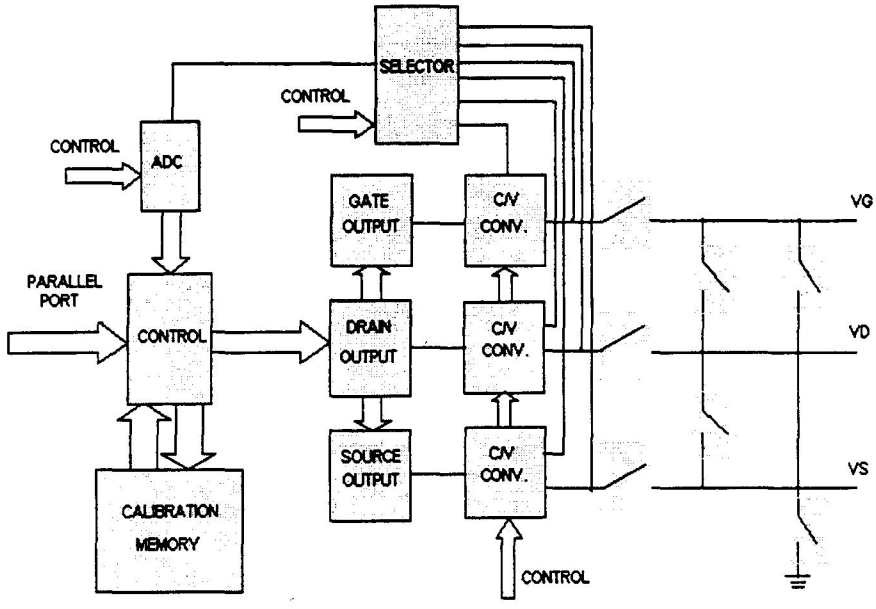

Fig.1. Block Diagram of Curve Tracer.

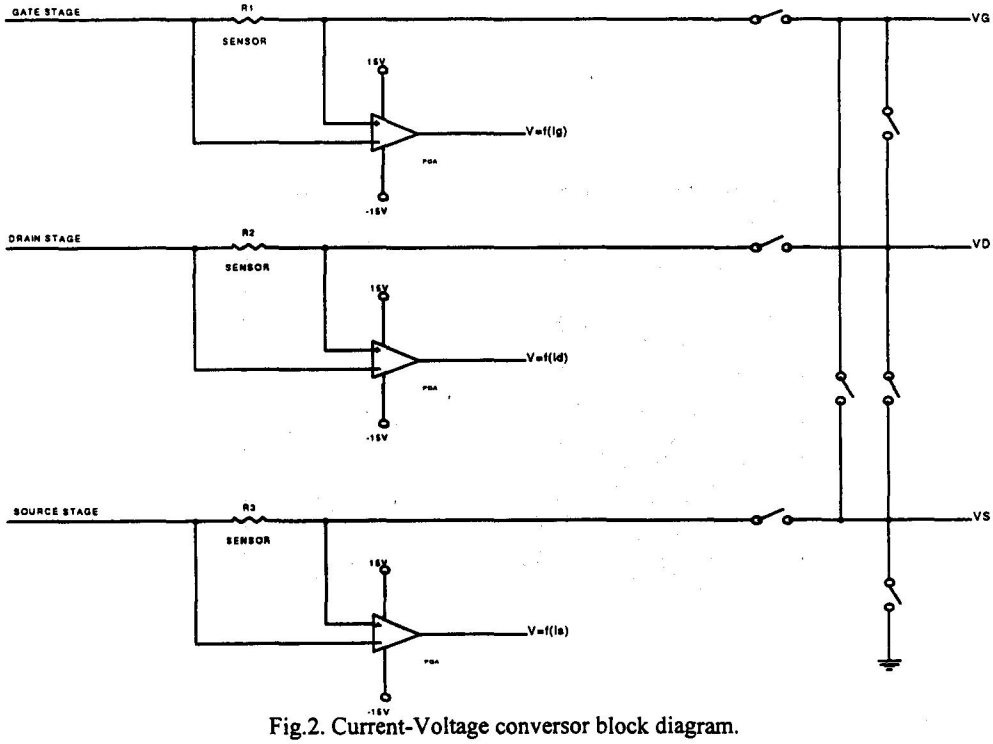

Fig.2. Current-Voltage conversor block diagram.

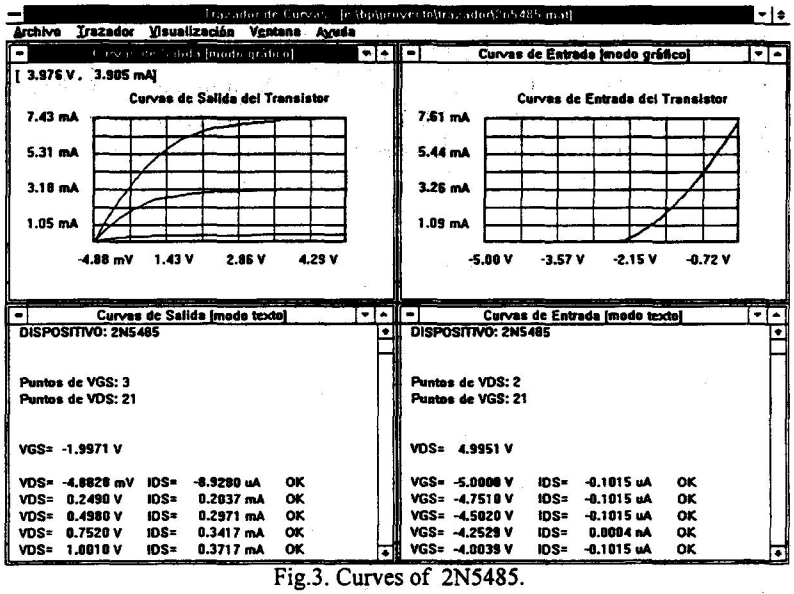

Fig.3. Curves of 2N5485.

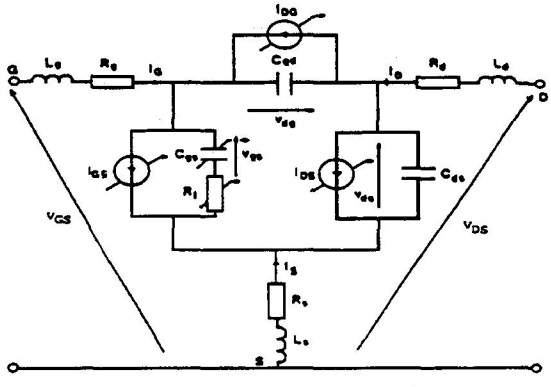

Fig.4. MESFET non linear model.

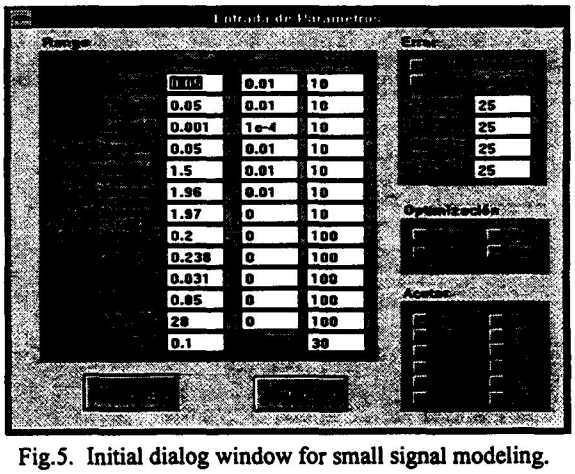

Fig.5. Initial dialog window for small signal modeling.

Fig.6. Final values for small signal modeling.