UNIVERSIDAD DE LAS PALMAS
DE GRAN CANARIA

TESIS DOCTORAL

Design of Radio Frequency Integrated Circuits for Ultra Wide Band Communications

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Instituto Universitario de Microelectrónica Aplicada

Las Palmas de Gran Canaria, Mayo 2012

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Que el Consejo de Doctores del Departamento en su sesión de fecha.....tomó el acuerdo de dar el consentimiento para su tramitación, a la tesis doctoral titulada “Design of Radio Frequency Integrated Circuits for Ultra Wide Band Communications” presentada por el doctorando D. Roberto Díaz Ortega y dirigida por los doctores D. Francisco Javier del Pino Suárez, D. Sunil Lalchand Khemchandani y D. Antonio Hernández Ballester.

Y para que así conste, y a efectos de lo previsto en el Artº 6 del Reglamento para la elaboración, defensa, tribunal y evaluación de tesis doctorales de la Universidad de Las Palmas de Gran Canaria, firmo la presente en Las Palmas de Gran Canaria, a…....de.....de dos mil.....

UNIVERSIDAD DE LAS PALMAS
DE GRAN CANARIA

Departamento: Instituto Universitario de Microelectrónica Aplicada

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Título de la Tesis

Design of Radio Frequency Integrated Circuits for Ultra Wide Band Communications

Tesis Doctoral presentada por D. Roberto Díaz Ortega

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(firma)	**(firma)**	**(firma)**

Las Palmas de Gran Canaria, a _____ de_____ de 20__

"The most incomprehensible thing about our universe
is that it can be comprehended."
Albert Einstein.

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1 Introduction

1.1 Introduction

In the last years the so-called wireless personal area network (WPAN) systems are becoming popular replacing cables and enabling new consumer applications. Such systems are nowadays dominated by standards like Bluetooth and Zigbee, which operate in the 2.4 GHz ISM band. In order to improve the data rate to several hundreds of Mb/s with a low power transmission, it has been proposed Ultra Wide Band (UWB) communications.

Since ultra wide band communications has appeared such as a suitable solution for high data rate wireless transmission, a great number of companies have focused their effort to develop commercial solutions based on it. Some examples of these companies could be the following:

Alereon [1]: Alereon is a fabless semiconductor company based on Austin (Texas) which develops high-bandwidth, high-performance low-power Certified Wireless USB and WiMedia ultra wide band chipsets. One of their products is the AL5100/AL5301 Worldwide ultra wide band Chipset.

The Alereon AL5100 transceiver integrates sensitive analog frontend components including synthesizer VCO/PLL, anti-alias filters, LNAs, PAs, and transmit/receive (T/R) switches it supports a single-ended connection to the antenna eliminating external baluns. When combined with the Alereon AL5301 BBP/MAC, the AL5100 RF transceiver supports all current mandatory WiMedia specifications for worldwide band groups 1, 3, 4, and 6.

Wisair [2]: Wisair is a fabless semiconductor company based on Israel which

Figure 1.1: Veebeam HD system.

provides single-chip ultra wide band and wireless USB solutions for computing, consumer electronics and mobile devices. One of their products is the Wisair WSR601.

The Wisair WSR601 is a single-die CMOS chip that implements PHY, MAC and wireless USB subsystem based on ultra wide band communications. The WSR601 chip is suitable for a wide range of applications such as notebooks, PC peripherals, consumer electronic and portable devices.

Veebeam: [3] Based in Cambridge (UK), Veebeam Ltd is a technology company that architechs, designs and develop wireless technology products. Veebeam has focused its efforts in wireless device-to-device video stream systems. One of their products is Veebam HD.

Veebam HD (Figure 1.1) is a solution which combines of an ultra wide band transmitter and receiver, enabling the possibility to stream video and audio content from a laptop to a HDTV system.

The reception architecture of ultra wide band commercial solutions is usually similar to the structure shown in Figure 1.2. The antenna signal is filtered by an external passive pre-select filter to reduce the level of out-of-band interferers. The frontend consists of a wide band low noise amplifier (LNA) and a quadrature mixer that converts the signal down to low or zero-IF. The synthesizer provides the frequency quadrature LO signals. The baseband filter provides both filtering and variable gain. The filtered baseband signal is digitized by the ADC, which is followed by the digital baseband processor.

In this architecture one of the most challenging components is the LNA. This

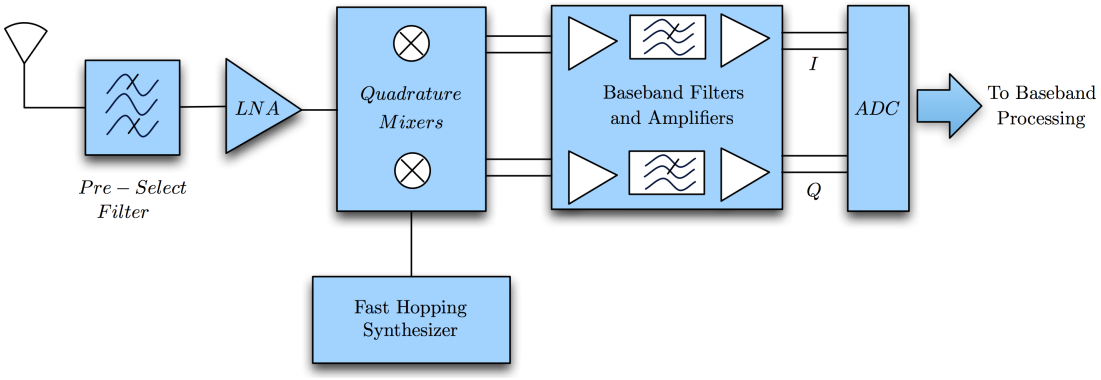


Figure 1.2: Generic receiver architecture.

circuit must have a precise amplification over a wide range of frequencies with a wide band input matching and a low noise contribution. Due to these strict requirements, the low noise amplifiers are usually composed by a large numbers of inductors having a high power consumption.

In mobile applications the power consumption is directly related to battery life. On the other hand, the area consumption is related to fabrication costs. In order to get commercial solutions, it is fundamental to obtain a low cost implementation with a low power consumption.

1.2 Objectives

The aim of this research work is to present different alternatives to implement power and area efficient low noise amplifiers for ultra wide band communications based on ECMA-368 / ISO/IEC 26907 specifications. The results of the present work are integrated in other more ambitious research projects:

- SR2 - Short Range Radio, Spanish Ministry of Industry, Tourism and Trade. 2010-2011.
- SR2 - Short Range Radio, Spanish Ministry of Industry, Tourism and Trade. 2009-2010.
- WITNESS - WIreless Technologies for small area Networks with Embedded and Security & Safety. MEDEA+ from UE - Spanish Ministry of Industry, Tourism and Trade. 2005 - 2007.

In order to achieve the objective, the following milestones have been determined and achieved:

1. From the ECMA-368 / ISO/IEC 26907 is important obtain a reference system in order to stablish the low noise amplifier specification.

2. Explore different alternatives to implement low noise amplifiers for ultra wide band in order to optimize the power and area consumption.

3. Explore different inductors structures in order to reduce the area consumption.

4. Explore the inductorless techniques to avoid the use of inductors in order to reduce the area consumption.

1.3 Outline of the Research

This work consists of seven chapters, which are briefly outlined in this section.

Chapter 1 (the current chapter) introduces the reader to ultra wide band communications, shows some commercial implementations and outlines the research objectives. After getting an insight into the research context, the system design is presented in *Chapter 2*. In this chapter the main requirements of ECMA-368 / ISO/IEC 26907 are presented. With those requirements a reference system is designed and the low noise amplifier specifications are extracted. *Chapter 3* is devoted to the most classical wide band amplifier architecture, the distributed amplifiers. After this first approach and with the objective of solving the distributed amplifiers drawbacks, in *Chapter 4* different implementations of wide band low noise amplifier are presented. In order to continue improving the area and power consumption, in *Chapter 5* feedback techniques and some inductors structures suited for that topologies are explored. *Chapter 6* is devoted to explore inductorless techniques to improve the area saving of low noise amplifiers. Finally some conclusions and areas for further research are presented in *Chapter 7*.

2 Ultra Wide Band Overview and System Approach

2.1 Introduction

As a starting point of this work, this chapter will cover a study about ECMA-368 / ISO/IEC 26907 specification.

After a brief summary about the history and the main specifications adopted by the standard, a receiver system analysis will be developed. This process will take into account the restrictions and specifications imposed by the standard.

The obtained receiver specifications will be taken as a reference point for the circuits designed in the rest of the work.

2.2 History of Ultra Wide Band Communications

The origins of UWB technology has been established around 1962 and it was referred to impulse radio or baseband carrier-free communications. However, the term "ultra wide band" was first used in 1989 in a patent document by U.S. defence department.

In 2002, the Federal Communications Commission (FCC), with the inform 02-48, allocates an unlicensed radio spectrum from 3.1 GHz to 10.6 GHz. In order to define a device as an UWB device, it must be considered that channels have to occupy a band greater than 20 percent of the centre frequency or a minimum channel bandwidth of 500 MHz.

After the first attempt of standardization by the FCC, the MultiBand OFDM Alliance (MBOA), was established in 2003. It is dedicated to promoting the global standard for ubiquitous UWB wireless solutions. The MBOA created a complete

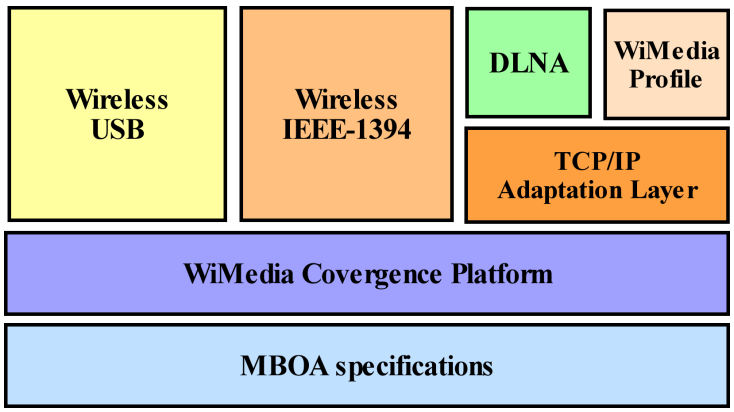


Figure 2.1: WiMedia layers stack.

specification for a Physical Layer (PHY) and a Media Access Controller layer (MAC).

In parallel to the MBOA, in January of 2003 was created the IEEE 802.15.3a task group in order to study the possibility of using the new FCC spectrum specifications in wireless local area networks and personal area networks.

Outside the IEEE 802.15.3a, different companies formalized their relationships to provide a legal context. From this formalization, in 2004 the WiMedia Alliance was born to promote wireless connectivity and interoperability among multimedia devices. The objective of WiMedia is developing a common abstraction platform as shown in Figure 2.1, which enable multiple applications to run over one common radio. The WiMedia radio platform is based technically on MB-OFDM specifications. The combination of MB-OFDM and this convergence platform allows the implementation of wireless version of USB, IEEE 1394, DLNA and other IP-based application protocols.

On January 2006, after three years of a jammed process, the IEEE 802.15.3a was abandoned without conclusion. At this moment, without the support of the IEEE, the WiMedia Alliance had to seek for a new alternative to standardize UWB communications. After this process of seeking and hard work, in 2007 was approved the first version of standard ECMA-368 / ISO/IEC 26907 that regulate the UWB communications at Physical and Media Access Controller layers.

2.3 ECMA-368 / ISO/IEC 26907 Receiver Specifications

2.3.1 Operating Frequency Band

The physical layer operates in a frequency range from 3.1 to 10.6 GHz. The relationship between the centre frequency (fc) and the channel number (BAND_ID number or n_b) is given by Equation 2.1.

$$f_c(n_b) = 2904 + 528 \cdot n_b \; MHz \qquad where \; n_b = 1, ..., 14 \tag{2.1}$$

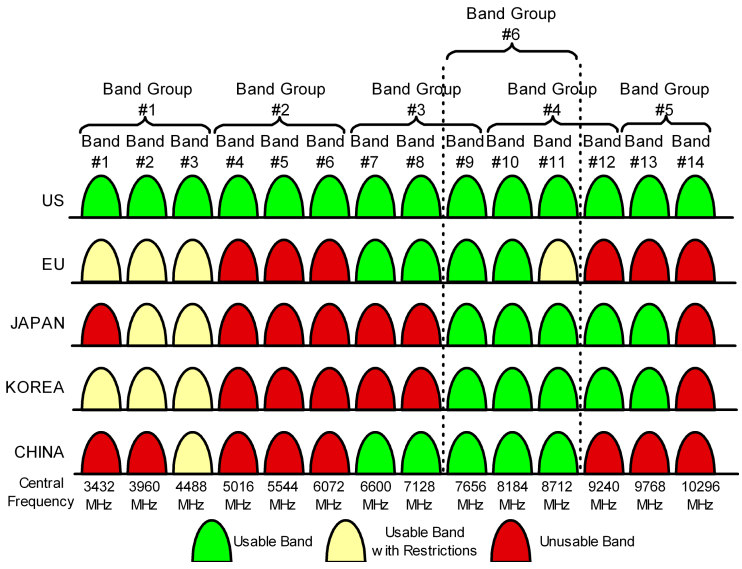


Figure 2.2: UWB operating bands limitations.

This definition provides a unique numbering system for all channels that have a spacing of 528 MHz. As defined in Figure 2.2, six band groups are defined. Band groups 1 to 4 consist of 3 bands each, spanning the band 1 to 12. Band group 5 contains the two bands 13 and 14. Band group 6 contains the bands 9, 10 and 11. The allocation band is summarized in Table 2.1. In spite of this recommendation about the allocation bands, each country can create more restrictive rules about the frequency band use.

Band Group	Band ID (n_b)	Lower Frequency (MHz)	Center Frequency (MHz)	Upper Frequency (MHz)
1	1	3168	3432	3696
	2	3696	3960	4224
	3	4224	4488	4752
2	4	4752	5016	5280
	5	5280	5544	5808
	6	5808	6072	6336
3	7	6336	6600	6864
	8	6864	7128	7392
	9	7392	7656	7920
4	10	7920	8184	8448
	11	8448	8712	8976
	12	8976	9240	9504
5	13	9504	9768	10032
	14	10032	10296	10560
6	9	7392	7656	7920
	10	7920	8184	8448
	11	8448	8712	8976

Table 2.1: Band group allocation.

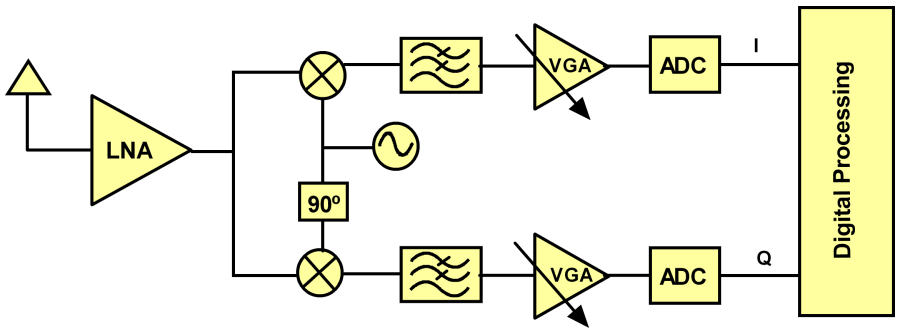


Figure 2.3: Direct conversion architecture.

2.3.2 Receiver Sensitivity

For a Packet Error Rate (PER) of less than 8% with a Physical layer Service Data Unit (PSDU) of 1024 octets, the minimum receiver sensitivity numbers with a Additive White Gaussian Noise (AWGN) for the different data rates are listed in Table 2.

Data Rate (Mb/s)	Sensitivity (dBm)
53.3	-80.8
80	-78.9
106.6	-77.8
160	-75.9
200	-74.5
320	-72.8
400	-71.5
480	-70.4

Table 2.2: Sensitivity versus data rate.

2.4 Receiver System Design

Due to the huge channel bandwidth, a direct conversion receiver architecture has been chosen. Figure 2.3 shows the direct conversion receiver diagram block, where the LO frequency is equal to the input carrier frequency. Note that channel selection requires only a low pass filter with relative sharp cut-off characteristics.

This architecture has several issues. First, in a direct conversion topology, the

down converted band extends to zero frequency. As a result, offset voltages can corrupt the signal and saturate the following stages. This issue is also related to the LO leakage because the LO radiation could appear as a DC voltage at the receiver output. Second, as shown in Figure 2.3, phase and frequency modulation requires shifting either RF or LO signal output by 90º. This shifting generally introduces errors and noise. Due to this error I/Q mismatches could appear, thereby raising the bit error rate. Third, in baseband, the even-order harmonics could be into the desired channel. Fourth, due to the desired channel is translated directly to baseband, the Flicker noise could affect the signal.

On the contrary, the simplicity of the direct conversion architecture offers two important advantages. First, the problem of the image frequency does not appears. As a result, no image filter is required. Second, the IF-SAW filter and other down-conversion stages, used for instance in heterodyne receivers, are replaced with low-pass filters and baseband amplifiers, so this architecture is more suitable for a monolithic integration with a relatively low area and low power consumption.

2.4.1 Noise Figure

As shown in previous section, the ECMA-368 / ISO/IEC 26907 specifies a sensitivity of -70.4 dBm (S_{in}) for the highest data rate of 480 Mb/s (R) and a sensitivity of -80.8 dBm for the lowest data rate (53.3 Mb/s) with a channel bandwidth of 528MHz (BW). The noise figure is defined as the degradation of the signal to noise ratio as it is shown in Equation 2.2:

$$NF = SNR_{in} - SNR_{out} \tag{2.2}$$

Where,

$$SNR_{in} = S_{in} - (174 + 10 \cdot log(BW)) \tag{2.3}$$

$$SNR_{out} = \left(\frac{E_b}{N_0}\right)_{dB} + \left(\frac{R}{BW}\right)_{dB} \tag{2.4}$$

In order to obtain the value of energy per bit to noise power spectral density ratio (E_b/N_0), the standard defines a QPSK modulation for each sub-carrier and a

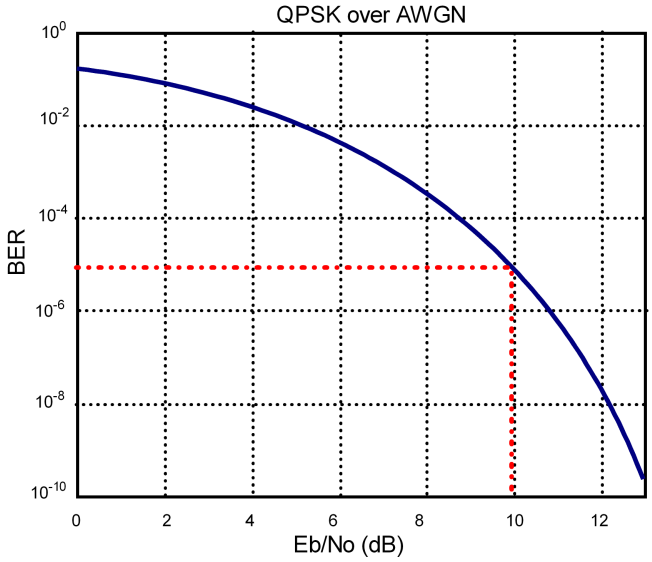


Figure 2.4: BER stimation.

PER of 8% for a 1024 byte packet. With this PER a Bit Error Rate (BER) of 10^{-5} is obtained. Finally from Figure 2.4, it can be obtained the estimated value of E_b/N_0 (10 dB) for the calculated BER. Combining Equations 2.3 and 2.4, Table 2.3 shows the maximum and minimum noise figure values for different values of sensitivity and data rate.

Data Rate (MB/s)	Sensitiviy (dBm)	Noise Figure (dB)
480	-70.4	7.32
53.3	-80.8	18.9

Table 2.3: Receiver noise figure.

2.4.2 Channel Filter and ADC Specifications

In the frequency band occupied by ECMA-368 / ISO/IEC 26907, the most harmful interference is caused by WiFi (IEEE 802.11a) channels in the 5 GHz to 6 GHz band. According to standard specifications, the adjacent channels must be attenuated 36 dB (Figure 2.5).

The channel filtering is also defined as a trade-off between the analog to digital converter (ADC) and the channel filter. The filter specifications could be relaxed by increasing the ADC dynamic range and removing the interference through digital

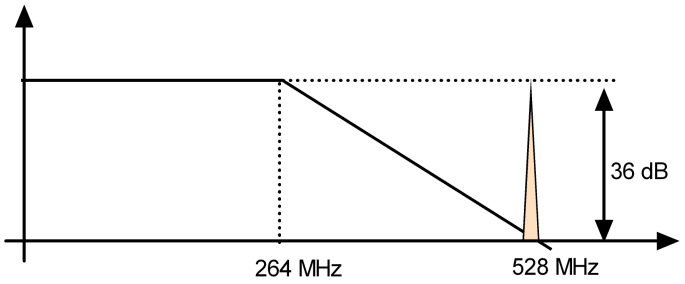


Figure 2.5: Filter requirements.

processing.

The dynamic range of the ADC (DR_{ADC}) is defined by Equation 2.5 [4], where A_{filter} is the filter attenuation. It is important to avoid saturating the ADC at the maximum input power, according to Equation 2.5 and taking into account the worst case: a minimum input power (P_{inMin}) of -80.8 dBm and a maximum input power (P_{inMax}) of -30 dBm (WiFi Interference), the ADC dynamic range is easily determined from Equation 2.5.

$$DR_{ADC} = \underbrace{(P_{inMax} - A_{Filter})}_{P_{max}} - \underbrace{(P_{inMin} - 15dB)}_{quantization\ noise} \tag{2.5}$$

Once the dynamic range of the ADC has been obtained, the ADC number of bits could be determined using Equation 2.6 [4]:

$$DR_{ADC} = 6.02 \cdot N + 1.76\ dB \tag{2.6}$$

With different filter specifications, ADC dynamic ranges and ADC number of bits, different configurations can be obtained. Table 2.4 shows different combinations for the filter and ADC specifications:

Filter roll-off (dB/oct)	Filter order	ADC dinamic Range (dB)	ADC bit numbers
12	2º	53.8	≥ 9
24	4º	41.8	≥ 7
36	6º	29.8	≥ 5

Table 2.4: Channel filter and ADC specifications.

According to the standard specifications, the maximum input power is -41 dBm for a desired in-band signal. In the worst case, the maximum dynamic range is 39.8 dB. In consequence, in Table 2.4 the third configuration must be rejected because in this configuration the ADC will be saturated with the input power worst case.

2.4.3 ADC and Frontend Gain Specifications

The quantization noise is given by [4]:

$$N_Q = \frac{(\frac{V_{FS}}{2^N})^2}{12 \cdot (\frac{2 \cdot f_s}{f_{bW}}) \cdot R_o} = \frac{(\frac{V_{FS}}{2^N})^2}{12 \cdot p \cdot \rho_o} \tag{2.7}$$

Expressed in dBm with $R_o = 50\ \Omega$, the quantization noise results in:

$$N_Q = -6.02 \cdot N + 20 \cdot log(V_{FS}) - 10 \cdot log(\rho) + 2.2\ dBm \tag{2.8}$$

where, V_{FS} is the ADC full range voltage input, N is the ADC number of bits and ρ is the oversampling factor expressed as $\rho = 2 \cdot f_s/BW$. Considering a V_{FS} of 2V the quantization noise is given by:

$$N_Q = -6.02 \cdot N - 10 \cdot log(p) + 8.22 \tag{2.9}$$

On the other hand, the output thermal noise is given by the following expression:

$$N_T = -174 + 10 \cdot log(BW) + G_{max} + NF = G_{max} - 79.77 \tag{2.10}$$

Combining Equations 2.9 and 2.10 and taking into account that $N_T = N_Q + 15$, The minimum total gain of the receiver could be expressed as:

$$G_{min} = -6.02 \cdot N - 10 \cdot log(p) + 102.99 \tag{2.11}$$

In Table 2.5, the gain values for different oversampling factors and ADC number of bits are shown.

ADC bits	Oversampling factor (p)	G_{min} (dB)
7	1	60.86
	2	57.86
9	1	48.81
	2	45.81

Table 2.5: Minimum receiver gain specifications.

2.4.4 Automatic Gain Control

In the previous section, the minimum gain value has been determined to obtain a quantization noise level 15 dB less than the thermal noise. However, the calculated gain values could saturate the ADC input. The maximum power level at the ADC input is given by:

$$P_{ADC} = \frac{\left(\frac{V_{FS}}{2}\right)^2}{2 * R_0} = 10\ mW\ \Rightarrow\ 10\ dBm \tag{2.12}$$

In consequence, in order to avoid to saturate the ADC, the system should satisfy the following expression:

$$S_{Imax} + G_{min} \leq 10\ dBm \tag{2.13}$$

In the worst case, the maximum desired input power (S_{Imax}) is -41 dBm. Under this condition, the maximum permitted gain for the entire reception chain should be less than 51 dB because with this gain value, the power level at ADC input is 10 dBm. As it can be observed in Table 2.5, the ADC number of bits should be fixed at least to 9 bits, because with this number of bits, the minimum system gain is less than the maximum permitted gain at the ADC input.

On the other hand, to obtain the maximum receiver gain, the ADC dynamic range should be considered. From Table 2.4, an ADC of 9 bits should have a dynamic range of 53.8 dB. The ADC dynamic range is defined by the following expression:

$$\Delta AGC = S_{Imax} - S_{Imin} \tag{2.14}$$

Table 2.5, shows the receiver gain specifications, as mentioned above, the maximum power level at the ADC input is 10 dBm so, from Equation 2.14, the minimum

ADC input signal level is: -43.8 dBm. On the other hand, for the weak signal and the minimum gain established in 48.81 dB, so in this condition the power level at the ADC input is -32dBm.

As a conclusion from the previous results, the AGC is not needed because in the minimum and maximum input power level condition, the ADC input is not saturated.

2.4.5 Linearity Requirements

The interference scenario is dominated by IEEE 802.11a. In a typical case, a IEEE 802.11a channel at a distance of 0.2m could reach a power level of -31.9 dBm. This interference should coexist with a desired ECMA-368 / ISO/IEC 26907 signal with a power level of -80.8 dBm. From this interference scenario, the linearity is defined by the following expression:

$$IIP3 = S_{desired} + \frac{3}{2} \cdot (S_{interference} - S_{desired}) \;\Rightarrow\; IIP3 \geq -8.65\ dBm \qquad (2.15)$$

where $S_{desired}$ is the desired signal power and $S_{interference}$ is interference signal power.

2.4.6 Synthesizer Requirements

As the radio has to cover the six bands defined in the ECMA-368 / ISO/IEC 26907 and a zero-IF architecture is proposed, the synthesizer should provide the center frequencies of the bands shown in Table 2.1.

In the MBOA proposal, frequency hopping between sub-bands occurs once every symbol period of 312.5 ns. This period contains a 60.6 ns suffix, which is followed by a 9.5 ns guard interval. The frequency generator used to drive the switching core of both, the down-conversion mixer in the receive path and up-conversion mixer in the transmit path, needs to switch within this 9.5 ns to accomplish the frequency hopping.

The demands on the purity of the generated carriers are also very stringent due to the presence of strong interferer signals. For example, for Mode 1 operation all spurious tones in the 5 GHz range must be below 50 dBc to avoid down-conversion of strong out-of-band Wireless LAN (WLAN) interferers into the wanted bands. For

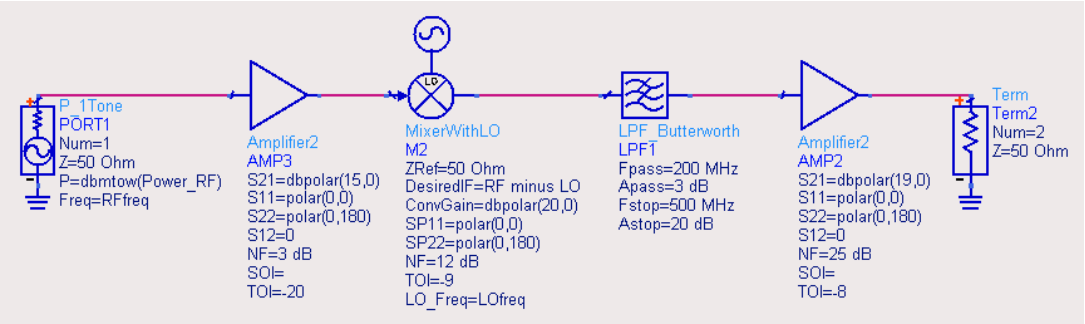


Figure 2.6: System simulations schematic.

Component	Gain (dB)	Noise Figure (dB)	IIP3 (dBm)
LNA	15	3	-20
Mixer	20	12	-9
Baseband filter	-3	3	-
Baseband amplifier	19	25	-8

Table 2.6: Receiver blocks specifications.

the same reason, the spurious tones in the 2 GHz range should be below 45 dBc to allow co-existence with the systems operating in the 2.4 GHz ISM band, such as 802.11 b/g and Bluetooth.

Finally, to ensure that the system SNR will not be degraded by more than 0.1 dB due to the LO generation, the VCO phase noise specification is set to 100 dBc/Hz at 1 MHz offset and the overall integrated phase noise should not exceed 3.5 degrees rms [5, 6].

2.4.7 Budget Simulations

In order to obtain the receiver block specifications, the simulation tool ADS has been used. The budget simulation checks the receiver chain performance to verify that the specifications of each block of the receiver allow to the entire reception chain to fulfil the specifications stated in above sections.

As starting point, a first assumption for each block parameter has been set, with the help of the state of art and the design group experience. The final value of the specifications have been set using the simulation tool ADS with the budget analysis and a iterative simulation process. Figure 2.6 shows the simulation schematic for the budget analysis. It can be observed how the entire receiver chain follows the

Receiver parameter	Specification	Budget simulation
Sensitive (dBm)	-80.8	-85
Noise Figure (dB)	7.32	7.27
Gain (dB)	48.81	50.9
Maximum input level (dBm)	-41	-35
IIP3 (dBm)	-8.65	-8.15

Table 2.7: Budget simulation results.

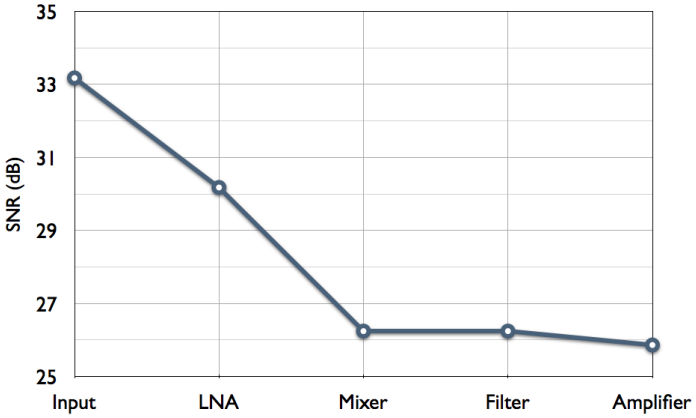


Figure 2.7: SNR budget simulation.

schematic shown in Figure 2.3.

Table 2.6 summarizes the final specifications of each receiver component, obtained from simulations. As it can be observed in Table 2.7, the budget simulation results are compliant with the global receiver requirements.

Figure 2.7 shows the SNR variation through the receiver. Obviously, at the receiver input, the SNR is the highest; however as the signal moves through the receiver chain, it is corrupted by noise and in consequence the SNR drops. The difference between the SNR at the input and output of the receiver is the noise figure. In this case, there is a different between input and output of 7.2 dB.

Figure 2.8 shows the gain contribution of each block to the entire receiver. As it can be observed, the gain specification is divided equally between the LNA, the mixer and the baseband amplifier. This situation provides a relaxed scenario for circuit designers because if one block does not reach the proposed gain, this situation could be solved increasing the gain in a subsequent block.

As it can be observed in Figure 2.9, the noise figure contribution depends mainly

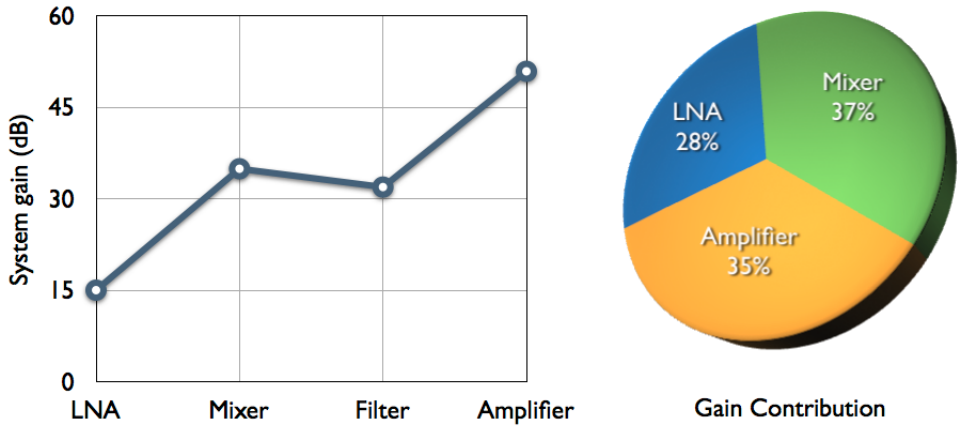


Figure 2.8: Gain budget simulation.

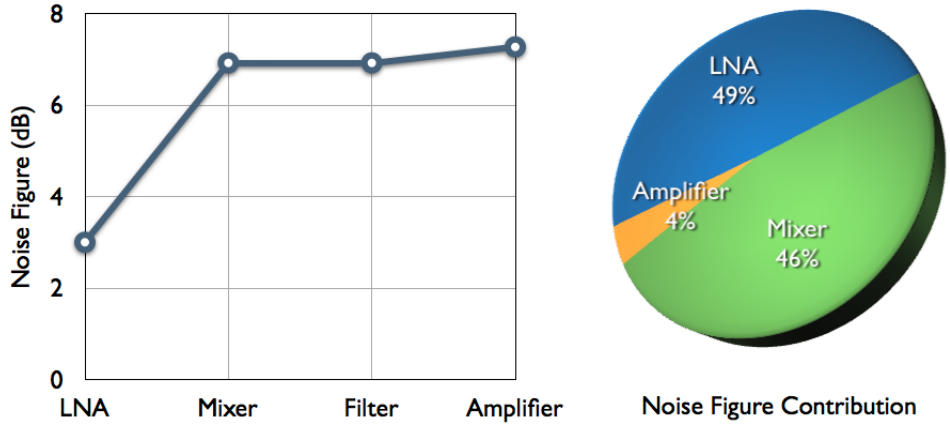


Figure 2.9: Noise figure budget simulation.

on the LNA and Mixer, so the design of those circuits will be fundamental to satisfy the noise figure specifications.

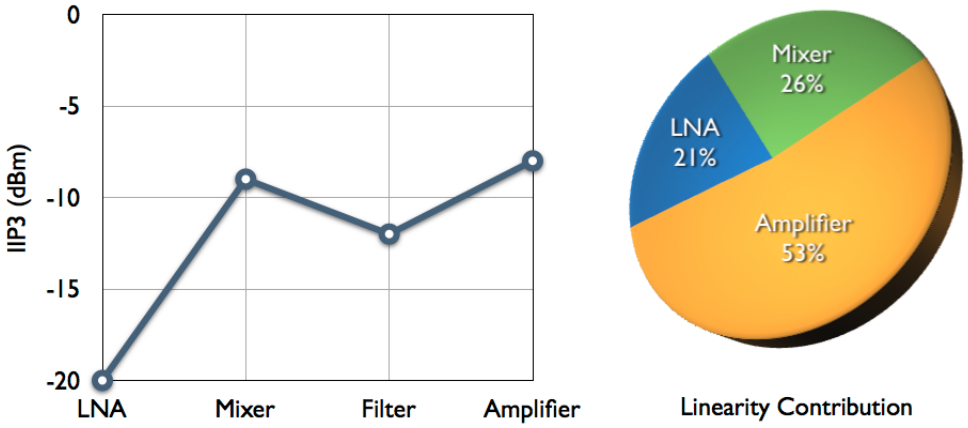


Figure 2.10: Linearity budget simulation.

Finally, Figure 2.10 shows the contribution of each individual block to the receiver linearity. In this case, the main contribution are stablished by the mixer and the baseband amplifier. In this situation the circuit designers will have to center their effort to obtain the maximum linearity in both circuits.

2.5 Conclusion

In this chapter, the history and the main characteristics of the ultra wide band standard ECMA-368 / ISO/IEC 26907 have been presented. From these specifications, a receiver system analysis has been done and validated through simulations, obtaining the individual block specifications.

Parameter	value
Gain (dB)	15
Noise Figure (dB)	3
IIP3 (dBm)	-20
Power Comsuption (mW)	minimum
Area Comsuption (mm^2)	minimum

Table 2.8: Low noise amplifier specifications.

As a summary, Table 2.8 shows the low noise amplifier specifications. These specifications will be taken as reference to develop low noise amplifiers in the following

chapters.

The next chapter is devoted to the distributed amplifier, one of the most classical structure to develop wide band low noise amplifiers.

3 Distributed Amplifiers

3.1 Introduction

The design of low noise amplifiers for ultra wide band communications has a big challenge to solve, the huge bandwidth.

Distributed amplifiers is the first approach to obtain a low noise amplifier for ultra wide band systems. With this structure a high bandwidth with a relative low noise and a moderate gain can be obtained.

3.2 Theoretical Approach

The frequency response of a MOS device degrades due to the pole formed by the input/output capacitance of the transistor and the resistance it sees. The MOSFET's transconductance rapidly falls with frequency and any attempt to increase the transconductance by increasing the size of the device will also increase its input/output capacitance. Thus, while low-frequency gain has been increased, the gain-bandwidth product remains about the same. The distributed amplification (DA) was proposed to overcome this limitation.

Distributed amplifier employs a topology in which the gain stages are connected such that their capacitances are separated, yet the output currents still combine in an additive fashion (Figure 3.1). Series inductive elements are used to separate capacitances at the inputs and outputs of adjacent gain stages. The resulting topology, given by the interlaying series inductors and shunt capacitances, forms a lumped-parameter artificial transmission line. The additive nature of the gain

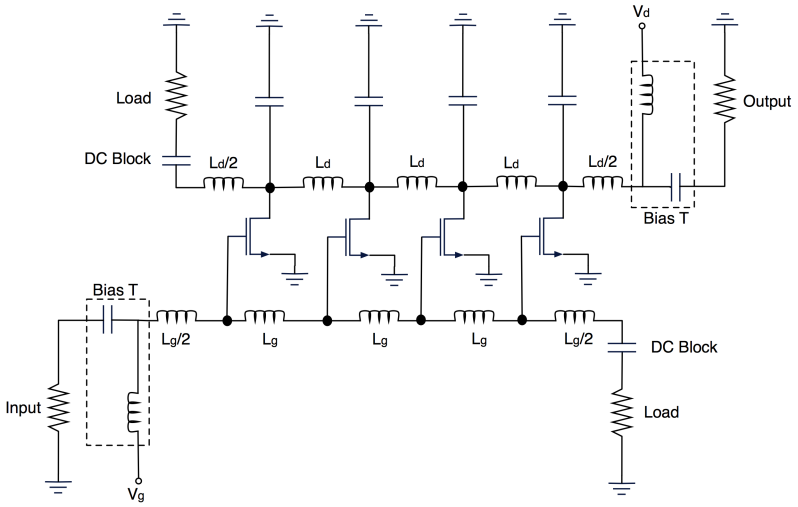


Figure 3.1: Distributed amplifier schematic.

dictates a relatively low gain; however, the distributed nature of the capacitance allows the amplifier to achieve very wide bandwidths. Distributed amplification overcomes the gain bandwidth limitation absorbing the MOS input/output capacitance as part of the lumped elements of the artificial transmission line, formed with the series inductance that connects adjacent drains and gates. The characteristic impedance (Z_0) and cut-off frequency (f_c) of lossless transmission line are given at a first approximation by:

$$Z_0 = \sqrt{\frac{L_{TL}}{C_{TL}}} \tag{3.1}$$

$$f_c = \frac{1}{\pi\sqrt{L_{TL}C_{TL}}} \tag{3.2}$$

where subindex TL accounts for the drain and gate transmission lines. Since Z_0 and f_c of both the drain and gate lines are the same, their capacitances and inductances should be the same. As the drain-to-bulk capacitance C_{db} of a MOSFET is usually less than its gate-to-source capacitance C_{gs}, a capacitor C_d is added to the drain to make the capacitances equal.

$$L_g = L_d \tag{3.3}$$

$$C_{gs} = C_{db} + C_d \tag{3.4}$$

As the amplified signals at each stage travels towards the load, the signal gets attenuated due to non-zero losses associated with the transmission lines. Finite inductors quality factor (Q) are the primary source of losses in the gate line. Losses in the drain line can be attributed to lossy inductors L_d and the drain-to-source resistance (r_{ds}). The gain of the DA can be expressed as [7]:

$$A = -g_m \frac{Z_0}{2\sqrt{1-\left(\frac{f}{f_c}\right)^2}} . \frac{e^{-N\frac{(A_g+A_d)}{2}} . sinh\left(N\frac{A_d-A_g}{2}\right)}{sinh\left(N\frac{A_d-A_g}{2}\right)} \tag{3.5}$$

where A_d and A_g are the attenuation of the drain and gate lines, g_m is the MOSFET transconductance and N is the total number of stages. This equation assumes the following:

- Unilateral MOSFET model (ignores C_{gd}).
- Image impedance matched terminations.
- Equal gate and drain phase velocities.

The optimum number of stages that maximizes the gain is a function of gate and drain line attenuation. Those attenuations are complex functions and depend on the specific MOSFET parameters and also on the operating and cut-off frequencies. As the signal propagates along the gate line towards the termination, less signal is available for each MOSFET because of attenuation and, as a consequence, the overall gain degrades with further increase in the number of stages. The number of stages for this work is chosen as 4.

Knowing the gain, number of stages, and drain-line inductance and capacitance, the required g_m can be found from the low frequency gain using Equation 3.5:

$$g_m = \frac{2.A}{N}\sqrt{\frac{C_d}{L_d}} \Rightarrow g_m = \frac{2.A}{N.Z_0} \tag{3.6}$$

Then, the transistor width-length ratio can be derived from:

$$\frac{W}{L} = \frac{g_m}{\mu_n C_{ox}(V_{gs} - V_T)} \tag{3.7}$$

Component	Value
$L_g = L_d$	1.465 nH
$L_g/2 = L_d/2$	1.15 nH
C_d	586 fF
L (transistor length)	0.425 μm
W (transistor width)	4.42 μm

Table 3.1: Calculated components values.

where

- W transistor gate width.
- L transistor gate length.
- n electron mobility.
- C_{ox} gate oxide capacitance per unit area.
- V_T threshold voltage.
- V_{gs} gate-source voltage.

Finally, the device length and width can be found by combining Equation 3.7 with the following expression:

$$W.L = \frac{C_g}{Cox} \tag{3.8}$$

Taking into consideration the previous equations and a four stage structure, a DA with a gain of 10 dB and a cut-off frequency of 11 GHz has been designed. Table 3.1 shows the calculated component values.

An important conclusion can be extracted from the previous analysis: this kind of circuits is composed by a considerable number of inductors. As it will be pointed out in the next section, inductors occupy a big amount of layout area and, as a consequence, it is very important to study the effect of inductors and their distribution over the circuit area.

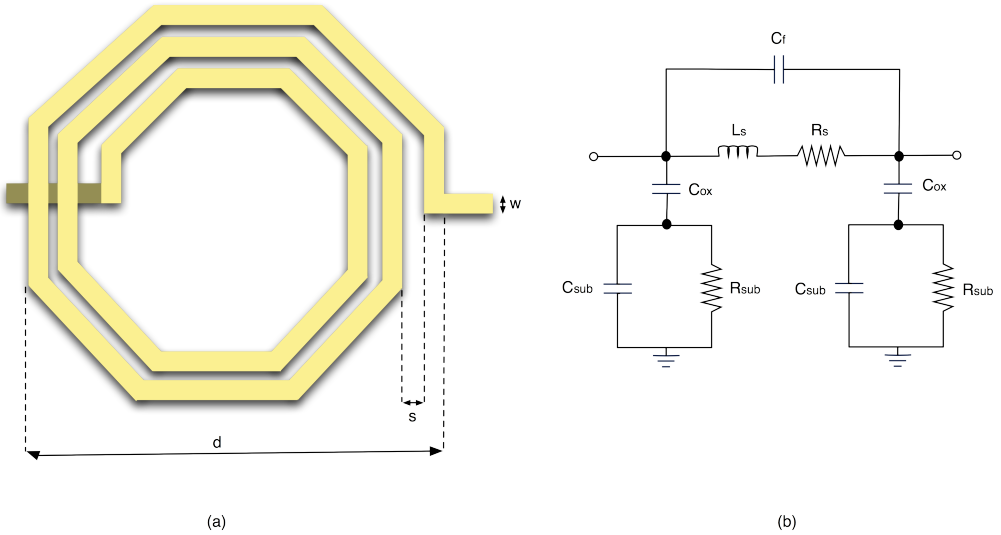


Figure 3.2: (a) Layout and design parameters for an on-chip spiral inductor. (b) Simplified lumped-component inductor model.

3.3 Area Optimization

3.3.1 Compact Design

The most evident method for reducing the area of a circuit is to compact its layout which, in the case of a DA, suggests locating the inductors as close as possible. Figure 3.2 (a) shows the typical layout of an on-chip spiral inductor. The design parameters of such structure are the outer diameter d, the metal width w, the spacing between the wiring metal s and the number of turns n. The standard lumped-element model associated to this structure is shown in Figure 3.2 (b) [8]. In this model, L_S and R_S represent the series inductance and resistance, C_F is the fringing capacitance between the metal traces and the overlap capacitance between the spiral inductor and the underpass metal, C_{OX} accounts for the spiral-to-substrate capacitance, and R_{SUB} and C_{SUB} models the behavior of leakage currents across the oxide and the substrate (bulk) and additional capacitive effects related to the substrate.

In CMOS technologies, on-chip inductors suffer from three main loss mechanisms, namely the ohmic, capacitive and inductive losses. Ohmic losses result from the current flowing through the resistance of the metal tracks. Those losses can be reduced using a wider metal line but, it also increases the capacitive losses (in particular the metal-to-substrate capacitance) causing a decrease in the overall quality factor

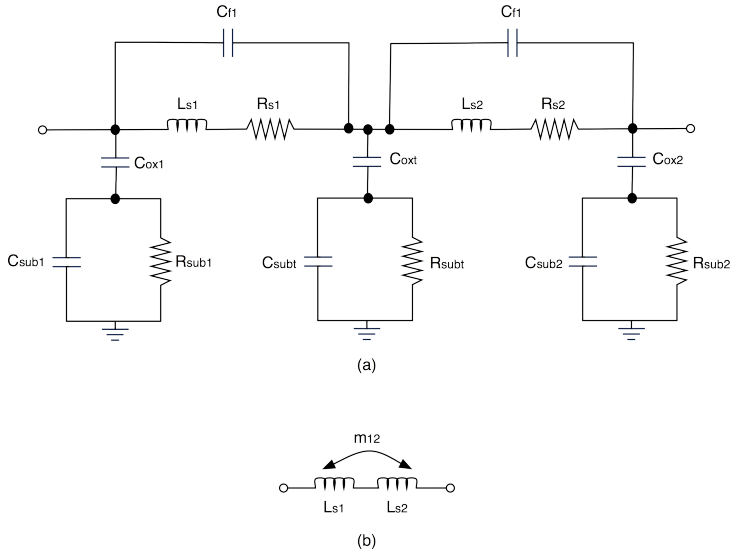


Figure 3.3: (a) Model of two on-chip inductors in series. (b) Simplified model of two inductors in series.

(Q) and self-resonance frequency (f_{SR}). The displacement currents conducted by the metal-to-substrate capacitance and eddy current generated by the magnetic flux penetrating into de substrate result in capacitive and inductive losses respectively. In the design of DA other undesired effects also appear like the mutual coupling between inductors. This fact worsens if, as stated above, inductors are situated close to each other in order to achieve a compact design.

Figure 3.3 (a) shows the electrical model of two series connected on-chip inductors, where each inductor has been modelled with the simplified lumped-element model shown previously. If the frequency range of interest is limited to few GHz, this model can be simplified neglecting substrate and metal capacitance. Other elements, such R_S and R_{SUB}, can also be of minor importance for the coupling estimation. So, stripped to its essential, the model is reduced to its inductive elements resulting the simplified circuit shown in Figure 3.3 (b).

This simplified model is composed of two series connected inductors and a mutual coupling between them. Depending on the coiling direction, the total inductance (L_T) can be calculated using Equation 3.9 or 3.10. Thus, if both inductors are coiled following the same direction, the mutual coupling is positive and if the spirals

are coiled in opposite directions the coupling is negative.

$$L_{T1} = L_{S1} + L_{S2} + 2.m_{12} \tag{3.9}$$

$$L_{T2} = L_{S1} + L_{S2} - 2.m_{12} \tag{3.10}$$

To evaluate the coupling between integrated spiral inductors, electromagnetic (EM) simulations have carried on using a commercially available planar EM simulator (Momentum). In order to get the simulator to generate useful data, the substrate definition was first calibrated. This was accomplished by using measured data from previously fabricated inductors as a reference, and adjusting the substrate definition until it produced closely correlated data [9],[10],[11].

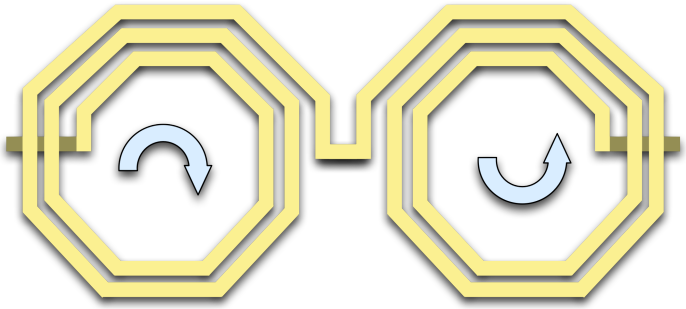
Figure 3.4 shows the layouts of the simulated structures: L_{T1}, and L_{T2}. In the first case the inductors are coiled in the same direction, whereas in the latter case both inductors are coiled in opposite directions. The simulated quality factor and inductance of both structures along with the isolated inductor response (L_P) is depicted in Figure 3.5. As it can be observed, in the case where the spirals are coiled in the same direction, the total inductance is around 7 nH at 4 GHz, i.e. more than two times the isolated inductance. Conversely, in the case where the spirals are coiled in opposite directions, the total inductance is 6.4 nH at the same frequency, that is, less than the sum of both inductances.

Regarding to the quality factor, the situation is the same. L_{T1} shows a higher Q than L_{T2} because both structures share the same series resistance but their inductances are different.

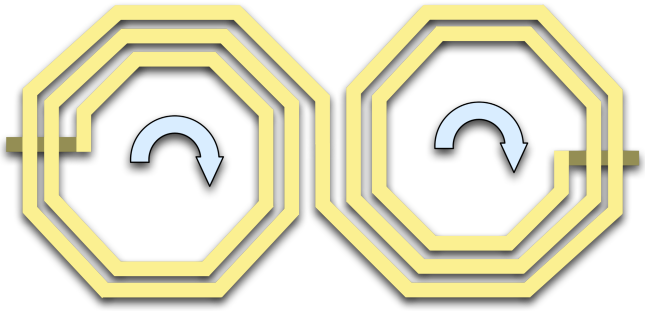
From the results showed in Figure 3.5, it can be stated that, in the design of DA where inductors are situated close to each other to reduce the chip area, it is important to correctly orientate the inductors to minimize the effect of mutual coupling.

3.3.2 Stacked Inductors

Area reduction can also be achieved by adopting a multi-level or stacked structure (MLS) [10],[12],[13],[14],[15],[16](see Figure 3.6), instead of the usual single-level structure (SLS). The main difference between these two possibilities is, in the SLS



(a) LT1



(a) LT2

Figure 3.4: Layouts of series inductors coiled in the same way (a) and in the opposite way (b).

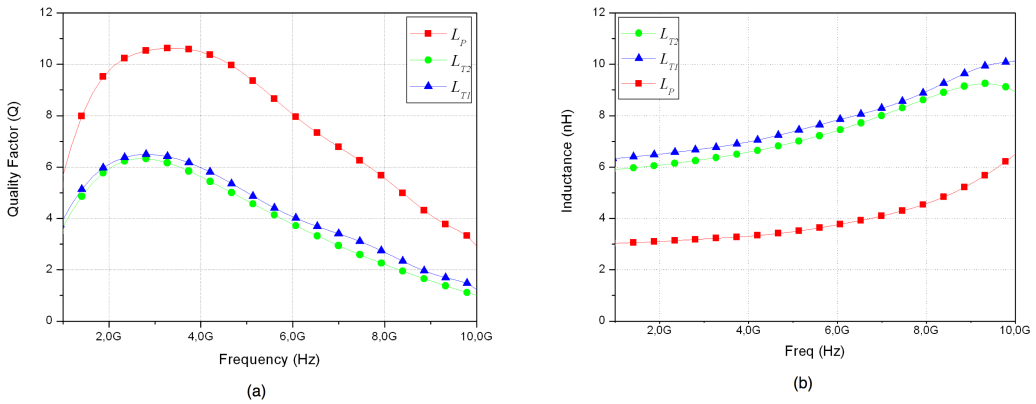


Figure 3.5: Influence of mutual coupling in series connected inductors over quality factor and inductance.

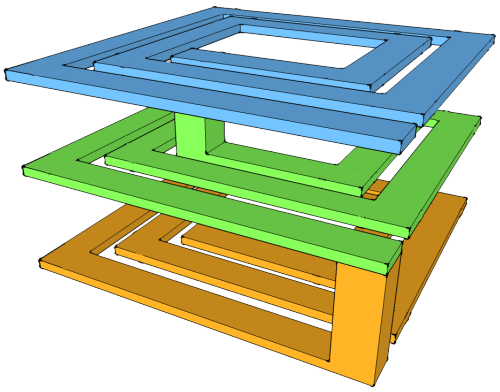


Figure 3.6: Stacked inductor layout.

case, the inductor is made with one metal layer, usually the top one because it is thicker than the lower metal layers, and in the MLS the turn is expanded vertically. This causes that, for a fixed geometry, the multilevel structure presents a bigger length than the single-level one and, as a consequence, the inductance is increased. This is the main advantage of the multilevel structure: same inductor values can be obtained occupying less area than with the single-level one.

The analysis of this type of inductors does not differ from the SLS. This is because, from the physical point of view, the metal-to-metal and the metal-to-substrate capacitances are larger in the MLS than in the SLS. Therefore the lumped element equivalent circuit that describes the behaviour of SLS can be applied to characterize the MLS.

In order to compare both structures, Figure 3.7 shows the inductance and quality factor of two 1 nH SLS and MLS inductors. As the figure suggests, the quality factor (Q) and the self resonant frequency f_{SR} of stacked inductors are lower than that of planar spiral inductors [10].

3.4 Experimental Results

In order to validate the area reduction techniques, three prototypes have been fabricated in a low cost CMOS 0.35 μm process. The circuits are called DA1, DA2 and DA3 and they correspond, respectively, to the conventional design, compact design and compact design with stacked inductors. The microphotographs of the fabricated circuits are shown in Figure 3.8. The design issues concerning the implementation

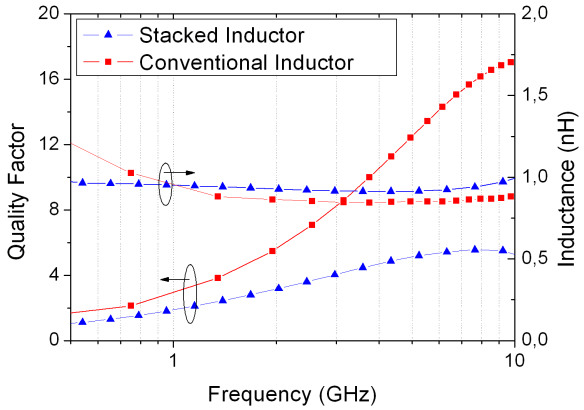


Figure 3.7: Conventional inductor Vs. Stacked inductor.

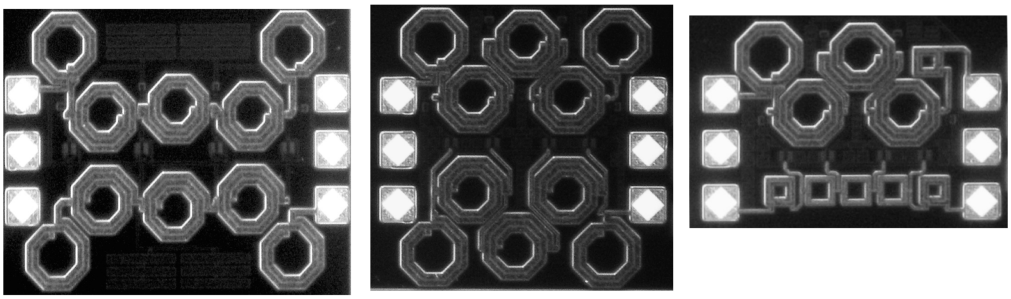


Figure 3.8: a) DA1: conventional design (0.7 mm^2), (b) DA2: compact design ($0.6mm^2$), (c) DA3: compact design with stacked inductors ($0.4mm^2$).

of the three circuits will be described in the following paragraphs.

One of the difficulties in designing a fully integrated DA is creating the required high-quality inductors. Figure 3.9 shows the simulated quality factor and inductance of the inductors used in the three designs. Table 3.2 shows the geometrical parameters of the chosen coils. The first one is a conventional planar spiral inductor and the second is a stacked inductor. The conventional inductor was used to generate $L_d = L_g$ and $L_d/2 = L_g/2$ in DA1 and DA2. As it can be observed in Figure 3.9, at 5 GHz this inductor presents a quality factor and an inductance of 9.28 and 1.3 nH, respectively. Although this inductor does not have half of the inductance than $L_d = L_g$, its physical layout perfectly match with the other components in both designs. On the other hand, the stacked inductor was used in the gate line of DA3. This circuit keeps the conventional inductor in the drain line because the current

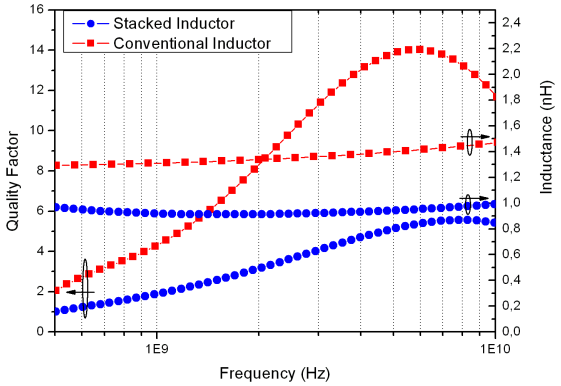


Figure 3.9: Inductors employed in the DA.

	s(μm)	n	r(μm)	W(μm)
Conventional	2	2.5	100	16
Stacked	2	2x1.5	40	10

Table 3.2: Inductors Geometrical Parameters.

flowing through this line is too high to be supported by stacked inductors.

Due to the very high frequency of operation, special attention has been paid to the layout. Thus, enough design accuracy has been achieved by adding accurate high-Q inductor model and optimizing parasitic effects coming from discontinuity and interconnection. The designed DAs utilize a transistor size of 130 μm (equivalent to a 13 gates with 10 μm gate width) and a capacitance C_d of 150 fF.

The DA1 circuit occupies an area of 0.74 mm^2, which includes the pad frame. In contrast to the conventional design, the compact design DA2 occupies a total area of 0.61 mm^2, i.e. 17% a reduction of area. Finally, the Compact design with stacked inductors DA3 occupies a total area of 0.47 mm^2 which implies a 36% of saving area.

After the measurement of several samples, the frequency response is shown in Figure 3.10. The power gain of DA1 is 6 dB with $\pm$0.6 dB flatness from 1 GHz to 5 GHz and a unity gain around 8.6 GHz. The input and output matching are better than -10 dB over the bandwidth. The increase in gain at low frequency is due to the higher impedance of the blocking capacitance at low frequency. All measurements were taken under identical DC bias condition, 3 V on the drain and 0.8 V on the gate. At this bias point the DA consumes 30 mA giving a total power dissipation

Ref.	Gain (dB)	BW (GHz)	NF (dB)	P_{1dB} (dBm)	Area (mm^2)	ft^* (Tech.)	P_{DC} (mW)	FOM^1	FOM^2
[7]	6.1	5.5	6.8	8.8	1.12	10.5(0.6μ)	83.4	151	132
[17]	5.5	8.5	10.85	N/A	2.86	10.5(0.6μ)	286	57	-
[18]	7.3	22	5.2	10	1.6	33.7(0.18μ)	52	108	95
[18]	10.6	14	4.35	5.3	1.35	33.7 (0.18μ)	52	124	106
[19]	6	27	6	10	1.62	33.7 (0.18μ)	68	107	94
[20]	4	8	5.4	8	0.84	33.7 (0.18μ)	23	208	182
[21]	10	11	4.6	N/A	1.44	33.7 (0.18μ)	19.6	119	-
[21]	16	11	4.5	N/A	1.44	33.7 (0.18μ)	100	110	-
DA1	7	6.5	5	12.3	0.74	8.13 (0.35μ)	90	231	207
DA2	7	6.5	4.5	12.4	0.61	8.13 (0.35μ)	90	282	253
DA3	5.5	6.5	6	11.2	0.47	8.13 (0.35μ)	90	364	325

[1]FOM not including P_{1dB}, [2]FOM including P_{1dB}

Table 3.3: Sumary of LNA performance and comparison with previously published designs.

of 90 mW. Finally, Figure 3.10 shows the noise response. The noise figure is under 5 dB from 1 GHz to 6.5 GHz, and it is around 7.5 dB at 8.5 GHz.

The frequency response of DA2 is approximately the same of DA1. Regarding to the noise figure, DA2 performance is better than DA1 mainly because the parasitics associated to the connection tracks have been reduced.

With respect to DA3, in spite of the stacked inductor performance is worse than the conventional ones, its response is very similar to DA1 and DA2. The noise figure is a little bit higher than that of the conventional design. This is due to the series resistance associated to stacked inductors is larger than that of conventional inductors.

Table 3.3 summarizes the performance of the presented amplifiers, with comparison to previously published DAs.

To provide an objective method to compare the developed circuits and other similar works, a figure of merit has been used:

$$FOM = \frac{P_{1dB}}{P_{noise}} \frac{1}{P_{DC}} \frac{f_h}{f_t^*} \frac{1}{AREA} \tag{3.11}$$

This expression includes the DC power consumption (P_{DC}) and output noise power ($P_{noise} = P_{th} FGain$), where $P_{th} = kT$ is the thermal noise floor given by -174

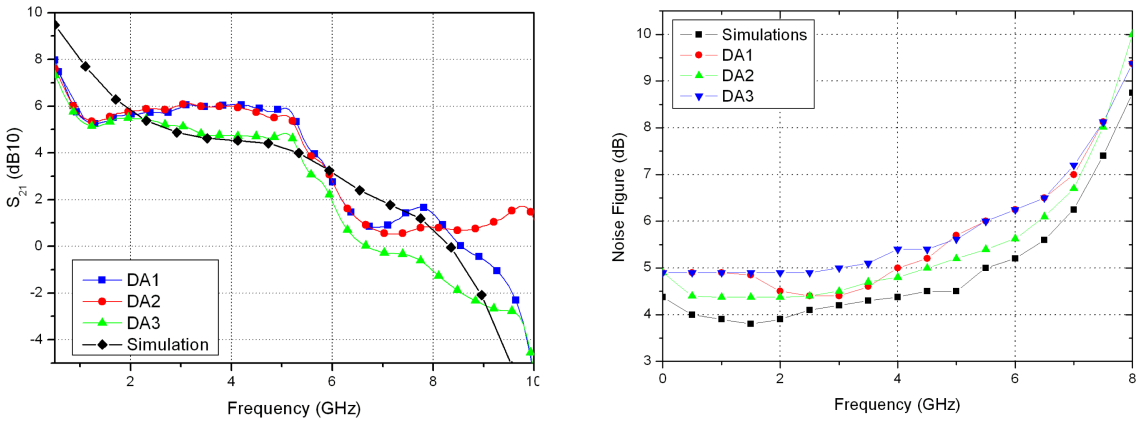


Figure 3.10: S_{21} and noise figure measurements.

dBm/Hz at T=290K. In addition, in order to quantify how efficient the available bandwidth of the technology is utilized, a relative measure for bandwidth is introduced through the f_h/f_t^* factor, where f_h is the upper LNA corner frequency and f^* is the technology unity current gain bandwidth (f_t) around the maximum of the product $(g_m/I_D)f_t$. Finally, AREA is the area occupied by the circuit and it allows comparing the designs in terms of area consumption. The proposed FOM includes the output 1-dB compression power (P_{1dB}) as a measure for linearity. However, some authors do not include this measurement and, as a consequence, two FOMs have been plotted in Table 3.3: one including the P_{1dB} and the other one without any linearity reference.

The DA presented in [7] has an excellent FOM, mainly because it utilizes very efficiently the available bandwidth of the technology. However, the area of this circuit almost doubles our designs and, as a consequence, its FOM is lower than ours. The same authors utilize a fully differential topology in [17] to achieve a wider bandwidth than its single-ended counterpart. However both, area and power consumption double and the achieved FOM is low.

The works of [18] exhibit both higher gain and bandwidth than our designs. Also the power dissipated is low being the NF similar than our designs. However, our DAs achieve better FOMs mainly because they utilize more efficiently the available area.

The low power techniques presented in [20] and [21] use a low P_{DC} to achieve low noise figure and good gain, but they are, however, fundamentally limited by large

area.

Finally the DA reported in [19] uses coplanar waveguides to implement the required inductances. This technique achieves a very high frequency of operation but at the cost of a very large area.

Regarding to the presented designs, the best FOM is achieved, as expected, by DA3. This design employs stacked inductors to reduce area. This kind of inductor occupies less chip area than that of planar spiral since the turn is expanded vertically. Usually, top metal is thicker than lower metal layers, and thus the Q-factor of stacked inductors is lower than that of planar spiral inductors. However, as the area occupation is much smaller, substrate losses are smaller, so only little performance degradation of the stacked inductor circuit is achieved over the planar spiral inductor one. This result demonstrates that it is possible to reduce the area with a minimum influence over the circuit response.

3.5 Conclusions

Design	Gain (dB)	BW (GHz)	NF (dB)	P_{1dB} (dBm)	Area (mm^2)	P_{DC} (mW)
DA1	7	6.5	5	12.3	0.74	90
DA2	7	6.5	4.5	12.4	0.61	90
DA3	5.5	6.5	6	11.2	0.47	90

Table 3.4: Distributed amplifiers specifications.

In this chapter, a first approach to low noise amplifier for ultra wide band communications has been presented. Distributed amplifiers are the most classical way to implement amplifiers with a huge bandwidth and a relative gain.

The main drawbacks of this structure are the high power consumption and the elevated area. In order to reduce the area, in this chapter two different techniques have been reported. The first one consists on reallocate the drain and gate line inductors but minimizing the mutual inductance between them. The other technique employs stacked inductors. Although the quality factor of stacked inductor is lower than planar inductor, as the area is much smaller, substrate losses are also smaller, and only little circuit performance degradation is achieved when stacked inductors

are used. Using the above techniques, three fully integrated distributed amplifiers have been designed, fabricated and tested. Table 3.4 shows a summary of their specifications.

The next chapter will explore other alternatives to implement low noise amplifiers for ultra wide band communications trying to reduce the power consumption and the occupied area.

4 Wide Band Low Noise Amplifiers

4.1 Introduction

The distributed amplifiers developed in the previous chapter exhibit a high power consumption and occupy a considerable area. In this chapter, different alternatives of low noise amplifiers will be exposed in order to reduce the power consumption and area.

4.2 Wide Band Low Noise Amplifier

4.2.1 Narrow Band Inductively Degenerated Amplifier

In this section, the typical narrow band inductively degenerated amplifier configuration is studied as it is the base of the wide band LNA.

Figure 4.1 shows the typical schematic of a narrow band LNA. The input transistor (Q_{CAS1}) is in common emitter configuration and it is the mainly contributor to the circuit noise. The noise figure of the LNA depends directly on the emitter area and on the bias of Q_{CAS1}. The cascode stage, composed by Q_{CAS1} and Q_{CAS2}, reduces the Miller capacitance, decreasing the effective base collector capacitance (C_{bc}) of (Q_{CAS2}). This makes the amplifier unilateral, i.e., with low S_{21}.

This is a requisite of many communication systems to prevent leakage of local oscillator power from the mixer back to the antenna [22]. The cascode also enhances the overall gain by increasing the output impedance. The resonant circuit composed by L and C is the load of the cascode stage. This allows a high gain with a low

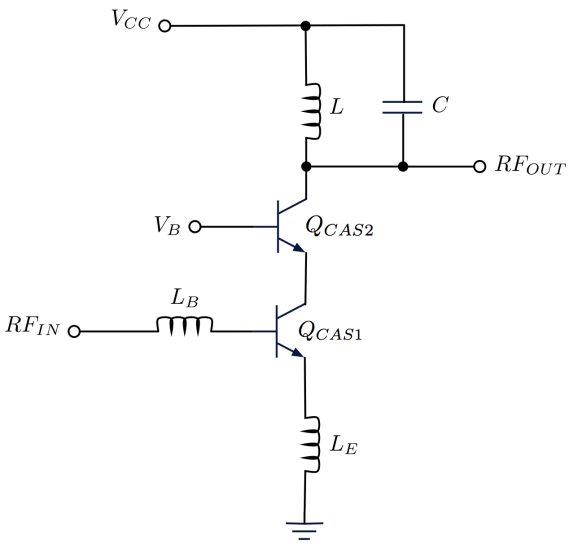


Figure 4.1: Simplified schematic of the LNA with inductive degeneration.

voltage supply. The tank resonant frequency is adjusted to the frequency of interest (ω_0).

The noise in a transistor is proportional to the transistor base and emitter resistances, r_b and r_e, and to the transistor small signal transconductance $g_m = 1/re = I_C/V_T$ (V_T is the thermal voltage and I_C is the collector current). To minimize r_b, the transistor must have a large area and to maximize g_m, I_C must be high. If the transistor area is increased, the input capacitance will also increase. This will attenuate the input signal and it will raise the NF. As a result the NF will reach a minimum for a particular combination of area and polarization current.

The next step in minimizing the noise is matching the LNA input. The antenna output impedance is 50 Ω and through inductive degeneration it is possible to match the input having an excellent trade-off between conjugate matching and minimum noise. The inductive degeneration consists on introducing a series inductance (L_E) at the emitter as it is shown in Figure 4.1. The inductance value is approximately given by Equation 4.1:

$$L_E \approx \frac{Z_0}{\omega_T} \tag{4.1}$$

The higher transistor $\omega_T = g_m/C_i$, the lower the value of L_E needed for matching, and the lower the amount of noise added to the LNA by the series resistance of the

inductor. L_E changes the real part of the input impedance, and to modify the imaginary part another inductor L_B is introduced as shown in Figure 4.1. An expression of the noise factor for the LNA with inductive degeneration that takes into account the above discussion is shown in Equation 4.2 [8]:

$$F = 1 + \frac{R_b + R_e}{Z_0} + \frac{g_m}{2} \cdot Z_0 \cdot \left(\frac{\omega_0}{\omega_T}\right)^2 \tag{4.2}$$

Alternatively this expression can be expressed as:

$$F = 1 + \frac{r_b + r_e}{Z_0} + \frac{1}{2 \cdot g_m \cdot Z_0 \cdot Q^2} \tag{4.3}$$

where Q is the quality factor of the input matching network. The noise factor improves with a higher Q because more voltage gain is seen across the input capacitance of the transistor. The input impedance is resistive only in a narrow bandwidth (ω_0/Q) around the resonance frequency ω_0. To obtain a wide band impedance matching, the Q of the matching circuit should be significantly lowered. This will largely degrade the noise figure which defeats the purpose. As a result, this type of amplifier cannot be used for wide band applications.

4.2.2 Wide Band Inductively Degenerated Amplifier

Wide band impedance matching expands the use of an inductively degenerated amplifier, by embedding the input network of the amplifying device in a multisection reactive network so that the overall input reactance is resonated over a broad bandwidth. In this way, a wide band input match is achieved and, at the same time, good noise performance is attained. In the proposed design, shown in Figure 4.2, a fourth-order doubly terminated band-pass filter is used to resonate the reactive part of the input impedance over the whole band. As long as the upper and lower cutoff frequencies (ω_U and ω_L) of the filter are far from each other, this second-order band-pass filter can be seen as a combination of two filter sections, one in a low-pass configuration and the other one in a high-pass configuration. The high-pass filter section is composed by L_B and C_π and its cutoff frequency is given by:

$$high - pass \begin{cases} L_B = \dfrac{R}{\omega_L}; C_\pi = \dfrac{1}{\omega_L R} \end{cases} \tag{4.4}$$

On the other hand, the low-pass filter section is composed by L_E and C_B and its cutoff frequency is given by:

$$low - pass \begin{cases} L_E = \dfrac{R}{\omega_U}; C_B = \dfrac{1}{\omega_U R} \end{cases} \tag{4.5}$$

These two circuits provide an input impedance equal to R in the pass-band between ω_U and ω_L.

In order to provide a wide band operation, one would think on replacing the resonant load in the narrow band circuit by a resistor. However, this would lead to gain response falling with the frequency due to the pole generated by the resistor load (R_L) and the capacitance of the output node (C_{OUT}). A technique commonly used to increase the bandwidth is to replace the load resistor by a shunt-peaking resistor [8] composed by L_L and R_L (see Figure 4.2). The addition of an inductance in series with the load resistor provides an impedance component that increases with frequency (i.e. introduces a zero), which helps offset to decrease the impedance of the load capacitance, leaving a net impedance that remains roughly constant over a broader frequency range than that of the original RC network. R_L should be sufficiently low so that the inductive region of the impedance spans the pass-band.

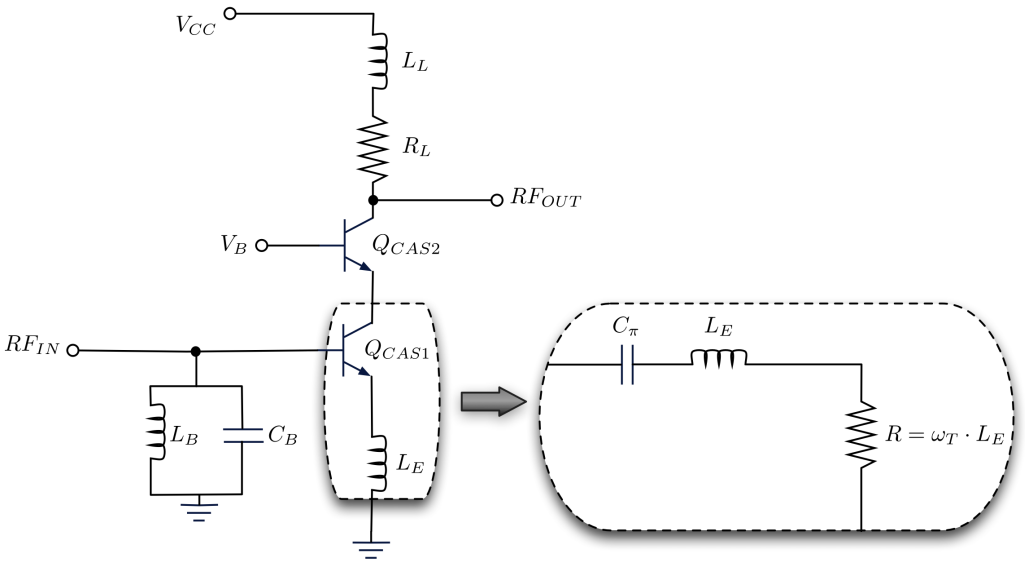


Figure 4.2: Simplified schematic of the LNA with wide band impedance matching and wide band load.

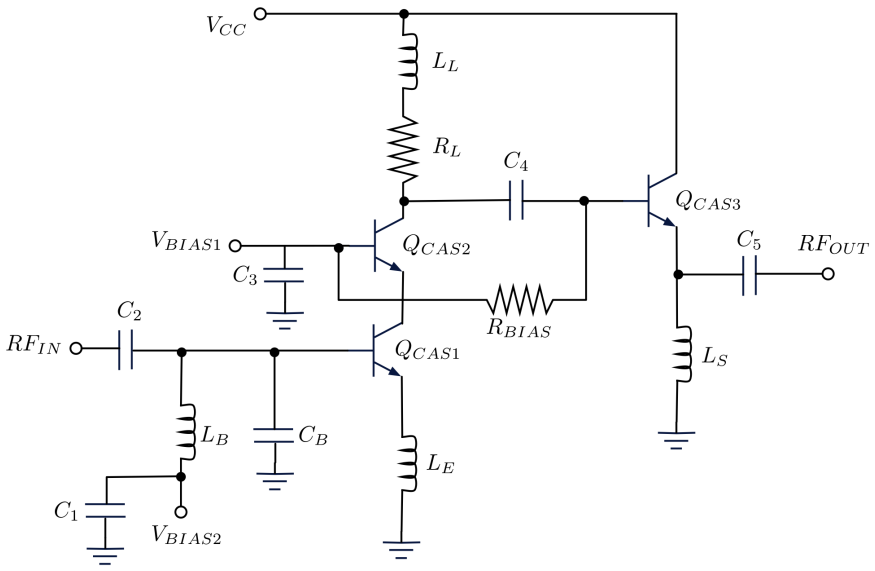


Figure 4.3: Schematic of the wide band LNA.

With this configuration the inductive load equalizes the voltage gain to a constant value across the pass-band. The problem is that C_{OUT} introduces a spurious resonance with L_L (peaking), which must be kept out-of-band. As long as C_{OUT} represents all the loading on the output node, including the transistor output capacitance, the loading by interconnect and subsequent stages and parasitic capacitances of the inductor, all these contributions should be minimized to ensure self resonance beyond ω_U.

4.2.3 Wide Band Low Noise Amplifier Design

Figure 4.3 shows the designed wide band LNA circuit. For measurement purposes, an emitter follower buffer is included to drive an external 50 Ω load. C_2 and C_5 capacitors are for AC decoupling and R_{BIAS} has a large value in order to bias the output buffer with V_{BIAS1} voltage.

The performance of a narrow band LNA is determined by the limited quality factor of the integrated inductors [23]. Its optimization relies on achieving the highest Q for a given inductance value at the frequency of operation. In the case of a wide band operation, this assumption is not convenient and a further study is needed. In shunt peaking applications, the biggest issue is the reduction of bandwidth because of additional parasitic capacitance introduced by on-chip inductors. As a conse-

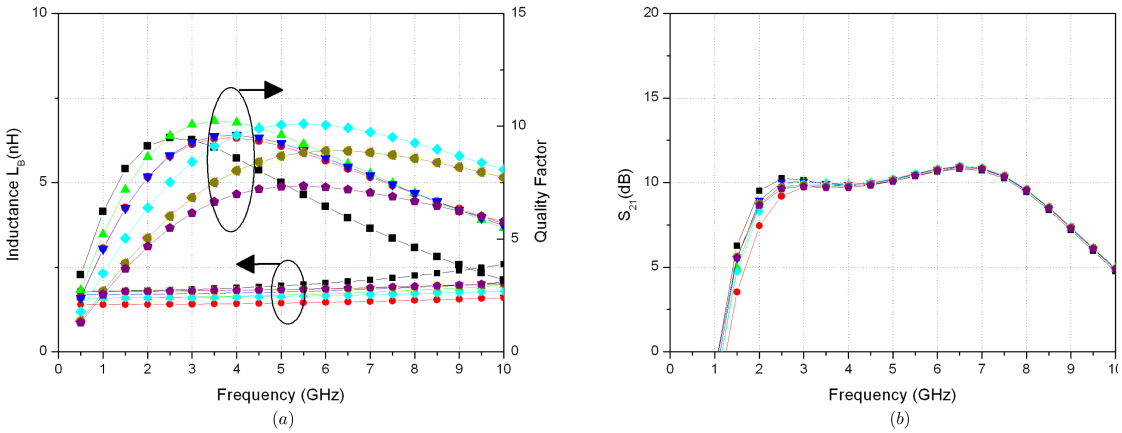


Figure 4.4: (a) Quality factor and inductance of spirals suitable for L_B. (b) Power gain for differents L_B.

quence, prior to their use in any circuit, spiral planar inductors must be modelled accurately over a wide range of frequencies. In this work, the analytical model proposed in [11] has been used to implement an optimization algorithm that provides the geometry of the inductor with the best quality factor for a given inductance value and frequency of operation. For every inductor of the circuit, a set of spirals with the same inductance but optimized for different frequencies were simulated. In order to better predict the inductor performance, S parameters from full-wave electromagnetic simulations were used to simulate the circuit. A commercially available planar EM simulator (Momentum) was used to predict the broadband response of inductors. The inductors were designed using the top level metal, which is thicker and more conductive than the rest. All of them were laid out in an octagonal fashion, with external radio (r) up to 170 μm, metal width (w) between 5 and 25 μm and up to 5.5 turns (n). The spacing between tracks is fixed to the minimum allowed by the technology, 2 μm, in order to maximize the inductance value.

The simulated quality factor and inductance of the spirals are reported in Figures 4.4 to 4.7. In the same Figures, the wide band LNA simulated power gain using the above spirals is also plotted.

As it can be seen the circuit performance is insensitive to inductors L_B and L_E quality factors. With maximum quality factor frequencies (f_{Qmax}) for L_B ranging from 2 to 5 GHz, the gain remains unaltered. Only little variations are observed at low frequency and must be attributed to the slight differences in inductance value.

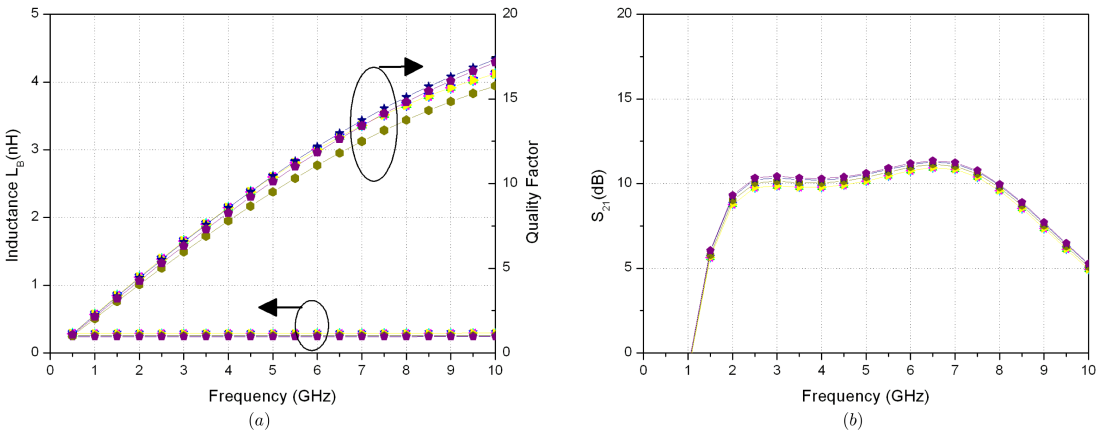


Figure 4.5: (a) Quality factor and inductance of spirals suitable for L_E. (b) Power gain for differents L_E.

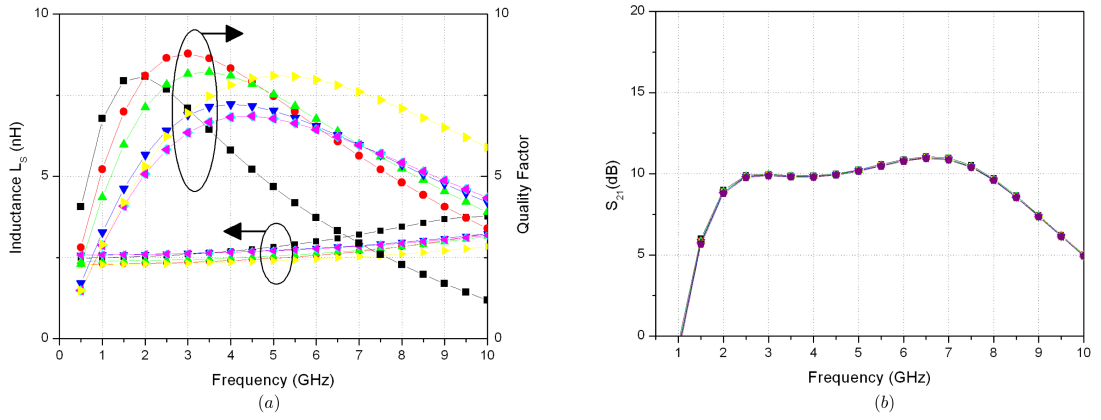


Figure 4.6: (a) Quality factor and inductance of spirals suitable for L_S. (b) Power gain for differents L_S.

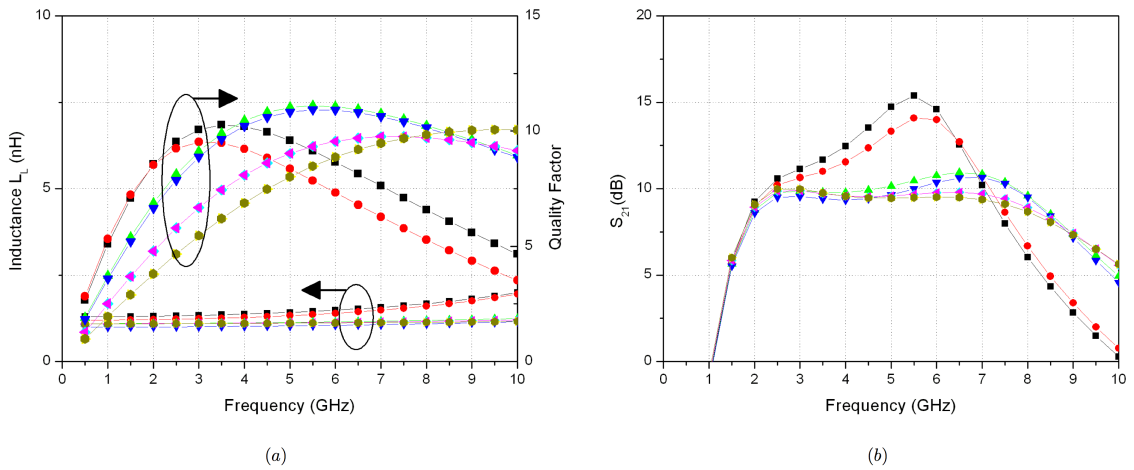


Figure 4.7: (a) Quality factor and inductance of spirals suitable for L_L. (b) Power gain for differents L_L.

In the case of L_E, the inductance value is low and the geometrical characteristics of the simulated spirals are similar. As a result, the gain flatness is not affected.

On the other hand, L_S is used for biasing purposes and does not affect in the frequency response of the circuit. However, this result no longer holds for the case of L_L. As it can be seen in Figure 4.7, the gain flatness is strongly affected by the inductor Q. The best results are obtained for inductors that exhibit an equalized quality factor through the entire band, despite of those having Q with an irregular shape through the band of interest.

4.2.4 Experimental Results

Figure 4.8 shows the final wide band LNA photography. The total chip size, including probe pads, is 665x665 μm^2. The amplifier draws 5.3 mA and the output buffer draws 6.5 mA from a 3.3 V supply.

The layout has been implemented using a 0.35 μm BiCMOS process. The amplifier was measured on wafer using a Cascade SUMMIT 9000 probe station, 35 GHz probes and 20 GHz Agilent 8720ES vector network analyzer. The probe pads were octagonal, optimized for RF. Three ground-signal-ground (GSG) and one signal-ground-signal (SGS) pad structures with 150 μm pitch were used, as depicted in Figure 4.8.

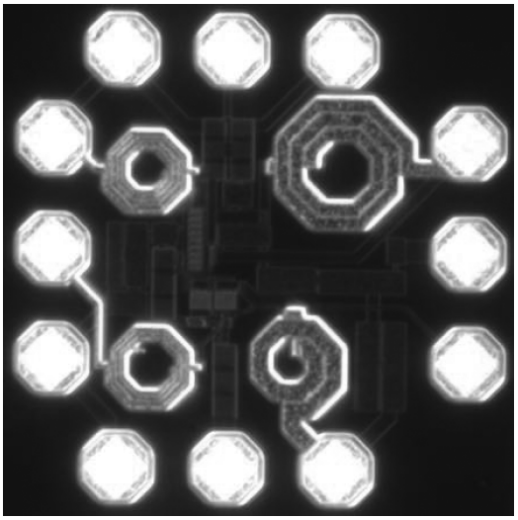


Figure 4.8: Wide band amplifier layout.

Figure 4.9 shows measured and post layout simulated S parameters of the wide band amplifier which agree quite well except the S_{22}, which is better in measurements. This is due to parasitic resonance of the output buffer which has not been taken into account in simulations. As expected, a maximum power gain of 12.5 dB was achieved at 3.4 GHz with a -3 dB bandwidth of 1.7-5.3 GHz. A unity gain was measured at 9.4 GHz. The measured input return loss (S_{11}) is lower than -5 dB over the bandwidth. The output return loss (S_{22}) has a maximum value of -4 dB due to the source follower output stage. The reverse isolation (S_{12}) is greater than 23 dB due to cascode stage. The NF measurement was done in a noise free environment with an E4440 Agilent 26.5 GHz spectrum analyzer and a 346C noise source. Figure 4.10 shows the amplifier measured and simulated NF. The NF varies from 4.3 dB at 3.9 GHz, to 5.2 dB at 5.3 GHz. This result shows good agreement between measured and simulated data. The IIP3 was measured as -4 dBm.

Measured results and a brief comparison with similar amplifiers are summarized in Table 4.1. It is shown that the designed LNA, using an cheap technology, has a good trade-off between bandwidth, noise figure, gain, linearity and power consumption. Keep in mind that although the power consumption is the highest, the circuit has been fabricated in an older technology compared to the other publications.

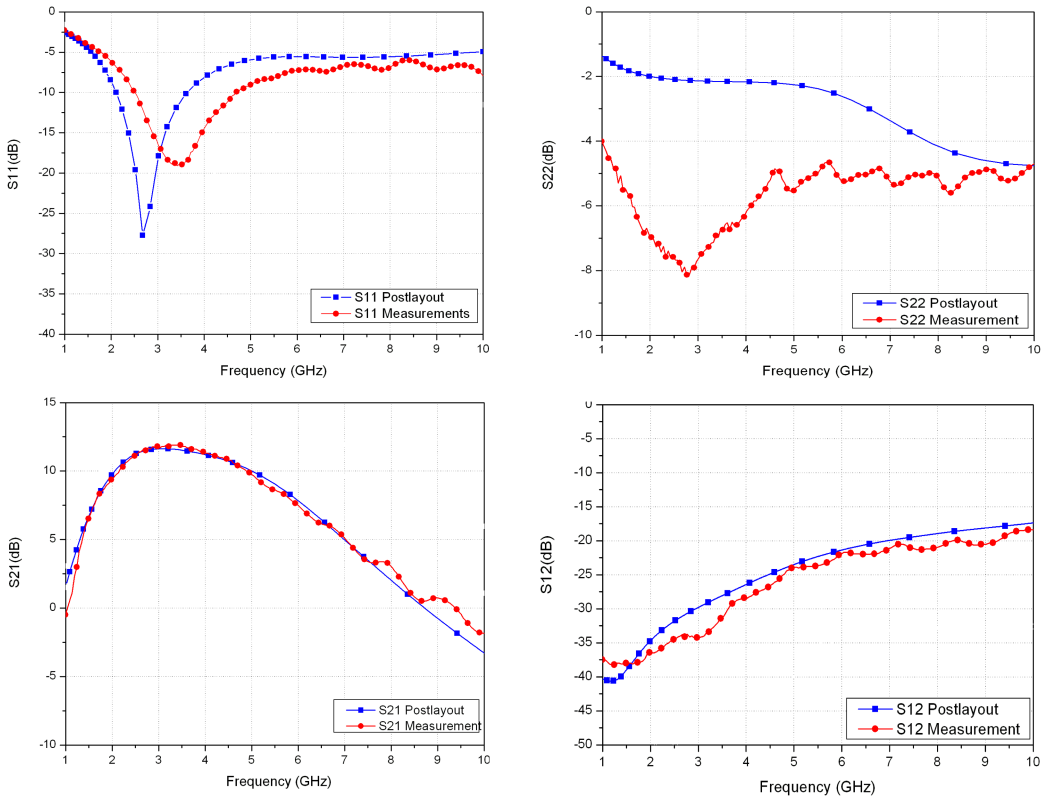


Figure 4.9: Measured and simulated scattering parameters for the designed wide band LNA.

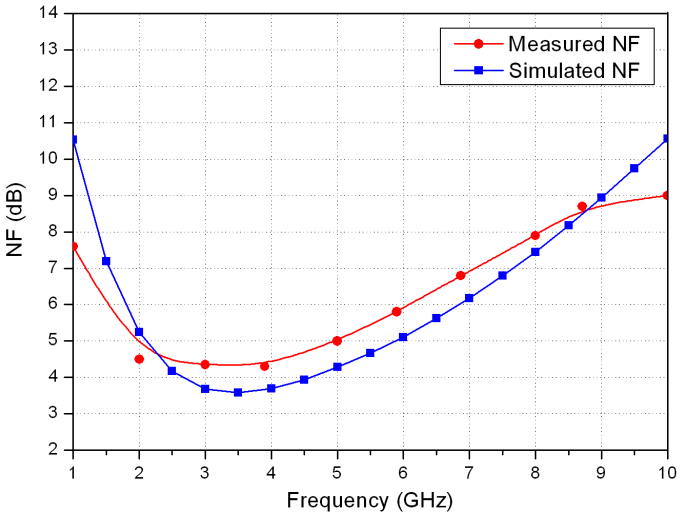


Figure 4.10: Measured and simulated NF for the designed wide band LNA.

Author	BW 3 dB (GHz)	Max. Gain (dB)	Max. NF (dB)	IIP3 (dBm)	P_{DC} (mW)	Technology	Year
[24]	3.1-10.6	9.18	7.2	7.25	23.5	0.18 μm	2007
[25]	2.0-4.6	9.8	5.2	-7	12.6	0.18 μm	2005
[26]	3.1-4.8	15	4.9	-2.2	20	0.25 μm	2006
[27]	3.0-5.0	12.7	5.02	-9.7	16.4	0.18 μm	2005
[28]	3.1-7.5	19.1	3.8	-2.2	32	0.18 μm	2006
[29]	3.0-5.0	12	4.5	-	20	0.18 μm	2009
This work	1.7-5.3	12.5	5.0	-4	32	0.35 μm	2011

Table 4.1: Comparison with recently published wide band amplifiers.

4.3 Flatness Improvement

One of the main drawbacks of the wide band amplifier is the gain flatness. Usually, to extend the gain bandwidth, the load is composed of a shunt-peaking resistor. This technique imposes an upper limit to maximum gain and flatness. To overcome this issue, a modification of the conventional shunt-peaking will be presented. In this case a CMOS technology has been used.

4.3.1 Circuit Description

The schematic of the wide band input matched CMOS LNA is shown in Figure 4.11. As in the previous circuit, it consists of a wide band input matching circuit, a gain stage with inductive degeneration (L_g and L_s) and a wide band output load. In order to buffer the output to an external 50 Ω load, an emitter follower (M3) has been included. As the figure shows, the input matching circuit consists of a filter embedded with the input impedance of M1. In this case, a third-order bandpass Chebyshev filter in T configuration was selected. In order to increase the flexibility of the filter, C_P is introduced between the gate and source of M1.

The gain stage is composed of a cascode stage where the width and polarization current of the transistors are optimized for noise and power consumption.

Figure 4.12 shows the typical shunt peaking resistor load used to provide a wide band operation [8]. With this configuration the overall amplifier gain should be flat across the pass-band. The amplifier gain is given by the product of the transistor transconductance (g_m) and the magnitude of the impedance of the shunt-peaking

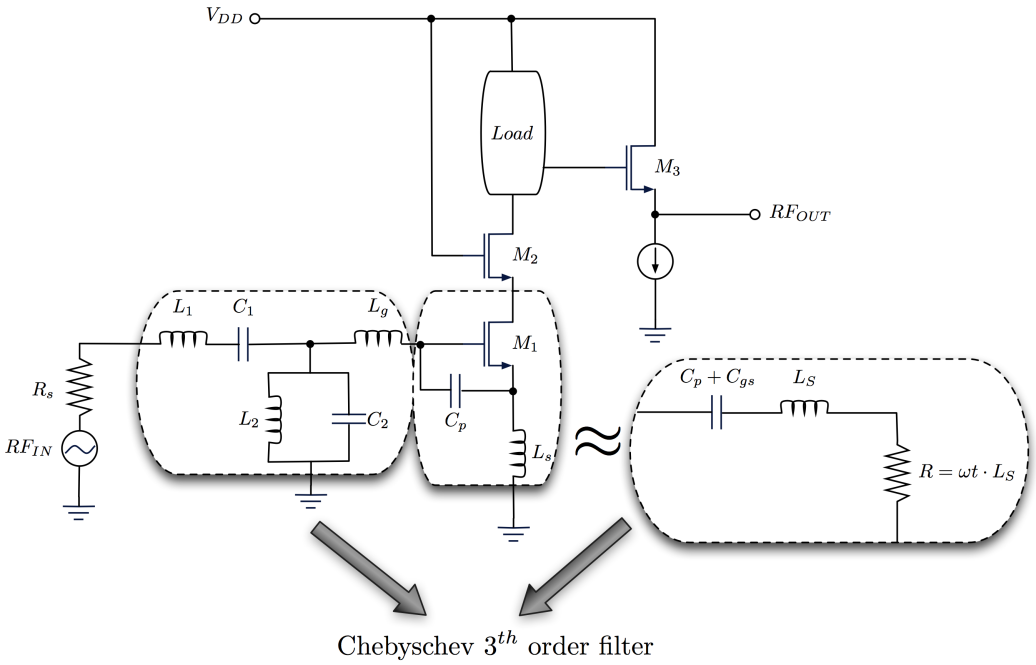


Figure 4.11: Wide band LNA simplified schematic with wide band input impedance matching.

load, given by:

$$Z_L(j\omega) = \frac{R_L + \omega L_L}{1 - \omega^2 L_L C_{out} + j\omega C_{out} R_L} \tag{4.6}$$

where C_{out} represents the equivalent capacitance at the output node, which includes the transistor output capacitance, the loading by interconnections and subsequent stages, and the parasitic capacitance of the inductor. This expression contains a zero and two complex poles. The extended bandwidth comes from the $|Z(j\omega)|$ increase due to the poles below the L_L C_{out} resonance ($\omega_0 = 1/L_L \cdot C_{out}$) and to the zero ($\omega z = R_L/L_L$). Unfortunately, this leads to a peak in the frequency response, thus degrading the flatness. As explained above, a possible solution is to keep both resonances out-of-band by using a low value of L_L, which in turn implies a low gain.

In order to have a large gain, R_L should be chosen sufficiently high to improve the gain at lower frequencies. However, the voltage headroom imposes an upper limit to R_L and, as a consequence, to maximum gain and flatness. To overcome this issue, a modification of the conventional shunt-peaking load is proposed.

The proposed shunt-peaking load is shown in the Figure 4.12 (b). It is based on a conventional shunt-peaking resistor, decoupled from the cascode stage through a

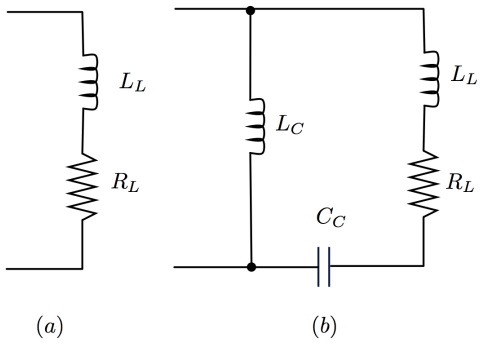


Figure 4.12: Conventional shunt-peaking load (a) and modified shunt peaking load (b).

capacitor C_C. To bias the active stage, an inductance L_C is placed between V_{DD} and the M_2 drain. The impedance of the new shunt-peaking load is given by:

$$Z(j\omega) = \frac{j\omega L_C R_L \left(\frac{j\omega L_L}{R_L} + 1\right)}{1 - j\omega^3 L_C L_L C_{out} - \omega^2 L_C R_L C_{out} + j\omega(L_C + L_L)} \tag{4.7}$$

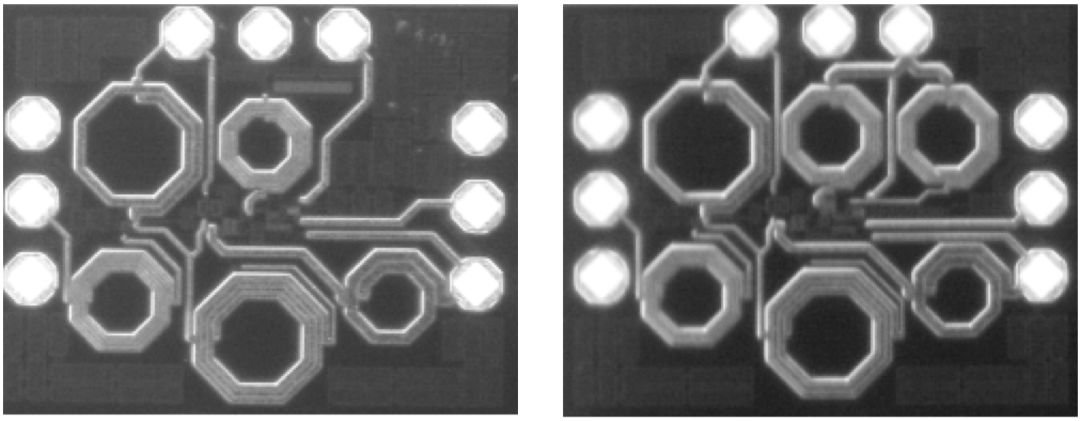
The C_C value has been chosen high; consequently, its effect is neglected and it does not appear in Equation 4.7. With this configuration, R_L can be chosen higher than in a conventional shunt-peaking load, overcoming the voltage headroom limitation. The immediate consequence is that a flatness improvement is achieved.

4.3.2 Experimental Results

To demonstrate the practical viability of the proposed structure in CMOS technology, both the proposed topology and the conventional one have been applied to a 3.1 to 4.8 GHz wide band amplifier, based on a 0.35 μm standard CMOS process. Both circuits were optimized with the pads and on-chip spiral inductors analysed with the Momentum electromagnetic simulator [30].

Figure 4.13 shows the photos of two LNAs, one with shunt-peaking load and the other with the modified shunt-peaking load, respectively. As it can be observed, the layouts are very similar with the exception of the L_C inductor in the upper right corner. In both designs the chip size, including the probe pads, is 949 x 760 μm. Each amplifier draws 17 mA from a 3.3 V supply.

The measured forward gain and input return loss of the amplifiers are shown in



(*a*) (*b*)

Figure 4.13: Photograph of the LNA with the shunt-peaking load and modified shunt-peaking load respectively.

Figure 4.14 for frequencies from 2 to 6 GHz. For the proposed shunt-peaked LNA, the power gain is fairly flat at approximately 10 dB for frequencies ranging from 3.1 to 5 GHz. However, the same cannot be said for the conventional case, where a peak is evident. To flatten the insertion gain, the zero pole frequency should be placed as close as possible to the upper edge of the band by lowering L_L. However, this entails a gain reduction, as can be seen in Figure 4.15, where the simulated S_{21} is plotted for different ideal L_L inductors. As the inductance decreases, the flatness and bandwidth increase but the gain drops.

In both amplifiers, the input return losses remain the same, because both circuits share identical input matching circuits. As a consequence, the noise figure (see Figure 4.16) is also the same in both cases.

4.4 Wide Band Folded Cascode Amplifier

In previous sections, two different alternatives to implement wide band amplifiers based on cascode topology have been presented. One of the drawbacks of the cascode amplifier is that this topology suffer from reduced linearity due to the stacking of two transistors, which reduces the available output swing.

In order to solve this problem, single transistor topologies are preferred for low voltage operation like the folded cascode LNA presented in this section.

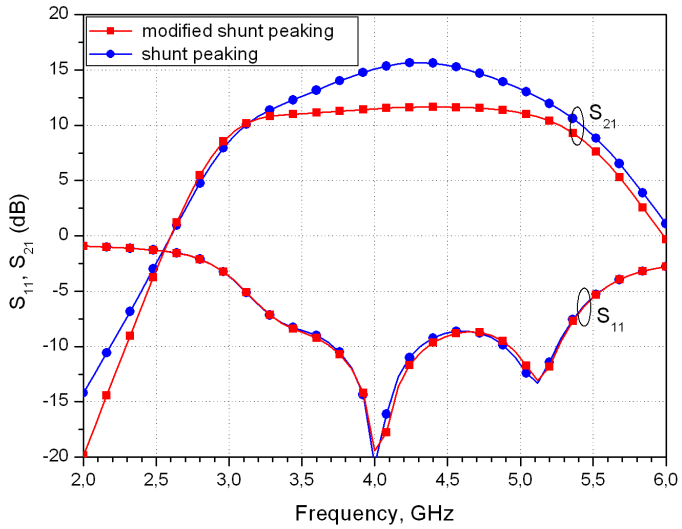


Figure 4.14: Measured S-parameters for LNA with shunt-peaking load and modified shunt-peaking load.

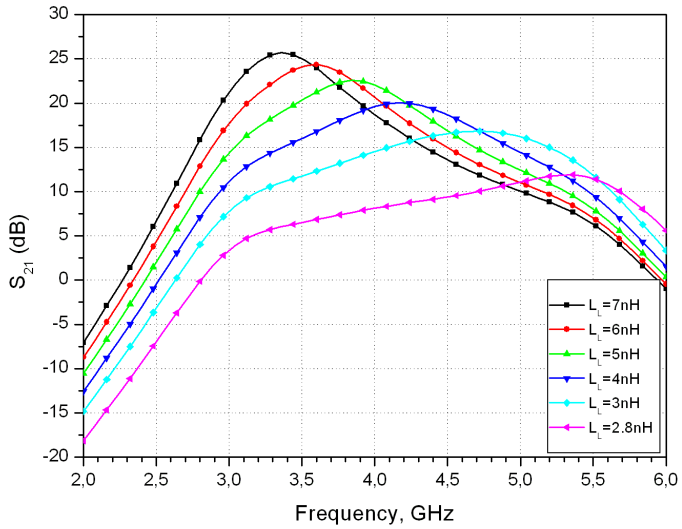


Figure 4.15: Gain simulation for different L_L inductance using conventional shunt-peaking.

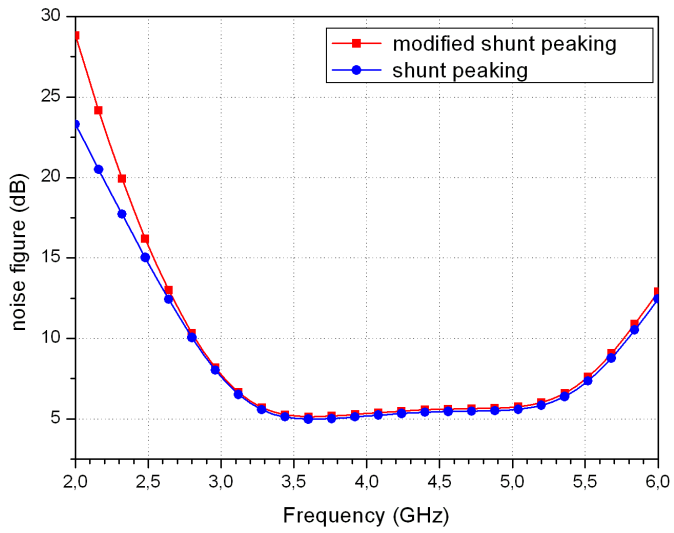


Figure 4.16: Measured noise figure for both LNAs.

4.4.1 Narrow Band Folded Cascode Amplifier

Figure 4.17 shows the typical schematic of a narrow band folded cascode LNA. The input transistor (Q_1) is in common emitter configuration and it is the main contributor to the circuit noise. The folded cascode stage is formed by Q_1 and Q_2, and the resonant circuit formed by L_L and the output capacitance (C_{out}) is the load of the circuit. This folded structure permits a high gain with a low voltage supply.

To ensure that the circuit operates as a cascode amplifier, two conditions must be met simultaneously. First, to reduce the Miller effect, the signal gain at the collector of Q_1, relative to the input RF signal, should be near unity, and second, the entire RF signal current ($g_m \cdot |v_{be}|$) generated by Q1 should be fed into the emitter of Q_2. This is done by setting the L_C tanks (L_{T1} and L_{T2}) to resonate (i.e., have high impedances) at the frequency of interest. However, due to the finite quality factors of the integrated inductors, the impedances of the LC tanks at resonance are also finite. They are given by the following Equations:

$$R_{tank1} = (Q_{tank1} + 1) \cdot R_{L1} \tag{4.8}$$

$$R_{tank2} = (Q_{tank2} + 1) \cdot R_{L2} \tag{4.9}$$

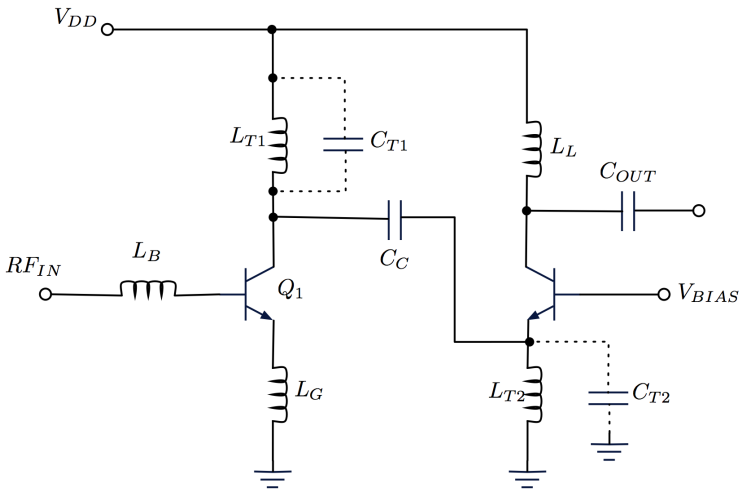


Figure 4.17: Simplified schematic of the LNA with inductive degeneration.

where R_{tankn} and Q_{tankn} are impedances and the quality factors of the LC tanks at resonance, and R_{Ln} is the series resistance of the inductors. To avoid signal losses along the signal path, two considerations must be taken into account: to minimize signal divider losses, the LC tank impedance R_{tank1} must be much larger than the impedance looking into the coupling capacitor C_C. Similarly, to avoid signal losses to ground, the L_C tank impedance R_{tank2} must be larger than the impedance looking into the emitter of Q_2 (re_2). The above constraints are summarized as follow:

$$R_{tank1} >> \frac{1}{j\omega C_C} + R_{tank2}||r_{e2} \tag{4.10}$$

$$R_{tank2} >> r_{e2} = \frac{1}{g_{m2}} \tag{4.11}$$

The main benefit of using a folded cascode topology is its ability to operate at low supply voltages or, in other words, to exhibit a high linearity operation.

Linearity is an important parameter that specifies the ability of the circuit to handle large signals. The linearity is typically measured in terms of the input referred third-order intercept point (IIP3). The IIP3 of the amplifier is equal to the IIP3 of the degenerated transistor multiplied by 2 because of the potential divider at the input across the source impedance Z_0. Neglecting the effect of the non linearity of

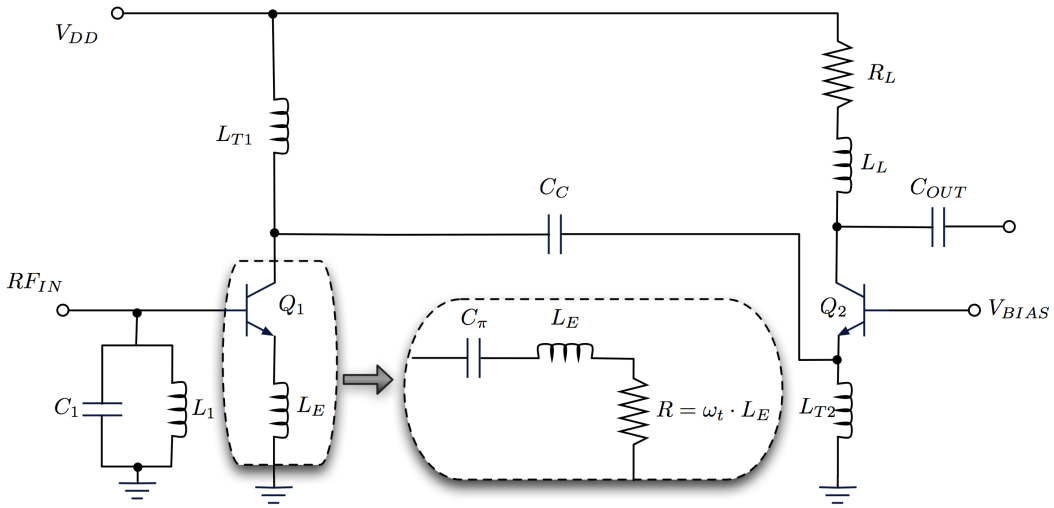


Figure 4.18: Simplified schematic of the LNA with wide band impedance matching.

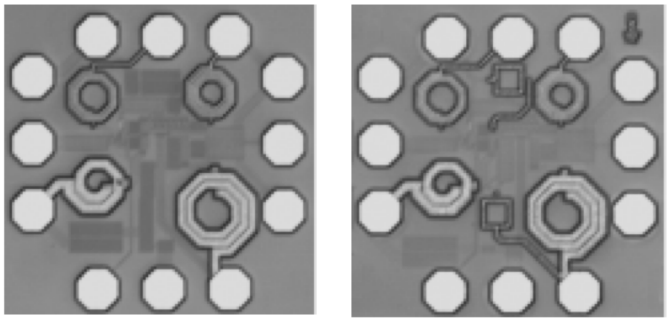
the transistor parasitic capacitor, the amplifier IIP3 is given by [8]:

$$V_{IIP3} = 4 \cdot \sqrt{2 \cdot V_T} \cdot \left(1 + \left(\frac{I_C \omega L_E}{V_T}\right)^2\right)^{\frac{3}{4}} \tag{4.12}$$

This means that, unlike the noise factor, IIP3 gets better with frequency and, to obtain a wide band operation, special care should be taken at the lower end of the band.

4.4.2 Wide Band Folded Cascode Amplifier Topology

In the proposed wide band design, shown in Figure 4.18 as in previous circuits a fourth order doubly terminated band-pass filter is used to resonate the active part of the input impedance over the whole band. The typical cascode has been divided in two different branches. The L_{T1} and L_{T2} has been added in order to bias the collector of Q_1 and the emitter of Q_2 respectively. On the other hand, the capacitor C_C has been added in order to decouple the signal between the two branches. The output load is formed with a shunt-peaking as in previous designs.



(a) (b)

Figure 4.19: (a) Cascode LNA and (b) folded cascode photograph.

4.4.3 Experimental Results

To verify the functionality of the proposed low-voltage topology, a comparison is made between two UWB LNAs: (a) the conventional cascode topology developed in section 4.2.3 and (b) the folded topology. The circuit was fabricated in the same 0.35 μm BiCMOS process than the conventional cascode amplifier. The die photographs of those circuits are shown in Figure 4.19. As it can be seen, thanks to the use of MLS inductors for L_{T1} and L_{T2}, the total chip size of both circuits is the same (665 x 665 μm). For our comparison, we have ensured that both designs were similar except for the use of the capacitively coupled resonating element in the low-voltage topology; i.e., the same transistor geometries and the same biasing conditions were used in both designs.

Figures 4.20 – 4.23 show the measurements of both LNAs. Note that the measurements include the probe pads and buffer. This worsens the performance comparing with the typical applications. In most of the wireless transceivers, the following stage of the LNA is a mixer which is a capacitive load rather than a 50 Ω load.

Figure 4.20 shows the S_{21} and S_{11} measurements of both LNAs. As expected, the response of the two designs is approximately the same. As shown in Figure 4.21, the folded cascode shows an enhanced NF with respect to the cascode LNA. This is due to the Q_2 shot noise filtering associated with the capacitively coupled resonating elements and the fact that the gain at Q_1 collector is greater than 0 dB because of the RF tanks [31].

The measured IIP3 for the cascode and folded cascode LNAs are shown in Figures

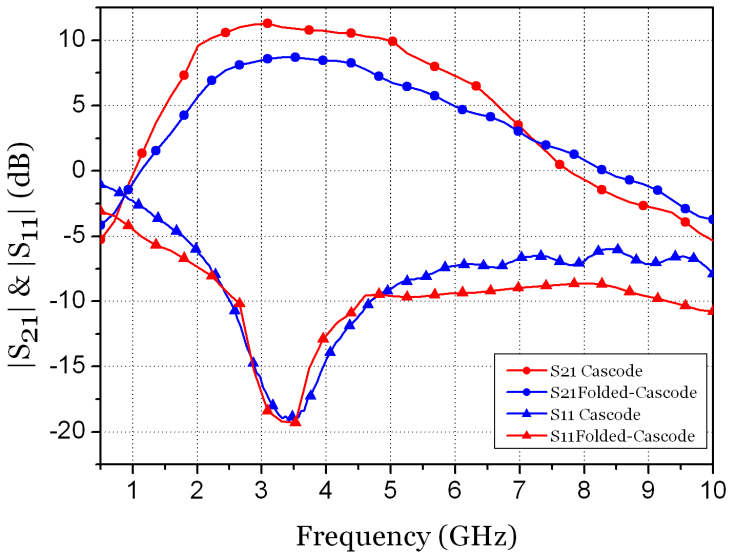


Figure 4.20: Measured S_{21} and S_{11} versus frequency.

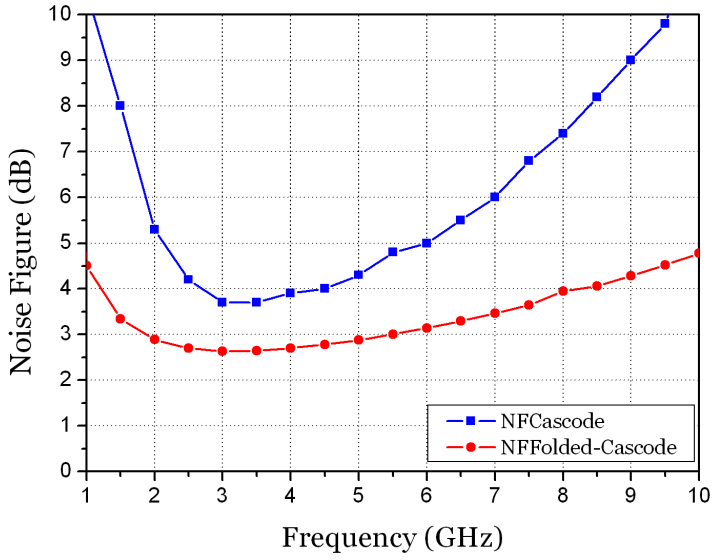


Figure 4.21: Measured noise figure versus frequency.

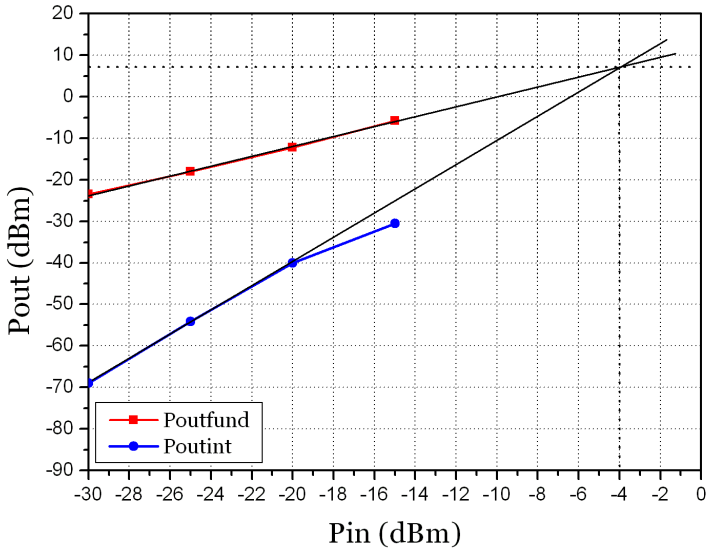


Figure 4.22: Measured IIP3 for cascode LNA.

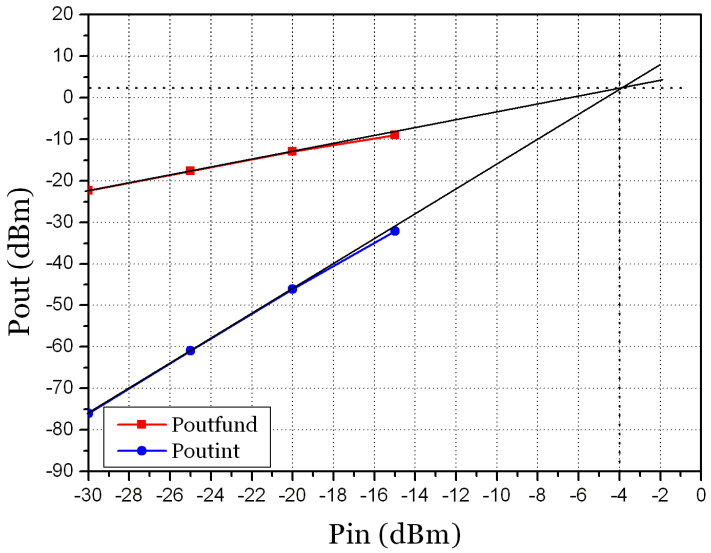


Figure 4.23: Measured IIP3 for folded cascode LNA.

Parameter	Cascode	Folded cascode
Supply voltage (V)	3	1.5
Power (mW)	18.93	18.87
$V_{CE}(Q_1, Q_2)$ (V)	1.5	1.5
$V_{BE}(Q_1, Q_2)$ (V)	0.8	0.8
NF @ 4 GHz (dB)	3.19	2.96
Gain-S_{21} @ 4 GHz (dB)	10.1	7.8
IIP3 @ 5GHz (dBm)	-4	-4

Table 4.2: Comparison between cascode and folded cascode LNA.

Design	Gain (dB)	BW (GHz)	NF (dB)	IIP3 (dBm)	Area (mm^2)	P_{DC} (mW)
Wide band Amplifier	12.5	5.3	4.3	-4	0.13	32
Modified Shunt-peaking	11.2	5	5	-4	0.29	56.1
Folded cascode	7.8	2.96	3	-4	0.13	18.93

Table 4.3: Wide band amplifiers specifications.

4.22 and 4.23, respectively. As it can be seen, the third-order input intermodulation point was determined to be equal for both designs.

In Table 4.2, a summary of the two designs is given. As Table 4.2, there is no significant degradation in performance when using the low voltage cascode.

4.5 Conclusions

In this chapter three different alternatives for ultra wide band low noise amplifier have been presented. The first alternative, the wide band amplifier, presents a good frequency response but with a low gain flatness. In order to solve the gain flatness the modified shunt peak amplifier has been introduced. Finally the folded cascode topology has a low voltage operation and high linearity. Table 4.3 shows a performance summary of these circuits.

In comparison with the distributed amplifier the circuits developed in this chapter have improved the power and the area consumption. In order to improve the area and power consumption, in the next chapter the feedback techniques will be explored .

5 Feedback Wide Band Low Noise Amplifiers

5.1 Introduction

In general, feedback techniques help to improve the amplifiers performance. The feedback loop helps to increase the gain and the bandwidth and, in some cases, even reduces the noise figure and power consumption. In this chapter, feedback techniques will be explored in order to develop a wide band low noise amplifier.

5.2 Circuit Analysis

Figure 5.1 shows a common emitter with shunt feedback. Ignoring the transistor capacitances, the voltage gain is given by

$$A_V = \frac{v_o}{v_i} = \frac{\frac{R_L}{R_F} - g_m R_L}{1 + \frac{R_L}{R_F}} \approx \frac{-g_m R_L}{1 + \frac{R_L}{R_F}} \tag{5.1}$$

where g_m is the transconductance of the transistor Q_1. This means that the gain without feedback ($-g_m R_L$) is reduced by the presence of feedback.

The input impedance of the feedback amplifier also changes with respect to the open loop amplifier. Ignoring the base-emitter capacitance, the input impedance can be given by

$$Z_{in} = \frac{R_F + R_L}{(1 + g_m R_L)} \approx \frac{R_F + R_L}{g_m R_L} \tag{5.2}$$

Feedback results in a reduction of the role the transistor plays in determining

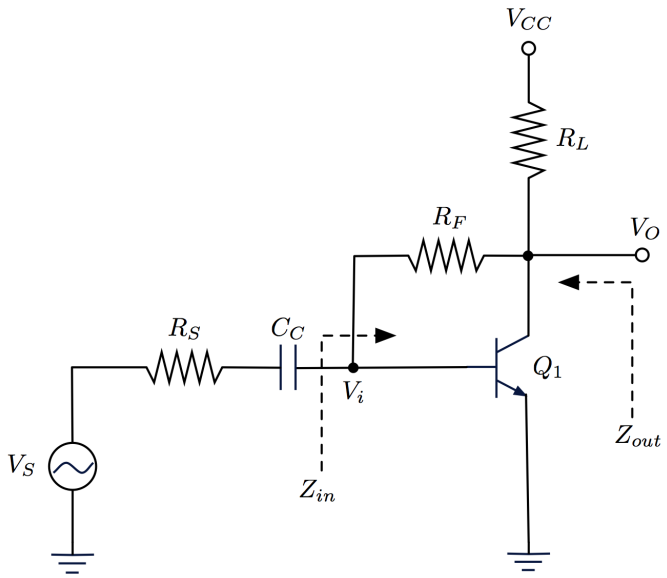


Figure 5.1: Schematic of the amplifier with shunt feedback.

the gain and therefore improves linearity. However, the presence of R_F may degrade the noise performance depending on the value of this resistor. By performing the noise analysis, a simplified expression for the amplifier's noise factor is derived:

$$F = 1 + \frac{r_b + r_e}{R_S} + \frac{1}{2g_m R_S} + \frac{g_m R_s}{2\beta} + \frac{g_m R_S}{2\beta^2} + \frac{1}{2g_m}\frac{R_S}{{R_F}^2} + \frac{R_S}{R_F} \tag{5.3}$$

where r_b and r_e are the base and emitter parasitic resistances, and β is the small signal current gain. The noise analysis shows that the feedback resistor R_F can significantly impact the overall amplifier noise figure due to its relative magnitude with respect to the source resistance, R_S. The required linearity, typically measured in terms of the third-order intercept point (IIP3), is specified by:

$$IIP3_{LNA} \propto {g_m}^2 \propto {I_{bias}}^2 \tag{5.4}$$

Intuitively, the higher the g_m, the larger the loop gain, which improves linearity [32]. A larger g_m means more current consumption. However, for high-frequency operation, more current consumption is usually needed to drive the parasitic capacitances and obtain enough gain. This results in a little flexibility in the choice of g_m. The voltage gain given by Equation 5.1 sets a relation between R_L and R_F for

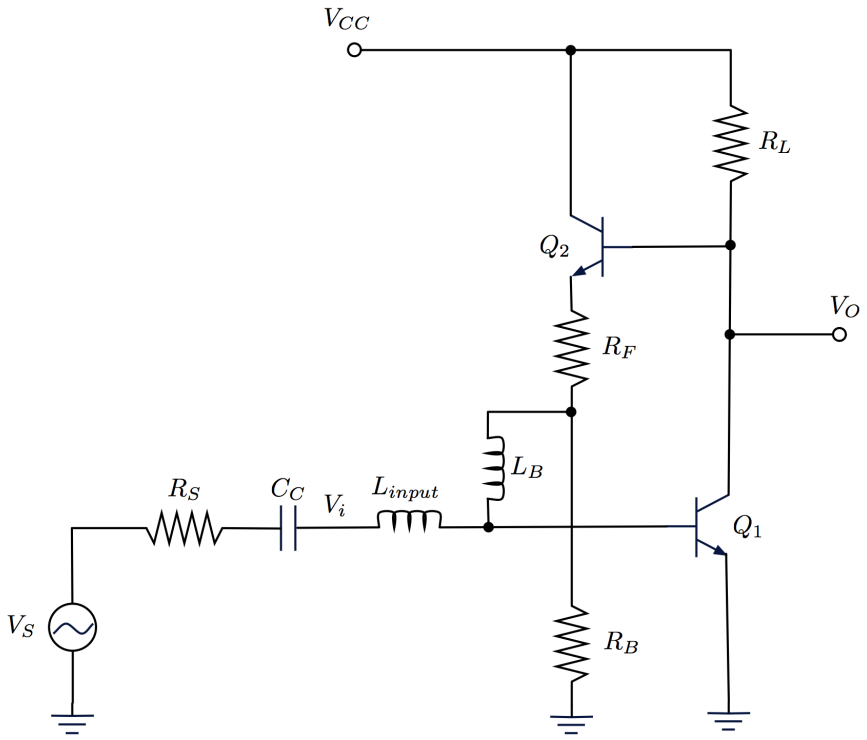


Figure 5.2: Schematic of the amplifier with active feedback.

a given g_m. As a result, the noise factor and input resistance are coupled because, as shown in Equations 5.2 and 5.3, they both depend on R_L and R_F. Because of this trade-off, it is generally difficult to achieve an arbitrarily low noise factor for an input impedance of 50 Ω with a reasonable current consumption.

To resolve this issue, the resistive feedback can be replaced by a feedback through an emitter follower. Figure 5.2 shows the proposed topology. The amplifier consists of a single stage in common emitter configuration and an emitter follower in the feedback path.

At low frequency the input impedance can be given by

$$Z_{in} = \frac{1 + g_{m2}R_F}{g_{m2}(1 + g_{m1}R_L)} \approx \frac{R_F}{g_{m1}R_L} \tag{5.5}$$

where g_{m2} is the transconductance of the transistor Q_2 in the source follower.

Under the input matching condition ($Z_{in} = 50\ \Omega$) and for the same voltage gain, the required value of R_F is now enhanced compared with the previous case, and from Equation 5.3 a low noise factor is achieved.

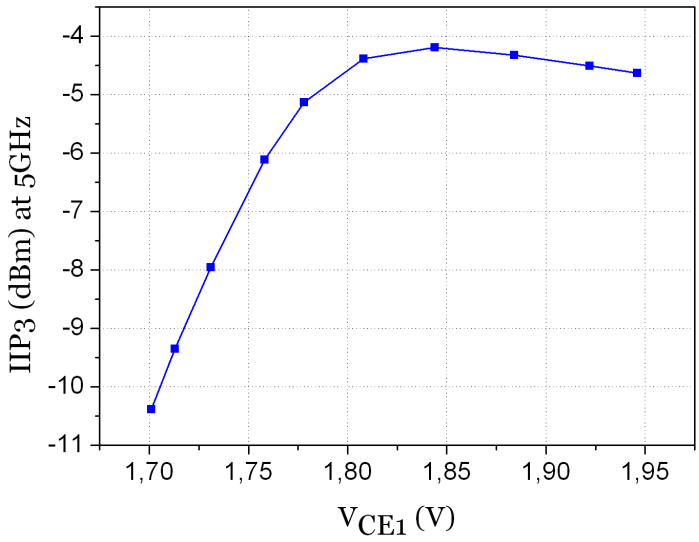


Figure 5.3: IIP3 @ 5GHz Vs V_{CE1} simulation.

Another advantage of the proposed topology is that thanks to the use of R_F, R_B, and Q_2 in the feedback path, the collector-emitter voltage of Q_1 can be modified.

$$V_{CE1} \approx V_{BE2} + V_{BE1} \cdot \left(\frac{R_F}{R_B} + 1 \right) \tag{5.6}$$

As a result, a higher f_T of the transistor and an improved large signal behaviour can be achieved. This can be seen on Figure 5.3, where the IIP3 is plotted as a function of V_{CE1}. As the figure suggests, there exists an optimum collector-emitter voltage to maximize the IIP3.

To enhance the bandwidth of an amplifier, such as in previous chapter the inductor shunt peaking technique has been used. As stated in previous chapter, this technique consists of adding an inductor in series with the load resistor to resonate out the capacitive parasitics and extend the circuit bandwidth. However, the inductance value of the added inductor can be large and this consumes much chip area.

An inductor L_B placed inside the feedback loop is proposed. Figure 5.4 shows the simulation results with several L_B values. It clearly shows that the bandwidth of the amplifier is increased when increasing L_B. However, large values for the inductance of L_B lead to peaking in the frequency response. While this allows extending the

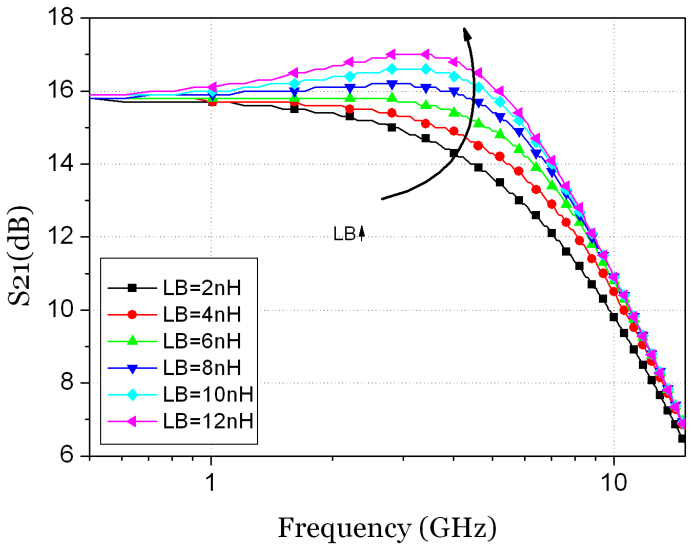


Figure 5.4: S_{21} Vs. L_B simulation.

bandwidth to higher frequencies, excessive peaking is undesirable for broadband communications systems which require a flat group delay. The quality factor (Q) of this inductor is only of minor importance in this application, due to its low noise contribution in the signal path. Indeed, the lower the quality factor, the higher the series resistance associated to it. This series resistance adds to R_F enhancing the circuit noise performance.

In this work, we propose two options to implement L_B: a conventional spiral inductor and a modified miniature 3D inductor. A detailed study of the latter will be presented in next section.

The inductor L_{input} is used to achieve a good response the whole frequency range (from 0 GHz to 15 GHz). This coil is in the direct path of the signal but its inductance value is low. Fortunately, as low inductance spirals are achieved with a small number of turns, the quality factor is high and, in consequence, its contribution to the total noise figure will be low.

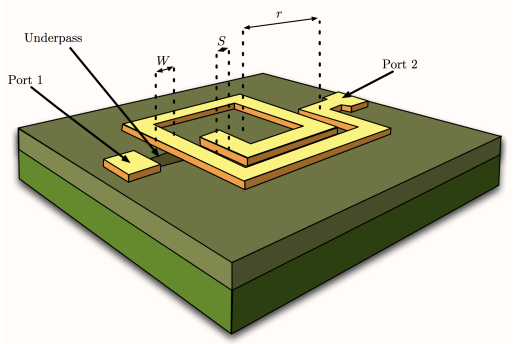


Figure 5.5: Layout and geometric parameter of and on-chip inductor.

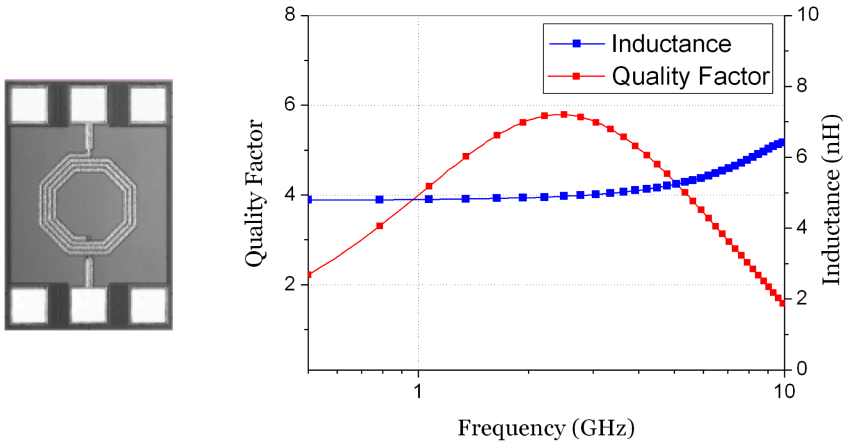


Figure 5.6: Microphotograph and measured quality factor and inductance of the proposed inductor.

5.3 Modified Miniatured 3D Inductor

As explained earlier, the conventional approach to design an integrated inductor on silicon is to layout a simple metallic spiral directly on the substrate (see Figure 5.5). At least two metal levels must be available, because an underpass is required to give access to one of the inductor's port. The challenge is to choose, for a given technology with fixed metal properties, the optimum combination of the number of turns (n), the metal width (w), the spacing between tracks (s), and the external radio (r) to provide a specific inductance and optimum quality factor at the frequency we are working on. This task is disturbed at high frequencies by the eddy current effects in substrate and metal turns and skin effect in the metal conductor.

Large inductance values typically combine with large areas and small Q_S: an

increase of the number of turns in the spiral coil or an increase of the coil radii results in an increased magnetic flux and thus a higher inductance value, but also in a proportionally higher series resistance. This can be seen in Figure 5.6, where the micro photograph and measured L and Q of a conventional high inductance spiral coil is shown (n=3.5, w=10 μm, s=2 μm and r=120 μm). The low-cost employed technology, SiGe 0.35 μm, provides four metal levels. Three of them are similar, with equal thickness and conductivity, and the top level metal is thicker and more conductive. Standard coils are designed using this top metal, which presents a lower series resistance and is far from substrate enough to work at high frequencies.

As discussed in section 3.3.2, to save some silicon area, some authors employ stacked inductors. As it can be seen in Figure 3.6, it consists of series connected spiral inductors in different metal layers. Since the spirals are identical, the inductance value of each spiral separately will be the same. Spiral inductor segments in different layers, close to each other, have positive mutual inductance between them because current flows to the same direction. So, the total inductance value of the structure will increase due to the strong mutual coupling between them, and it can be achieved high inductance in small area.

However, the use of more metal layers makes the capacitive parasitic effects amplify because of the metal-to-metal new capacitance and the increase of the metal-to-substrate oxide capacitance. Thus, the stacked inductor suffers from low self-resonance frequency. In an attempt to preserve the advantages of stacked inductor, and at the same time, to increase the resonant frequency and the quality factor, Tang et al. proposed in 2002 the miniature 3D inductors [33]. This structure consists of at least two or more stacked inductors by series connections, and every stacked inductor has only one turn in every metal layer.

For example, if there are two stacked inductors with different diameters, and one of them is a one-turn stacked inductor from the metal layer 4 to the metal layer 1, and the other is a one turn stacked inductor from the metal layer 1 to the metal layer 3, then the miniature 3D inductor is formed by connecting two stacked inductors at the metal 1, as Figure 5.7 shows.

The proposed structure for inductor L_B consists of two 3D rectangular coils serially connected through the lower metal level, as shown in Figure 5.8. This way, part of the magnetic flux generated by the coils is shared. Consequently, the structure total inductance is greater than the addition of both 3D inductance values

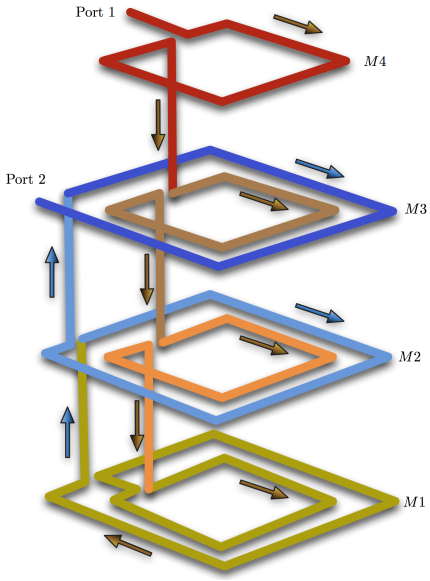


Figure 5.7: Miniature 3D Inductor.

separately.

Figure 5.9(a) shows a micro photograph of the implemented inductor. The structure occupies an area of 98 x 98 μm^2, which corresponds to the 25% of the area occupied by a standard inductor with similar inductance response versus frequency. Figure 5.9(b) shows the measured quality factor and inductance value of the proposed inductor. With this structure, in addition to reducing the occupied area a larger inductance is obtained.

5.4 Circuit Design

To test the proposed technique, two LNAs, LNA1 and LNA2 were designed using conventional and modified miniature 3D inductor for L_B. Except for the structure employed to implement L_B, both circuits follow the same design considerations. The LNAs were fabricated using AMS SiGe 0.35 μm BiCMOS technology.

It is readily seen from Equation 5.3 that the noise factor of the amplifier is determined by the collector and base shot noise of the first stage transistor Q_1, the thermal noise of the shunt feedback resistor, and the thermal noise of Q_1's base and emitter parasitic resistors. The bias current of Q_1 shall be optimized together with its emitter length for minimum noise. In our final design, the effective emitter area

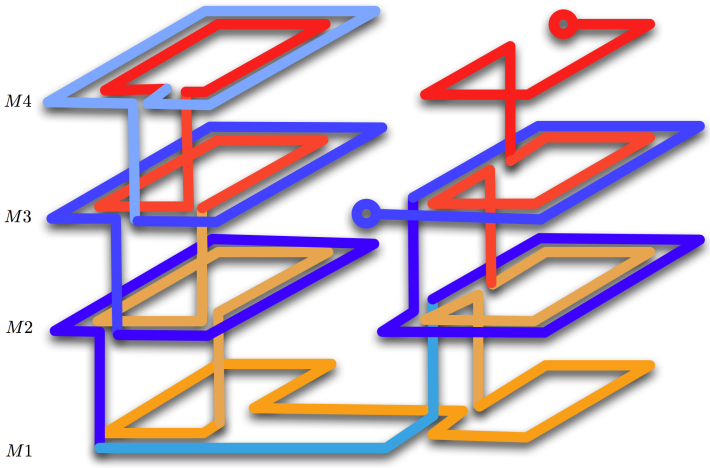


Figure 5.8: Modified miniature 3D Inductor.

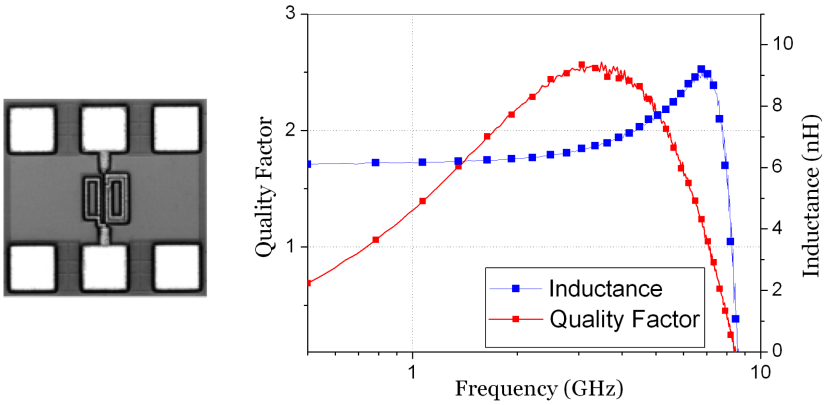


Figure 5.9: Microphotograph and measured quality factor and inductance of the proposed modified 3D inductor.

of Q_1 is 36 μm^2. The emitter follower Q_2 contributes only little to the output noise and an effective emitter area of 1.6 μm has been chosen.

The feedback resistor, R_F, has a large impact on the noise factor. To reduce its noise contribution, a large value shall be used in conjunction with the consideration for input impedance match. The choice of the feedback resistor determines the operating bandwidth. Low R_F increases the operating bandwidth with the sacrifice of the gain and noise performance. The use of the peaking inductor L_B in the feedback path allows alleviating this trade-off, and its inductance value should be chosen as high as possible up to where it can meet the bandwidth requirement without excessive peaking. As explained in previous sections, the quality factor of inductor L_B is not relevant. In this case, achieving a high-value inductance in a small area is the major requirement. For that reason a modified miniature 3D inductor could be a better solution for L_B. A different situation is observed for L_{input}. This inductor is in series with the input and is used to help matching the input impedance within the entire band. Its quality factor should be as high as possible, since its value affects the overall noise performance. As the required inductance value is low, a conventional spiral inductor can be used in the implementation (1.5 turns).

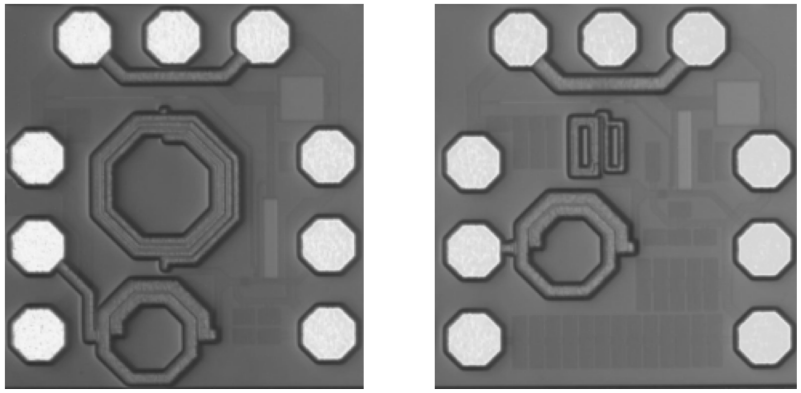
The load, consisting of a poly-silicon resistor R_L, is designed to achieve a flat broadband gain over the entire UWB band. According to analysis showed in previous sections, amplifier linearity depends on V_{CE1} selection through the feedback circuit. The value of R_B is chosen to maximize IIP3 and is calculated using bias current and supply voltage to bias the device at its low tolerance point to the distortion.

5.5 Experimental Results

The die photographs of LNA1 and LNA2 are shown in Figure 5.10. The chip area excluding the test pads is 490 x 355 μm^2 for LNA1 and 330 x 310 μm^2 for LNA2. Note that the proposed technique achieves a 40% of area reduction, and as we will show later, with minor performance degradation over the same circuit implemented with conventional inductors.

The S parameters and the noise figure of both circuits were measured using ground-signal-ground microwave probes. Both circuits operate with a supply voltage of 3.3 V and consume 4 mA.

Figures 5.11 and 5.12 show the measured gain and noise figure for 50 Ω source



(a) (b)

Figure 5.10: Chip photograph of (a) LNA1: with conventional spiral inductor and (b) LNA2: with modified miniature 3D inductor

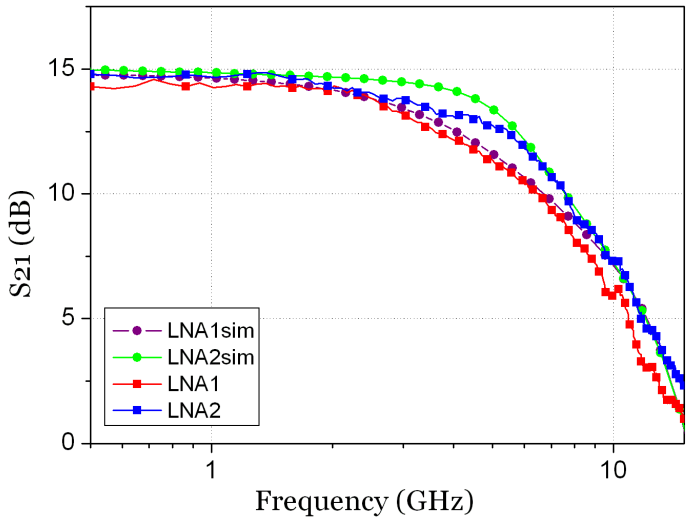


Figure 5.11: Simulated and measured gain.

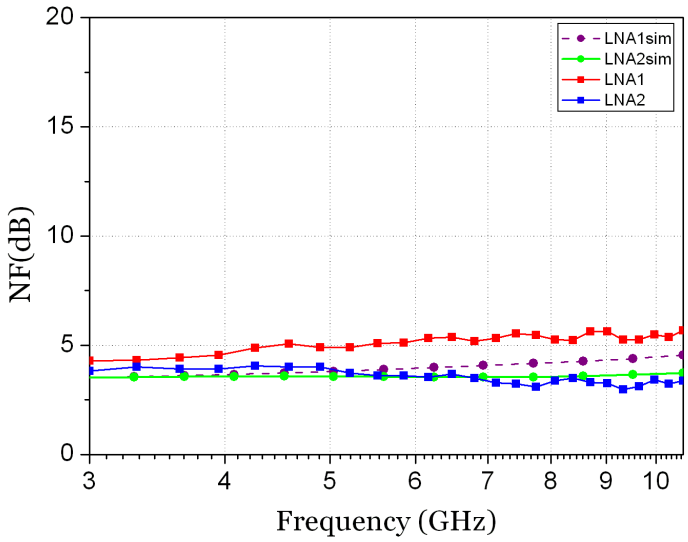


Figure 5.12: Simulated and measured noise figure.

and load impedance. Both amplifiers provide a gain which varies from 14 dB to 7 dB in the band between 3.1 GHz and 10.6 GHz, being greater than 1 dB from 0.1 GHz to 15 GHz. The gain response is flat, which indicates that no excessive peaking was employed to obtain the desired bandwidth. The low frequency gain of LNA1 is 15 dB and the 3 dB bandwidth is 5.5 GHz. For LNA2, the gain is similar but the bandwidth is higher (6.7 GHz). This is due to the greater L_B inductance value obtained with the 3D inductor (6 nH) compared with the conventional spiral inductor (5 nH). Another positive effect associated to the use of a 3D inductor in the feedback path is an improved noise performance. As shown in Figure 5.12, the measured noise figure of LNA1 is 4.2 dB for low frequencies and rises to 5.6 at 10.6 GHz. The noise figure of LNA2 is between 2.9 dB and 4 dB from 3.1 GHz to 10.6 GHz. The noise figure improves at high frequencies due to the added resistance associated to the low Q 3D inductor.

Figure 5.13 shows the measured input and output return loss of both amplifiers. S_{11} and S_{22} for LNA2 are lower than -9 dB between 3.1 GHz and 10.6 GHz.

The two-tone test for third-order intermodulation distortion (IIP3) is shown in Figure 5.14 for LNA1 and LNA2. The test is performed at 5 GHz. Tone spacing is 100 KHz. LNA1 and LNA2 achieve an IIP3 of -3.4 dBm and -4.4 dBm, respectively.

The measurement results of the two wide band LNAs and several previously

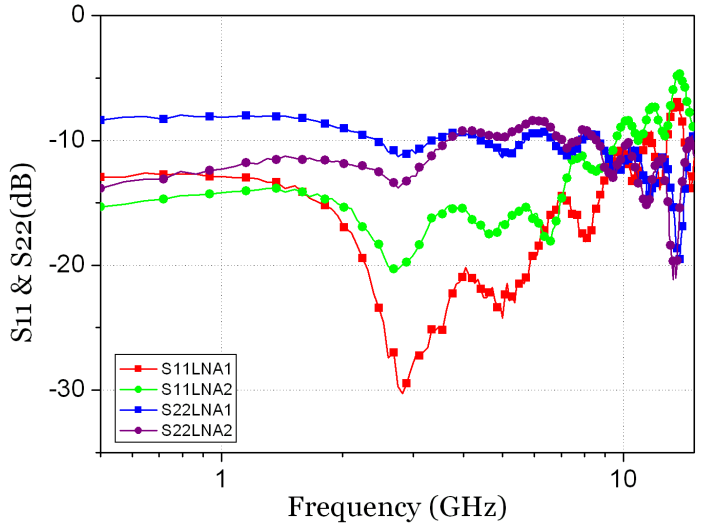


Figure 5.13: Measured input and output return loss (S_{11} and S_{22}).

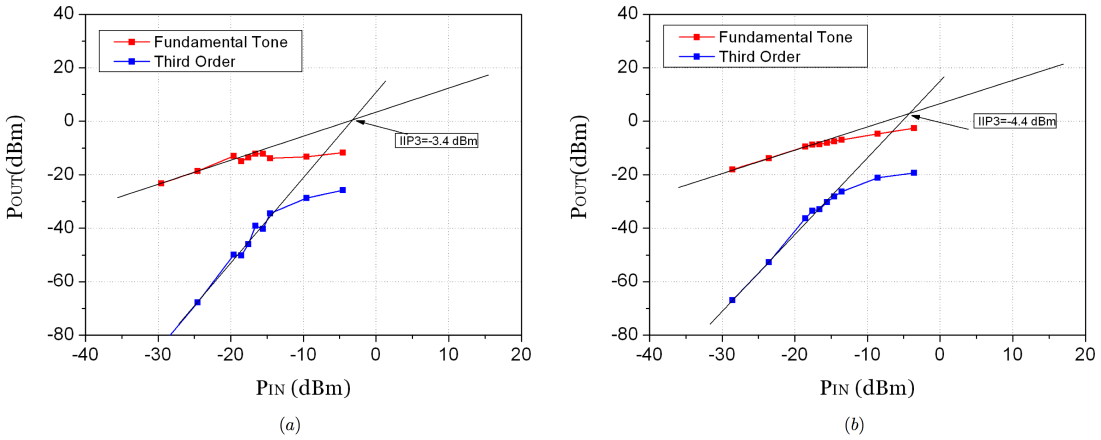


Figure 5.14: Measured two tone test at 5GHz (a) LNA1 (b) LNA2.

Ref.	S_{21} (dB)	NF (dB)	3dB BW (GHz)	IIP3 (dBm)	P_{dc} (mW)	Active Area (mm)	Tech.
[34]	9.3	<9	2-23	-6.7	9	1.1	0.18μm CMOS
[35]	21	<4.5	2-10	>-5.5	30	0.55	0.18μm SiGe
[36]	9.3	<9.2	2.3-9.2	>-6.7	9	0.66	0.18μm CMOS
[37]	8.5	<5.3	1.3-10.7	>8	4.5	1	0.18μm CMOS
[37]	8.2	<5.5	1.3-12.3	>8	4.5	1	0.18μm CMOS
[18]	10.6	<5.4	0.01-14	>10	52	1.35	0.18μm CMOS
[38]	20	<4.5	3-10	>-11.75	42.5	0.18	0.18μm CMOS
[39]	22	<3.9	3.1-14.5	>-32.5	13.2	0.49	0.18μm SiGe
[40]	15.3	<2.98	3.1-10.6	>-8.5	9	0.87	0.25μm SiGe
[41]	12	<4	2-10	>1.9	24	0.25	0.13μm CMOS
[42]	13	<3.3	2-10	>-7.5	9.6	0.88	0.18μm SiGe
[42]	11.5	<3.5	2-10	>-7.5	7.2	0.88	0.18μm SiGe
[43]	11.5	4.7	3.1-10.6	-10	10.57	0.665	0.18μm CMOS
Std.ind	14	<5.6	0.1-5.5	>-3.4	13.2	0.1	0.35μm SiGe
3D ind.	14	<4	0.1-6.7	>-4.4	13.2	0.1	0.35μm SiGe

Table 5.1: Comparative Results.

published results are listed for comparison in Table 5.1. As shown in Table 5.1, the modified 3D inductor active feedback LNA achieves low noise figure, high gain, and high IIP3 while simultaneously occupying the lowest area yet published in a commercial SiGe BiCMOS process.

5.6 Conclusions

Design	Gain (dB)	BW (GHz)	NF (dB)	P_{1dB} (dBm)	Area (mm^2)	P_{DC} (mW)
Standard Inductor	14	5.5	< 4	-3.4	0.17	13.2
3D inductor	14	6.7	< 4	-4.4	0.10	13.2

Table 5.2: Wide band feedback amplifiers specifications.

In this chapter other alternative to implement wide band low noise amplifiers has been presented. In this case, a feedback low noise amplifier has been presented. In order to reduce the area, a modified 3D inductors have been used.

Table 5.2 shows a performance summary. In comparison with the developed circuits in previous chapters, the feedback amplifiers have the better performance with the minimum area and minimum power consumption.

In spite of area saving with the developed circuits, the most part of the area is occupied by the integrated inductors. In order to find the maximum area saving, the next chapter is devoted to the explore the inductorless techniques.

6 Inductorless Techniques

6.1 Introduction

The number of inductors and the area occupied by them is an inconvenience in radiofrequency integrated circuit design. In previous chapters, an area saving has been achieved with different topologies of inductors but the inductors are still necessary in these designs.

In order to reduce the area consumption, it is important trying to avoid the use of inductors, for this reason, this chapter is devoted to explore the inductorless techniques with the design of a front-end based on a common gate LNA inductorless and a quadrature Gilbert cell mixer.

6.2 Common Gate LNA

Common-gate (CG) LNA is a widely used topology in wireless communications [44],[8],[4],[45]. In this section, the CG LNA is studied, i.e., the relationship between the input matching and voltage gain or the noise figure.

6.2.1 Input Matching and Voltage Gain

The desired input impedance of a CG input stage is achieved by adjusting the bias current, aspect ratio, and overdrive voltage. Thus, for an input impedance of 50 Ω, the objective is to obtain $1/g_m$ of approximately of 20 mS . The CG stage does not suffer from the Miller effect, and thus an adequate reverse isolation can be achieved

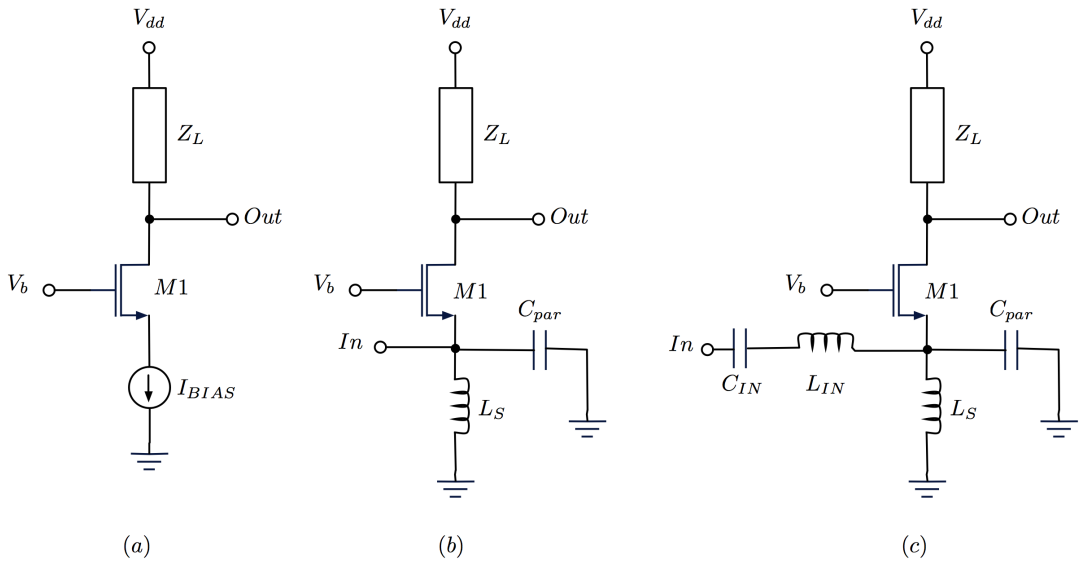


Figure 6.1: Common-gate LNA imput interfaces: a) current source, b) parallel LC resonator, and c) series and parallel LC resonators.

with a single transistor stage. Therefore, the input matching network and load can be designed separately.

Large impedance towards the signal ground is needed to steer the signal into the input transistor source. This can be achieved with a current source I_{BIAS} shown in Figure 6.1a. That topology is not typically utilized in LNAs since the current source I_{BIAS} increases the noise. A better noise performance is achieved by using a source inductor L_S as shown in Figure 6.1b. The L_S forms a parallel LC resonator with the parasitic capacitance C_{par} associated with the source node of the M1. When on-wafer measurements are not applicable, the source node typically needs to be connected either to package or PCB by using a bondwire inductance L_{IN} as shown in Figure 6.1c. The L_{IN} is resonated at the wanted frequency with a DC blocking capacitor C_{IN} which can be either an on-chip or an external component.

In Figure 6.1b and Figure 6.1c, the capacitor C_{par} includes the parasitic capacitances at the source node, i.e. source-body junction capacitance of M1, substrate capacitance of L_S, and capacitance caused by the bonding pads and on-chip metal wiring. Furthermore, the value of the source inductor L_S can be decreased by adding an additional shunt capacitor C_S in parallel with L_S (the C_S is not shown in Figure 6.1b or Figure 6.1c. Therefore, all the capacitance at the source node can be

included in a single source capacitor C_T used in the following calculations:

$$C_T = C_{GS} + C_{PAR} + C_S \tag{6.1}$$

The input impedance Z_{IN} of a CG input stage, shown in Figure 6.1b, can be calculated as

$$Z_{IN} = \frac{sL_S}{1 + sL_S gm + s^2 + L_S C_T} \tag{6.2}$$

The source inductance L_S resonates with the capacitance C_T at the frequency of

$$\omega_o = \frac{1}{\sqrt{L_S C_T}} \tag{6.3}$$

and at that frequency, Equation 6.2 simplifies to $1/g_m$. The impedance Z_{IN} of a CG input stage shown in Figure 6.1c is

$$Z_{IN} = \frac{1 + s^2 C_{IN} L_{IN}}{sC_{IN}} + \frac{sL_S}{1 + sL_s gm + s^2 L_S C_T} \tag{6.4}$$

With a perfect impedance matching ($1/gm = R_S$), where R_S is the source output resistance. The voltage gain of the CG amplifier becomes a division of output load versus the source impedance, i.e. Z_L/R_S. The assumption is valid if the drain-to-source resistor r_{ds} is much larger than the load resistance at the drain. Otherwise, the gain and input resistance formulas should be modified to:

$$A_V = \frac{g_m Z_L}{\left(a + \frac{Z_L}{r_{ds}}\right)} \tag{6.5}$$

and

$$R_{IN} = \frac{1}{gm}\left(1 + \frac{Z_L}{r_{ds}}\right) \tag{6.6}$$

6.2.2 Noise of a CG Stage

The noise factor of a CG LNA is expressed as [46]:

$$F = 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+\chi}\right)^2 \frac{1}{gmR_S} \tag{6.7}$$

where γ is the coefficient of channel thermal noise, gm is the transistor transconductance, χ is the ratio of the transistor substrate transconductance gm_b and gm, R_S is the source resistance and α is gm/gd_o. Because the minimum NF of a common source LNA increases along with the frequency, CG LNAs can be a better option at very high frequencies. When χ is neglected and perfect input matching is assumed, the minimum noise factor typically presented in the literature is achieved:

$$F = 1 + \frac{\gamma}{\chi} = \frac{5}{3} = 2.2dB \tag{6.8}$$

With imperfect input matching, the noise factor can be lowered according to

$$F = 1 + \gamma \frac{1 + S_{11}}{1 - S_{11}} \tag{6.9}$$

where α is neglected.

Equation 6.8 does not take into account the noise of the load. If resistive load R_L is used, taking into account its noise contribution, assuming that $gm = 1/R_S$ the noise factor becomes

$$F = 1 + \frac{1}{gmR_S}\left(\frac{\gamma}{\alpha} + \frac{(1 + gmR_s)^2}{gmR_L}\right) \simeq 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L} \tag{6.10}$$

Thus, the resistive load can make a significant contribution to the overall noise.

6.2.3 Differential Operation of CG Stage

In Figure 6.2, the capacitor cross-coupling method, which is suitable for differential input configurations, is presented. Due to the capacitor divider between C_{GS} and coupling capacitance C_p, the inverting gain is approximately $A = C_p/(C_p + C_{GS})$, which is always less than one.

6.3 Mixer Design

6.3.1 Quadrature Mixers

Normally, the down conversion to zero or IF frequency is usually performed with quadrature (I/Q) mixers [47]. For I/Q mixers, there are different possibilities to implement the interface between input transconductor and switch quad. The first

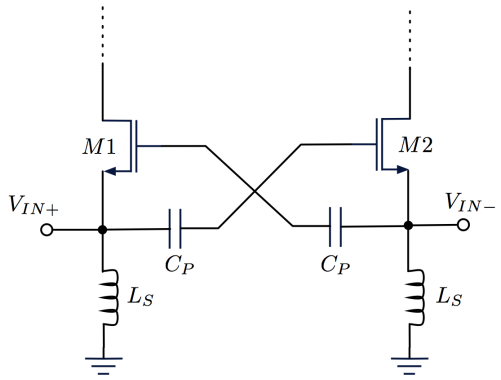


Figure 6.2: Capacitor cross-coupled CG stage.

topology is shown in Figure 6.3. The RF signal is fed into two separate input stages, which drive their respective switch quads. Another possibility is to utilize a single input stage, which drives both switch quads, as it is shown in Figure 6.4.

Since the transconductor of the mixer, shown in Figure 6.4, drives both switch quads, the conversion gain is 3 dB lower than the basic Gilbert cell mixer of Figure 6.3. In adittion, complete switching requires larger LO amplitude when quadrature switch quads are driven from a single transconductor.

6.3.2 Mixers with Current Boosting

The current boosting method [44], [47], [48] is used in the mixer and it is shown in Figure 6.5. The optimum bias for the input and switching stages can be optimized separately with current boosting. For proper gain and linearity performance, the input transconductance stage should be biased with rather higher current. However, the performance of the switch quad may require quite low current level for optimum operation. The conversion gain increases for two main reasons: the mixer requires a lower LO swing to switch completely and a larger load resistor value can be used to increase the voltage gain. Alternatively, if the load resistor value is kept unchanged, mixer design for lower supply voltages is alleviated with current boosting, since the voltage drop at the resistive load is reduced.

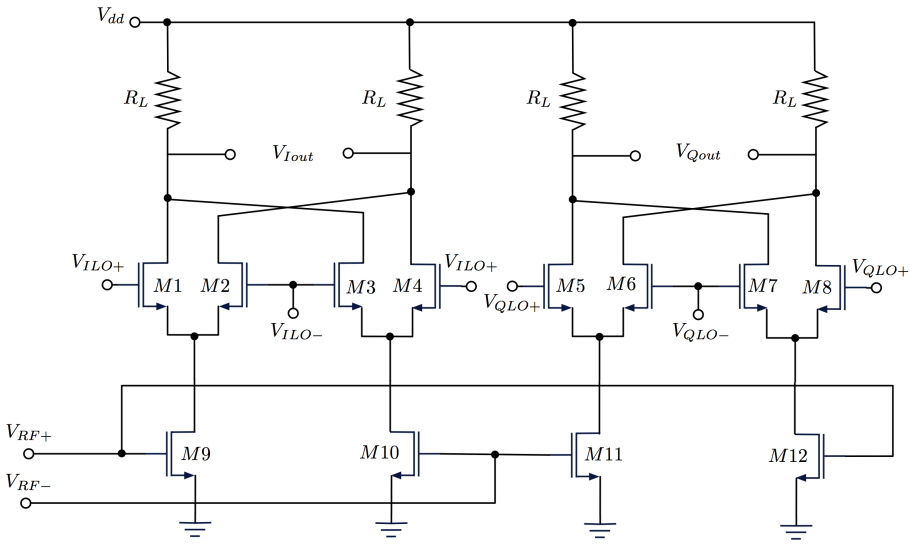


Figure 6.3: Two separate Gilbert mixers driven by quadrature LO signals.

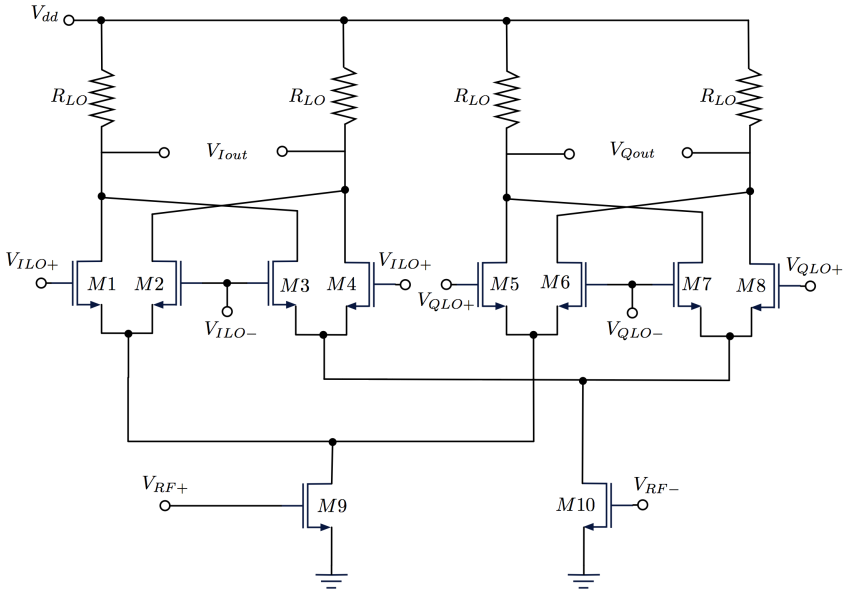


Figure 6.4: Quadrature mixer with single input stage.

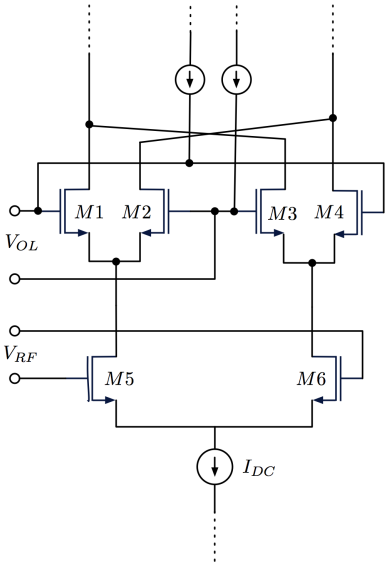


Figure 6.5: Current boosting with constant current source.

6.4 Inductorless Operation

Figure 6.6 shows a simplified interface between the LNA and mixer. Biasing and AC coupling have been omitted for clarify. In this Figure, M_0 represents the LNA transconductor, wich is realized as a CG stage. Further, M_1 represents the RF transconductor of the mixer. The circuit in Figure 6.6a shows the use of conventional inductive peaking to extend the bandwidth at the LNA output (It is really the LNA-mixer interface bandwidth that is being extended.). This bandwidth extension occurs due to the addition of a zero in the transfer function due to the inductor. A zero can also be introduced by capacitive degeneration as shown in Figure 6.6b [49]. In this circuit, the R_C combination of C_S and R_S provides a zero that extends the high frequency response. Effectively, capacitive degeneration provides bandwidth extension properties similar to inductive peaking [50].

6.5 Experimental Results

6.5.1 Frontend I

Figure 6.7 shows an RF frontend composed by a differential common-gate shunt-peaking LNA followed by differential double balanced Gilbert mixer. The layout of

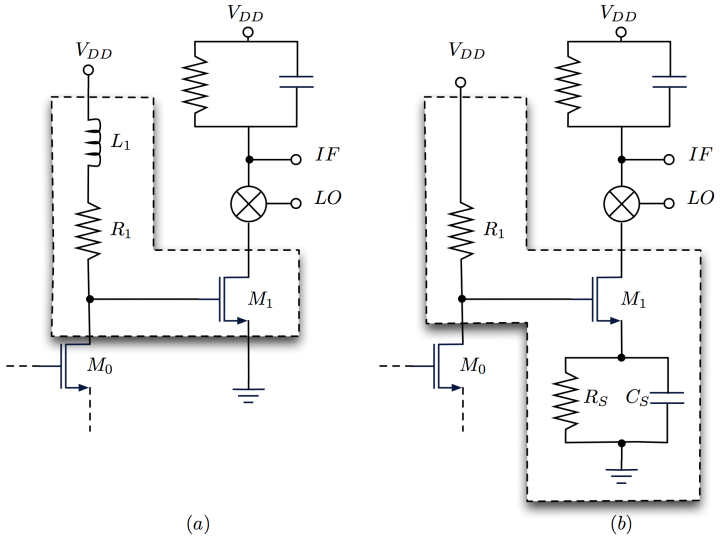


Figure 6.6: Simplified circuits for (a) inductive peaking and (b) capacitive peaking.

the circuit, named as Frontend I, is shown in Figure 6.8. The Frontend I chip area, including the test pads, is 1410.63 x 693.39 μm^2.

Conversion gain and noise figure simulation results are shown in Figure 6.9 and Figure 6.10 respectively, for a 400 MHz channel located at the center of the band. Frontend I has a conversion gain of 12.1 dB at 5.2 GHz and a noise figure of 11.2 dB (IF=200MHz).

The two-tone test for third-order intermodulation distortion (IIP3) of Frontend I is shown in Figure 6.11. The test was performed at 5 GHz and an IIP3 of -5.7 dBm was obtained.

6.5.2 Frontend II

Figure 6.12 shows an RF frontend composed by a differential common-gate resistive load LNA followed by differential double balanced Gilbert mixer with capacitive degeneration. The layout of the circuit, named as Frontend II, is shown in Figure 6.13.

The Frontend II chip area, including the test pads, is 698.89 x 744.76μm^2. Due to the non existence of inductors, the occupied area of this design is 54% lower than Frontend I.

Conversion gain and noise figure simulation results are shown in Figure 6.14 and

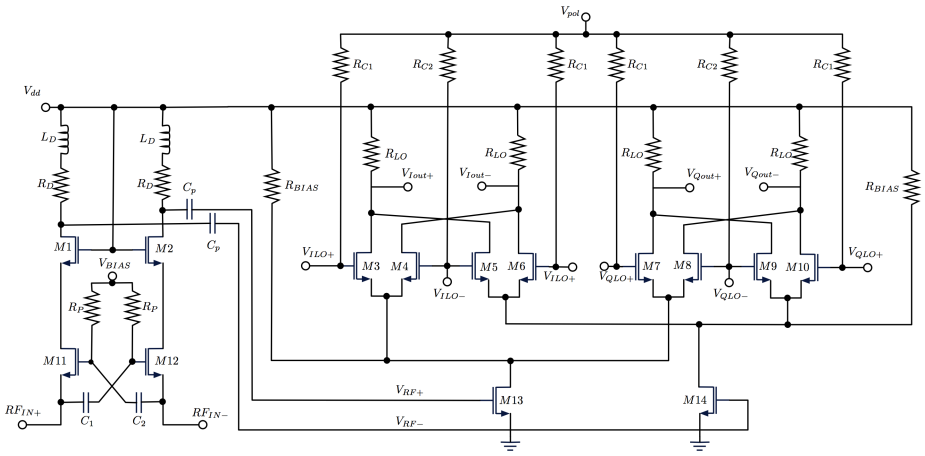


Figure 6.7: Frontend I schematic.

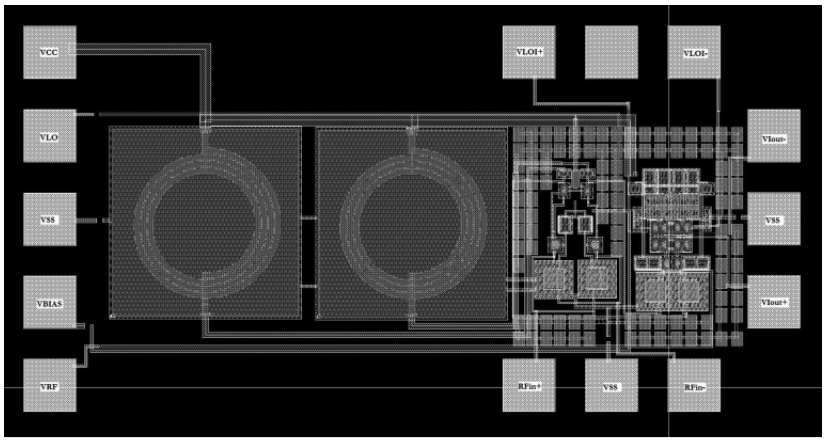


Figure 6.8: Frontend I layout.

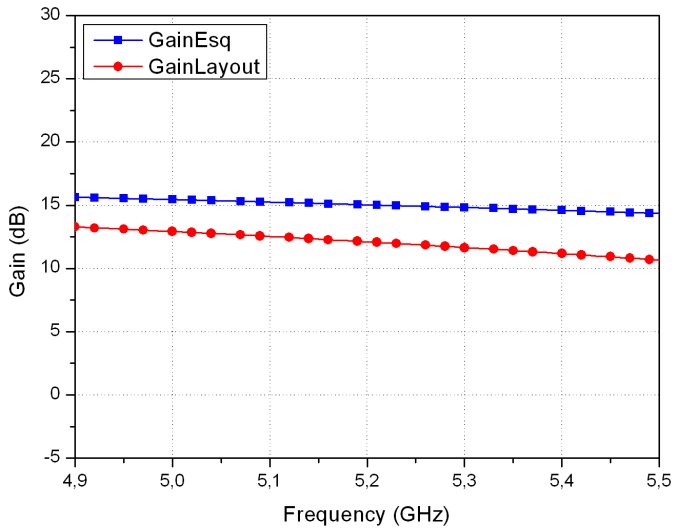


Figure 6.9: Frontend I conversion gain simulations results.

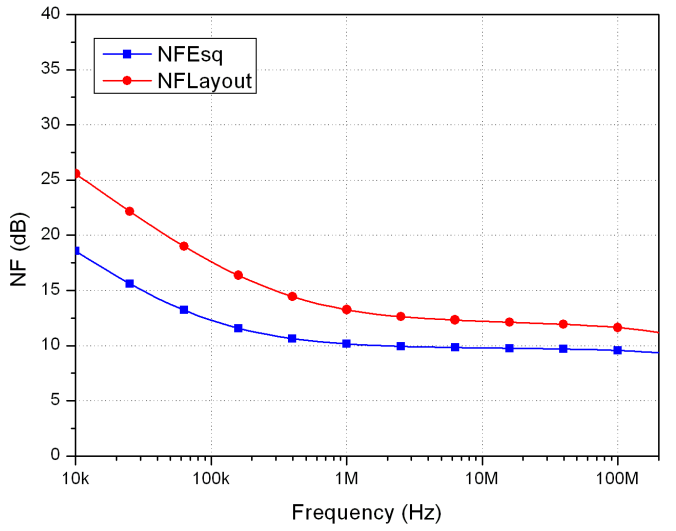


Figure 6.10: Frontend I noise figure simulations results.

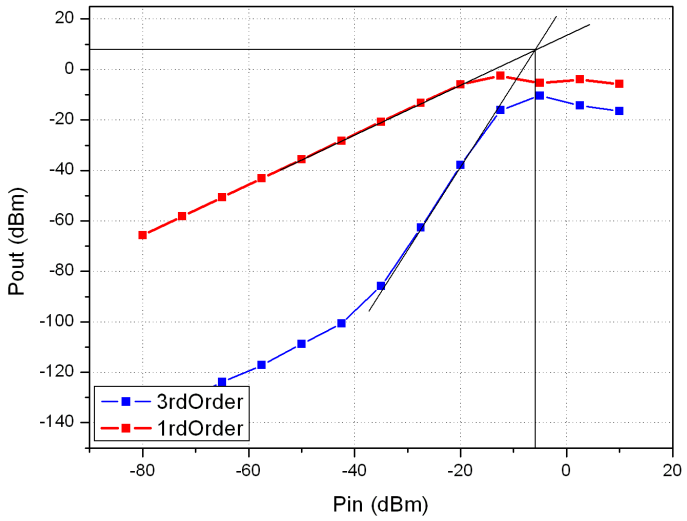


Figure 6.11: Frontend I IIP3 simulations results.

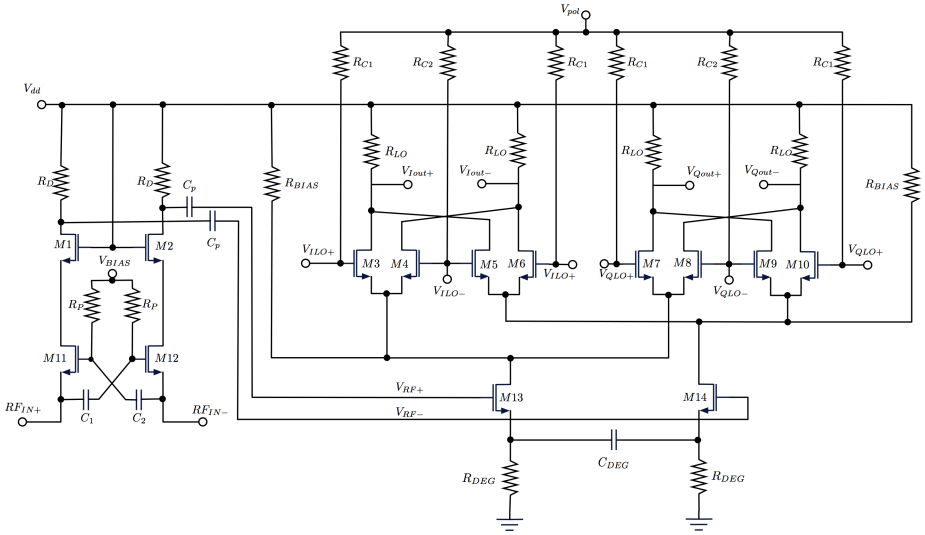


Figure 6.12: Frontend II schematic.

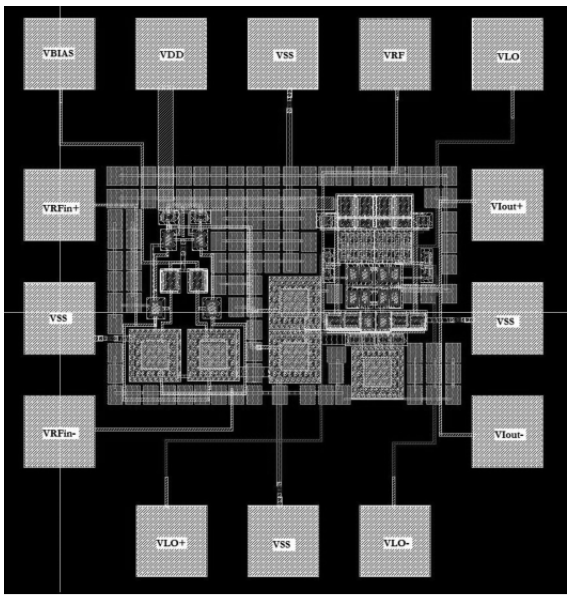


Figure 6.13: Frontend II layout.

Figure 6.15 respectively, for a 400 MHz channel located at the center of the band. Frontend II has a conversion gain of 7.2 dB at 5.2 GHz and a noise figure of 13.71 dB (IF=200MHz).

The linearity of the Frontend II was evaluated with a two tone test. The result is plotted in Figure 6.16. The IIP3 is -2.1 dBm.

6.6 Conclusions

Design	Frontend I	Frontend II
NF (dB)	11.2	13.7
Gain (dB)	12.1	7.2
IIP3 (dBm)	-5.6	-2.1
Consumption (mW)	16	14
Area (mm^2)	0.97	0.52

Table 6.1: Frontends performance summary.

In this chapter, an inductorless techniques has been explored. The inductorless wide band amplifier can been achieved if the amplifier works in conjunction with a

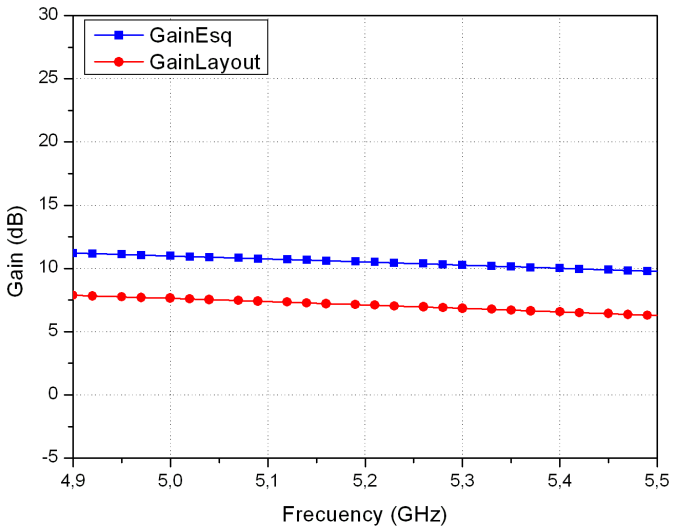


Figure 6.14: Frontend II gain simulation results.

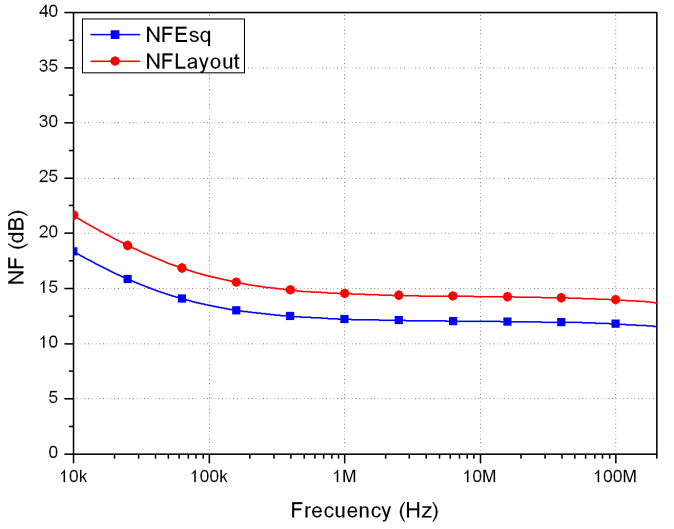


Figure 6.15: Frontend II noise figure simulation results.

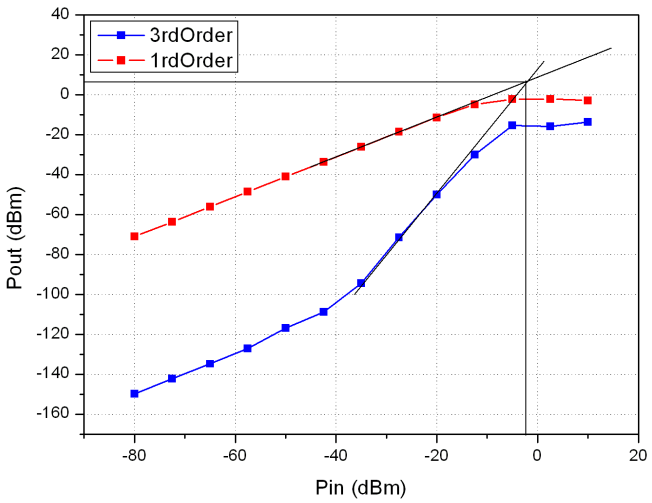


Figure 6.16: Frontend II IIP3 simulation results.

Gilbert Cell mixer because the mixer input is part of the low noise amplifier output matching network. For this reason, in this chapter also a Gilbert Cell mixer with current boosting has been designed.

In order to validate the area saving without a significant performance degradation, another wide band low noise amplifier with shunt-peaking followed by a Gilbert cell mixer has been designed.

Table 6.1 shows the performance comparative of both frontends. Simulations results shows that the proposed topology with the same bandwidth has better linearity, comparable noise figure and uses less power. The silicon area for the inductorless LNA and I/Q mixers 54% less than the traditional inductor based designs showing area savings and improved portability.

7 Conclusions and Areas for Further Research

7.1 Conclusions

The main work of this research has been focused on optimizing the area and power consumption of low noise amplifiers for ultra wide band communications based on ECMA-368 / ISO/IEC 26907 specifications.

In order to have a reference set of specifications for the LNA, in chapter two the ECMA-368 / ISO/IEC 26907 standard was studied. From this study a reference system was designed and based on budget simulations, the LNA reference specifications where extracted.

In chapter three the most classical wide band amplifier was presented, the distributed amplifier. With this topology a wide band operation is obtained with a relatively constant performance through the whole band. The main drawbacks of this topology are a high power consumption and a large area due to the significant number of inductors employed. In order to reduce the area, three different versions of the distributed amplifier were designed. The first one is a classical structure without any area saving technique that was used as a reference design. In the version, a compacting technique was used. The objective here was to reduce the impact of mutual coupling between inductors through the correct coiling of the spirals. Finally, the third version employs multilevel stacked inductors achieving the most important area saving (36%) with a minimum influence over the distributed amplifier performance.

Although an important saving in the area was achieved, the distributed amplifier still use a large area. For this reason, in chapter four, three different alternatives

Design	Gain (dB)	BW (GHz)	NF (dB)	IIP3 (dBm)	Area (mm^2)	P_{DC} (mW)
Distributed amplifier 1	7	6.5	5	21.3	0.74	90
Distributed amplifier 2	7	6.5	4.5	21.4	0.61	90
Distributed amplifier 3	5.5	6.5	6	20.2	0.47	90
Wide band amplifier	12.5	3.6	4.3	-4	0.13	32
Modified Shunt-peaking	11.2	4	5	-4	0.29	56.1
Folded cascode	7.8	2.96	3	-4	0.13	18.93
Feedback amplifier standard ind.	14	5.6	< 4	-3.4	0.17	13.2
Feedback amplifier 3D ind.	14	6.8	< 4	-4.4	0.10	13.2
Receiver 1 (inductor based)	12.1	5	11.2	-5.6	0.97	16
Receiver 2 (inductorless)	7.2	5	13.7	-2.1	0.52	14

Table 7.1: Designed circuits specifications.

of wide band amplifiers were studied. The first one is a classical cascode topology transformation to wide band operation. In this design, the input narrowband matching network was transformed into a wide band matching network and the output load was also transformed to a wide band load. The immediate consequence is a reduction in the area and power consumption but, the problem is that it is difficult to keep the gain constant over the whole band.

To solve the gain flatness problem, the modified shunt peaking topology was introduced in the same chapter. This technique improves the gain flatness but it has a negative consequence in area due to the introduction of an additional inductor. Another alternative studied in this chapter was a folder cascode topology. With this structure, a low voltage operation is possible with a minimal influence over the circuit performance. In this design, stacked inductors were introduced as folding elements achieving an important reduction in the area.

In chapter five, feedback techniques were studied to improve low noise amplifier performance. In this chapter, an inductor placed inside the active feedback loop is proposed to improve the bandwidth of the amplifier. It was found out that the inductance of this inductor is very important in determining the bandwidth of operation, but its quality factor is not relevant in terms of this and the others parameters. In fact, a low quality factor improves the noise performance of the circuit and, for this reason, a modified miniature 3-D inductor was used. As a consequence, this technique improves the area and also the noise performance.

The area is mainly related with the number of inductors employed in the circuit. In chapter six a circuit methodology for designing UWB RF frontends without the use of inductors is described. To validate this design methodology two receiver RF frontends were designed; a traditional inductor based design and an inductorless design. Both design use a common-gate LNA followed by two quadrature Gilbert cell mixers. In the inductorless version, the LNA shunt-peaking load was replaced by a resistive load and a capacitive degeneration was included in the mixer. Simulations results show that the inductorless topology has better linearity, comparable noise figure and uses less power with the same bandwidth. The silicon area for the inductorless LNA and I/Q mixers is roughly 54% less than the traditional inductor based design, showing an important area saving and improving the circuit portability.

As a summary, Table 7.1 shows the main features of all the circuits developed in the framework of this research work.

7.2 Areas for Further Research

In this research work several alternatives to implement an UWB LNA in low cost technologies have been explored. An inductor less frontend was also introduced. The main objective was to reduce the power consumption and area with a relatively high bandwidth. There are several technical challenges that need further research as:

- **Design and integration of the rest of the receiver:** This includes the study and design of mixers, filters and baseband amplifiers for ultra wide band, optimizing the power consumption and area.
- **Inductors structures:** Explore different alternatives to reduce the area of integrated inductors with minimum impact on the circuit performance. This implies also exploring new circuit topologies that require inductors with lower performance.
- **Inductor less structure:** Improve the performance of inductorless receivers. This is a promising technique since avoiding the use of inductors improve the portability to other process technologies.

A

Resumen en Castellano

A.1 Introducción

En los últimos años las de Redes de Área Personal (WPAN) se están volviendo cada vez más populares. Estos sistemas permiten llevar a cabo la eliminación del cableado de interconexión en muchas aplicaciones a la vez que abren nuevas oportunidades para el desarrollo de novedosas aplicaciones de consumo. Actualmente, los sistemas WPAN están dominados por comunicaciones basadas en las especificaciones de Bluetooth y Zigbee, que son estándares de comunicación que operan en la banda libre de 2.4 GHz. Para aumentar la tasa de transferencia de datos a unos cientos de Mb/s, sin una incidencia considerable en el consumo de potencia, se han propuesto las comunicaciones de ultra banda ancha (UWB).

El hecho de que las comunicaciones de ultra banda ancha suponen una solución viable al problema de la transferencia de datos en comunicaciones WPAN, esta provocando que numerosas empresas están centrando sus esfuerzos para sacar al mercado soluciones basadas en esta tecnología. Algunas de estas empresas son las siguientes:

Alereon [1]: Es una empresa con sede en Austin (Texas) que desarrolla circuitos de banda ancha con bajo consumo y que cumplen la especificación de USB inalámbrico, así como la especificación "WiMedia Ultra Wide Band". Uno de los productos desarrollador por Alereon es el Chipset AL5100/5301.

El chip Alereon AL5100 integra todo lo necesario para llevar a cabo una comunicación de ultra banda ancha. Internamente incluye los sintetizadores de frecuencia, osciladores controlados por tensión, amplificadores de bajo ruido y de potencia

Figura A.1: Sistema Veebeam HD.

así como un conmutador interno para poder llevar a cabo la recepción y la transmisión con una única antena. En combinación con el chip AL5301, que implementa la capa de control de acceso al medio, el AL5100 constituye una solución integrada de comunicación de ultra banda ancha.

Wisair [2]: Es una empresa Israelí, que desarrolla soluciones integradas para sistemas de comunicaciones de ultra banda ancha y USB inalámbrico para equipos electrónicos de consumo y dispositivos móviles. Uno de los productos desarrollados por Wisair es el WSR601.

El chip WSR601 integra todo lo necesario a nivel de capa física, control de acceso al medio e implementación de protocolo de comunicaciones de USB inalámbrico para poder ser integrado en cualquier tipo de producto de consumo, habilitando de esta forma la posibilidad de llevar a cabo comunicaciones de ultra banda ancha a un bajo coste.

Veebeam [3]: Es una empresa inglesa con sede en Cambridge que diseña y desarrolla productos basados en tecnologías inalámbricas. Veebeam ha centrado sus esfuerzos en el desarrollo de soluciones inalámbricas de transmisión de video en tiempo real con alta definición.

Uno de sus productos, el Veebeam HD (Figura A.1), es la combinación de un emisor y un receptor de ultra banda ancha que permite llevar a cabo la realización de streaming de audio y vídeo en tiempo real y con alta definición desde un equipo portátil a un equipo de televisión.

La arquitectura interna de la etapa de recepción de cualquiera de los productos

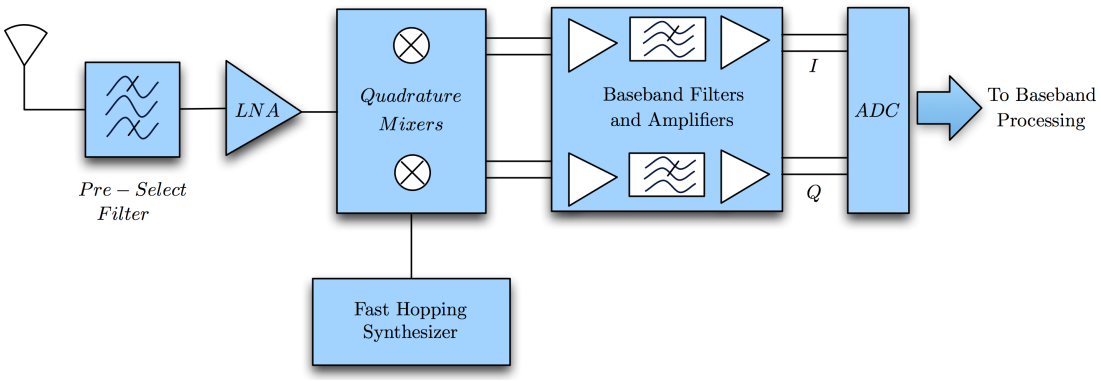


Figura A.2: Arquitectura de un receptor genérico.

anteriormente presentados, tiene una estructura muy similar a la mostrada en la Figura A.2. En esta arquitectura, la señal procedente de la antena es filtrada por un filtro externo que se encarga de preseleccionar la banda de interés para reducir las interferencias de señales fuera de la banda. Una vez preseleccionada la banda, los amplificadores de bajo ruido (LNA) y los mezcladores de cuadratura se encargan de amplificar la señal y trasladarla a baja frecuencia. El filtrado en banda base se encarga de acondicionar la señal deseada. Finalmente se lleva a cabo una digitalización de la señal por medio de los conversores analógico-digitales (ADC), de manera que la señal ya puede ser procesada digitalmente.

En esta arquitectura, uno de los puntos críticos del diseño es el amplificador de bajo ruido (LNA). Este circuito debe presentar ganancia a lo largo de toda la banda de trabajo con una correcta adaptación de impedancia a la entrada y la mínima aportación de ruido posible. Debido a estas restricciones en el diseño, normalmente los LNAs están compuestos por un gran número de bobinas y tienen un alto consumo de potencia.

En las aplicaciones móviles, el consumo de potencia está directamente relacionado con la duración de la carga de la batería. Por otro lado, el área ocupada por los diferentes circuitos es directamente proporcional al coste del mismo. Con el fin de desarrollar circuitos comerciales competitivos es necesario llevar a cabo una implementación con un mínimo consumo de área y potencia.

A.1.1 Objetivos

El principal objetivo de este trabajo de investigación es presentar diferentes

alternativas para implementar amplificadores de bajo ruido con un bajo consumo de potencia y un uso eficiente del área ocupada. Los resultados de este trabajo de investigación están integrados dentro de los siguientes proyectos de investigación:

- SR2 - Short Range Radio, Ministerio Español de Industria, Turismo y Comercio. 2010-2011.

- SR2 - Short Range Radio, Ministerio Español de Industria, Turismo y Comercio. 2009-2010.

- WITNESS - WIreless Technologies for small area Networks with Embedded and Security & Safety. MEDEA+ de la Unión Europea - Ministerio Español de Industria, Turismo y Comercio. 2005 - 2007.

De cara a alcanzar el objetivo de este trabajo se han planteado los siguientes hitos:

1. Obtener las especificaciones de un sistema de referencia basado en las especificaciones impuestas por el estándar ECMA-368 / ISO/IEC 26907.

2. Explorar diferentes alternativas para la implementación de amplificadores de bajo ruido para sistemas de ultra banda ancha, prestando especial atención en la optimización de consumo de área y potencia.

3. Explorar diferentes estructuras de inductores integrados con el fin de reducir el consumo de área de las misma.

4. Explorar nuevas alternativas de desarrollo de amplificadores de bajo ruido para sistemas de ultra banda ancha que eviten el uso de inductores integrados con el fin de reducir el consumo de área.

A.1.2 Estructura de la memoria

El documento principal de este trabajo de investigación esta compuesto por siete capítulos distribuidos de la siguiente manera. El *Capítulo 1* introduce al lector a las comunicaciones de ultra banda ancha mostrando una visión general del estado actual del mercado. Por otro lado, en este capítulo se plantean los objetivos del trabajo de investigación. Después de esta pequeña introducción, en el *Capítulo 2* se plantean

las principales características de la especificación ECMA-368 / ISO/IEC 26907. A partir de estas especificaciones se lleva a cabo el diseño de un sistema de recepción a nivel de bloques. A partir de este sistema de referencia se extraen las especificaciones de partida para los diferentes amplificadores de bajo ruido que se irán desarrollando en capítulos posteriores.

El *Capítulo 3* se centra en estudiar una de las estructuras más clásicas en el desarrollo de amplificadores de ultra banda ancha, los amplificadores distribuidos. Con el fin de solucionar algunos de los principales inconvenientes de los amplificadores distribuidos, en el *Capítulo 4*, se presentan diferentes alternativas para la implementación de amplificadores de bajo ruido para ultra banda ancha.

Con el fin de continuar llevando a cabo una optimización de consumo de potencia y área, en el *Capítulo 5* se exploran las técnicas de realimentación aplicadas al diseño de amplificadores de bajo ruido. El *Capítulo 6* esta centrado en el desarrollo de amplificadores de bajo ruido evitando el uso de inductores integrados, consiguiendo de esta forma una mejora importante en el consumo de área total de los LNAs.

Finalmente, en el *Capítulo 7* se presentan las principales conclusiones obtenidas del trabajo realizado. Por otro lado, se presentan las posibles líneas de trabajo para continuar avanzando y explorando en el desarrollo de amplificadores de bajo ruido para comunicaciones de ultra banda ancha.

En las siguientes secciones, tal y como regula la Universidad de Las Palmas de Gran Canaria en el Reglamento para la elaboración, tribunal, defensa y evaluación de tesis doctorales en el artículo 2, se presentará un resumen de cada uno de los capítulos del trabajo de investigación donde se recogerán los siguientes aspectos: Objetivos, Planteamiento y metodología, Aportaciones originales y Conclusiones obtenidas.

A.2 Análisis del Sistema

A.2.1 Objetivos

Como punto de partida de la investigación, los principales objetivos de este capítulo son: llevar a cabo un estudio de la especificación ECMA-368 / ISO/IEC 26907 y obtener un conjunto de especificaciones de referencia para los amplificadores

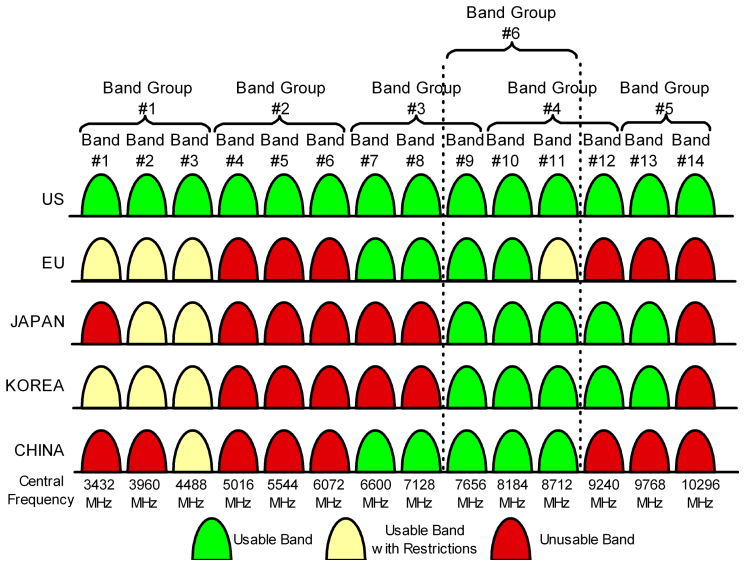


Figura A.3: Distribución espectral de canales.

de bajo ruido que se desarrollarán en los capítulos posteriores.

A.2.2 Planteamiento y metodología

A.2.2.1 Especificaciones del sistema

Para llevar a cabo el diseño del sistema de referencia es necesario conocer las principales especificaciones y requerimientos impuestos por el estándar ECMA-368 / ISO/IEC 26907. A continuación se enumeran las principales especificaciones a nivel físico.

Bandas de frecuencia

A nivel físico el rango de frecuencias va desde los 3.1 a los 10.6 GHz, dividiendo el espectro en canales de 528 MHz. Tal y como se define en la Figura A.3, el espectro está dividido en 6 grupos de banda. Los grupos del 1 al 4 están compuestos por cuatro canales, (canales del 1 al 12). El grupo 5 está compuesto por los canales 13 y 14. Finalmente, el grupo 6 contiene los canales 9, 10 y 11. En la Tabla A.1 se muestra la distribución de canales. A pesar de existir esta recomendación de frecuencias en algunos países se crean especificaciones mucho más restrictivas que prohíben la utilización de canales concretos.

Sensibilidad del receptor

Otro parámetro fundamental a la hora de diseñar el sistema es conocer la sensi-

Grupo de Banda	Band ID (n_b)	Frecuencia Inferior (MHz)	Frecuencia Central (MHz)	Frecuencia Superior (MHz)
1	1	3168	3432	3696
	2	3696	3960	4224
	3	4224	4488	4752
2	4	4752	5016	5280
	5	5280	5544	5808
	6	5808	6072	6336
3	7	6336	6600	6864
	8	6864	7128	7392
	9	7392	7656	7920
4	10	7920	8184	8448
	11	8448	8712	8976
	12	8976	9240	9504
5	13	9504	9768	10032
	14	10032	10296	10560
6	9	7392	7656	7920
	10	7920	8184	8448
	11	8448	8712	8976

Tabla A.1: Dstribución de canales.

Tasa de Transferencia (Mb/s)	Sensibilidad (dBm)
53.3	-80.8
80	-78.9
106.6	-77.8
160	-75.9
200	-74.5
320	-72.8
400	-71.5
480	-70.4

Tabla A.2: Sensibilidad para las diferentes tasas de transferencia.

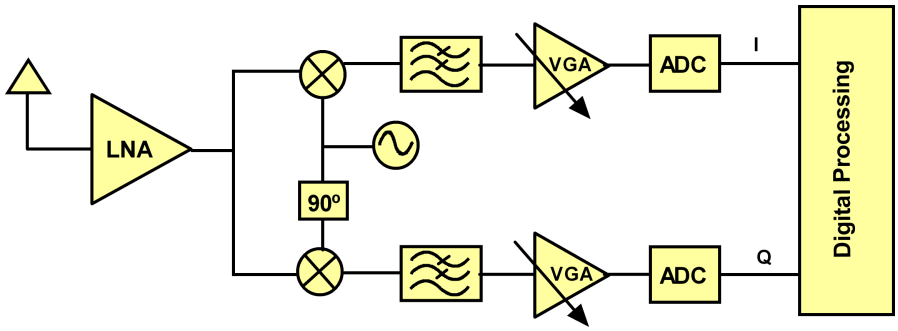


Figura A.4: Arquitectura de conversión directa.

bilidad mínima a la que debe trabajar. Según las especificaciones se debe conseguir un Error de Transferencia de Paquetes (PER) inferior al 8 % con una carga útil por paquete de 1024 octetos. Teniendo en cuenta este error de transferencia se puede obtener la sensibilidad mínima para cada una de las velocidades de transferencia soportadas por el estándar tal y como se muestra en la Tabla A.

A.2.2.2 Arquitectura del receptor

Debido al gran ancho de banda que presentan los canales se ha optado por llevar a cabo la implementación de un sistema de conversión directa. La Figura A.4 muestra un diagrama a nivel de bloques de un receptor de conversión directa, en este tipo de receptores la frecuencia del oscilador local es igual a la frecuencia de la señal de entrada, de esta forma al llevar la señal a banda base para proceder a la selección del canal es necesario solamente el uso de un filtro paso bajo.

La arquitectura de conversión directa presenta algunos inconvenientes. En este tipo de arquitectura la señal de banda base llega hasta 0 Hz. En esta situación la

aparición de señales continuas pueden corromper e incluso saturar a las etapas de procesado en banda base. Asociado a este fenómeno están relacionados los acoplamientos de la señal del oscilador local a través del puerto de RF. Este acoplamiento resulta en una señal continua que puede contribuir a corromper la señal en banda base. Por otro lado, en este tipo de receptores es necesario llevar a cabo el proceso de mezclado en cuadratura, por lo que cualquier desajuste en los desfasadores pueden provocar un empeoramiento de la calidad de la señal. Otro inconveniente de esta arquitectura es que los armónicos de tercer orden pueden aparecen dentro de la señal deseada provocando una degradación de la misma. Finalmente, como la señal se lleva directamente a cero el ruido Flicker asociado a los dispositivos puede influir negativamente en la señal deseada.

A pesar de estos inconvenientes, la simplicidad de los receptores de conversión directa presentan dos importantes ventajas. En este tipo de arquitectura no aparece el problema de la frecuencia imagen porque la señal se lleva a banda base en un único paso. Como resultado de esto no es necesario el uso de filtros externos para el rechazo de imagen. Por otro lado, al llevar a cabo todo el proceso de conversión en un único paso, esta arquitectura es mucho más sencilla de integrar en un único chip con un consumo de potencia significativamente menor que otras arquitecturas de receptores.

Una vez definida la arquitectura del sistema teniendo en cuenta las diferentes especificaciones establecidas por el estándar ECMA-368 / ISO/IEC 26907, se puede proceder a obtener las especificaciones a nivel de bloques del sistema. En este aspecto inicialmente se obtiene la figura de ruido total a partir de las especificaciones de sensibilidad, ancho de banda del canal y tasa de transferencia en el canal.

Una vez definida la figura de ruido total del sistema, se procede a calcular las especificaciones del filtrado de banda base así como las especificaciones de los conversores analógico digital necesarios para transformar la señal al dominio digital para su posterior proceso digital.

Con la especificación de los conversores analógico digitales se puede obtener la ganancia general que necesita el sistema. Una vez determinada la ganancia máxima y mínima que debe tener el sistema se determina si es necesario el uso de un control automático de ganancia para asegurar que la ganancia está siempre entre los valores máximos y mínimos determinados.

Finalmente, para terminar de llevar a cabo el diseño del sistema es necesario

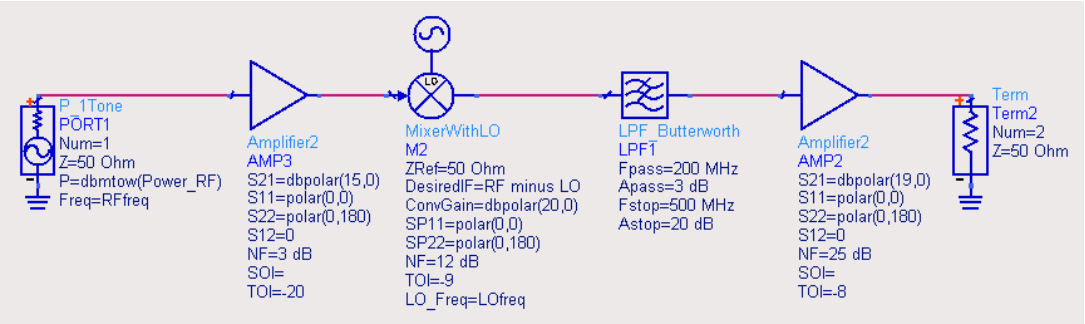


Figura A.5: Esquemático de simulación del sistema.

Parámetro	Especificación	Simulación
Sensibilidad (dBm)	-80.8	-85
Figura de ruido (dB)	7.32	7.27
Ganancia (dB)	48.81	50.9
Maximum input level (dBm)	-41	-35
IIP3 (dBm)	-8.65	-8.15

Tabla A.3: Resultados de simulación del sistema.

determinar los requerimientos de linealidad del mismo, teniendo en cuenta el peor escenario de interferencias al que se puede ver sometido el sistema.

Llegados a este punto ya se dispone de todo el sistema diseñado y es el momento de validar el diseño por medio de simulaciones. Para llevar a cabo estas simulaciones se ha usado el simulador comercial ADS. La simulación realizada al sistema se centra en determinar las especificaciones de cada uno de los bloques del sistema para que en su conjunto se consiga que el sistema completo cumpla las especificaciones calculadas inicialmente.

En este proceso de simulación, como punto de partida, a cada bloque se le asigna un conjunto de especificaciones que han sido establecidas teniendo en cuenta la experiencia de trabajo del grupo en circuitos previos y el estado del arte. Lógicamente, el ajuste final de las especificaciones de cada bloque serán determinadas por medio de la simulación. La Figura A.5 muestra el esquemático de simulación empleado para determinar las especificaciones de cada uno de los bloques que constituye el sistema.

Después de llevar a cabo el proceso de simulación y ajustadas las especificaciones de cada bloque, en la Tabla A.3 se muestra la comparativa entre las especificaciones calculadas inicialmente y las obtenidas finalmente a través de simulación, como

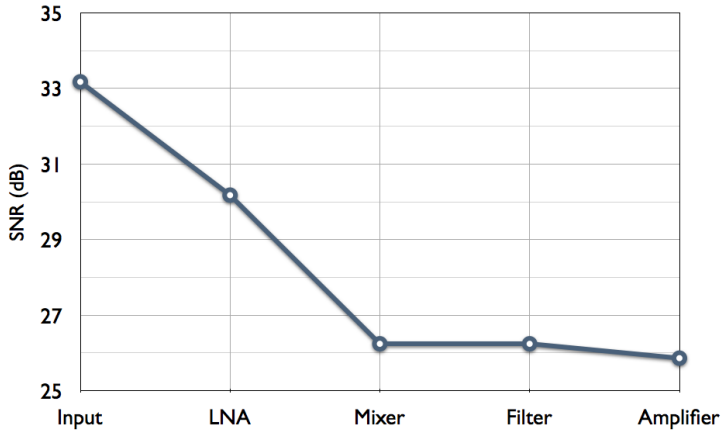


Figura A.6: Simulación de la SNR del sistema.

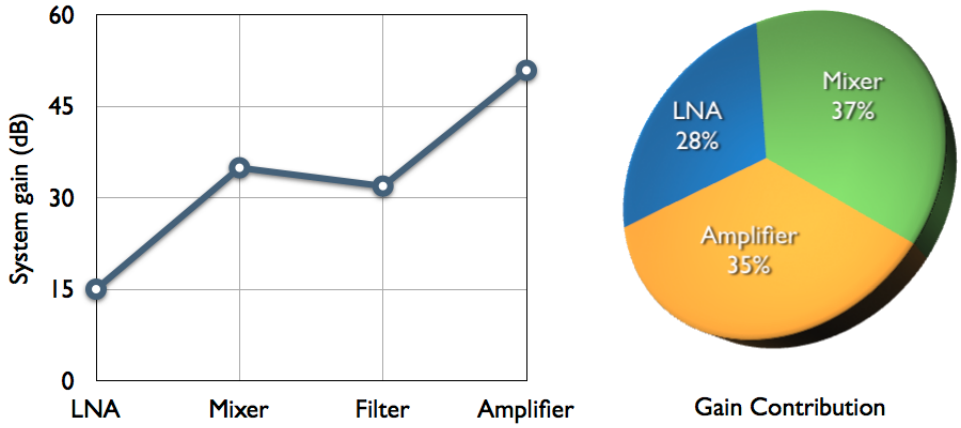


Figura A.7: Simulación de ganancia del sistema.

puede observarse los valores son muy próximos.

La Figura A.6 muestra la variación de la relación señal a ruido (SNR) a lo largo de toda la cadena de recepción. Lógicamente la mayor SNR se encuentra en la entrada del receptor. A medida que la señal va pasando a través del receptor la SNR va disminuyendo porque la señal se va viendo corrompida por el ruido. La diferencia entre los valores de la SNR a la entrada y a la salida constituyen la figura de ruido de la cadena de recepción. En este caso el valor de la figura de ruido está en torno a los 7.2 dB.

La Figura A.7 muestra la contribución a la ganancia de cada uno de los bloques que constituye la cadena de recepción. La ganancia total del sistema está dividida

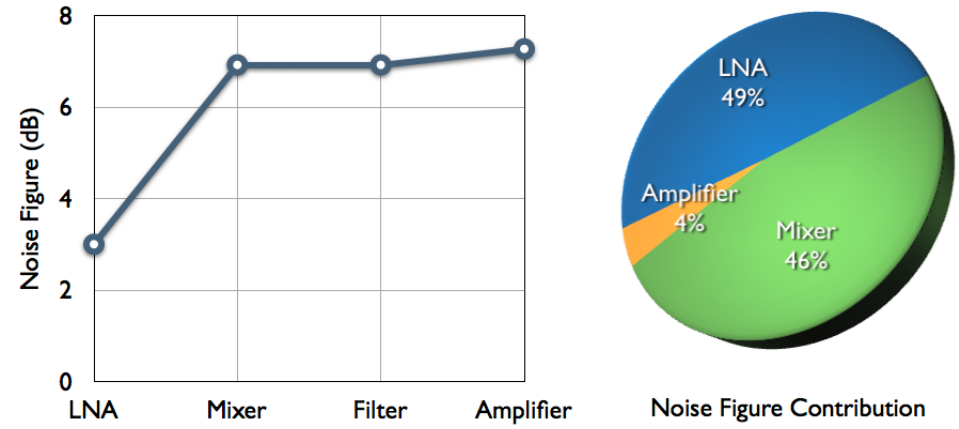


Figura A.8: Simulación de figura de ruido del sistema.

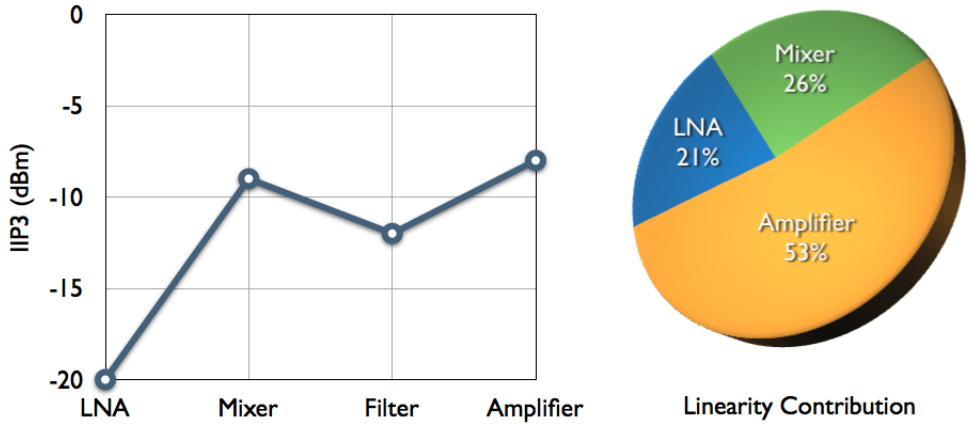


Figura A.9: Simulación de linealidad del sistema.

equitativamente entre el LNA los mezcladores y los amplificadores de banda base. Esta situación proporciona un escenario relajado para los diseñadores de los diferentes bloques porque si un bloque no llega a alcanzar la ganancia propuesta, se puede intentar solucionar el problema aumentando la ganancia de los bloques posteriores.

Por otro lado, tal y como se muestra en la Figura A.8, la contribución de ruido depende mayoritariamente del LNA y los mezcladores. Debido a esta condición el diseño del LNA y de los mezcladores deberá realizarse teniendo en cuenta intentar cumplir al máximo posible la especificación de ruido.

Finalmente, en la Figura A.9 se muestra la contribución a la linealidad de cada uno de los bloques. En este caso la mayor contribución la lleva a cabo los amplifica-

Parámetro	valor
Ganancia (dB)	15
Figura de Ruido (dB)	3
IIP3 (dBm)	-20
Consumo de potencia (mW)	mínimo
Consumo de Área (mm^2)	minimo

Tabla A.4: Especificaciones del LNA.

dores de banda base. Teniendo en cuenta esto, a la hora de diseñar los amplificadores de banda base habrá que prestar especial atención a este parámetro en concreto.

A.2.3 Aportaciones originales

Como principal aportaciones de este capítulo cabe destacar el diseño de una cadena de recepción a nivel de bloques así como la verificación del sistema y distribución de las especificaciones globales en especificaciones particulares de cada uno de los bloques que constituyen el sistema.

A.2.4 Conclusiones obtenidas

En este capítulo se han sentado las bases para el trabajo posterior. Después de estudiar las especificaciones de ECMA-368 / ISO/IEC 26907 se procedió a diseñar un sistema completo a nivel de bloques y se llevó a cabo la distribución de las especificaciones globales en las diferentes especificaciones locales de cada uno de los bloques. En la Tabla A.4 se muestra un resumen de las especificaciones de los LNAs que serán tomadas como especificaciones de referencia en los capítulos posteriores.

A.3 Amplificadores distribuidos

A.3.1 Objetivos

El diseño de amplificadores de bajo ruido para sistemas de ultra banda ancha es un desafío debido precisamente al gran ancho de banda. El principal objetivo de este capítulo es explorar una de las estructuras más clásicas para la implementación de

amplificadores para sistemas de ultra banda ancha, los amplificadores distribuidos.

A.3.2 Planteamiento y metodología

A.3.2.1 Aproximación teórica

La respuesta en frecuencia de los dispositivos MOS se ve degradada a medida que aumenta la frecuencia debido al polo formado por las capacidades tanto de entrada como de salida del dispositivo así como la resistencia que tienen asociada. En el caso de los transistores MOSFET, la transconductancia de los mismos decrece rápidamente con la frecuencia. Para solucionar este problema, un posible intento podría ser aumentar el tamaño del transistor provocando también un aumento de las capacidades parásitas asociadas. Como consecuencia, la ganancia en baja frecuencia ha aumentado pero el producto ganancia/ancho de banda del dispositivo se mantiene igual. Una forma de solucionar este problema es hacer uso de los amplificadores distribuidos.

El amplificador distribuido esta formado por una topología en la que las etapas de ganancia están conectadas pero sus capacidades asociadas están separadas. La señal de salida es formada por la combinación de las corrientes de cada una de las etapas de ganancia (Figura A.10). En este caso se emplean inductores en serie para llevar a cabo la separación entre la salida de una etapa y la entrada de la siguiente. Como resultado la topología de los amplificadores distribuidos puede resumirse en el intercalado de inductores en serie con capacidades en paralelo, formando una línea de trasmisión artificial. El carácter distribuido de la topología hace que se consigan ganancias relativamente bajas, pero por el contrario la naturaleza distribuida de las capacidades en este circuito hace que se alcancen un gran ancho de banda. Mediante la ganancia distribuida se consigue sobrepasar la limitación de ancho de banda debido a que parte de la capacidad de los dispositivos MOS es absorbida por la línea de transmisión artificial formada por los inductores en serie que conectan las puertas y drenadores adyacentes. La impedancia característica (Z_0) y la frecuencia de corte (f_c) relacionada con las pérdidas de la línea de transimisión vienen dadas por las siguientes expresiones:

$$Z_0 = \sqrt{\frac{L_{TL}}{C_{TL}}} \tag{A.1}$$

$$f_c = \frac{1}{\pi\sqrt{L_{TL}C_{TL}}} \tag{A.2}$$

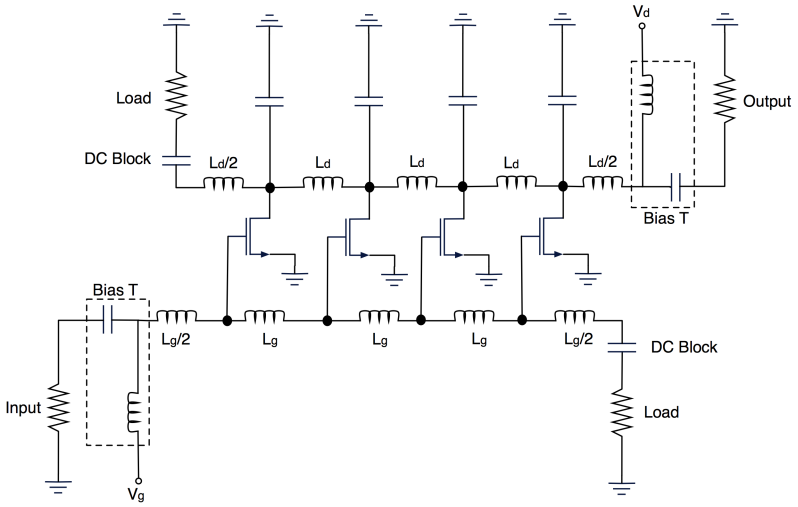


Figura A.10: Esquemático del amplificador distribuido.

donde el subíndice TL hace referencia a la línea de transmisión de puerta y de drenador. Z_0 y f_c tanto para la línea de drenador como la de puerta deberían ser iguales, por lo tanto las capacidades y la inductancia asociada a cada línea de transmisión debería ser la misma. Como normalmente la capacidad drenador-sustrato (C_{db}) de un MOSFET es menor que la capacidad puerta-surtidor (C_{gs}), se añade una capacidad adicional C_d para conseguir que la capacidad del drenador sea igual que la capacidad de la puerta.

$$L_g = L_d \tag{A.3}$$

$$C_{gs} = C_{db} + C_d \tag{A.4}$$

Como la señal amplificada va viajando a través de toda la línea de transmisión, se verá afectada por las pérdidas de la misma. En la línea de puerta estas pérdidas están asociadas principalmente a los valores finitos de factor de calidad (Q) que presentan los inductores integrados. En el caso de la línea de drenador, las pérdidas están asociadas principalmente a los inductores L_d y a la resistencia parásita que aparece entre el drenador y el surtidor (r_{ds}). La ganancia del amplificador distribuido

puede expresarse como [7]:

$$A = -g_m \frac{Z_0}{2\sqrt{1-\left(\frac{f}{f_c}\right)^2}} . \frac{e^{-N\frac{(A_g+A_d)}{2}} . sinh\left(N\frac{A_d-A_g}{2}\right)}{sinh\left(N\frac{A_d-A_g}{2}\right)} \tag{A.5}$$

donde A_d y A_g son las atenuaciones asociadas a la línea de drenador y puerta respectivamente, g_m es la transconductancia del MOSFET y N es el número total de etapas de la línea de transmisión. Esta ecuación esta teniendo en cuenta las siguientes suposiciones:

- Modelo unilateral del MOSFET (despreciando el valor de C_{gd}).
- Adaptación de impedancias perfecta en las terminaciones.
- Igual velocidad de fase tanto en la línea de puerta como en la de drenador.

El número optimo de etapas debe ser tal que maximice la ganancia en función de la atenuación de las líneas de puerta y drenador. Estas atenuaciones son unas funciones complejas y dependen de parámetros específicos del MOSFET empleado. Debido a que la señal viaja por medio de la línea de transmisión hasta las terminaciones, a medida que se va avanzando se va reduciendo la señal debido a las atenuaciones de cada etapa. Buscando un compromiso entre ganancia y atenuación se ha decidido definir un número total de 4 etapas en este trabajo.

Una vez conocido el número de etapas y las capacidades asociadas a cada línea se puede obtener la transconductancia necesaria a partir de la expresión de la ganancia A.5.

$$g_m = \frac{2.A}{N}\sqrt{\frac{C_d}{L_d}} \Rightarrow g_m = \frac{2.A}{N.Z_0} \tag{A.6}$$

A partir de la expresión anterior se puede obtener la relación de aspecto de los transistores a partir de la siguiente expresión:

$$\frac{W}{L} = \frac{g_m}{\mu_n C_{ox}(V_{gs} - V_T)} \tag{A.7}$$

donde:

- W es la ancho de la puerta.
- L es la longitud de la puerta.

Componente	Valor
$L_g = L_d$	1.465 nH
$L_g/2 = L_d/2$	1.15 nH
C_d	586 fF
L (longitud de puerta)	0.425 μm
W (ancho de puerta)	4.42 μm

Tabla A.5: Valores de los componentes calculados.

- n es la movilidad de los electrones.
- C_{ox} es la capacidad del óxido de puerta por unidad de área.
- V_T es la tensión de umbral.
- V_{gs} es la tensión puerta surtidor.

Finalmente, la longitud y ancho de los transistores puede ser determinada combinando con la siguiente expresión:

$$W.L = \frac{C_g}{C_{ox}} \tag{A.8}$$

Teniendo en cuenta las ecuaciones anteriores para un amplificador distribuido de cuatro etapas con una ganancia de 10 dB y una frecuencia de corte de 11 GHz, en la Tabla A.5 se muestra un resumen de los componentes calculados.

A partir de todo el estudio teórico anterior se puede extraer una conclusión importante, las arquitecturas distribuidas presentan un gran número de inductores, por lo que, en consecuencia, ocuparán un gran área a la hora de llevar a cabo la implementación física. Por este motivo es importante llevar a cabo un estudio de la influencia de los inductores en el consumo de área de los amplificadores distribuidos.

A.3.2.2 Resultados experimentales

De cara a optimizar el consumo de área de los amplificadores distribuidos, se han llevado a cabo tres implementaciones diferentes. La primera versión (DA1) se diseñó evitando que exista algún tipo de influencia entre los inductores integrados para ser tomado como diseño de referencia. La segunda versión diseñada (DA2) se compactó el diseño y se llevó a cabo un estudio para minimizar el acoplamiento

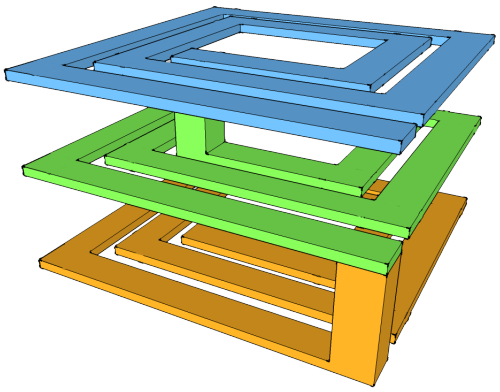


Figura A.11: Bobina multinivel.

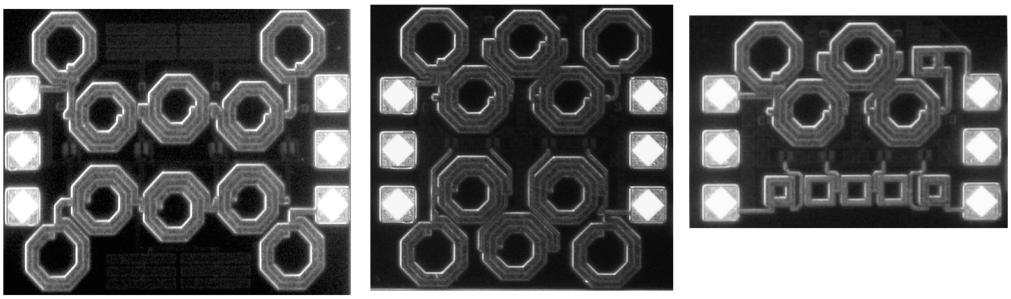


Figura A.12: a) DA1: diseño convencional (0.7 mm^2), (b) DA2: diseño compactado (0,6mm^2), (c) DA3: diseño con bobinas multinivel (0,4mm^2).

mútuo entre los inductores. Finalmente, en la tercera versión (DA3) se sustituyeron la mayor parte de los inductores integrados por inductores multinivel.

Los inductores multinivel, al contrario que los inductores integrados que se encuentran en un único nivel de metalización, se forman en distintos niveles tal y como se muestra en la Figura A.11. Con este tipo de estructura se puede conseguir una reducción de área importante aunque con una influencia negativa en el rendimiento del inductor.

En la Figura A.12 se muestra una fotografía de las tres versiones de amplificadores distribuidos desarrollados. Una de las dificultades a la hora de implementar amplificadores distribuidos integrados es conseguir inductores integrados de alta calidad. En la Figura A.13 se muestra la simulación de la inductancia y el factor de calidad de los inductores integrados en los diseños. Puede observarse como el inductor convencional tiene un factor de calidad de 9.28 y una inductancia de 1.3 nH a

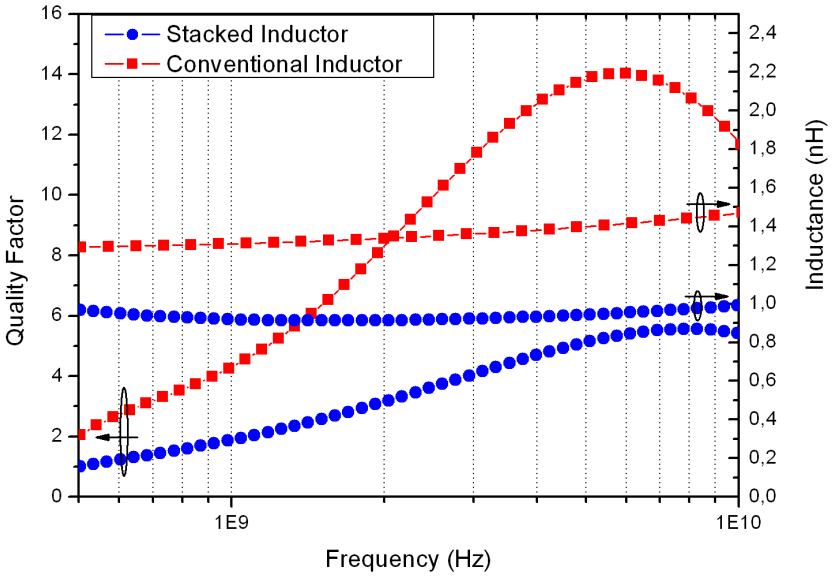


Figura A.13: Comparativa inductor convencional frente a inductor multinivel.

una frecuencia de 5 GHz. Como ya se había adelantado anteriormente puede observarse como el rendimiento de los inductores multinivel es inferior al de los inductores convencionales. Esto es debido a las capacidades asociadas a los metales inferiores que influyen negativamente en el rendimiento del inductor.

Gracias a la correcta compactación del diseño como al uso de los inductores multinivel se ha conseguido una reducción de área importante. El diseño inicial (DA1) ocupa un área total de 0.74 mm^2, incluyendo los pads de medida. Por el contrario, el diseño compactado (DA2) presenta un área total de 0.61 mm^2 lo que implica una reducción de área del 17 % con respecto al diseño inicial. Finalmente, el diseño con inductores multinivel (DA3) ocupa un área total de 0.47 mm^2, lo que implica una reducción de área de un 36 % con respecto al diseño inicial.

Después de la medida de múltiples muestras, la respuesta en frecuencia se muestra en la Figura A.14. La ganancia de la versión DA1 es de 6 dB con una planitud de ganancia de unos 0.6 dB desde 1 GHz hasta 5 GHz y con una ganancia unitaria alrededor de los 8.6 GHz. Por otro lado, el circuito presenta una figura de ruido por debajo de los 5 dB desde 1 GHz hasta los 6.5 GHz. El incremento de ganancia en banda base es debido a la alta impedancia de los condensadores de bloqueo de

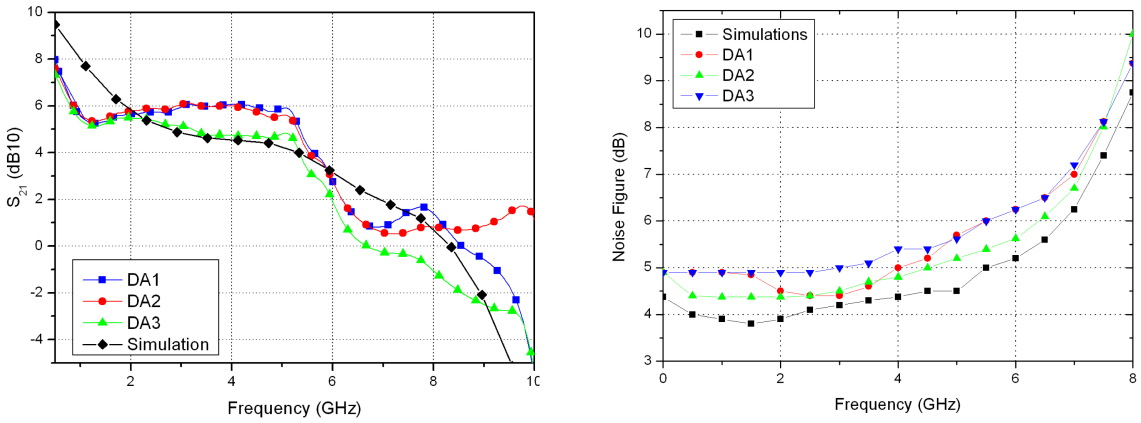


Figura A.14: Medida del S21 y la figura de ruido.

continua a baja frecuencia. La adaptación tanto de entrada como de salida es mejor de -10 dB en todo el ancho de banda.

La respuesta en frecuencia de la versión DA2 es aproximadamente la misma que la versión DA1, excepto en la mejora que aparece en la figura de ruido. Esta mejora es debido a una reducción de los parásitos asociados al reducir la longitud de muchas líneas de interconexión.

Finalmente, con respecto a la versión DA3 y a pesar de que el rendimiento de los inductores multinivel es peor que el de los inductores convencionales, la respuesta de DA3 es muy similar a la obtenida con las versiones DA1 y DA2. La figura de ruido en este caso es un poco superior debido a la resistencia serie asociada a los inductores multinivel que es un poco superior a la resistencia serie de los inductores convencionales.

Hay que mencionar que todas las medidas se hicieron bajo las mismas condiciones de polarización y que las tres versiones tienen un consumo de potencia de 90 mW.

A.3.3 Aportaciones originales

La principal aportación de este capítulo es la implementación de diferentes técnicas para la reducción de área en los amplificadores distribuidos. Como se ha podido comprobar, se ha pasado de un área total ocupada de 0.7 mm^2 a un área total de 0.4 mm^2 gracias a las técnicas de compactación empleadas y al uso de inductores

Circuito	Ganan (dB)	BW (GHz)	NF (dB)	P_{1dB} (dBm)	Area (mm^2)	P_{DC} (mW)
DA1	7	6.5	5	12.3	0.74	90
DA2	7	6.5	4.5	12.4	0.61	90
DA3	5.5	6.5	6	11.2	0.47	90

Tabla A.6: Especificaciones de los amplificadores distribuidos.

multinivel.

A.3.4 Conclusiones

Con la implementación de los amplificadores distribuidos se ha tomado contacto con el diseño de amplificadores de bajo ruido para sistemas de ultra banda ancha. Como se ha podido comprobar, los amplificadores distribuidos presentan un gran ancho de banda aunque con relativamente poca ganancia.

El principal problema de esta estructura radica en el alto consumo de potencia que presenta así como el área ocupada. Para conseguir reducir el área ocupada se han presentado dos soluciones diferentes. Primeramente se ha llevado a cabo una recolocación de los inductores en el circuito intentando minimizar la influencia del acoplamiento mútuo entre éstas. Por otro lado, se han introducido los inductores multinivel que a pesar de tener unas especificaciones peores que los inductores convencionales, el área ocupada es mucho menor. A pesar de tener peores especificaciones los inductores multinivel provocaron una influencia mínima en el rendimiento de los amplificadores distribuidos.

Usando estas técnicas se diseñaron tres versiones de amplificadores distribuidos para poder llevar a cabo comparaciones entre ellos y se obtuvieron resultados satisfactorios en cuanto a la reducción de área. En la Tabla A.6 se muestra un resumen de las especificaciones de los amplificadores distribuidos desarrollados.

A.4 Amplificadores de banda ancha

A.4.1 Objetivos

Los amplificadores distribuidos presentan un elevado consumo de potencia y ocupan un área elevada. De cara a optimizar el consumo de potencia y el área ocupada, el principal objetivo de este capítulo es la exploración de diferentes arquitecturas de amplificadores para sistemas de comunicación de ultra banda ancha intentando

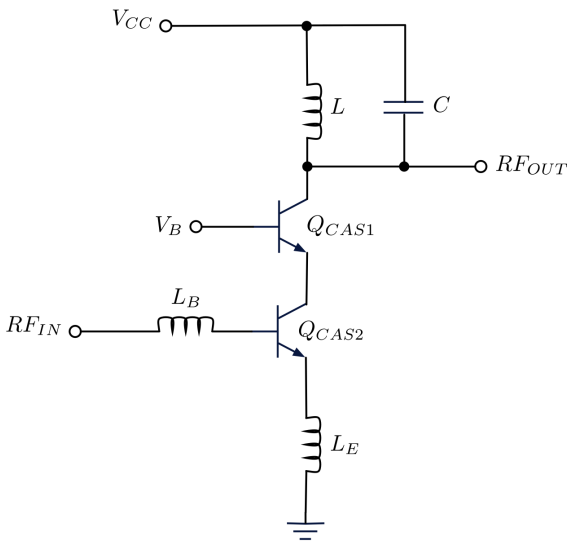


Figura A.15: Esquema simplificado de un LNA con degeneración inductiva.

optimizar el consumo de potencia y el área consumida por los mismos.

A.4.2 Planteamiento y metodología

A.4.2.1 Amplificador de banda ancha

Para llevar a cabo la implementación del amplificador de banda ancha se toma como partida la estructura de un amplificador cascodo de banda estrecha como el mostrado en la Figura A.15. Para conseguir transformar este amplificador de banda estrecha en un amplificador de banda ancha se lleva a cabo una modificación de la red de adaptación de entrada. En la estructura mostrada en la Figura A.16 puede observarse como la etapa de entrada puede considerarse compuesta por un filtro paso banda de cuarto orden. Este filtro de cuarto orden a su vez se puede dividir en dos etapas de segundo orden. Estos filtros de segundo orden están compuestos por una sección paso bajo y otra sección paso alto. La sección paso alto del filtro está compuesto por L_B y C_π. La relación existente entre los componentes y la frecuencia de corte es la siguiente:

$$high - pass \begin{cases} L_B = \dfrac{R}{\omega_L}; C_\pi = \dfrac{1}{\omega_L R} \end{cases} \tag{A.9}$$

Por otro lado, la sección paso bajo del filtro esta constituida por L_E y por C_B. En

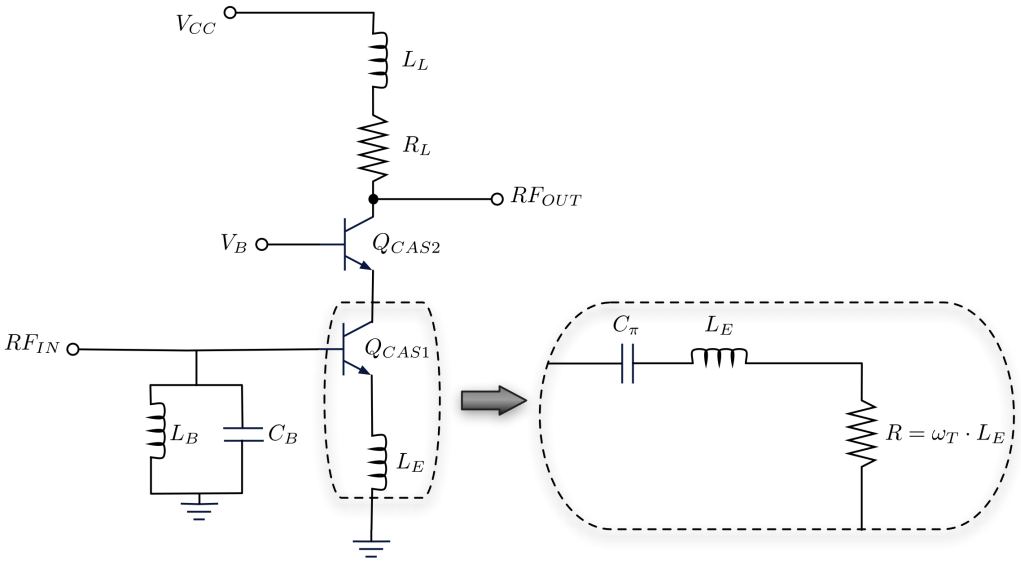


Figura A.16: Esquema simplificado LNA con adaptación de banda ancha.

este caso, la relación entre los componentes y la frecuencia de corte es la siguiente:

$$low - pass \begin{cases} L_E = \dfrac{R}{\omega_U}; C_B = \dfrac{1}{\omega_U R} \end{cases} \tag{A.10}$$

Las dos etapas de filtrado proporcionan una impedancia igual a R en la banda de paso entre ω_U y ω_L. De cara a conseguir una operación en banda ancha, una opción puede ser sustituir la carga resonante del circuito por una simple resistencia. Esta solución presenta un problema importante porque el polo parásito generado por la resistencia de salida y la capacidad parásita del nodo de salida provoca una caída a alta frecuencia. Una técnica típica para solucionar este problema es cambiar la resistencia por una carga shunt-peaking [8] compuesta por un inductancia colocada en serie a la carga de salida. Esta inductancia en serie provoca un aumento de la frecuencia de corte debido a que la inductancia introduce un cero que elimina la influencia del polo formado por la resistencia de carga y la capacidad parásita asociada al nodo de salida.

Con esta configuración la carga inductiva ecualiza la ganancia a un valor constante a lo largo de la banda de paso. El problema es que la combinación entre la carga inductiva y C_{out} introduce una resonancia que debe mantenerse siempre fuera de la banda. Como C_{out} representa la capacidad total en el nodo de salida incluyen-

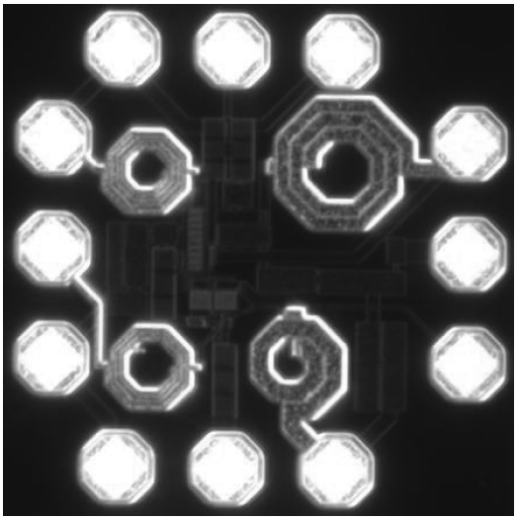


Figura A.17: Fotografía del amplificador de banda ancha.

do capacidades parásitas asociadas a las conexiones y a las propias capacidades del transistor, es necesario minimizar siempre ese efecto para asegurar que la resonancia entre la carga inductiva y C_{out} se produzca por encima de ω_U.

En la Figura A.17 se muestra una fotografía del LNA desarrollado. El área total del chip incluyendo los pads de medida es de 665x665 μm^2. El amplificador consume 5.3 mA de una fuente de alimentación de 3.3 V. En la Figura A.18 se muestra una comparativa entre la medida y la simulación del amplificador de banda ancha desarrollado y puede observarse como los resultados de las medidas son bastante similares a los obtenidos en simulación. La ganancia máxima está alrededor de 12.5 dB a una frecuencia de 3.4 GHz y el ancho de banda a 3 dB va desde 1.7 a 5.3 GHz. La ganancia unitaria del circuito es de 9.4 GHz. La medida de las pérdidas de retorno en la entrada (S_{11}) es inferior a -5 dB en toda la banda de trabajo. Por otro lado, las pérdidas de retorno a la salida (S_{22}) se encuentran también por debajo de los -4 dB en toda la banda. En la Figura A.19 se muestra la comparativa entre la simulación y la medida de la figura de ruido. La figura de ruido varía desde los 4.3 dB a 3.9 GHz hasta los 5.2 dB a 5.3 GHz, observándose como hay una similitud entre los valores de figura de ruido medidos y simulados. Finalmente, el punto de intercepción de tercer orden del circuito se encuentra en -4 dBm.

A.4.2.2 Amplificador Shunt-peaking modificado

Uno de los principales problemas del amplificador de banda ancha es que no

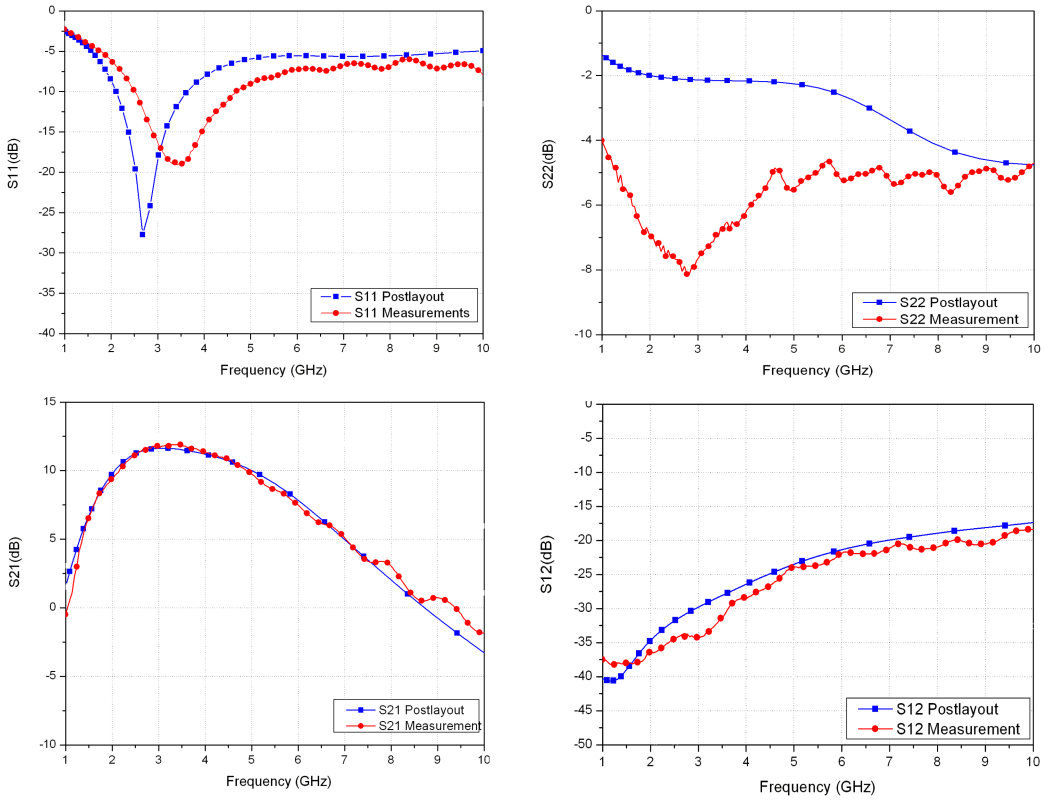


Figura A.18: Comparativa de simulación y medida de los parámetros S.

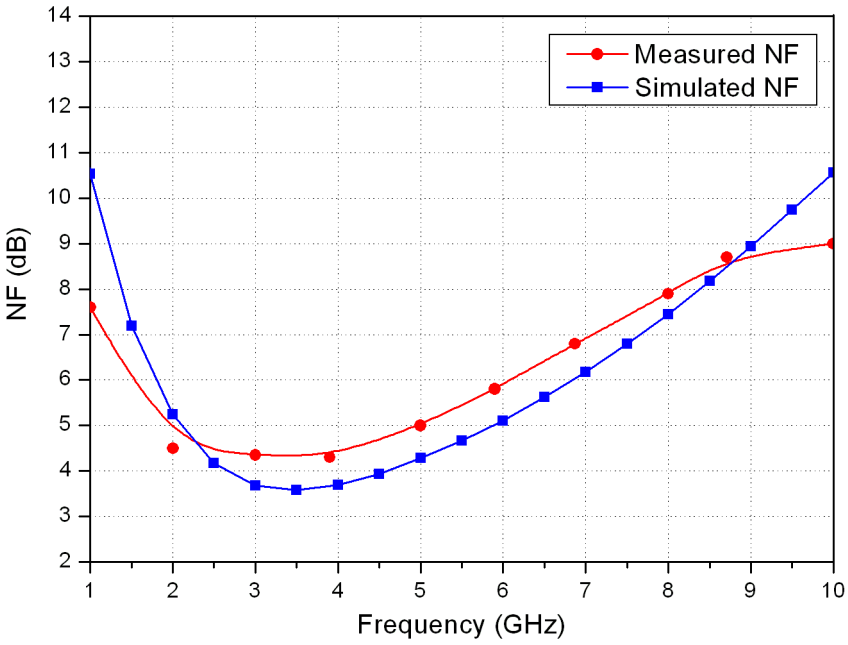


Figura A.19: Comparativa de simulación y medida de la figura de ruido.

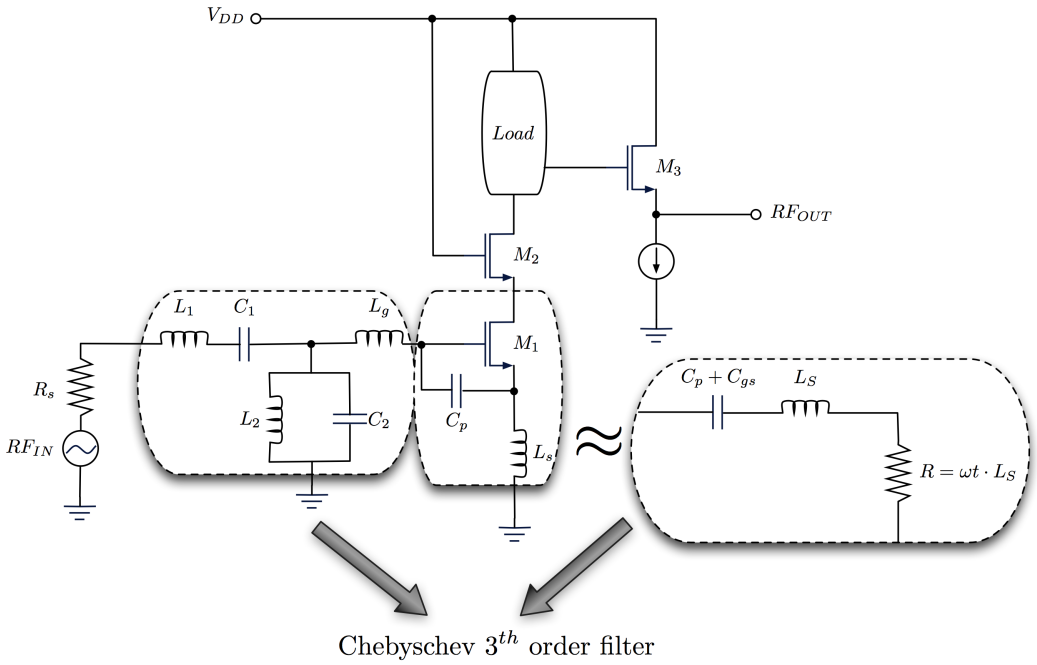


Figura A.20: Esquemático del LNA banda ancha con transistores MOSFET.

mantiene la ganancia constante a lo largo de toda la banda, esta falta de planitud en la ganancia está directamente relacionado con la carga de salida empleada.

En la Figura A.20 se muestra una versión con transistores MOSFET del amplificador de banda ancha. Este circuito esta compuesto por una etapa de ganancia con degeneración inductiva (L_g y L_s) y una carga de salida de banda ancha. Con el fin de adaptar la señal de salida a 50 Ω se ha añadido un seguidor de emisor en la salida (M3). Al igual que en el caso anterior, la impedancia de entrada esta formada por la combinación de dos filtros paso bajo y paso alto.

La ganancia de esta estructura la proporciona una estructura cascodo que mejora el aislamiento en inversa y disminuya el efecto de la capacidad Miller sobre la respuesta en frecuencia del circuito. El dimensionado de los transistores ha sido determinado para obtener un bajo ruido y un bajo consumo de potencia. Como se muestra en la Figura A.21, y al igual que en el caso anterior, para conseguir una operación de banda ancha se ha cambiado la red resonadora por una red shunt-peaking. Con esta estructura, la ganancia dentro de la banda debería ser plana y el valor de esta ganancia es proporcional a la tranconductancia del par cascodo y a la impedancia de salida de la estructura shunt-peaking que viene dada por la siguiente

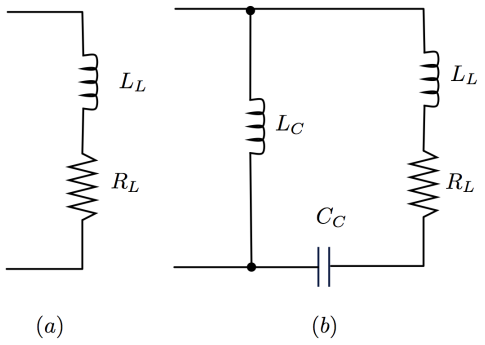


Figura A.21: (a) shunt-peaking convencional (b) shunt-peaking modificado.

expresión:

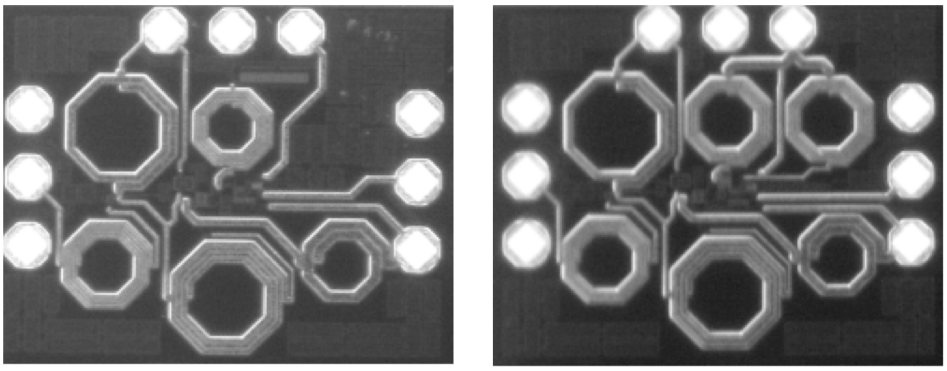
$$Z_L(j\omega) = \frac{R_L + \omega L_L}{1 - \omega^2 L_L C_{out} + j\omega C_{out} R_L} \tag{A.11}$$

donde C_{out} representa la capacidad equivalente en el nodo de salida del circuito incluyendo las capacidades parásitas de los transistores y todas las capacidades asociadas al interconexionado. Como se puede observar, la expresión anterior contiene dos polos y un cero. La existencia de estos polos y ceros provoca la aparición de un pico en la respuesta en frecuencia del circuito, degradando la planitud de la ganancia. Una posible solución a este problema es mantener ambas resonancias fuera de la banda usando un valor bajo para L_L, pero esa solución implica una baja ganancia del circuito.

Con el fin de mantener una alta ganancia se debe elegir un valor de R_L suficientemente alto para mejorar la ganancia a baja frecuencia. Sin embargo, el rango dinámico del circuito impone una limitación en cuanto al valor resistivo de R_L. Para intentar solucionar estos inconvenientes se propone una modificación de la estructura shunt-peaking.

La modificación de la estructura shunt-peaking tal y como se ve en la Figura A.21 esta basada en una estructura convencional shunt-peaking que actua de manera desacoplada de la etapa cascodo a través del condensador C_C. Para polarizar la etapa activa se ha colocado el inductor L_C entre V_{DD} y el drenador del transistor M2. En consecuencia, la impedancia de esta nueva etapa viene dada por:

$$Z(j\omega) = \frac{j\omega L_C R_L \left(\frac{j\omega L_L}{R_L} + 1\right)}{1 - j\omega^3 L_C L_L C_{out} - \omega^2 L_C R_L C_{out} + j\omega(L_C + L_L)} \tag{A.12}$$



(a) (b)

Figura A.22: Fotografía del LNA con shunt-peaking y LNA con shunt-peaking modificado respectivamente.

Como el valor de C_C es un valor alto, su efecto es despreciable en la expresión anterior. Con esta configuración, el valor de la resistencia R_L puede ser incrementado sin ningún problema evitando el problema impuesto por la estructura shunt-peaking tradicional, por lo que inmediatamente se consigue una mejora en la planitud de la ganancia del circuito.

En la Figura A.22 se muestra una fotografía del LNA con shunt-peaking tradicional y con el shunt peaking modificado desarrollados. Como puede observarse, ambos layout son muy similares a excepción de la inductancia L_C situada en la esquina superior derecha. El tamaño del circuito incluyendo los pads es de 949 x 760 μm^2. Cada amplificador consume 17 mA de una fuente de alimentación de 3.3 V.

La medida de la ganancia (S_{21}) y la adaptación de entrada (S_{11}) se muestra en la Figura A.23. Como puede observarse la ganancia es mucho más plana en el caso del LNA con shunt-peaking modificado y tiene un valor aproximado de 10 dB. En ambos amplificadores la adaptación de entrada es muy similar ya que ambos circuitos tienen la misma estructura de entrada. Del mismo modo, como ambos tienen la misma etapa de entrada, en la Figura A.24 puede observarse como la figura de ruido de ambos circuitos es muy similar.

A.4.2.3 Amplificador cascodo doblado

Tanto el amplificador de banda ancha desarrollado anteriormente como el amplificador con shunt-peaking modificado están basados en una estructura cascodo. En la estructura cascodo es necesario llevar a cabo la polarización de dos transistores,

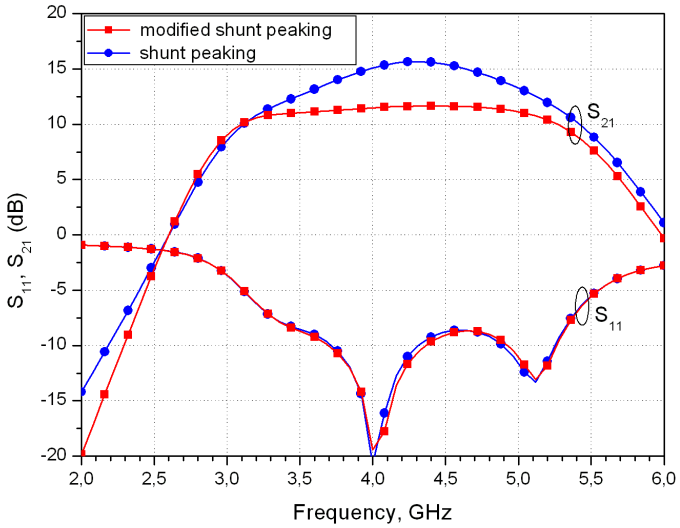


Figura A.23: Medida de los parámetros S.

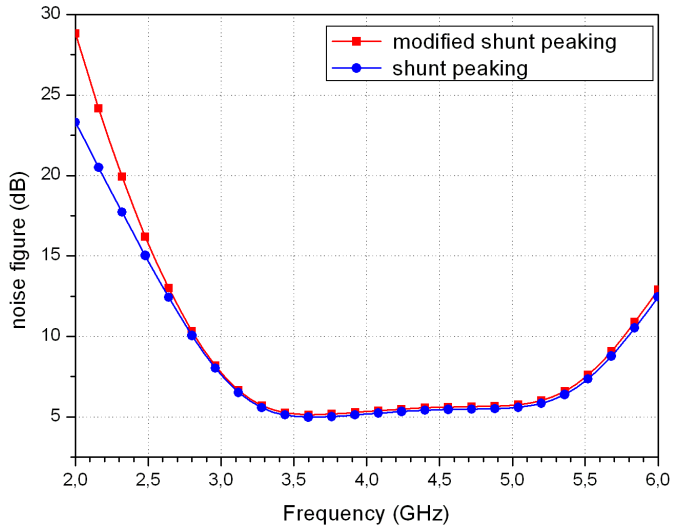


Figura A.24: Medida de la figura de ruido de los LNA con shunt peaking normal y modificado.

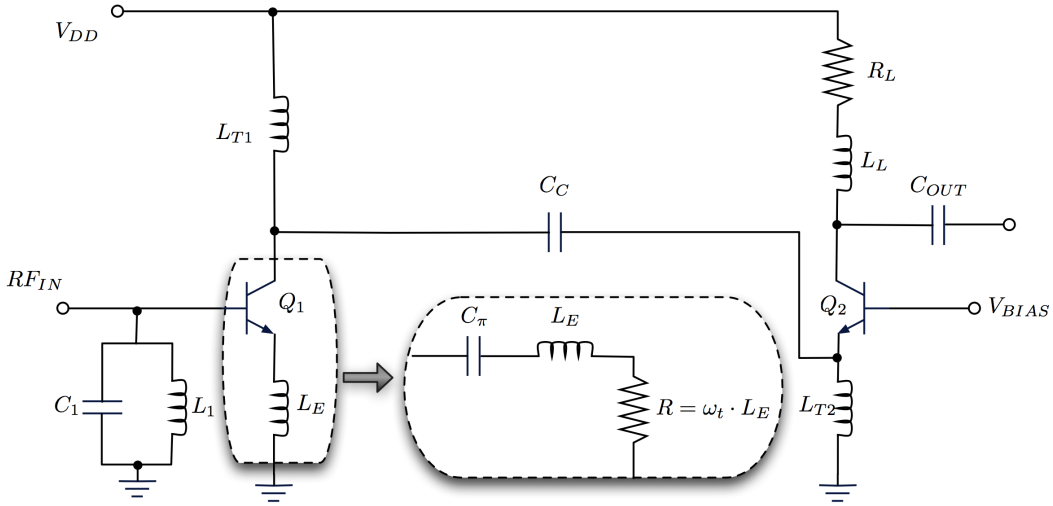


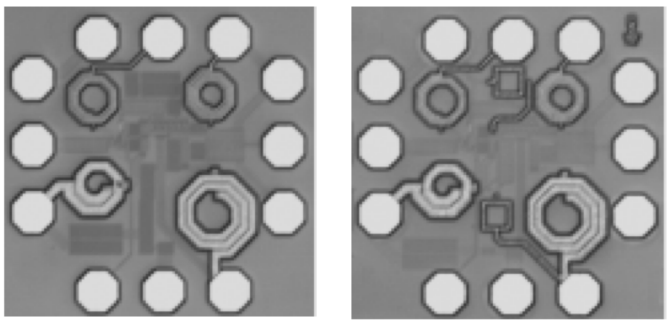
Figura A.25: Esquemático simplificado del LNA cascodo doblado.

esta polarización hace que la excursión de señal alterna permitida en esta estructura se vea reducida. De cara a solucionar este problema aparece la estructura cascodo doblado.

En la Figura A.25 se muestra el esquemático del amplificador cascodo doblado. Como se puede observar, la etapa de entrada es igual a la etapa empleada en los circuitos anteriores. La principal diferencia radica en el hecho de que el cascodo se separa en dos ramas independientes con alimentaciones separadas. Esta separación implica que ahora solamente es necesario polarizar un transistor por rama por lo que la excursión de señal alterna en esta estructura es mayor.

De cara a comprobar la funcionalidad del amplificador cascodo doblado se desarrollaron dos versiones una versión cascodo y una versión cascodo doblado para poder llevar a cabo la comparación en el rendimiento de ambas. En la Figura A.26 puede verse la fotografía de ambos circuitos. En la versión doblada además se ha hecho uso de los inductores multiniveles tal y como se hizo con los amplificadores distribuidos para conseguir una mejora en el consumo de área del circuito. El tamaño de ambos circuitos es de 665x665 μm^2.

La Figura A.27 muestra la medida de la ganancia (S_{21}) y la medida de las pérdidas de inserción (S_{11}) de ambos LNAs. Como era de esperar la respuesta de ambos circuitos es muy similar. Por otro lado, en la Figura A.28 se muestra la simulación de figura de ruido de ambos circuitos, en este aspecto el cascodo doblado



(a) (b)

Figura A.26: (a) LNA cascodo y (b) LNA cascodo doblado.

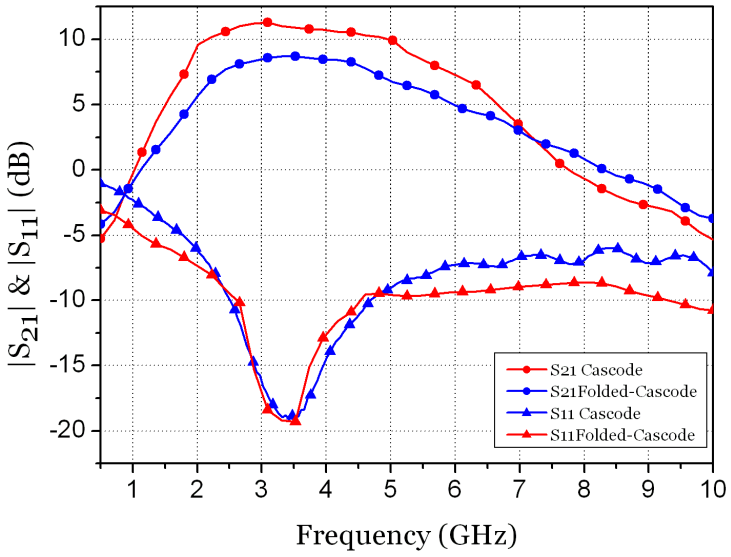


Figura A.27: Medidas del S_{21} y S_{11}.

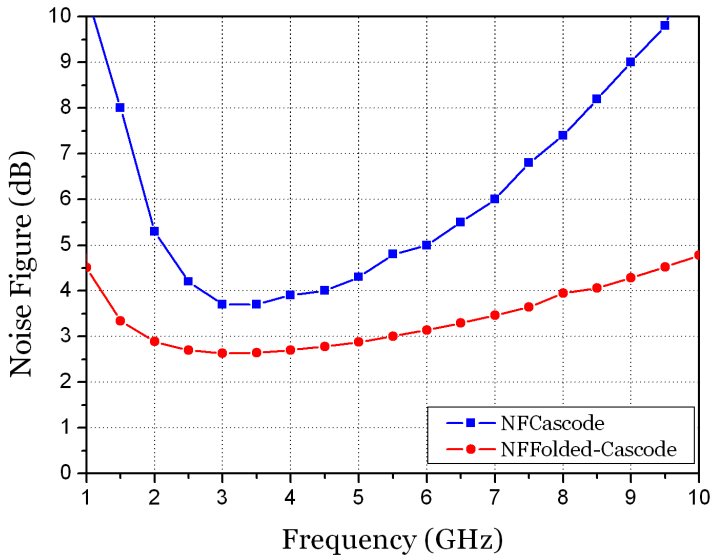


Figura A.28: Medida figura de ruido del cascodo convencional y el cascodo doblado.

Parámetro	Cascodo	Cascodo doblado
Tensión de alimentación (V)	3	1.5
Consumo de potencia (mW)	18.93	18.87
$V_{CE}(Q_1, Q_2)$ (V)	1.5	1.5
$V_{BE}(Q_1, Q_2)$ (V)	0.8	0.8
NF @ 4 GHz (dB)	3.19	2.96
Ganancia-S_{21} @ 4 GHz (dB)	10.1	7.8
IIP3 @ 5GHz (dBm)	-4	-4

Tabla A.7: Comparación entre el cascodo convencional y el cascodo doblado.

presenta una mejora con respecto al diseño cascodo convencional.

Finalmente tal y como se muestra en las figuras A.29 y A.30 la linealidad es similar en ambos circuitos teniendo en cuenta que el amplificador en cascodo doblado esta alimentado con la mitad de tensión que el cascodo convencional. En la Tabla A.7 se muestra un resumen de las especificaciones de ambos circuitos.

A.4.3 Aportaciones originales

Las aportaciones de este capítulo han sido el desarrollo de tres amplificadores para comunicaciones de ultra banda ancha, mejorando las especificaciones obtenidas por los amplificadores distribuidos. Además de desarrollar estos tres circuitos se ha

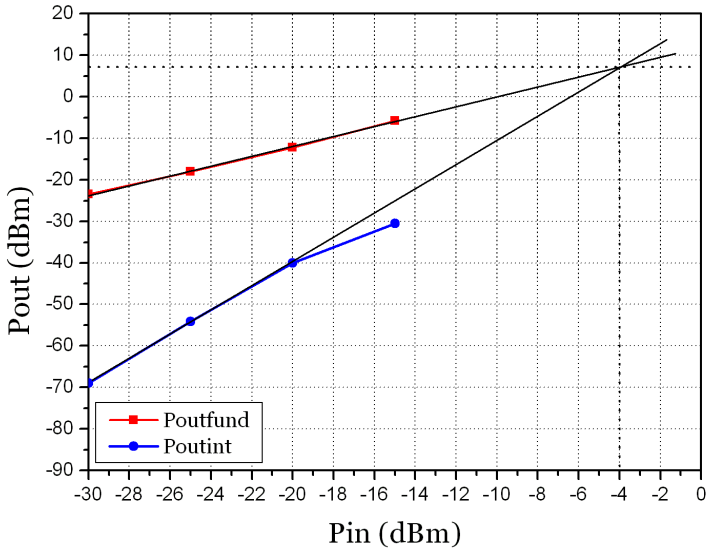


Figura A.29: Medida del IIP3 del LNA cascodo.

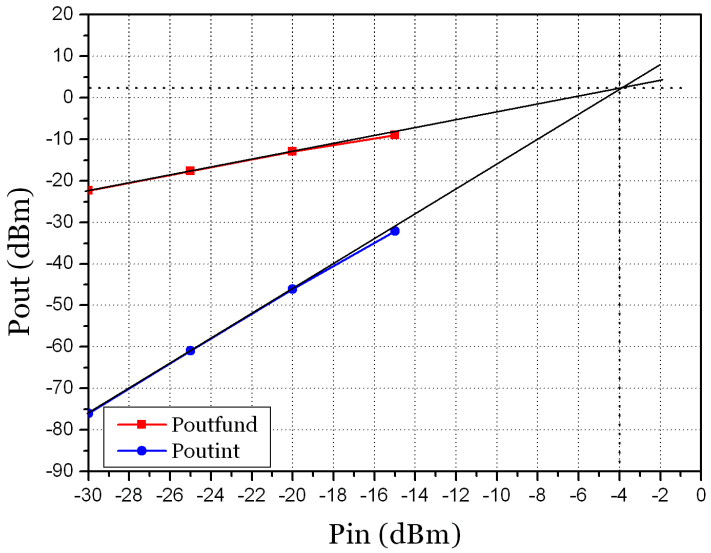


Figura A.30: Medida IIP3 del LNA cascodo doblado.

Diseño.	Ganancia (dB)	BW (GHz)	NF (dB)	IIP3 (dBm)	Area (mm^2)	P_{DC} (mW)
Banda ancha	12.5	5.3	4.3	-4	0.13	32
Shunt-peaking modificado	11.2	5	5	5.1	0.29	56.1
Cascodo doblado	8.24	2.96	3	-4	0.13	18.93

Tabla A.8: Especificaciones de los amplificadores desarrollados.

trabajado también en la optimización de área de los mismos utilizando inductores multinivel cuando ha sido posible.

A.4.4 Conclusiones

A lo largo de este capítulo se han presentado tres diferentes alternativas para la implementación de LNAs para comunicaciones de ultra banda ancha con unas especificaciones superiores a las obtenidas con los amplificadores distribuidos. La primera alternativa presentada fue el amplificador de banda ancha que tiene una buena respuesta en frecuencia pero presenta algunos problemas para mantener la planitud de la ganancia. Para solucionar este problema se desarrolló el circuito con una estructura shunt-peaking modificada. Finalmente, se desarrolló una estructura cascodo doblado que puede trabajar con bajos niveles de tensión, presentando una linealidad superior a la obtenida con las otras estructuras. A modo resumen, en la Tabla A.8 se recogen las especificaciones de los circuitos desarrollados.

A.5 Amplificadores realimentados

A.5.1 Objetivos

En general, las técnicas de realimentación ayudan a mejorar el rendimiento en amplificadores. El bucle de realimentación ayuda a incrementar el ancho de banda y la ganancia y en algunos casos, incluso colabora a conseguir una reducción de la figura de ruido y el consumo de potencia. Es por estos motivos por los que es interesante estudiar la posibilidad de aplicar técnicas de realimentación al diseño de

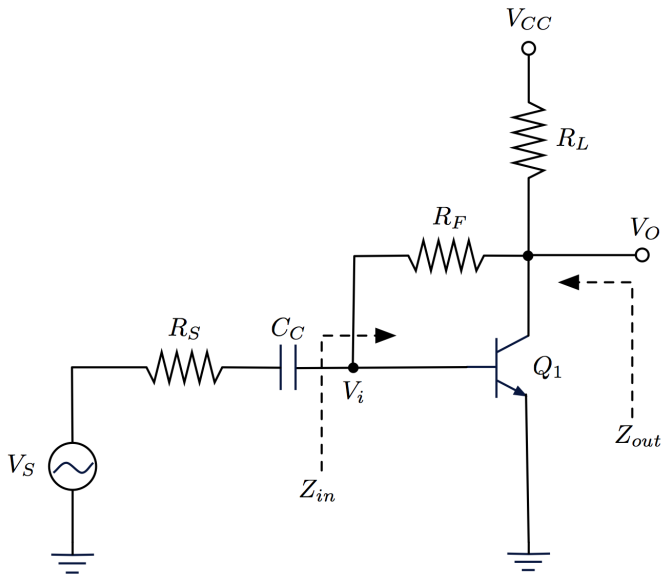


Figura A.31: Esquemático LNA realimentado.

amplificadores de bajo ruido para sistemas de ultra banda ancha.

A.5.2 Planteamiento y metodología

A.5.2.1 Aproximación téorica

La Figura A.31 muestra el esquemático de un amplificador emisor común realimentado. Ignorando algunos problemas asociados a las capacidades parásitas del transistor, la ganancia de tensión viene dada por la siguiente expresión:

$$A_V = \frac{v_o}{v_i} = \frac{\frac{R_L}{R_F} - g_m R_L}{1 + \frac{R_L}{R_F}} \approx \frac{-g_m R_L}{1 + \frac{R_L}{R_F}} \tag{A.13}$$

donde g_m es la transconductancia del transistor Q1.

Esto significa que la ganancia sin la realimentación ($-g_m R_L$) es reducida por la presencia del bucle de realimentación. La impedancia de entrada también cambia con respecto al amplificador en bucle abierto. Ignorando los efectos de capacidades parásitas la impedancia de entrada queda acorde a la siguiente expresión:

$$Z_{in} = \frac{R_F + R_L}{(1 + g_m R_L)} \approx \frac{R_F + R_L}{g_m R_L} \tag{A.14}$$

En este caso concreto, la realimentación colabora a mejorar la linealidad del circuito. En cambio, a pesar de mejorar la linealidad se produce un empeoramiento en el factor de ruido debido a la influencia de un nuevo inductor en la entrada del circuito. Llevando a cabo un análisis de ruido, se puede obtener que el factor de ruido sigue la siguiente expresión:

$$F = 1 + \frac{r_b + r_e}{R_S} + \frac{1}{2g_m R_S} + \frac{g_m R_s}{2\beta} + \frac{g_m R_S}{2\beta^2} + \frac{1}{2g_m}\frac{R_S}{{R_F}^2} + \frac{R_S}{R_F} \tag{A.15}$$

donde r_b y r_e son las resistencias parásitas de base y emisor y β es la ganancia en corriente de pequeña señal. Tal y como se había comentado del análisis de ruido se extrae que la resistencia de realimentación R_F influye negativamente en el ruido del circuito. Esto es debido a que la resistencia R_F tiene una magnitud similar a la resistencia de base R_S. La relación existente entre la linealidad del circuito y los parámetros del mismo es la siguiente:

$$IIP3_{LNA} \propto {g_m}^2 \propto {I_{bias}}^2 \tag{A.16}$$

Intuitivamente, un valor grande de g_m mejorará la linealidad del circuito. Una mayor g_m implica un mayor consumo de corriente. Sin embargo, cuando se trabaja en alta frecuencia es necesario inyectar más corriente para minimizar el efecto de los parásitos y obtener ganancia. El hecho de tener que inyectar más corriente proporciona cierta flexibilidad a la hora de obtener el valor de g_m. La ganancia de tensión dada por la Ecuación A.13 proporciona una relación entre R_L y R_F para una g_m dada. Como resultado de esto, el factor de ruido y la impedancia de entrada están acoplados porque tal y como se muestra en las ecuaciones A.13 y A.15 ambos elementos dependen de los valores de R_L y R_F. Debido a esta relación puede ser complicado llegar a conseguir un compromiso entre ambos valores para un bajo factor de ruido y una adaptación de entrada de 50 Ω.

Para resolver este inconveniente, puede ser útil reemplazar el bucle de realimentación pasivo por un bucle activo compuesto por un seguidor de emisor tal y como se muestra en la Figura A.32. En este caso, la impedancia del circuito viene dada por la siguiente expresión:

$$Z_{in} = \frac{1 + g_{m2}R_F}{g_{m2}(1 + g_{m1}R_L)} \approx \frac{R_F}{g_{m1}R_L} \tag{A.17}$$

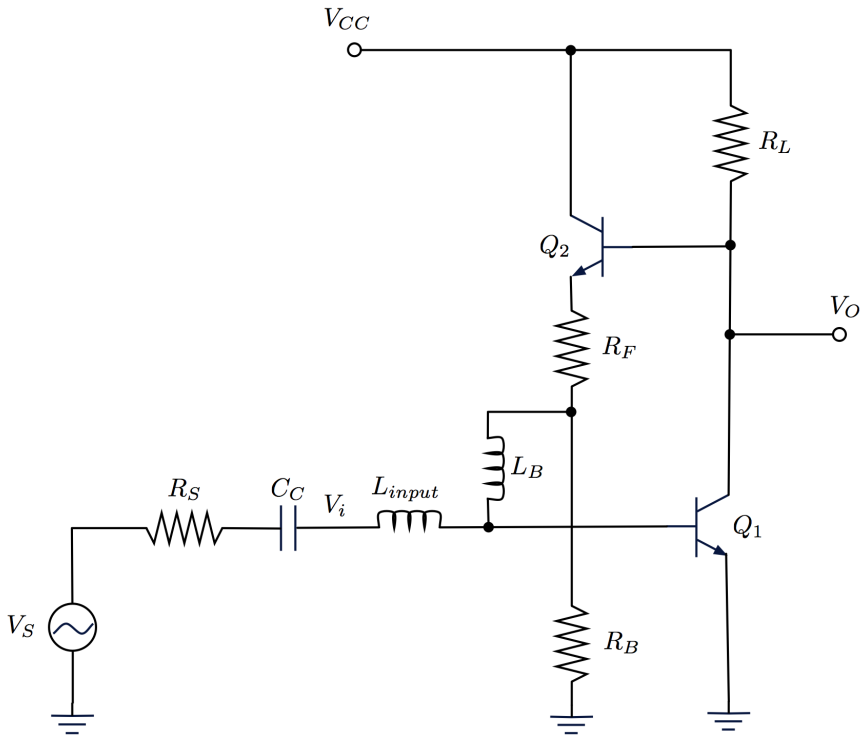


Figura A.32: Esquemático LNA realimentado con bucle activo.

donde g_{m2} es la transconductancia del transistor Q_2. Para una impedancia de entrada de 50 Ω y para la misma ganancia de tensión el valor de R_F mejora en este caso con respecto al caso anterior. Otra ventaja de esta alternativa es que gracias al uso de R_F, R_B y Q_2, la tensión de colector de Q_1 puede ser modificada tal y como se muestra en la siguiente expresión:

$$V_{CE1} \approx V_{BE2} + V_{BE1} \cdot \left(\frac{R_F}{R_B} + 1 \right) \tag{A.18}$$

Como resultado, se puede aumentar la linealidad total del circuito. Finalmente, en el diseño propuesto de cara a mejorar el ancho de banda se ha reemplazado la carga de salida por una carga shunt-peaking tal y como se ha hecho en otros circuitos.

A.5.2.2 Resultado Experimentales

De cara a reducir el área total del circuito, se ha optado por utilizar inductores multinivel modificados tal y como se muestra en la Figura A.33. Como puede observarse, el inductor va desde el nivel más alto de metalización al más bajo y luego

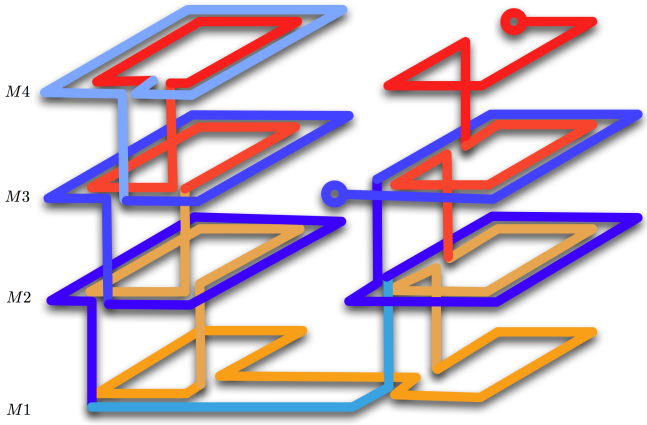


Figura A.33: Estructura de inductor 3D.

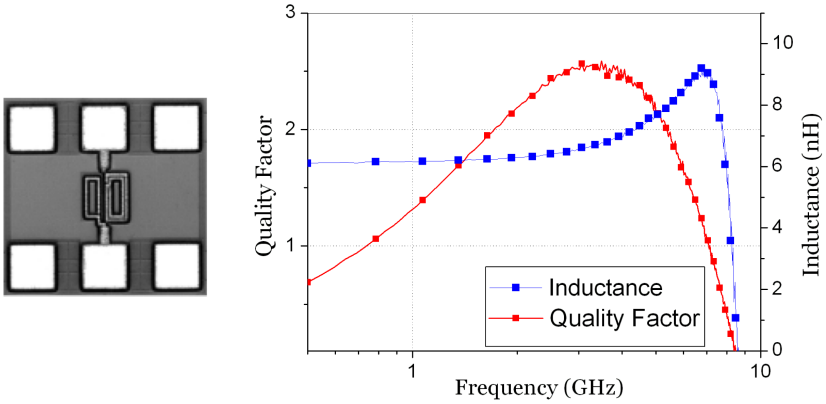
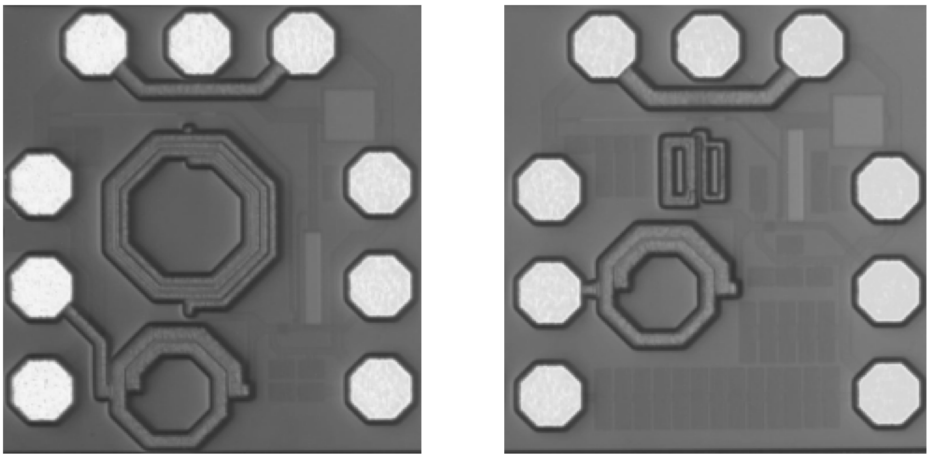


Figura A.34: Layout y medida del inductor 3D modificado.



(*a*) (*b*)

Figura A.35: Fotografía de los LNAs: (a) versión inductores convencionales, (b) versión inductor 3D modificado.

vuelve a subir. En la Figura A.34 se puede ver el layout y resultados de simulación del inductor. Como se puede observar, presenta un factor de calidad relativamente bajo. Este factor de calidad tan bajo es debido al incremento de los parásitos con respecto al sustrato al bajar a través de los diferentes niveles de metalización.

Para comprobar el correcto funcionamiento del circuito con la bobina 3D modificada, se han desarrollado dos versiones del circuito. En la primera versión se han empleado inductores convencionales y en la segunda versión se ha usado el inductor modificado 3D. En la Figura A.35 se muestra una fotografía de ambos circuitos. las dimensiones del área activa de ambos circuitos es de 490x355 μm^2 para el LNA1 y de 330x310 μm^2 para el LNA2. Utilizando los inductores 3D modificados, se ha conseguido un ahorro de área de un 40 % con una influencia mínima en las especificaciones del circuito.

En la Figura A.36 y en la Figura A.37 se muestra la simulación de ganancia del circuito y de la figura de ruido. Ambos amplificadores tienen una ganancia que varía desde los 14 dB hasta los 7 dB en la banda que va desde los 3.1 GHz hasta los 10.6 GHz. La figura de ruido para el LNA1 va desde los 4.2 dB hasta los 5.6 dB a 10.6 GHz. En el caso del LNA2 la figura de ruido pasa desde los 2.9 a 4 dB en el rango de 3.1 a 10.6 GHz. Ambos circuitos presentan una correcta adaptación de entrada y salida en el rango de 3.1 GHz a 10.6 GHz.

Finalmente, en la Figura A.38 se muestra la simulación de linealidad de ambos

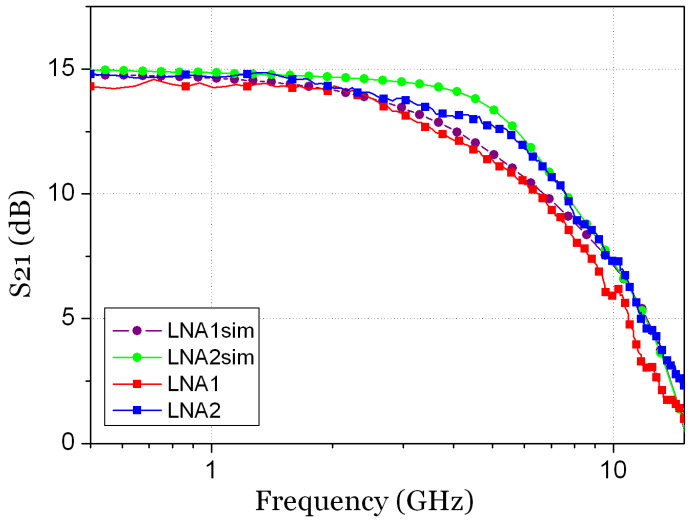


Figura A.36: Simulación y medida de ganancia.

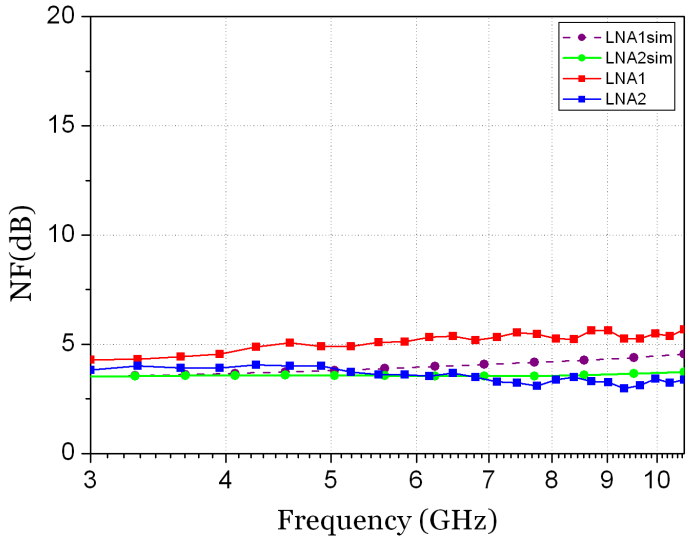


Figura A.37: Simulación y medida de figura de ruido.

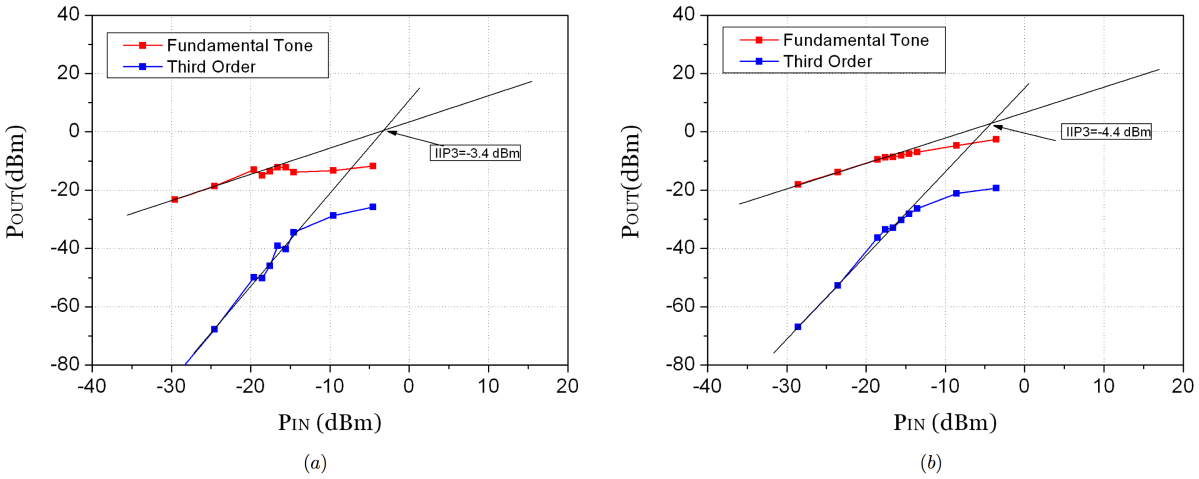


Figura A.38: Medida linealidad (a) LNA1 (b) LNA2.

circuitos. Como puede observarse, el LNA1 tiene un IIP3 de -3.4 dBm y el LNA2 presenta un IIP3 de -4.4 dBm.

A.5.3 Aportaciones originales

En este capítulo se ha hecho uso de las técnicas de realimentación y se ha podido obtener un LNA con unas especificaciones superiores a cualquiera de los desarrollados en capítulos anteriores. El uso de inductores multinivel 3D ha posibilitado reducir el área del circuito en un 40 % con una mínima influencia en las especificaciones del circuito.

A.5.4 Conclusiones

El uso de las técnias de realimentación ha permitido mejorar las prestaciones del LNA desarrollado, provocando una mejora considerable con respecto a los circuitos desarrollados en capítulos anteriores. Por otro lado, el uso de inductores 3D modificados ha posibilitado una reducción de área considerable en comparación a circuitos desarrollados con inductores convencionales.

En la Tabla A.9 se muestra un resumen de las especificaciones de los circuitos

Ref.	Ganan (dB)	BW (GHz)	NF (dB)	P_{1dB} (dBm)	Area (mm^2)	P_{DC} (mW)
Inductor estándar	14	5.5	< 4	-3.4	0.17	13.2
Inductor 3D	14	6.7	< 4	-4.4	0.10	13.2

Tabla A.9: Especificaciones de los amplificadores.

desarrollados en este capítulo.

A.6 Técnicas sin inductores

A.6.1 Objetivos

A lo largo de todo el trabajo se ha podido comprobar que la mayor parte del área esta ocupada por los inductores integrados. De cara a reducir el área, en este capítulo se explorará el desarrollo de una estructura sin inductores.

A.6.2 Planteamiento y metodología

A.6.2.1 Aproximación teórica

Para el desarrollo del LNA sin inductores se ha optado por desarrollar un LNA puerta común. La estructura en puerta común no sufre del efecto Miller, de hecho la red de adaptación de entrada y la red de salida pueden ser diseñadas de forma independiente.

La estructura más básica de amplificador puerta común es la mostrada en la Figura A.39 (a). Para que el circuito funcione correctamente es necesario que haya una gran impedancia desde el nodo de entrada a tierra, la opción más sencilla es colocar una fuente de corriente, pero esa fuente de corriente hará empeorar las especificaciones de ruido del circuito. Una solución a este problema puede ser la solución mostrada en la Figura A.39 (b) donde se sitúa un inductor en serie que forma un resonador con la capacidad parásita asociada C_{par}. Esta situación puede darse en casos en los que no sea necesaria conexión externa. Cuando es necesaria una conexión externa aparece el caso mostrado en la Figura A.39 (c) donde aparece un inductor en serie (asociado al conexionado) así como una capacidad de entrada. En esta estructura concreta se puede conseguir una adaptación de entrada a 50 Ω utilizando capacidades.

La Figura A.40 muestra de manera resumida la interfaz de unión entre el LNA y

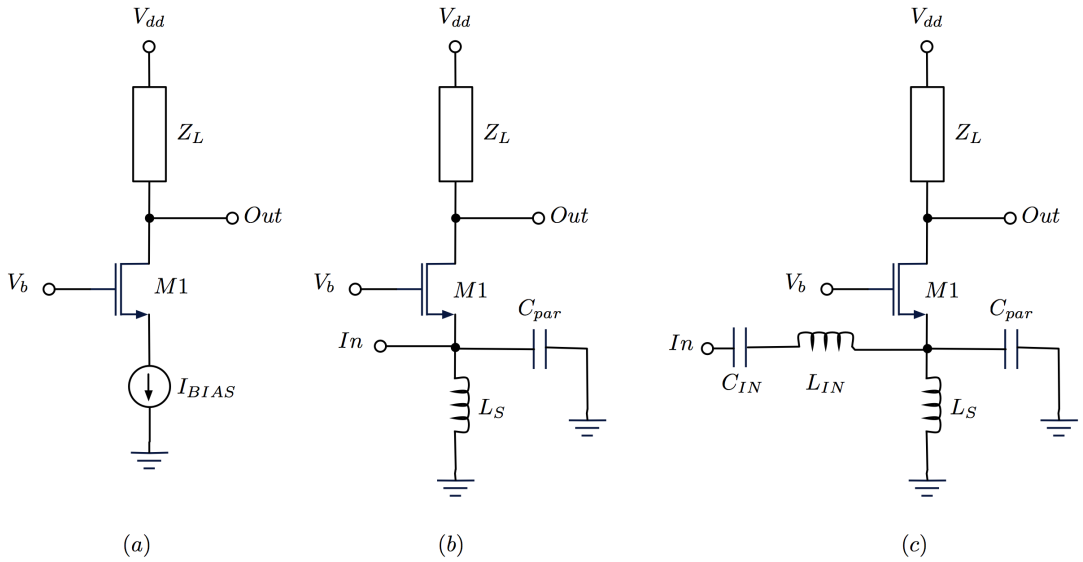


Figura A.39: Etapas de entrada LNA puerta común: a) fuente de corriente, b) resonador paralelo c) resonadores en serie y paralelo.

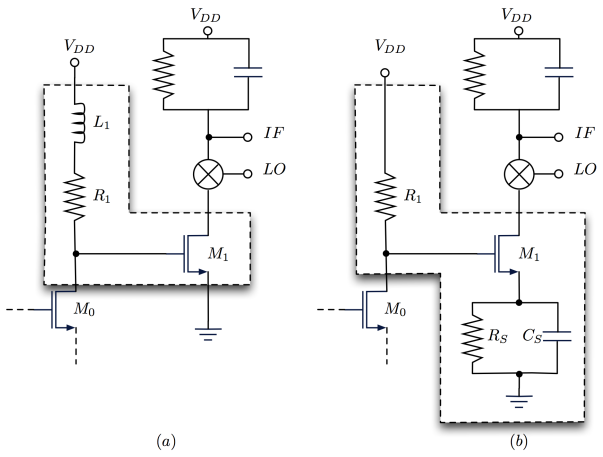


Figura A.40: Conexionado simplificado de (a) shunt-peaking y (b) degeneración capacitiva.

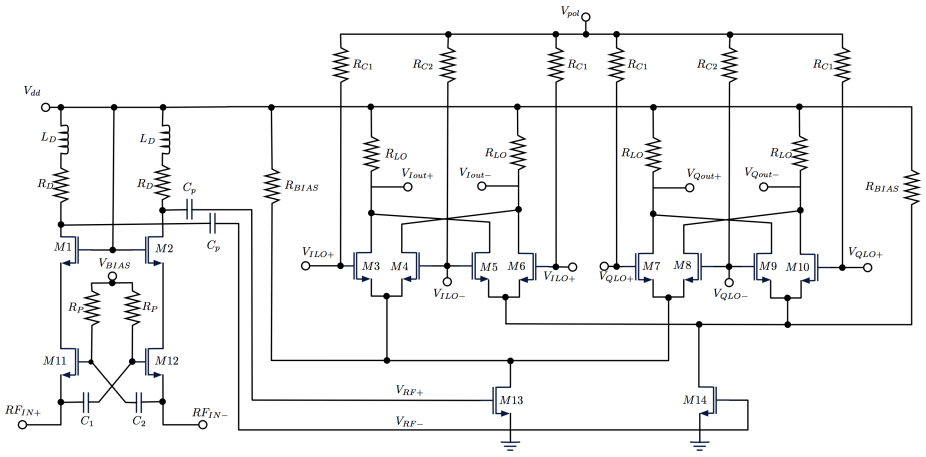


Figura A.41: Esquemático del Receptor I.

el mezclador. Los elementos de polarización y acoplo de AC se han eliminado para clarificar el diagrama. En esta Figura, M_0 representa el transconductor del LNA que se ha implementado con una estructura de puerta común. Por otro lado, M_1 representa el transconductor de RF del mezclador. En la Figura A.40a se muestra la clásica carga de salida con shunt-peaking para aumentar el ancho de banda del circuito. Este aumento del ancho de banda se produce por la introducción de un cero en la función de transferencia debido al inductor. Otra alternativa para introducir el cero necesario para aumentar el ancho de banda puede conseguirse, como se muestra en la Figura A.40b por medio de una degeneración capacitiva, donde la combinación de R_C y C_S generan el cero necesario para aumentar el ancho de banda total del circuito.

De cara a poder llevar a cabo una comparativa de rendimiento se han desarrollado dos circuitos que aplican las técnicas que se han comentado. La primera versión va a utilizar la carga shunt-peaking, tal y como muestra la Figura A.41. Por el contrario, para evitar el uso de inductores se creará una degeneración capacitiva en el mezclador Gilbert como se ha comentado. De esta forma se evita el uso de inductores, como se muestra en la Figura A.42.

A.6.2.2 Resultados Experimentales

La Figura A.43 muestra el layout del Receptor I compuesto por un LNA puerta común con carga shunt peaking y un mezclador Gilbert doblemente balanceado. El

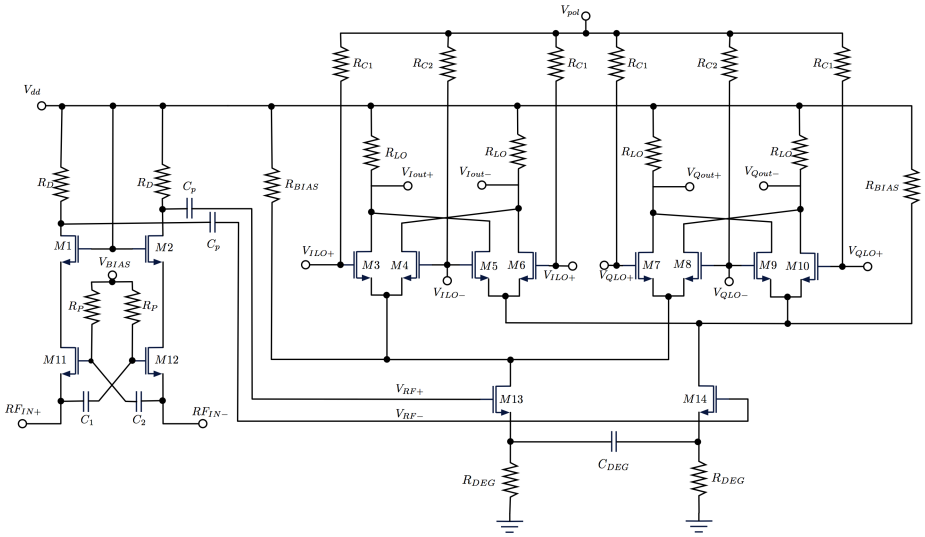


Figura A.42: Esquemático del Receptor II.

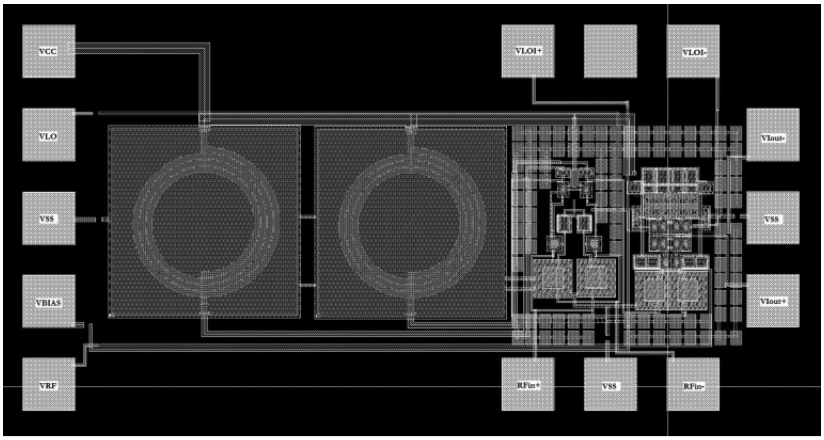


Figura A.43: Layout del Receptor I.

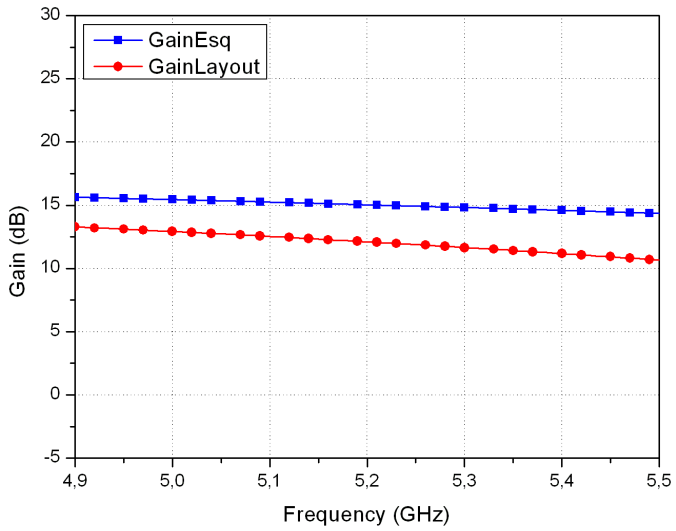


Figura A.44: Simulación de la ganancia del Receptor I.

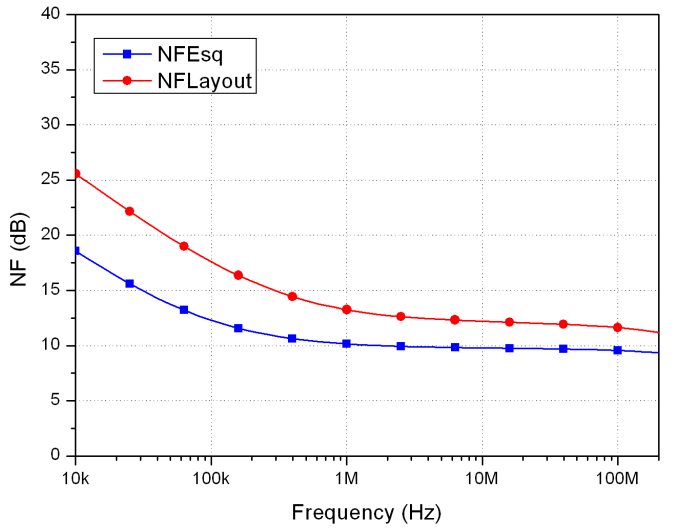


Figura A.45: Simulación del ruido del Receptor I.

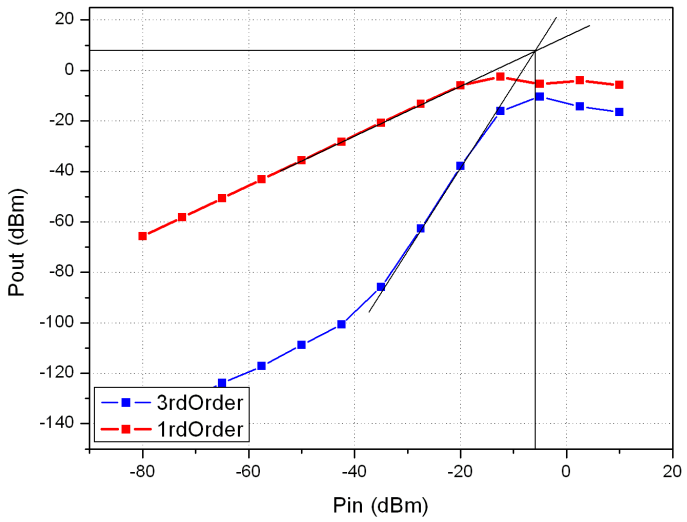


Figura A.46: Simulación del IIP3 del Receptor I.

área de este circuito es de 1410x693 μm^2.

En la Figura A.44 se muestra la simulación de ganancia del Receptor I, puede observarse como el circuito presenta una ganancia alrededor de 13 dB. Por otro lado, en la Figura A.45 se muestra la simulación de la figura de ruido, presentando el Receptor I una figura de ruido alrededor de los 13 dB. Este elevado valor de la figura de ruido puede estar condicionado por la propia estructura del LNA puerta común. Finalmente en la Figura A.46 se muestra la simulación de la linealidad del circuito, presentando el Receptor I un IIP3 de unos -3.3 dBm.

Por otro lado, en la Figura A.47 se muestra el layout del Receptor II compuesto por un LNA puerta común sin inductores. Como se ha comentado, en este caso la carga de salida del LNA esta formada por la etapa de entrada del mezclador Gilbert doblemente balanceado. El área total ocupada por el Receptor II es de 698x744 μm^2, provocando un ahorro de área del 54 % con respecto al Receptor I.

En la Figura A.48 se muestra la simulación de la ganancia del Receptor II, comprobando como la ganancia de este receptor está en torno a los 7.2 dB. En la Figura A.49 se muestra la simulación de la figura de ruido y puede verse como está en torno a los 13 dB. Finalmente la linealidad de este segundo receptor también es muy similar a la del primer receptor tal y como se muestra en la Figura A.50, donde se

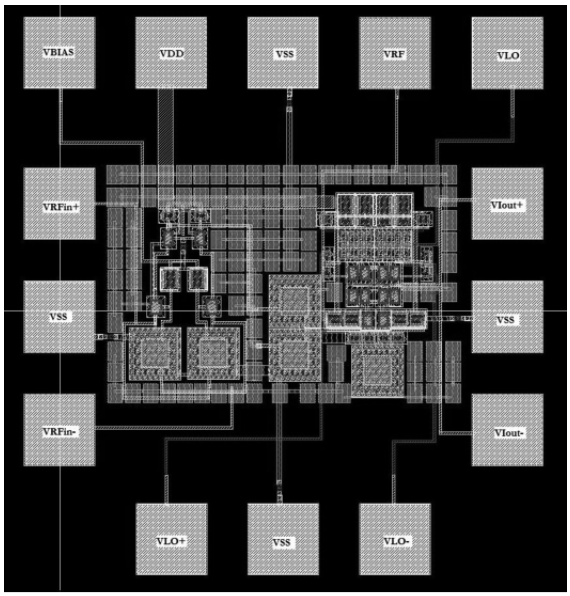


Figura A.47: Layout del Receptor II.

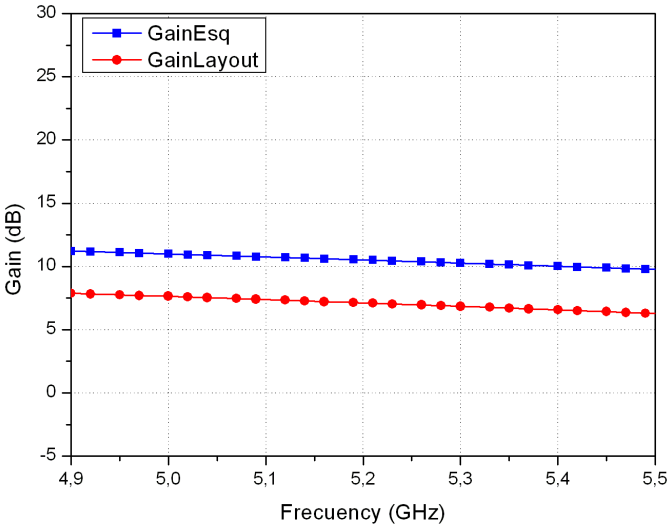


Figura A.48: Simulación de la ganancia del Receptor II.

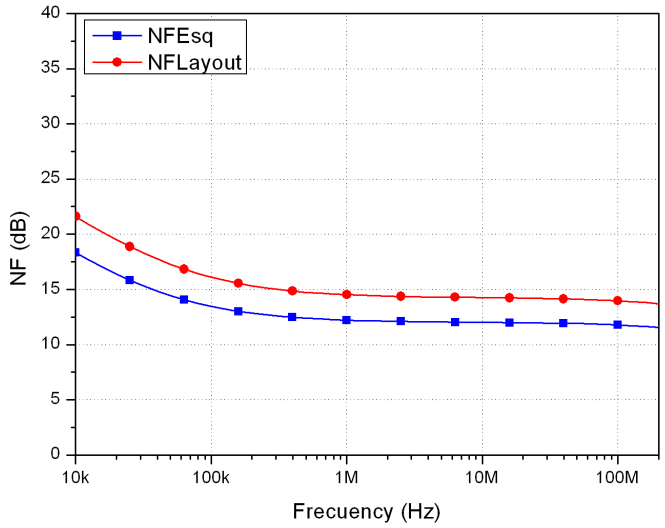


Figura A.49: Simulación de la figura de ruido del Receptor II.

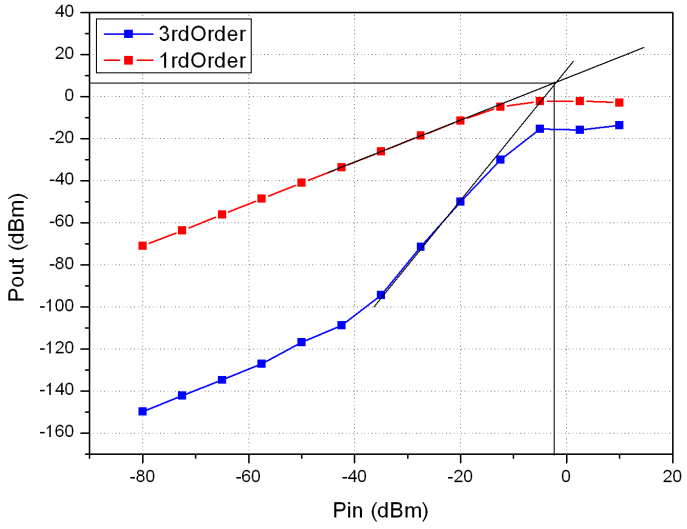


Figura A.50: Simulación del IIP3 del Receptor II.

Receptor	Receptor I	Receptor II
NF (dB)	11.2	13.7
Ganancia (dB)	12.1	7.2
IIP3 (dBm)	-3.3	-2.1
Consumo (mW)	16	14
Área (mm^2)	0.97	0.52

Tabla A.10: Resumen de especificaciones de los receptores.

observa que el Receptor II presenta una linealidad de unos -2.1 dBm.

A.6.3 Aportaciones originales

En este capítulo se ha abordado el desarrollo de circuitos sin el uso de inductores integrados. Este tipo de topologías ayuda en gran medida a reducir el área activa de los circuitos de comunicación de ultra banda ancha, así como su consumo.

A.6.4 conclusiones

Como se ha podido comprobar es posible llevar a cabo la implementación de LNAs sin la necesidad de usar inductores integrados. Para poder llegar a trabajar sin inductores, en este caso concreto ha sido necesario incluir en la etapa de salida del LNA parte de la etapa de entrada del mezclador Gilbert. A pesar de llegar a obtener un circuito funcional sin la neceisdad de inductores el rendimiento del mismo es muy inferior al obtenido usando inductores tal y como se recoge en la Tabla A.10:

A.7 Conclusiones y líneas futuras

A.7.1 Conclusiones

La mayor parte del trabajo de esta investigación se ha centrado en los amplificadores de bajo ruido para comunicaciones de ultra banda ancha basadas en el estándar ECMA-368 / ISO/IEC 26907, así como la optimización del consumo de potencia y área de los mismos.

De cara a tener un conjunto de especificaciones de diseño de referencia en el capítulo dos se llevó a cabo un estudio del estándar ECMA-368 / ISO/IEC 26907. A partir de este estudio se diseñó un sistema de referencia que fue validado por medio de simulación. A partir de estas simulaciones se extrajeron las especificaciones de referencia para el diseño de los LNAs.

En el capítulo tres se profundizó en la estructura más clásica de amplificador de ultra banda ancha, el amplificador distribuido. Con esta topología se consigue un rendimiento relativamente constante a lo largo de toda la banda de trabajo así como un alto ancho de banda. Los principales inconvenientes de los amplificadores distribuidos son el alto consumo de potencia y área que presentan, debido al elevado número de inductores empleados en el diseño. De cara a reducir el área, se desarrollaron tres versiones diferentes de amplificadores distribuidos. La primera versión, es la estructura más clásica sin ninguna técnica de reducción de área y que sería utilizado como referencia para el resto de diseños. En la segunda versión se utilizó una técnica de compactación. En esta segunda versión el principal objetivo era evitar la influencia del acoplamiento mutuo de los inductores, prestando especial atención al correcto arrolamiento de las espirales. Finalmente en la tercera versión se utilizaron inductores multinivel, consiguiendo en este caso la mayor reducción de área (36 %) con una mínima influencia sobre el rendimiento del circuito.

A pesar de haber conseguido una considerable reducción de área, los amplificadores distribuidos ocupan un gran área. Por esta razón en el capítulo cuatro, se estudiaron diferentes alternativas de amplificadores de banda ancha. El primer circuito estudiado es la típica transformación de una estructura cascodo desde banda estrecha a banda ancha, por medio de la modificación tanto de la red de adaptación de entrada como de la carga de salida a banda ancha. Como inmediata consecuencia, con esta estructura cascodo se redujo considerablemente tanto el consumo de potencia como el área ocupada con respecto a los amplifcadores distribuidos. El principal problema de este circuito reside en la dificultad de mantener la ganancia constante a lo largo de toda la banda de interés.

Para solucionar el problema de la planitud de la ganancia, en el capítulo cuatro se introdujo también el shunt-peaking modificado. Esta técnica provoca una mejora considerable en la planitud de la ganancia pero tiene un impacto negativo en el área ocupada por el circuito porque es necesario introducir un nuevo inductor en el diseño. Finalmente, otra topología estudiada en este capítulo fue el cascodo doblado, que es capaz de trabajar con bajos niveles de tensión con una mínima influencia sobre el rendimiento del circuito. En este último circuito, para evitar aumentar el área se utilizaron inductores multinivel para llevar a cabo las polarizaciones que posibilitan el efecto de doblado del circuito.

En el capítulo cinco se introdujeron las técnicas de realimentación para mejorar

Design	Gain (dB)	BW (GHz)	NF (dB)	IIP3 (dBm)	Area (mm^2)	P_{DC} (mW)
Amplificador Distribuido 1	7	6.5	5	21.3	0.74	90
Amplificador Distribuido 2	7	6.5	4.5	21.4	0.61	90
Amplificador Distribuido 3	5.5	6.5	6	20.2	0.47	90
Amplificador banda ancha	12.5	3.6	4.3	-4	0.13	32
Shunt-peaking modificado	11.2	4	5	-4	0.29	56.1
Cascodo doblado	7.8	2.96	3	-4	0.13	18.93
Amplificador realim. inductor est.	14	5.6	< 4	-3.4	0.17	13.2
Amplificador realim. inductor 3D	14	6.8	< 4	-4.4	0.10	13.2
Frontend con inductores	12.1	5	11.2	-5.6	0.97	16
Frontend sin inductores	7.2	5	13.7	-2.1	0.52	14

Tabla A.11: Especificaciones de los circuitos diseñados.

el rendimiento de los LNAs. En este capítulo se introdujo un inductor en el bucle de realimentación activa para mejorar el ancho de banda del circuito. Se comprobó que la inductancia de este inductor era muy importante para determinar el ancho de banda del circuito pero por otro lado, el factor de calidad del mismo no era relevante. De hecho, con un bajo factor de calidad se producía una mejora en la figura de ruido del circuito. Por esta razón, se utilizó una estructura de inductor 3D, mejorando el área ocupada por el circuito y el rendimiento del mismo.

El consumo de área esta relacionado directamente con el número de inductores empleados en el circuito. Por esta razón, en el capítulo seis se estudiaron las técnicas sin inductores. En este capítulo se profundizó en el diseño de cabezales de recepción sin el uso de inductores. Para validar esta técnica se desarrollaron dos cabezales de recepción. El primero de ellos era una estructura típica incluyendo inductores basado en un LNA puerta común y un par de mezcladores Gilbert en cuadratura. La segunda versión sin inductores estaba basada también en una LNA puerta común y un par de mezcladores Gilbert en cuadratura, pero la principal diferencia de esta versión residía en la modificación de la interfáz entre el LNA y los mezcladores, donde se modificó la típica carga shunt-peaking inductiva por una carga shunt-peaking capacitiva formada por una degeneración capacitiva del transconductor de entrada de los mezcladores. Los resultados de simulación demostraron que la estructura sin inductores mostraba una mejora en la linealidad, una figura de ruido comparable a la versión tradicional y una pequeña mejora en el consumo de potencia con respecto

a la versión con inductores. La mayor diferencia entre ambos circuitos estaba en el área total ocupada, ya que con la versión sin inductores se consiguió un ahorro de área de un 54 %.

A modo de resumen en la Tabla A.11 se muestran las principales características de los circuitos desarrollados a lo largo de este trabajo de investigación.

A.7.2 Líneas de trabajo

En este trabajo de investigación se han presentado diferentes alternativas para la implementación de LNAs para sistemas de comunicación de ultra banda ancha en tecnologías de bajos coste. Por otro lado, se han introducido también las técnicas sin inductores. El principal objetivo de este trabajo era conseguir mejorar el consumo de potencia así como el área ocupada por los LNAs intentando conseguir una mínima influencia sobre las prestaciones de los circuitos. A partir de este trabajo se abren algunas vías de investigación que necesitan ser estudiadas más en profundidad como:

- **Diseño e integración del resto del receptor:** Donde se incluye el estudio, diseño e implementación de mezcladores, amplificadores de banda base y elementos de filtrado para comunicaciones de ultra banda ancha, prestando especial atención en la optimización de consumo de potencia y área.

- **Estructuras de inductores:** Explorar diferentes alternativas para conseguir una reducción de área de los inductores con un mínimo impacto sobre sus características y sobre los circuitos que las utilizan. En esta línea se incluye también el estudio de nuevas topologías que no requieran de inductores con exigentes prestaciones.

- **Estructuras sin inductores integrados:** Mejorar el rendimiento de los cabezales sin inductores. Esta es una técnica muy prometedora, ya que evitar el uso de inductores en los diseños abre la puerta a mejorar los procesos de portabilidad de diseños a otros procesos tecnológicos.

References

[1] Alereon. http://www.alereon.com/, [Online; accessed 14-May-2012].

[2] Wisair. http://www.wisair.com/, [Online; accessed 14-May-2012].

[3] Veebeam. http://www.veebeam.com/, [Online; accessed 14-May-2012].

[4] B. Razavi, *RF Microelectronics*. Prentice Hall PTR, 1998.

[5] B. R. et all, "A 0.13 μm CMOS UWB transceiver," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, (San Francisco, CA), pp. 216–217, 2005.

[6] R. Roovers, D. M. W. Leenaerts, J. Bergervoet, K. S. Harish, R. C. H. van de Beek, G. van der Weide, H. Waite, Y. Zhang, S. Aggarwal, and C. Razzell, "An interference-robust receiver for ultra-wideband radio in SiGe BiCMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 12, 2005.

[7] B. M. Ballweber, R. Gupta, and D. J. Allstot, "Fully integrated 0.5-5.5 GHz CMOS distributed amplifier," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 231–239, 2000.

[8] T. H. Lee, *The design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 1998.

[9] O. Medina, J. del Pino, A. Goñi, S. L. Khemchandani, J. García, and A. Hernández, "A method to build-up an integrated inductor library," in *XX Design of Integrated Circuits and Systems Conference*, 2005.

[10] A. Goñi, F. J. del Pino, S. L. Khemchandani, J. A. García, B. González, and A. Hernández, "Study of stacked and miniature three-dimensional inductor performance for RF IC design," in *SPIE - The International Society for Optical Engineering's - Microtechnologies for the New Millennium Design (VLSI Circuits and Systems Conference)*, 2007.

[11] A. Goñi, J. del Pino, B. González, and A. Hernández, "An analytical model of electric substrate losses for planar spiral inductors on silicon," *IEEE Transaction on Electronic Devices*, vol. 54, pp. 546–553, 2007.

[12] A. M. Niknejad, "Analysis, design and optimization of spiral inductors and transformers for si RF ICs," Master's thesis, Univ. California, Berkeley, CA, 1998.

[13] J. N. Burghartz, K. A. Jenkins, and M. Soyuer, "Multilevel-spiral inductors using VLSI interconnect technology," *IEEE Electron Devices Letter*, vol. 17, pp. 428–430, 1996.

[14] M. Geen, R. Green, R. G. Arnold, and J. A. Jenkins, "Miniature multilayer spiral inductors for GAAS MMICs," in *11th Annual GaAs IC Symp.*, pp. 381–394, 1989.

[15] J. Aguilera, J. Meléndez, R. Berenguer, J. R. Sendra, A. Hernández, and J. del Pino, "A novel geometry for circular series connected multilevel inductors for CMOS RF integrated circuits," *IEEE Transaction on Electron Devices*, vol. 46, pp. 1084–1086, 2006.

[16] A. Zolfaghari, A. Chan, and B. Razavi, "Stacked inductors and transformers in CMOS technology," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 620–628, 2001.

[17] H. Ahn and D. J. Allstot, "A 0.5-8.5 GHz fully differential CMOS distributed amplifier," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 985–993, 2000.

[18] R. Liu, C. Lin, K. Deng, and H. Wang, "Design and analysis of DC-to-14-GHz and 22-GHz CMOS cascode distributed amplifiers," *IEEE Journal of Solid-State Circuits*, vol. 39, pp. 1370–1374, 2004.

[19] R. E. Amaya, N. G. Tarr, and C. Plett, "A 27 GHz fully integrated CMOS distributed amplifier using coplanar waveguide," in *IEEE RFIC Symp.*, pp. 193–196, 2004.

[20] H.-L. Huang, M.-F. Chou, K.-A. W. Wuenand W., and C.-Y. Chang, "A low power CMOS distributed amplifier," in *IEEE Annual Conference Wireless and Microwave Technology*, pp. 47–50, 2005.

[21] X. Guan and C. Nguyen, "Low-power-consumption and high-gain CMOS distributed amplifiers using cascade of inductively coupled common-source gain cells for UWB systems," *IEEE Transaction on Microwave Theory and Techniques*, vol. 54, pp. 3278–3283, 2006.

[22] Y. Yun, M. Nishijima, M. Katsuno, H. Ishida, K. Minagawa, T. Nobusada, and T. Tanaka, "A fully integrated broad-band amplifier MMIC employing a novel chip-size package," in *IEEE Trans. Microw. Theory Tech.*, pp. 2930–2937, 2002.

[23] J. del Pino, S. L. Khemchandani, A. Hernández, J. Sendra, J. García, B. González, and A. Núñez, "The impact of integrated inductors on low noise amplifiers," in *XVIII Design of Integrated Circuits and Systems Conference*, (Ciudad Real), Nov. 2003.

[24] R. Wang, M. Lin, C. C. Lin, and C. Yang, "A 1V full-band cascoded UWB LNA with resistive feedback," in *Proc. IEEE 2007 Int. Workshop on Radio-Frequency Integration Tech.*, (Singapore), Dec. 2007.

[25] K. Chang-Wan, K. Min-Suk, A. Tuan, K. Hoon-Tae, and L. Sang-Gug, "An ultra-wideband CMOS low noise amplifier for 3-5 GHz UWB system," *IEEE J. Solid-State Circuits*, vol. 40, pp. 544–547, 2005.

[26] A. Medi and N. Won, "A fully integrated low cost packaged CMOS low noise amplifier for the UWB radio," in *Proc. IEEE 2006 Radio and Wireless Symp.*, (San Diego, CA), Jan. 2006.

[27] C. S. Chih, W. Ruey-Lue, K. Ming-Lung, and K. Hsiang-Chen, "An integrated CMOS low noise amplifier for 3-5 GHz UWB applications," in *Proc. IEEE 2005 Conf. on Electron Devices and Solid-State Circuits*, (San Diego, CA), pp. 225–228, Dec. 2005.

[28] Y. Huang and T. E. Chen, "A fully-integrated UWB CMOS LNA using network synthesis approach," in *Proc.IEEE 2006 Microwave Symposium*, (San Francisco, CA), Jun. 2006.

[29] F. Gong, K. F. Lam, M. Ismail, S.-B. Park, and J. DeGroat, "A 3-5 GHz frequency tunable ultra wideband LNA for OFDM applications," in *Proc. 52nd IEEE International Midwest Symposium on Circuits and Systems*, (Cancun), Aug. 2009.

[30] J. Sendra, J. del Pino, A. Hernández, J. Hernández, J. Aguilera, A. García-Alonso, and A. Núñez, "Integrated inductors modeling and tools for automatic selection and layout generation," in *IEEE International Symposium on Quality in Electronic Design*, (San Jose), 2002.

[31] T. Manku, G. Beck, and E. Shin, "A low-voltage design technique for RF integrated circuits," *IEEE Trans Circuits Syst II Analog Digit Signal Process*, vol. 39, pp. 1408–1413, 1998.

[32] H. Hashemi and A. Hajimiri, "Concurrent multi-band low-noise amplifiers-theory, design, and applications," *IEEE Trans Microwave Theory Tech*, vol. 16, pp. 290–294, 1968.

[33] C.-C. Tang, C.-H. Wu, and S.-I. Liu, "Miniature 3-D inductors in standard CMOS process," *IEEE J Solid State Circuits*, vol. 37, 2002.

[34] B. R. et al., "A 0.13 μm CMOS UWB transceiver," in *IEEE International Solid State Circuits Conference Digest of Technical Papers*, (San Francisco, CA), pp. 216–217, 2005.

[35] A. Ismail and A. Abidi, "A 3 to 10 GHz LNA using a wideband LC-ladder matching network," in *ISSCC Digest of TechnicalPapers*, (San Francisco, CA), pp. 382–383, 2004.

[36] A. Bevilacqua and A. Niknejad, "An ultra-wideband CMOS LNA for 3.1 to 10.6 GHz wireless receivers," in *ISSCC Digest of Technical Papers*, (San Francisco, CA), pp. 384–385, 2004.

[37] S. Shekhar, J. Walling, and D. Allstot, "Bandwidth extension techniques for CMOS amplifiers," *IEEE J Solid State Circuits*, vol. 41, pp. 2424–2439, 2004.

[38] J. Lee and J. Cressler, "A 3–10 GHz SiGe resistive feedback low noise amplifier for UWB applications," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, (Long Beach, CA), pp. 545–548, 2005.

[39] N. Shiramizu, T. Masuda, M. Tanabe, and K. Washio, "A 3–10 GHz bandwidth low-noise and low-power amplifier for full-band UWB communications in 0.25 SiGe BiCMOS technology," in *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, (Long Beach, CA), pp. 39–42, 2005.

[40] M. Reiha and J. Long, "A 1.2-V reactive-feedback 3.1–10.6 GHz low-noise amplifier in 0.13 μm CMOS," *IEEE J Solid State Circuits*, vol. 42, pp. 1023–1033, 2007.

[41] H. Knapp, D. Zoschg, T. Meister, K. Aufinger, S. Boguth, and L.Treitinger, "15 GHz wideband amplifier with 2.8 dB noise figure in SiGe bipolar technology," in *Radio Frequency Integrated Circuits (RFIC) Symposium, 2001. Digest of Papers*, (Phoenix. AZ), pp. 287–290, 2001.

[42] Y. Park, C.-H. Lee, J. Cressler, and J. Laskar, "The analysis of UWB SiGe HBT LNA for its noise, linearity, and minimum group delay variation," *IEEE Trans Microwave Theory Tech*, vol. 54, pp. 1687–1697, 2006.

[43] C.-T. Fu and C.-N. Kuo, "3–11-GHz CMOS UWB LNA using dual feedback for broadband matching," in *Radio Frequency Integrated Circuits Digest*, (San Francisco, CA), pp. 67–70, 2006.

[44] J. Kaukovuori, *CMOS Radio Frequency Circuits For Short-Range Direct-Conversion Receivers*. PhD thesis, Helsinki University of Technology, Faculty of Electronics, Communications and Automation, Department of Micro and Nanosciences, 2008.

[45] B. Razavi, *Design of Analog CMOS Integrated Circuits*. Mc Graw Hill, 2001.

[46] L. C-F and L. S-I, "A broadband noise-canceling CMOS LNA for 3.1–10.6-GHz UWB receivers," *IEEE Journal of Solid-State Circuits*, vol. 42, pp. 329–339, 2007.

[47] J. del Pino, *Modelado y aplicaciones de inductores integrados en tecnologías de silicio*. PhD thesis, Departamento de Ingeniería Electrónica y Automática, Universidad de Las Palmas de Gran Canaria, 2002.

[48] R. Harjani and L. Cai, "1-10GHz inductorless receiver in 0,13μm CMOS," in *IEEE Radio Frequency Integrated Circuits Symposium, University of Minnesota, Minneapolis*, 2009.

[49] B. Razavi, *Design of Integrated Circuits for Optical Communications*. McGraw Hill, 2002.

[50] Q. Li and Y. P. Zhang, "An inductorless LNA with noise cancellation an inductorless LNA with noise cancellation for UWB receiver front-end," in *IEEE ASSCC*, 2006.

B

Publications

A list of journals and conference contributions directly related this research work are listed in this appendix.

Journal Papers

1. J. del Pino, Sunil L. Khemchandani, Roberto Díaz-Ortega, Rubén Pulido-Medina and Hugo García-Vázquez, "On-Chip Inductors Optimization For Ultra Wide Band Low Noise Amplifiers", Journal of Circuits, Systems, and Computers, Nov. 2011

2. J. del Pino, R. Díaz and S.L. Khemchandani, "Area Reduction Techniques for Full Integrated Distributed Amplifiers", International Journal in Electronics and Communications, Nov. 2010

Conference Papers

3. H. García-Vázquez, R. Díaz, D. Ramos-Valido, A. Santana, J. del Pino and S.L. Khemchandani, "Area Reduction in RF Fully Integrated Front-Ends for Ultra-Wideband", XXV Conference on Design of Circuits and Integrated Systems, Nov 2010.

4. H. García, R. Pulido, R. Díaz, S.L. Khemchandani, A. Goñi and J. del Pino, "A Feedback Wideband LNA with a Modified 3D Inductor for UWB Applications", XXIII Conference on Design of Circuits and Integrated Systems, Nov 2008.

5. G. Martín, R. Díaz, J. del Pino, S.L. Khemchandani, A. Hernández, "Design of a Fully Integrated DC to 8.5 GHz Distributed Amplifier in CMOS 0.35", XXI Conference on Design of Circuits and Integrated Systems, Nov 2006.

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Journal of Circuits, Systems, and Computers

ON-CHIP INDUCTORS OPTIMIZATION FOR ULTRA WIDE BAND LOW NOISE AMPLIFIERS

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In this work, the influence of the inductor quality factor in wide band low noise amplifiers has been studied. Electromagnetic simulations have been used to model the integrated inductor broad band response. The influence of the quality factor on LNA performance of the inductors that compound the impedance matching networks, inductive degeneration and broadband load has been studied, obtaining design guidelines for optimizing the amplifier gain flatness. Using this guidelines, an LNA with wideband input matching, shunt-peaking load, and an output buffer was designed. Using Austria Mikro Systems BiCMOS 0.35 µm process, a prototype has been fabricated achieving the following measured specifications: maximum gain of 12.5 dB at 3.4 GHz with a -3 dB bandwidth of 1.7-5.3 GHz, noise figure from 4.3 to 5.2 dB, and unity gain at 9.4 GHz.

Keywords: LNA; BiCMOS; UWB; wide band matching; shunt-peaking; RF.

1. Introduction

The design of wide band low noise amplifiers (LNA) for wireless communication is not easy. It presents two levels of challenges. First, having fast and low noise transistors depends on the available technology. Traditionally, microwave amplifiers relied on transistors fabricated with composite semiconductors, e.g., GaAs, because of the intrinsic superior frequency characteristics of such devices[1,3]. On the other hand, silicon technology has been employed to design amplifiers[4,5], even wide band ones, in the range of several GHz.

In wireless mobile communications systems, silicon integrated circuits have been widely employed in narrow-band systems, where limited gain and increased parasitics are tolerable due to lower operating frequencies, and the application of tuned networks. Most of them are distributed amplifiers[6,8] which require high levels of power consumption, high area, and they are not optimized for noise.

A new methodology to extend the reactively matched LNAs to wide bandwidths is presented in [9]. This approach satisfies the tough system requirement of a UWB system

with moderate power consumption. The proposed methodology is based on the concept of wide band impedance matching which makes extensive use of spiral inductors. However, the problem is that the overall amplifier gain should be flat across the pass-band, whiles the frequency response of integrated inductors is not.

The purpose of this paper is to study the influence of inductor parasitics on LNA wide band response. As an example, an amplifier with on-chip matching network spanning from 1.7 to 5.3 GHz is designed. To provide some background, section II briefly describes the design tradeoffs on the narrow band inductively degenerated amplifier. The concept of wide band impedance matching is explained in section III and it is used to extend the bandwidth of the narrow band LNA. The design methodology as well as some practical considerations regarding to the influence of the integrated inductors are discussed in section IV. Experimental results from a chip prototype are provided in Section V. Finally, some conclusions are given in Section VI.

2. Narrow band Inductively Degenerated Amplifier

First, the typical narrow band inductively degenerated amplifier configuration is studied. Fig. 1 shows the typical schematic of a narrow band LNA. The input transistor (Q_{CAS1}) is in common emitter configuration and it is the mainly contributor to the circuit noise. The noise figure (NF) of the LNA depends directly on the emitter area and on the bias of Q_{CAS1}. The cascode stage, composed by Q_{CAS1} and Q_{CAS2}, reduces Miller capacitance, decreasing the effective base-collector capacitance (C_μ) of Q_{CAS1}. This makes the amplifier unilateral, i.e., with low S_{12}. This is a requisite of many communication systems to prevent leakage of local oscillator power from the mixer back to the antenna[2]. The cascode also enhances the overall gain by increasing the stage's output impedance. The resonant circuit composed by L and C is the load of the cascode stage. This allows a high gain with a low voltage supply. The tank resonant frequency is adjusted to the frequency of interest (ω_0).

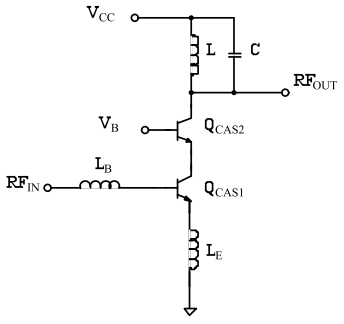


Fig. 1. Simplified schematic of the LNA with inductive degeneration.

The noise in a transistor is proportional to the transistor base and emitter resistances, r_b and r_e, and to the transistor small-signal transconductance $g_m=1/r'_e= I_C/V_T$ (V_T is the thermal voltage and I_C is the collector current). To minimize r_b, the transistor must present a great area and to maximize g_m, I_C must be high. If the transistor area is increased the input capacitance ($C_i= C_\pi+C_\mu$) will also increase. This will attenuate the input signal and it will raise the NF. As a result the NF will reach a minimum for a particular combination of area and polarization current.

The next step in minimizing the noise is matching the LNA input. The antenna output impedance is 50 Ω and through inductive degeneration it is possible to match the input having an excellent trade-off between conjugate matching and minimum noise. The inductive degeneration consists on introducing a series inductance (L_E) at the emitter as it is shown in Fig. 1. The inductance value is approximately given by (1):

$$L_E = \frac{Z_0}{\omega_T} \tag{1}$$

The higher transistor $\omega_T=g_m/C_i$, the lower the value of L_E needed for matching, and the lower the amount of noise added to the LNA by the series resistance of the inductor. L_E changes the real part of the input impedance, and to modify the imaginary part another inductor L_B is introduced as presented in Fig.1. An expression of the noise factor for the LNA with inductive degeneration that takes into account the above discussion is the following:

$$F = 1 + \frac{r_b + r_e}{Z_0} + \frac{g_m}{2} Z_0 \left(\frac{\omega_0}{\omega_T} \right)^2 \tag{2}$$

Alternatively this expression can be expressed as:

$$F = 1 + \frac{r_b + r_e}{Z_0} + \frac{1}{2 \cdot g_m \cdot Z_0 \cdot Q^2} \tag{3}$$

where Q is the quality factor of the input matching network. The noise factor improves with a higher Q because more voltage gain is seen across the input capacitance of the transistor. The input impedance is resistive only in a narrow bandwidth (ω_0/Q) around the resonance frequency ω_0. To obtain a wide band impedance matching, the Q of the matching circuit should be significantly lowered. This will largely degrade the noise figure which defeats the purpose. As a result, this type of amplifier cannot be used for wide band applications.

3. Wide band Amplifier

Wide band impedance matching expands the use of an inductively degenerated amplifier, by embedding the input network of the amplifying device in a multisection reactive network so that the overall input reactance is resonated over a broad bandwidth. In this way, a wide band input match is achieved and, at the same time, good noise performance is attained. In the proposed design, shown in Fig.2, a fourth-order doubly terminated band-pass filter is used to resonate the reactive part of the input impedance over the whole band. As long as the upper and lower cutoff frequencies (ω_U and ω_L) of the filter are far from each other, this second-order band-pass filter can be seen as a combination of two filter sections, one in a low-pass configuration and the other one in a high-pass configuration. The high-pass filter section is composed by L_B and C. and its cutoff frequency is given by:

$$\text{high}-\text{pass}\begin{cases} L_B = \dfrac{R}{\omega_L} \\ C_\pi = \dfrac{1}{\omega_L \cdot R} \end{cases} \tag{4}$$

On the other hand, the low-pass filter section is composed by L_E and C_B and its cutoff frequency is given by:

$$\text{low}-\text{pass}\begin{cases} L_E = \dfrac{R}{\omega_U} \\ C_B = \dfrac{1}{\omega_U \cdot R} \end{cases} \tag{5}$$

These two circuits provide input impedance equal to R in the pass-band between ω_U and ω_L.

In order to provide a wide band operation, one would think on replacing the resonant load in the narrow band circuit by a resistor. However, this would lead to gain response falling with the frequency due to the pole generated by the resistor load (R_L) and the capacitance of the output node (C_{OUT}). A technique commonly used to increase the bandwidth is to replace the load resistor by a shunt-peaking resistor[10] composed by L_L and R_L. The addition of an inductance in series with the load resistor provides an impedance component that increases with frequency (i.e. introduces a zero), which helps offset to decrease the impedance of the load capacitance, leaving a net impedance that remains roughly constant over a broader frequency range than that of the original RC network. R_L should be sufficiently low so that the inductive region of the impedance spans the pass-band.

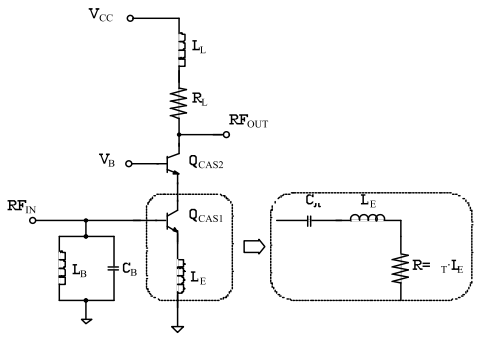


Fig. 2. Simplified schematic of the LNA with wide band impedance matching.

With this configuration the inductive load equalizes the voltage gain to a constant value across the pass-band. The problem is that C_{OUT} introduces a spurious resonance with L_L (peaking), which must be kept out-of-band. As long as C_{OUT} represents all the loading on the output node, including the transistor output capacitance, the loading by interconnect and subsequent stages and parasitic capacitances of the inductor, all these contributions should be minimized to ensure self resonance beyond ω_U.

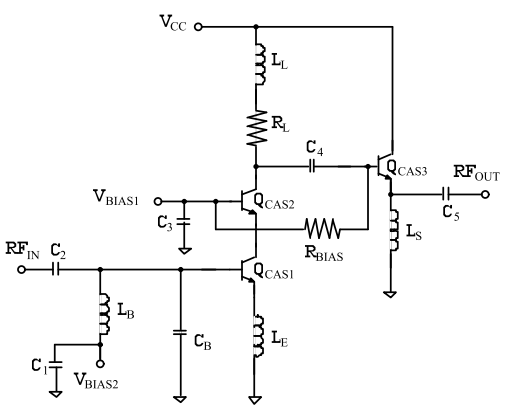
4. Design

Fig. 3 shows the designed wide band LNA circuit. An emitter follower buffer is included to drive an external 50 Ω load for measurement purposes. C capacitors are for AC decoupling and R_{BIAS} has a large value in order to bias the output buffer with V_{BIAS1} voltage.

The performance of a narrow band LNA is determined by the limited quality factor of the integrated inductors[11]. Its optimization relies on achieving the highest Q for a given inductance value at the frequency of operation. In the case of a wide band operation, this assumption is not convenient and a further study is needed. In shunt peaking applications, the biggest issue is the reduction of bandwidth improvement because of additional parasitic capacitance introduced by on-chip inductors. As a consequence, prior to their use in any circuit, spiral planar inductors must be modeled accurately over a wide range of frequencies. In this work, the analytical model proposed in [12] have been used to implement an optimization algorithm that provides the geometry of the inductor with the best quality factor for a given inductance value and frequency of operation. For every inductor of the circuit, a set of spirals with the same inductance but optimized for different frequencies were simulated. In order to better predict the inductor performance, S parameters from full-wave electromagnetic simulations were used to simulate the circuit. A commercially available planar EM simulator (Momentum©) was used to predict the broadband response of inductors in lossy silicon substrates. The inductors

were designed using the top level metal, which is thicker and more conductive than the rest. All of them are laid out in an octagonal fashion, with external radii (r) up to 170 μm, metal width (w) between 5 and 25 μm and up to 5.5 turns (n). The spacing between tracks is fixed to the minimum allowed by the technology, 2 μm, in order to maximize the inductance value.

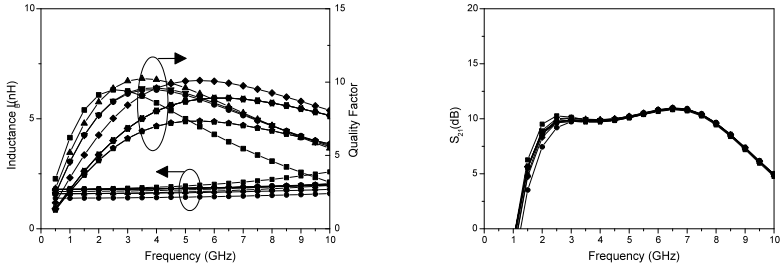
The simulated quality factor and inductance of the simulated spirals are reported in Figs. 4, 5, 6, and 7. In the same Figs., the wide band LNA simulated power gain using the above spirals is also plotted.



Q_{CAS1}	A=20/M=5*
Q_{CAS2}	A=20/M=5*
Q_{CAS3}	A=20/M=1*
L_E	0.27-0.35 nH
L_S	. nH
L_B	1. nH
L_L	1.4 1.6 nH
R_L	30
R_{BIAS}	5 K
C_1	10 pF
C_2	3 pF
C_3	3 pF
C_4	3 pF
C_5	5 pF
C_B	100 fF
C_L	4.2 pF
V_{CC}	3.3 V
V_{BIAS1}	0.8 V

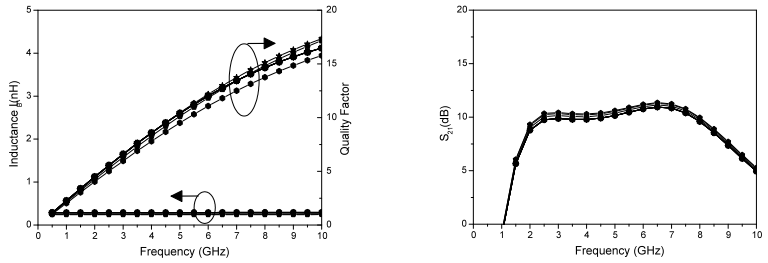
Fig. 3. Schematic of the wide band LNA.

It is shown that circuit performance is insensitive to inductors L_B and L_E quality factors. With maximum quality factor frequencies (f_{Qmax}) for L_B ranging from 2 to 5 GHz, the gain remains unaltered. Only little variations are observed at low frequency and must be attributed to the slight differences in inductance value. In the case of L_E, the inductance value is low and the geometrical characteristics of the simulated spirals are similar. As a result, the gain flatness is not affected.



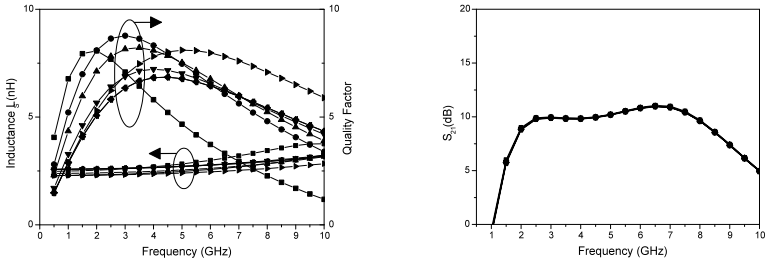
(a) (b)

Fig. 4. (a) Quality factor and inductance of spirals suitable for L_B. (b) Power gain for differents L_B.



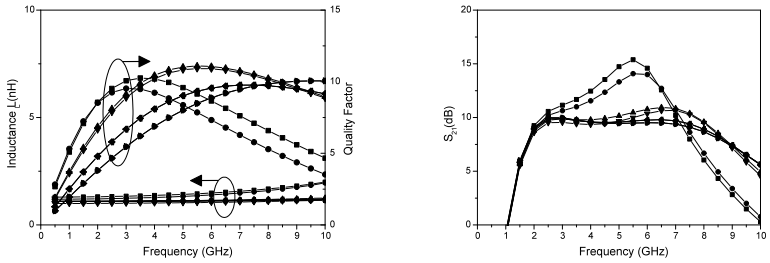
(a) (b)

Fig. 5. (a) Quality factor and inductance of spirals suitable for L_E. (b) Power gain for differents L_E.



(a) (b)

Fig. 6. (a) Quality factor and inductance of spirals suitable for L_S. (b) Power gain for differents L_S.



(a) (b)

Fig. 7. (a) Quality factor and inductance of spirals suitable for L_L. (b) Power gain for differents L_L.

On the other hand, L_S is used for biasing purposes and does not affect in the frequency response of the circuit. However, this result no longer holds for the case of L_L. As it can be seen in Fig. 7, the gain flatness is strongly affected by the inductor Q. The best results are obtained for inductors that exhibit an equalized quality factor through the entire band, despite of those having Qs with an irregular shape through the band of interest.

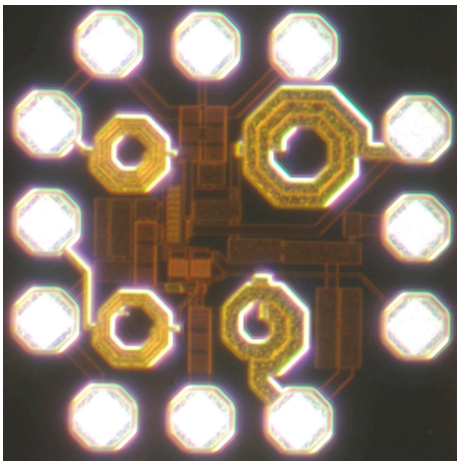


Fig. 8. Wide band amplifier layout.

5. Experimental Results

Fig. 8 shows the final wide band LNA photography. The total chip size, including probe pads, is 665×665 μm^2. The amplifier draws 5.3 mA and the output buffer draws 6.5 mA from a 3.3 V supply.

The layout has been implemented using a 0.35 μm BiCMOS process. The amplifier was measured on wafer using a Cascade SUMMIT 9000 probe station, 35 GHz probes and 20 GHz Agilent 8720ES vector network analyzer. The probe pads were octagonal, optimized for RF. Three ground-signal-ground (GSG) and one signal-ground-signal (SGS) pad structures with 150 μm pitch were used, as depicted in Fig. 8.

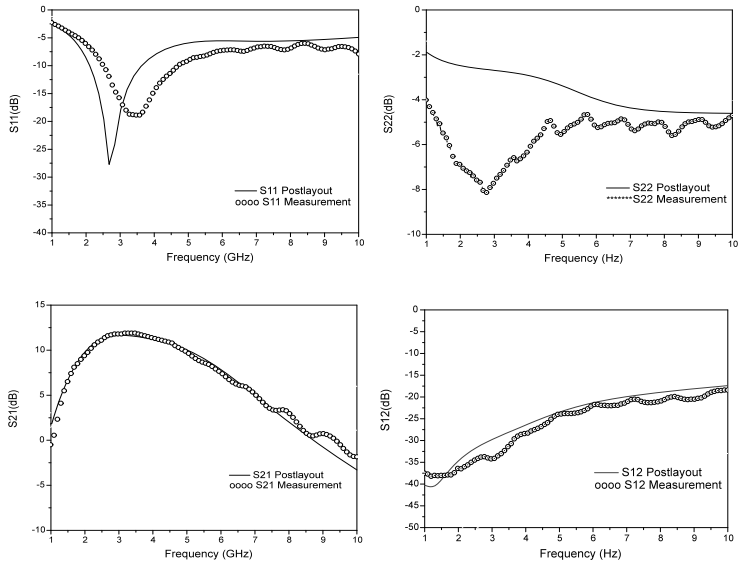


Fig. 9. Measured and simulated scattering parameters for the designed wide band LNA.

Fig. 9 shows measured and post layout simulated S parameters of the wide band amplifier which agree quite well except the S22, which is better in measurements. This is due to parasitic resonance of the output buffer which has not been taken into account in simulations. As expected, a maximum power gain of 12.5 dB was achieved at 3.4 GHz with a -3 dB bandwidth of 1.7-5.3 GHz. A unity gain was measured at 9.4 GHz. The measured input return loss (S_{11}) is higher than 5 dB over the bandwidth. The output return loss (S_{22}) has a maximum value of 13 dB due to the source follower output stage.

The reverse isolation (S_{12}) is greater than 23 dB due to cascode stage. The NF measurement was done in a noise free environment with an E4440 Agilent 26.5 GHz spectrum analyzer and a 346C noise source. Fig. 10 shows the amplifier measured and simulated NF. The NF varies from 4.3 dB at 3.9 GHz, to 5.2 dB at 5.3 GHz. This result shows good agreement between measured and simulated data. The $P_{1\text{-}dB}$ compression point was measured as –4.5 dBm.

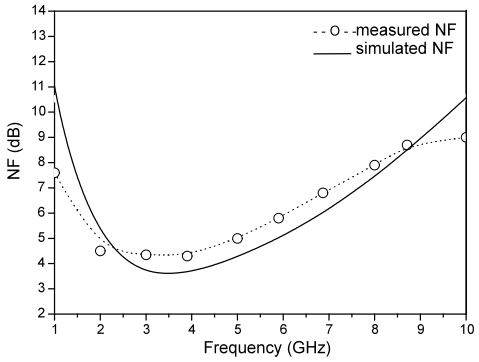


Fig. 10. Measured and simulated NF of the wide band LNA.

Measured results and a brief comparison with similar amplifiers are summarized in Table I. It is shown that the designed LNA, using an cheap technology, has a good trade-off between bandwidth, noise figure, gain, linearity and power consumption. Keep in mind that although the power consumption is the highest, the circuit has been fabricated in an older technology compared to the other publications.

TABLE I: Comparison with recently published wide band amplifiers

Author	BW 3-dB (GHz)	Max. Gain (dB)	Max. NF (dB)	IIP3 (dBm)	P_{DC} (mW)	Technology	Year
13	3.1-10.6	9.18	7.2	7.25	23.5	CMOS 0.18 µm	2007
14	2.0-4.6	9.8	5.2	-7	12.6	CMOS 0.18 µm	2005
15	3.1-4.8	15	4.9	-2.2	20	CMOS 0.25 µm	2006
16	3.0-5.0	12.7	5.02	-9.7	16.4	CMOS 0.18 µm	2005
17	3.1-7.5	19.1	3.8	-2.2	32	CMOS 0.18 µm	2006
18	3.0-5.0	12	4.5	-	20	CMOS 0.18 µm	2009
This work	1.7-5.3	12.5	5.0	5.1	32	BiCMOS 0.35 µm	2009

6. Conclusions

In this paper, the fundamental design aspects of cascode wide band LNAs with shunt peaking load with on chip inductors have been reported. A description of the LNA configuration was explained, emphasizing the influence of the design parameters in the circuit performance. A detailed study was done in order to analyze the influence of the inductors on the amplifier gain flatness. This parameter is strongly affected by the shunt peaking inductor quality factor and the best results are obtained for inductors with equalized performance over the whole band. As an example, a wide band amplifier with a frequency band spanning from 1.7 to 5.3 GHz is presented. The circuit was implemented in a standard BiCMOS 0.35 μm process and provides a maximum gain of 12.5 dB with a minimum NF of 4.3 dB at 3.9 GHz.

7. References

1. Y. Mimino, M. Hirata, K. Nakamura, K. Sakamoto, Y. Aoki, and S. Kuroda, "High Gain-Density K-Band P-HEMT LNA MMIC for LMDS and Satellite Communication," IEEE Radio Frequency Integrated Circuits Symposium, pp. 209–212, Jun. 2000.
2. Y. Yun, M. Nishijima, M. Katsuno, H. Ishida, K. Minagawa, T. Nobusada, and T. Tanaka, "A Fully Integrated Broad-Band Amplifier MMIC Employing a Novel Chip-Size Package," IEEE Transactions on Microwave Theory Techniques, vol. 50, pp. 2930–2937, Dec. 2002.
3. P. Marsh, S. Chu, S. Lardizabal, R. Leoni III, S. Kang, R. Wohlert, A. Bowlby,W. Hoke, R. McTaggart, C. Whelan, P. Lemonias, P. McIntosh, and T. Kazior, "Low Noise Metamorphic HEMT Devices and Amplifiers on GaAs Substrates," IEEE Microwave Theory and Techniques Symposium, pp. 105–108, Jun. 1999.
4. Y. Greshishchev, P. Schvan, J. L. Showell, M.-L. Xu, J. J. Ojha, and J. E. Rogers, "A Fully Integrated SiGe Receiver IC for 10-Gb/s Data Rate," IEEE Journal of Solid-State Circuits, vol. 35, pp. 1949–1957, Dec. 2000.
5. J. Cao, M. Green, A. Momtaz, K. Vakilian, D. Chung, K.-C. Jen, M. Caresosa, X. Wang, W.-G. Tan, Y. Cai, I. Fujimori and A. Hairapetian, "OC-192 Transmitter and Receiver in Standard 0.18 um CMOS," IEEE Journal of Solid-State Circuits, vol. 37, pp. 1768–1780, Dec. 2002.
6. H. T. Ahn and D. J. Allstot, "A 0.5–8.5-GHz Fully Differential CMOS Distributed Amplifier," IEEE Journal of Solid-State Circuits, vol. 37, pp. 985–993, Aug. 2002.
7. R.-C. Liu, K.-L. Deng and H.Wang, "A 0.6–22-GHz Broadband CMOS Distributed Amplifier," IEEE Radio Frequency Integrated Circuits Symposium, pp. 103–106, Jun. 2003.
8. B. M. Ballweber, R. Gupta and D. J. Allstot, "A Fully Integrated 0.5–5.5-GHz CMOS Distributed Amplifier," IEEE Journal of Solid-State Circuits, vol. 35, pp. 231–239, Feb. 2000.
9. A. Ismail, A. Abidi, "A 3–10-GHz Low-Noise Amplifier with Wideband LC-Ladder Matching Network" IEEE Journal of Solid-State Circuits, vol. 39, no. 12, Dec. 2004.
10. T. H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, 1st ed. New York: Cambridge Univ. Press, 1998.
11. J. del Pino, S. L. Khemchandani, A. Hernández, J.R. Sendra, J. García, B. González and A. Nunez "The Impact of Integrated Inductors on Low Noise Amplifiers " XVIII Design of Integrated Circuits and Systems Conference, Ciudad Real, Nov. 2003.
12. A. Goñi, J. del Pino, B. González and A. Hernández, An analytical model of electric substrate losses for planar spiral inductors on silicon, IEEE Trans. Electron Devices 54 (2007), 546-553.
13. R. Wang, M. Lin, C. Cheng Lin, C. Yang, "A 1V Full-band Cascoded UWB LNA with Resistive Feedback," IEEE International Workshop on Radio-Frequency Integration Technology, pp. 188-190, Dec. 2007, Singapore.

14. K. Chang-Wan, K. Min-Suk, A. Tuan, K. Hoon-Tae and L. Sang-Gug, “An Ultra-Wideband CMOS Low Noise Amplifier for 3-5 GHz UWB System,” IEEE Journal of Solid-State Circuits, vol. 40, iss. 2, pp. 544-547, Feb. 2005.
15. A. Medi and Namgoong Won, A Fully Integrated Low Cost Packaged CMOS Low Noise Amplifier for the UWB Radio,” IEEE 2006 Radio and Wireless Symposium, pp. 115-118, Jan. 2006.
16. C. S. Chih, W. Ruey-Lue, K. Ming-Lung and K. Hsiang-Chen, “An Integrated CMOS Low Noise Amplifier for 3-5 GHz UWB Applications,” 2005 IEEE Conference on Electron Devices and Solid-State Circuits, pp. 225-228, Dec. 2005.
17. Y. Huang, T. Emery Chen, “A Fully-Integrated UWB CMOS LNA Using Network Synthesis Approach,” 2006 IEEE Microwave Symposium Digest, pp. 320-323, Jun. 2006.
18. F. Gong, K. F. Lam, M. Ismail, Seok-Bae Park J. DeGroat, "A 3-5 GHz Frequency Tunable Ultra Wideband LNA for OFDM Applications," IEEE International Midwest Symposium on Circuits and Systems. 2009, pp. 1018-1021, Aug. 2009.

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Area reduction techniques for full integrated distributed amplifier

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ABSTRACT

This paper presents two techniques to reduce the area in the design of CMOS distributed amplifiers. The proposed techniques take into account the influence of compacting the layout and the use of stacked inductor for the artificial transmission lines on the distributed amplifier performance. Following these design guidelines, three prototypes have been fabricated in a low cost CMOS 0.35 μm process. The measured gain is about 6 dB with a cutoff frequency around 8 GHz. The noise figure varies from 5 to 7 dB and the circuits draw 30 mA from a 3.3 V voltage supply. With the developed area optimization design techniques, a maximum area reduction of 37% with respect to a conventional design has been achieved, without any significant performance degradation.

1. Introduction

In the last years the so-called wireless personal area network (WPAN) systems are becoming popular replacing cables and enabling new consumer applications. Such systems are nowadays dominated by standards like Bluetooth and Zigbee, which operate in the 2.4 GHz ISM band, and offer a limited data rate, typically around 1 or 2 Mb/s, which is insufficient for many applications like fast transfer of large files and high-quality video streaming. In order to increase the data rate to several hundreds of Mb/s with a low power transmission, it has been proposed ultra-wideband (UWB).

An UWB receiver is composed of an analog front-end, which translates the signal from radiofrequency to baseband, and a digital stage, that processes the signal at low frequency. One of the most important blocks in the front-end is the low noise amplifier because the receiver noise figure depends directly on this block. There are many research works related to ultra-wideband low noise amplifier design with new structures and design techniques [1]. Among them, one of the most used structures is the distributed amplifier (DA) [2].

In previous works related to CMOS based DA, authors focused their research on gain and bandwidth optimization. For example, in [2] the authors developed a method based on the concept of simulated annealing to optimize the gain flatness and phase linearity of a DA. The same procedure was used in a fully differential DA in [3]. Other authors tried to improve the gain-bandwidth product using other topologies like cascode [4] and cascade stages [5–7], or using coplanar waveguides [8] or bonding wires as inductive elements [9]. Those works show how the operating frequencies and gains of DAs have increased. However, they do not consider one of the main lacks of this kind of circuits, its large chip area due to the extensive use of integrated inductors.

In this paper design guidelines to optimize DA area based on modifying the circuit layout and using different kind of inductors is proposed. The organization of this paper is the following. In Section 2 the DA theory is presented. Section 3 is devoted to area reduction techniques and in Section 4 experimental results and a comparative with other works are shown. Finally some conclusions are given.

2. Distributed amplifier design

The frequency response of a MOS device degrades due to the pole formed by the input/output capacitance of the transistor and the resistance it sees. The MOSFET's transconductance rapidly falls with frequency and any attempt to increase the transconductance by increasing the size of the device will also increase its input/output capacitance. Thus, while low-frequency gain has been increased, the gain-bandwidth product remains about the same. The distributed amplification was proposed to overcome this limitation.

Distributed amplifier employ a topology in which the gain stages are connected such that their capacitances are separated, yet the output currents still combine in an additive fashion (Fig. 1). Series inductive elements are used to separate capacitances at the inputs and outputs of adjacent gain stages. The resulting topology, given by the interlaying series inductors and shunt capacitances, forms a lumped-parameter artificial

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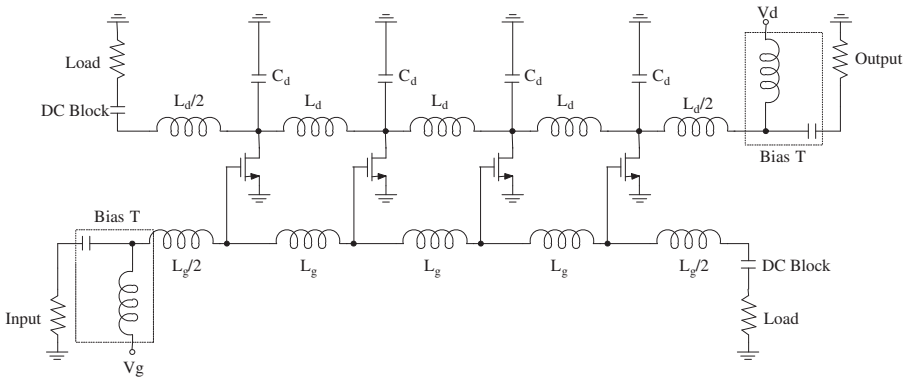

Fig. 1. Distributed amplifier.

transmission line. The additive nature of the gain dictates a relatively low gain; however, the distributed nature of the capacitance allows the amplifier to achieve very wide bandwidths. Distributed amplification overcomes the gain bandwidth limitation absorbing the MOS input/output capacitance as part of the lumped elements of the artificial transmission line, formed with the series inductance that connects adjacent drains and gates. The characteristic impedance (Z_0) and cut-off frequency (f_c) of lossless transmission line are given at a first approximation by

$$Z_0 = \sqrt{\frac{L_{TL}}{C_{TL}}} \tag{1}$$

$$f_c = \frac{1}{\pi\sqrt{L_{TL}C_{TL}}} \tag{2}$$

where subindex TL accounts for the drain and gate transmission lines. Since Z_0 and f_c of both the drain and gate lines are the same, their capacitances and inductances should be the same. As the drain-to-bulk capacitance C_{db} of a MOSFET is usually less than its gate-to-source capacitance C_{gs}, a capacitor C_d is added to the drain to make the capacitances equal:

$$L_g = L_d \tag{3}$$

$$C_{gs} = C_{db} + C_d \tag{4}$$

As the amplified signals at each stage travels towards the load, the signal gets attenuated due to non-zero losses associated with the transmission lines. Finite Q inductors are the primary source of losses in the gate line. Losses in the drain line can be attributed to lossy inductors L_d and the drain-to-source resistance (r_{ds}). The gain of the DA can be expressed as [2]

$$A = -g_m \frac{Z_0}{2\sqrt{1-\left(\frac{f}{f_c}\right)^2}} \cdot \frac{e^{-N(A_g+A_d)/2}\cdot\sinh\left(N\frac{A_d-A_g}{2}\right)}{\sinh\left(N\frac{A_d-A_g}{2}\right)} \tag{5}$$

where A_d and A_g are the attenuation of the drain and gate lines, g_m is the MOSFET transconductance and N is the total number of stages. This equation assumes the following:

- Unilateral MOSFET model (ignores C_{gd}).
- Image impedance matched terminations.
- Equal gate and drain phase velocities.

The optimum number of stages that maximizes the gain is a function of gate and drain line attenuation. Those attenuations are complex functions and depend on the specific MOSFET parameters and also on the operating and cut-off frequencies. As the signal propagates along the gate line towards the termination, less signal is available for each MOSFET because of attenuation and, as a consequence, the overall gain degrades with further increase in the number of stages. The number of stages for this work is chosen as 4.

Knowing the gain, number of stages, and drain-line inductance and capacitance, the required g_m can be found from the low frequency gain of (5):

$$g_m = \frac{2A}{N}\sqrt{\frac{C_d}{L_d}} \;\Rightarrow\; g_m = \frac{2A}{N\cdot Z_0} \tag{6}$$

Then, the transistor width-length ratio can be derived from

$$\frac{W}{L} = \frac{g_m}{\mu_n C_{ox}(V_{gs}-V_T)} \tag{7}$$

where

- W, transistor gate width.
- L, transistor gate length.
- n, electron mobility.
- C_{ox}, gate oxide capacitance per unit area.
- V_T, threshold voltage.
- V_{gs}, gate–source voltage.

Finally, the device length and width can be found by combining Eq. (7) with the following expression:

$$W\cdot L = \frac{C_g}{Cox} \tag{8}$$

Taking into consideration the previous equations and a four stage structure, a DA with a gain 10 dB and a cut-off frequency of 11 GHz has been designed. Table 1 shows the calculated component values.

From the previous analysis an important conclusion is extracted: this kind of circuits is composed of a considerable number of inductors. As it will be pointed out in the next section, inductors fill the most of layout area and, as a consequence, it is very important to study the effect of inductors and their distribution over the circuit area.

3. Area optimization

3.1. Compact design

The most evident method for reducing the area of a circuit is to compact its layout which, in the case of a DA, suggests locating the inductors as close as possible. Fig. 2(a) shows the typical layout of an on-chip spiral inductor. The design parameters of such structure are the outer diameter d, the metal width w, the spacing between the wiring metal s and the number of turns n. The standard lumped-element model associated to this structure is shown in Fig. 2(b) [10]. In this model, L_S and R_S represent the series inductance and resistance, C_F is the fringing capacitance between the metal traces and the overlap capacitance between the spiral inductor and the underpass metal, C_{OX} accounts for the spiral-to-substrate capacitance, and R_{SUB} and C_{SUB} models the behavior of leakage currents across the oxide and the substrate (bulk) and additional capacitive effects related to the substrate.

Table 1
Calculated components values.

Component	Value
$L_g = L_d$	1.465 nH
$L_g/2 = L_d/2$	1.15 nH
C_d	586 fF
L (transistor length)	0.425 μm
W (transistor width)	4.42 μm

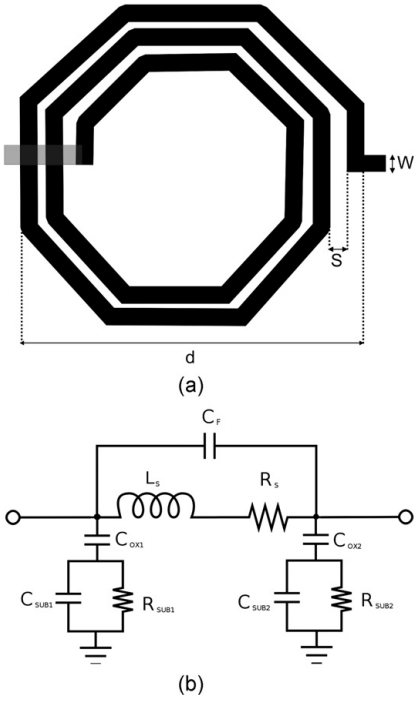

Fig. 2. (a) Layout and design parameter of the on-chip spiral inductor. (b) Simplified lumped-component inductor model.

In CMOS technologies, the on-chip inductors suffer from three main loss mechanisms, namely the ohmic, capacitive and inductive losses. Ohmic losses result from the current flowing through the resistance of the metal tracks. Those losses can be reduced using a wider metal line but, it also increases the capacitive losses (in particular the metal-to-substrate capacitance) causing a decrease in the overall quality factor (Q) and self-resonance frequency (f_{SR}). The displacement currents conducted by the metal-to-substrate capacitance and eddy current generated by the magnetic flux penetrating into the substrate result in capacitive and inductive losses, respectively. In the design of DA other undesired effects also appear like the mutual coupling between inductors. This fact worsens if, as stated above, inductors are situated close to each other in order to achieve a compact design.

Fig. 3(a) shows the electrical model of two series connected on-chip inductors, where each inductor has been modeled with the simplified lumped-element model shown previously. If the frequency range of interest is limited to few GHz, this model can be simplified neglecting substrate and metal capacitance. Other elements, such as R_S and R_{SUB}, can also be of minor importance for the coupling estimation. So, stripped to its essential, the model is reduced to its inductive elements resulting the simplified circuit shown in Fig. 3(b).

This simplified model is composed of two series connected inductors and a mutual coupling between them. Depending on the coiling direction the total inductance (LT) can be calculated using expression (9) or (10). Thus, if both inductors are coiled following the same direction, the mutual coupling is positive and if the spirals are coiled in opposite directions the coupling is negative:

$$L_{T1} = L_{S1} + L_{S2} + 2m_{12} \tag{9}$$

$$L_{T2} = L_{S1} + L_{S2} - 2m_{12} \tag{10}$$

To evaluate the coupling between integrated spiral inductors, electromagnetic (EM) simulations have carried on using a commercially available planar EM simulator (Momentum©). In order to get the simulator to generate useful data, the substrate definition was first calibrated. This was accomplished by using measured data from previously fabricated inductors as a reference, and adjusting the substrate definition until it produced closely correlated data [11–13].

Fig. 4 shows the layouts of the simulated structures: L_{T1}, and L_{T2}. In the first case the inductors are coiled in the same direction,

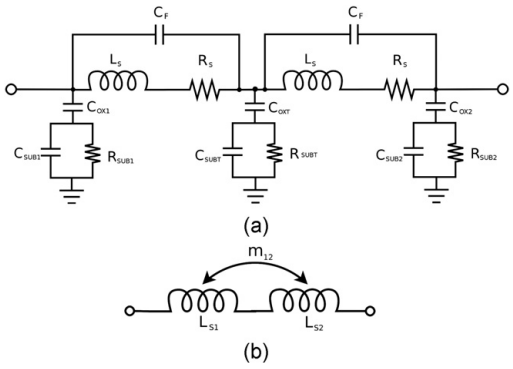

Fig. 3. (a) Model of two on-chip inductors in series. (b) Simplified model of two inductors in series.

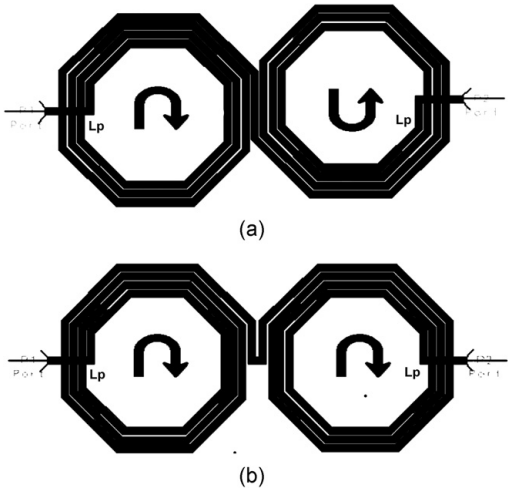

Fig. 4. Layouts of series inductors coiled in the same way (a) and in the opposite way (b).

whereas in the latter case both inductors are coiled in opposite directions. The simulated quality factor and inductance of both structures along with the isolated inductor response (L_P) is depicted in Fig. 5. As it can be observed, in the case where the spirals are coiled in the same direction, the total inductance is around 7 nH at 4 GHz, i.e. more than two times the isolated inductance. Conversely, in the case where the spirals are coiled in opposite directions, the total inductance is 6.4 nH at the same frequency, that is, less than the sum of both inductances.

Regarding the quality factor, the situation is the same. L_{T1} shows a higher Q than L_{T2} because both structures share the same series resistance but their inductances are different.

From the above results it can be stated that, in the design of DA where inductors are situated close to each other to reduce the chip area, it is important to correctly orientate the inductors to minimize the effect of mutual coupling.

3.2. Stacked inductors

Area reduction can also be achieved by adopting a multilevel or stacked structure (MLS) [12,14–17] (see Fig. 6), instead of the usual single-level structure (SLS). The main difference between these two possibilities is, in the SLS case, the inductor is made with one metal layer, usually the top one because it is thicker than the lower metal layers, and in the MLS the turn is expanded vertically. This causes that, for a fixed geometry, the multilevel structure presents a bigger length than the single-level one and, as a consequence, the inductance is increased. This is the main advantage of the multilevel structure: same inductor values can be obtained occupying less area than with the single-level one.

The analysis of this type of inductors does not differ from the SLS. This is because, from the physical point of view, the metal-to-metal and the metal-to-substrate capacitances are larger in the MLS than in the SLS. Therefore the lumped element equivalent circuit that describes the behavior of SLS can be applied to characterize the MLS.

In order to compare both structures, Fig. 7 shows the inductance and quality factor of two 1 nH SLS and MLS inductors. As the figure suggests, Q and f_{SR} of stacked inductors are lower than that of planar spiral inductors [12].

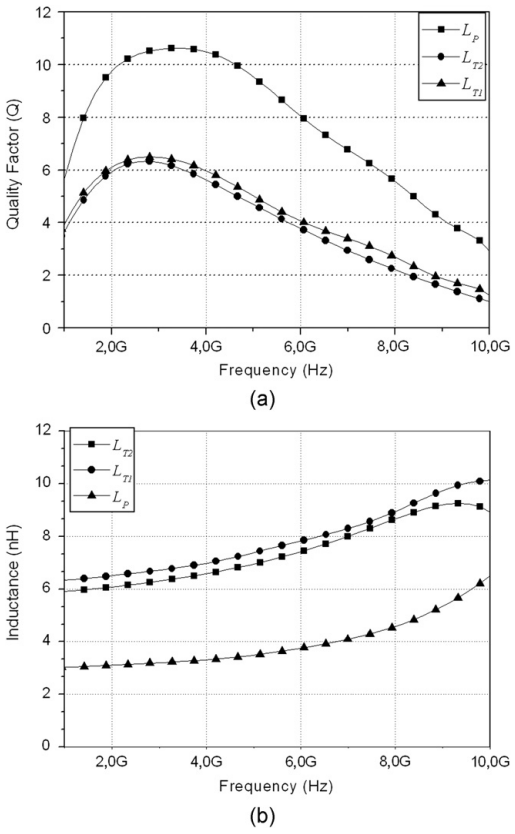

Fig. 5. Influence of mutual coupling in series connected inductors over quality factor and inductance.

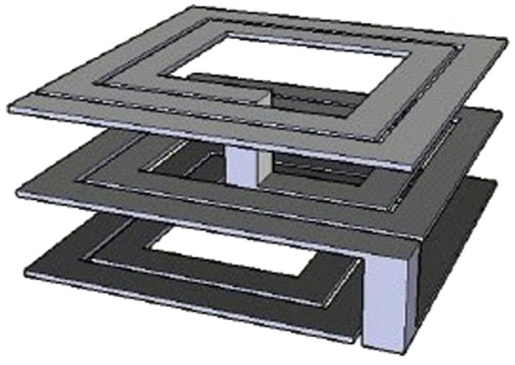

Fig. 6. Stacked inductor layout.

4. Experimental results

In order to validate the proposed area reduction techniques, three prototypes have been fabricated in a low cost CMOS 0.35 μm process. The circuits are called DA1, DA2 and DA3 and they correspond, respectively, to the conventional design, compact

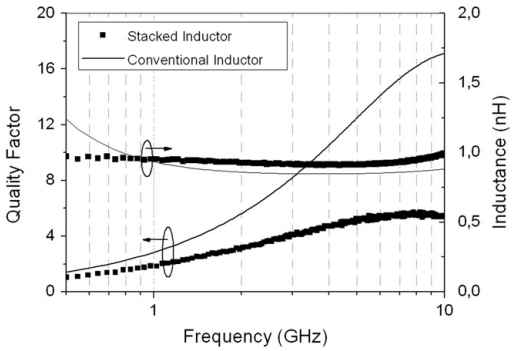

Fig. 7. Conventional inductor vs. stacked inductor.

design and compact design with stacked inductors. The micro-photographs of the fabricated circuits are shown in Fig. 8. The design issues concerning the implementation of the three circuits will be described in the following paragraphs.

One of the difficulties in designing a fully integrated DA is creating the required high-quality inductors. Fig. 9 shows the simulated quality factor and inductance of the inductors used in the three designs. Table 2 shows the geometrical parameters of the chosen coils. The first one is a conventional planar spiral inductor and the second is a stacked inductor. The conventional inductor was used to generate $L_d = L_g$ and $L_d/2 = L_g/2$ in DA1 and DA2. As it can be observed in Fig. 9, at 5 GHz this inductor presents a quality factor and an inductance of 9.28 and 1.3 nH, respectively. Although this inductor does not have half of the inductance than $L_d = L_g$, its physical layout perfectly match with the other components in both designs. On the other hand, the stacked inductor was used in the gate line of DA3. This circuit keeps the conventional inductor in the drain line because the current flowing through this line is too high to be supported by stacked inductors.

Due to the very high frequency of operation, special attention has been paid to the layout. Thus, enough design accuracy has been achieved by adding accurate high-Q inductor model and optimizing parasitic effects coming from discontinuity and interconnection. The designed DAs utilize a transistor size of 130 μm (equivalent to a 13 gates with 10 μm gate width) and a capacitance C_d of 150 fF.

The DA1 circuit occupies an area of 0.74 mm^2, which includes the pad frame. In contrast to the conventional design, the compact design DA2 occupies a total area of 0.61 mm^2, i.e. a reduction of area 17%. Finally, the Compact design with stacked inductors DA3 occupies a total area of 0.47 mm^2 which implies a 36% of saving area.

After the measurement of several samples of the DA, the frequency response is shown in Fig. 10. The power gain of DA1 is 6 dB with $\pm$0.6 dB flatness from 1 to 5 GHz and a unity gain around 8.6 GHz. The input and output matching are better than -10 dB over the bandwidth. The increase in gain at low frequency is due to the higher impedance of the blocking capacitance at low frequency. All measurements were taken under identical DC bias condition, 3 V on the drain and 0.8 V on the gate. At this bias point the DA consumes 30 mA giving a total power dissipation of 90 mW. Finally, Fig. 10 also shows the noise response. The noise figure is under 5 dB from 1 to 6.5 GHz, and it is around 7.5 dB at 8.5 GHz.

The frequency response of DA2 is approximately the same of DA1. Regarding the noise figure, DA2 performance is better than

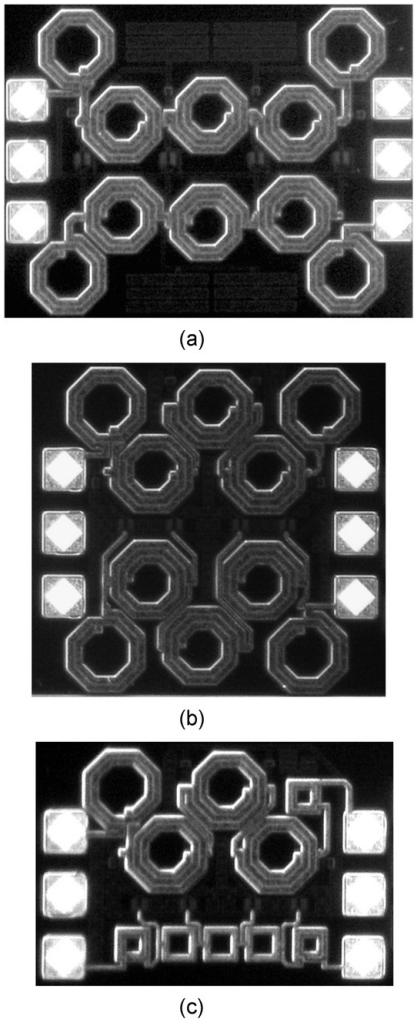

Fig. 8. Microphotograph of the fabricated DA: (a) DA1: conventional design (0.7 mm^2), (b) DA2: compact design (0.6 mm^2), (c) DA3: compact design with stacked inductors (0.4 mm^2).

DA1 mainly because the parasitic associated to the connection tracks has been reduced.

With respect to DA3, in spite of the stacked inductor performance is worse than the conventional ones, its response is very similar to DA1 and DA2. The noise figure is a little bit higher than that of the conventional design. This is due to the series resistance associated to stacked inductors is larger than that of conventional inductors.

Table 3 summarizes the performance of the presented amplifiers, with comparison to previously published DAs.

To provide an objective method to compare the developed circuits and other similar works, a figure of merit has been used:

$$FOM = \frac{P_{1\,\mathrm{dB}}}{P_{noise}} \frac{1}{P_{DC}} \frac{f_h}{f_t^*} \frac{1}{AREA} \tag{11}$$

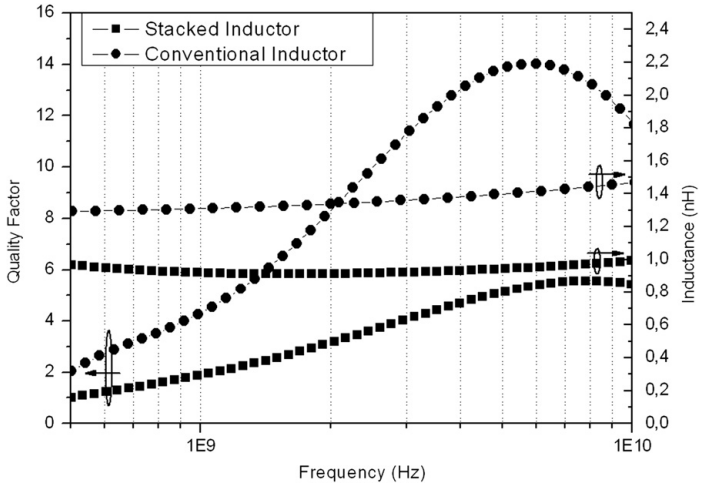

Fig. 9. Inductors employed in the DA.

Table 2
Inductors geometrical parameters.

	s (μm)	n	r (μm)	W (μm)
Conventional	2	2.5	100	16
Stacked	2	2 × 1.5	40	10

This expression includes the DC power consumption (P_{DC}) and output noise power ($P_{noise} = P_{th}FGain$), where $P_{th} = kT$ is the thermal noise floor given by -174 dBm/Hz at $T = 290$ K. In addition, in order to quantify how efficient the available bandwidth of the technology is utilized, a relative measure for bandwidth is introduced through the f_h/f_t^* factor, where f_h is the upper LNA corner frequency and f_h/f_t^* is the technology unity current gain bandwidth f_t around the maxima of the product $(g_m/I_D)f_t$. Finally, AREA is the area occupied by the circuit and it allows comparing the designs in terms of area consumption. The proposed FOM includes the output 1-dB compression power ($P_{1\,dB}$) as a measure for linearity. However, some authors do not include this measurement and, as a consequence, two FOMs have been plotted in Table 3: one including the $P_{1\,dB}$ and the other one without any linearity reference.

The DA presented in [2] has an excellent FOM, mainly because it utilizes very efficiently the available bandwidth of the technology. However, the area of this circuit almost doubles our designs and, as a consequence, its FOM is lower than ours. The same authors utilize a fully differential topology in [3] to achieve a wider bandwidth than its single-ended counterpart. However, both area and power consumption double and the achieved FOM is low.

The works of [4] exhibit both higher gain and bandwidth than our designs. Also the power dissipated is low being the NF similar than our designs. However, our DAs achieve better FOMs mainly because they utilize more efficiently the available area.

The low power techniques presented in [19,7] use a low P_{DC} to achieve low noise figure and good gain, but they are, however, fundamentally limited by large area.

Finally the DA reported in [18] uses coplanar waveguides to implement the required inductances. This technique achieves a very high frequency of operation but at the cost of a very large area.

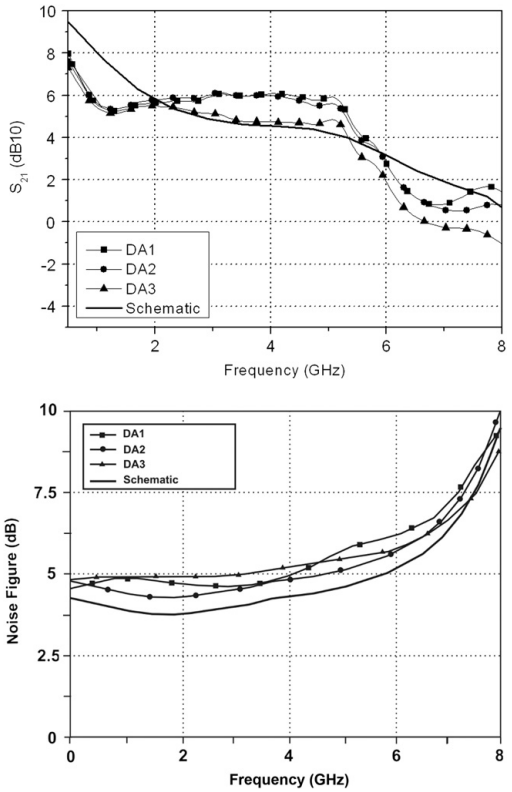

Fig. 10. S21 and noise figure measurements.

Regarding the presented designs, the best FOM is achieved, as expected, by DA3. This design employs stacked inductors to reduce area. This kind of inductor occupies less chip area than that

Table 3
Summary of LNA performance and comparison with previously published design.

Reference	Gain (dB)	BW (GHz)	NF (dB)	$P_{1\,dB}$ (dBm)	Area (mm^2)	ft[a] (Tech.)	P_{DC} (mW)	FOM[a]	FOM[b]
[2]	6.1	5.5	6.8	8.8	1.12	10.5(CMOS 0.6)	83.4	151	132
[3]	5.5	8.5	10.85	N/A	2.86	10.5(CMOS0.6)	286	57	–
[4]	7.3	22	5.2	10	1.6	33.7(CMOS 0.18)	52	108	95
[4]	10.6	14	4.35	5.3	1.35	33.7 (CMOS 0.18)	52	124	106
[18]	6	27	6	10	1.62	33.7 (CMOS 0.18)	68	107	94
[19]	4	8	5.4	8	0.84	33.7 (CMOS 0.18)	23	208	182
[7]	10	11	4.6	N/A	1.44	33.7 (CMOS 0.18)	19.6	119	–
[7]	16	11	4.5	N/A	1.44	33.7 (CMOS 0.18)	100	110	–
DA1	7	6.5	5	12.3	0.74	8.13 (CMOS 0.35)	90	231	207
DA2	7	6.5	4.5	12.4	0.61	8.13 (CMOS 0.35)	90	282	253
DA3	5.5	6.5	6	11.2	0.47	8.13 (CMOS 0.35)	90	364	325

[a] FOM not including $P_{1\,dB}$.
[b] FOM including $P_{1\,dB}$.

of planar spiral since the turn is expanded vertically. Usually, top metal is thicker than lower metal layers, and thus the *Q*-factor of stacked inductors is lower than that of planar spiral inductors. However, as the area occupation is much smaller, substrate losses are smaller, so only little performance degradation of the stacked inductor circuit is achieved over the planar spiral inductor one. This result demonstrates that it is possible to reduce the area with a minimum influence over the circuit response.

5. Conclusions

In this paper two techniques to reduce the area in CMOS DA have been reported. The first one consists on reallocate the drain and gate line inductors but minimizing the mutual inductance between them. The other technique employs stacked inductors. Although the quality factor of stacked inductor is lower than that of planar spiral inductor, as the area is much smaller, substrate losses are also smaller, and only little circuit performance degradation is achieved when using stacked inductor over planar spiral inductors. Using the above techniques, three fully integrated DA have been designed, fabricated and tested. The overall performance rivals recently published results reported for CMOS DA, achieving the highest FOM in only 0.47 mm^2 chip area. Since these DAs were fabricated using a commercial 0.35 μm CMOS technology, they can be easily integrated with other front-end circuits to build CMOS transceivers without requiring any additional masks or post-processing steps.

Acknowledgments

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References

[1] Bevilacqua AM, Niknejad A. An ultra-wideband cmos lna for 3.1 to 10.6 GHz wireless receivers. In: IEEE international solid-states circuits conference, 2004.
[2] Ballweber BM, Gupta R, Allstot DJ. Fully integrated 0.5–55 GHz CMOS distributed amplifier. IEEE Journal of Solid-State Circuits 2000;37:231–9.
[3] Ahn H, Allstot DJ. A 0.5–8.5 GHz fully differential cmos distributed amplifier. IEEE Journal of Solid-State Circuits 2000;37:985–93.
[4] Liu R, Lin C, Deng K, Wang H. Design and analysis of dc-to-14-GHz and 22-GHz cmos cascode distributed amplifiers. IEEE Journal of Solid-State Circuits 2004;39:1370–4.
[5] Worapishet A, Chongcheawchamnan M, Srisathit S. Broad-band amplification in CMOS technology using cascaded single-stage distributed amplifier. Electronics Letters 2002;38:675–6.
[6] Virdee AS, Virdee BS. 2–18 GHz ultra-broadband amplifier design using a cascaded reactively terminated single stage distributed concept. Electronics Letters 1999;35:2122–3.
[7] Guan X, Nguyen C. Low-power-consumption and high-gain cmos distributed amplifiers using cascade of inductively coupled common-source gain cells for uwb systems. IEEE Transaction on Microwave Theory and Techniques 2006;54:3278–83.
[8] Frank BM, Freundorfer AP, Antar YMM. Performance of 1–10 GHz traveling wave amplifiers in 0.18−μm cmos. IEEE Microwave Wireless Components Letter 2002;12:327–9.
[9] Sullivan PJ, Xavier BA, Ku WH. An integrated CMOS distributed amplifier utilizing packaging inductance. IEEE Transaction on Microwave Theory and Techniques 1997;45:1969–76.
[10] Lee TH. The design of CMOS radio-frequency integrated circuits. Cambridge: Cambridge University Press; 1998.
[11] Medina O, del Pino J, Goni A, Khemchandani SL, Garcia J, Hernandez A. A method to build-up an integrated inductor library. In: XX design of integrated circuits and systems conference, 2005.
[12] Goni A, del Pino FJ, Khemchandani SL, Garcia JA, Gonzalez B, Hernández A. Study of stacked and miniature three-dimensional inductor performance for rf ic design. In: SPIE – The international society for optical engineering's – microtechnologies for the new millennium design (VLSI circuits and systems conference), 2007.
[13] Goni A, del Pino J, Gonzalez B, Hernandez A. An analytical model of electric substrate losses for planar spiral inductors on silicon. IEEE Transaction on Electronic Devices 2007;54:546–53.
[14] Niknejad AM. Analysis, design and optimization of spiral inductors and transformers for si rf ics. Diploma thesis. Berkeley, CA: University of California, 1998.
[15] Burghartz JN, Jenkins KA, Soyuer M. Multilevel-spiral inductors using vlsi interconnect technology. IEEE Electron Devices Letter 1996;17:428–30.
[16] Geen M, RG, Arnold RG, Jenkins JA. Miniature multilayer spiral inductors for GaAs mmics. In: 11th annual GaAs IC symposium, 1989. p. 381–94.
[17] Aguilera J, Meléndez J, Berenguer R, Sendra JR, Hernández A, del Pino J. A novel geometry for circular series connected multilevel inductors for cmos rf integrated circuits. IEEE Transaction on Electron Devices 2006;46:1084–6.
[18] Amaya RE, Tarr NG, Plett C. A 27 GHz fully integrated cmos distributed amplifier using coplanar waveguide. In: IEEE RFIC symposium, 2004. p. 193–6.
[19] Huang H-L, Chou M-F, Wuen W-S, Wen K-A, Chang C-Y. A low power cmos distributed amplifier. IEEE annual conference wireless and microwave technology, 2005. p. 47–50.

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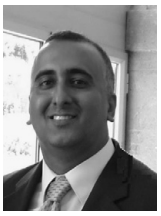

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Title	Area Reduction in RF Fully Integrated Front-Ends for Ultra-Wideband
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Date	November 2010

Area Reduction in RF Fully Integrated Front-Ends for Ultra-Wideband

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Abstract— This paper describes two RF front-ends for Ultra Wideband (3.1-10.6 GHz) implemented in UMC CMOS 0.18 µm process. The first one uses a differential common-gate with shunt peaking LNA followed by a Gilbert Cell based quadrature mixer. Post-layout simulations show a conversion gain of 12 dB, a 9.4 dB of noise figure and a third-order intermodulation intercept point of -3.3 dBm. This combination draws 16 mW from a 1.8 V supply. The second design, which is inductor less, uses a differential common-gate with resistive loaded LNA followed by a quadrature capacitive degeneration mixer circuit. Simulation results are 7.2 dB of conversion gain, 13.7 dB of noise figure and -2.1 dBm of IIP3. This combination draws 14 mW from a 1.8 V supply. The occupied area of this design is 54% lower than the first front-end.

Keywords-component: Front-end, Receiver, Low-Noise Amplifier (LNA), Mixer, Shunt-peaking, Ultra-Wideband.

I. INTRODUCTION

Ultra-Wideband technology (UWB) [1] has motivated a great interest in the domestic and office environments with the implementation of new electronic devices: PCs, digital video and audio systems, digital television, last generation mobile phones, PDAs, etc. They demand a wireless solution with a maximum bandwidth and minimum power consumption.

The WiMedia Alliance was born to boost up the UWB technology. Due to this active participation, in 2007 the WiMedia Alliance published the ISO/IEC 26907 [2] and ISO/IEC 26908 [3] standards to regulate the physical and the MAC layers, including the interface between them. The UWB frequency band of 3.1-10.6 GHz is divided into 14 sub-bands of 528 MHz each and employs OFDM in each band to transmit data rates as high as 480 MB/s. To ensure small interference with existing standards, the output power level of UWB transmitters has been fixed to -41 dBm. On the other hand, the minimum sensibility that allows an UWB receiver is -73 dBm.

This paper deals with the RF front-end of an UWB receiver. In this work two possible configurations for the RF front-end have been developed. One of them is inductor less, so it occupies less area and also has low power consumption. The paper is organized as follows: In section II the common gate LNA topology is explained. The quadrature mixers are studied in section III. In section IV the two front-ends are described and simulations results are shown. Finally, some conclusions are drawn in section V.

II. COMMON-GATE LNA

Common-gate (CG) LNA is a widely used topology in wireless communications [4]-[7]. In this section, the CG LNA is studied, i.e., we discuss the relationship between the input matching and voltage gain, we evaluate the noise figure and finally we show the Gm-boosted topology.

A. Input Matching and voltage gain

The desired input impedance of a CG input stage is achieved by adjusting the bias current, aspect ratio, and overdrive voltage such that 1/gm of approximately 20 mS. The CG stage does not suffer from the Miller effect, and thus an adequate reverse isolation can be achieved with a single transistor stage. Therefore, the input matching network and load can be designed separately.

Large impedance towards the signal ground is needed to steer the signal into the input transistor source. This can be achieved with a current source I_{BIAS} shown in Figure 1a. That topology is not typically utilized in the LNA since the current source I_{BIAS} increases the noise. A better noise performance is achieved by using a source inductor L_S as shown in Figure 1b. The L_S forms a parallel LC resonator with the parasitic capacitance C_{PAR} associated with the source node of the M1. When on-wafer measurements are not applicable, the source node typically needs to be connected either to package or PCB by using a bondwire inductance L_{IN} as shown in Figure 1c. The L_{IN} is resonated at the wanted frequency with a DC blocking capacitor C_{IN} which can be either an on-chip or an external component.

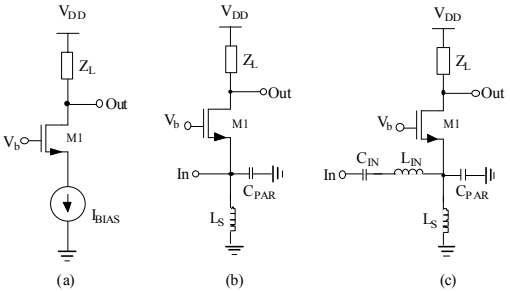

Figure 1 Common-gate LNA imput interfaces: a) current source, b) parallel LC resonator, and c) series and parallel LC resonators.

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In Figure 1b and Figure 1c, the capacitor C_{PAR} includes the parasitic capacitances at the source node, i.e. source-body junction capacitance of M1, substrate capacitance of L_S, and capacitance caused by the bonding pads and on-chip metal wiring. Furthermore, the value of the source inductor L_S can be decreased by adding an additional shunt capacitor C_S in parallel with L_S (the C_S is not shown in Figure 1b or Figure 1c). Therefore, all the capacitance al the source node can be included in a single source capacitor C_T used in the following calculations:

$$C_T = C_{GS} + C_{PAR} + C_S \tag{1}$$

The input impedance Z_{IN} of a CG input stage, shown in Figure 1b, can be calculated as

$$Z_{in} = \frac{sL_s}{1 + sL_S gm + s^2 L_S C_T} \tag{2}$$

The source inductance L_S resonates with the capacitance C_T at the frequency of

$$\omega_o = \frac{1}{\sqrt{L_S C_T}} \tag{3}$$

and at the frequency, (2) simplifies to 1/gm. The impedance Z_{IN} of a CG input stage shown in Figure 1c is

$$Z_{in} = \frac{1 + s^2 C_{IN} L_{IN}}{sC_{IN}} + \frac{sL_S}{1 + sL_S gm + s^2 L_S C_T} \tag{4}$$

With a perfect impedance matching ($1/gm = R_S$), the voltage gain of the CG amplifier becomes a division of output load versus the source impedance, i.e. Z_L/R_S. The assumption is valid if the drain-to-source resistor r_{ds} is much larger than the load resistance at the drain. Otherwise, the gain and input impedance formulas should be modified to

$$A_V = \frac{gmZ_L}{\left(1 + \frac{Z_L}{r_{ds}}\right)} \tag{5}$$

and

$$R_{IN} = \frac{1}{gm}\left(1 + \frac{Z_L}{r_{ds}}\right) \tag{6}$$

B. Noise of a CG stage

The noise factor of a CG LNA is expressed as

$$F = 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+\chi}\right)^2 \frac{1}{gmR_S} \tag{7}$$

where γ is the coefficient of channel thermal noise, gm is the transistor transconductance, χ is the ratio of the transistor substrate transconductance gm_b and gm, R_S is the source resistance and α is gm/g_{do}. Because the minimum NF of an common source LNA increases along with the frequency, CG LNA can be a better option at very high frequencies. When χ is neglected and perfect input matching is assumed, the minimum noise factor typically presented in the literature is achieved:

$$F = 1 + \frac{\gamma}{\alpha} = \frac{5}{3} = 2.2dB \tag{8}$$

With imperfect input matching, the noise factor can be lowered according to

$$F = 1 + \gamma \frac{1 + S_{11}}{1 - S_{11}} \tag{9}$$

where α is neglected.

In addition, (7) does not take into account the noise of the load. If resistive load R_L is used, taking into account its noise contribution, assuming that $gm=1/R_S$ the noise factor becomes

$$F = 1 + \frac{1}{gmR_S}\left(\frac{\gamma}{\alpha} + \frac{(1 + gmR_S)^2}{gmR_L}\right) \approx 1 + \frac{\gamma}{\alpha} + \frac{4R_S}{R_L} \tag{10}$$

Thus, the resistive load can make a significant contribution to the overall noise.

C. Gm-boosted CG stage

The input matching requirement prevents increasing *gm* of the input transistor to lower the noise factor. The link between noise factor and input matching can be separated by introducing inverting gain from the source to the gate of the input transistor (Figure 2). As a result, the effective transconductance of the boosted CG stage is

$$gm_{eff} = (1 + A)gm \tag{11}$$

where A is the gain between source and gate. The input matching is achieved, when

$$gm = \frac{1}{R_S}\frac{1}{(1+A)} \tag{12}$$

and the noise factor is reduced to

$$F = 1 + \frac{\gamma}{\alpha}\left(\frac{1}{1+A}\right) \tag{13}$$

According to (12) less bias current is required to achieve the required input matching and therefore, less drain current noise from the input transistor is obtained.

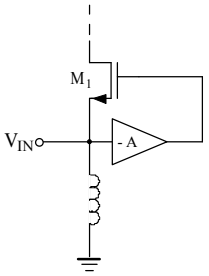
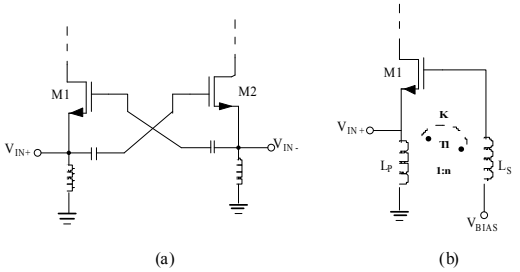


Figure 2 Gm-boosted common-gate input stage.

In Figure 3, the capacitor cross-coupling method, which is suitable for differential input configurations, is presented. Due to the capacitor divider between C_{GS} and coupling capacitance C_C, the inverting gain is approximately $A=C_C/(C_C+C_{GS})$, which is always less than one.

The transformer-coupled technique shown in Figure 3 is proposed to achieve inverted gain greater than one. The primary and secundary inductors L_P and L_S form a transformer, which provides an anti-phase operation between gate and source terminals.



(a) (b)

Figure 3 a) Capacitor cross-coupled CG stage, b) transformer-coupled CG stage.

III. MIXERS DESIGN

A. *Quadrature mixers*

Normally, the down conversion to zero or IF frequency is usually performed with quadrature (I/Q) mixers [8]. For I/Q-mixers, there are different possibilities to implement the interface between input transconductor and switch quad. The first topology is shown in Figure 4. The RF signal is fed into two separate input stages, which drive their respective switch quads. Another possibility is to utilize a single input stage, which drives both switch quads, as it is shown in Figure 5

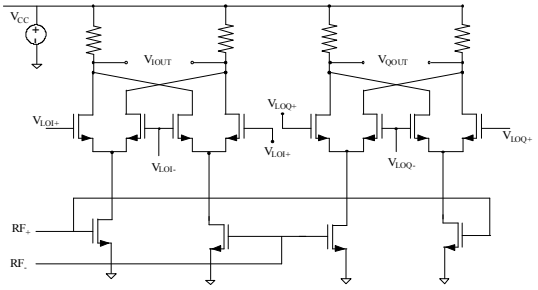


Figure 4 Two separate Gilbert mixers driven by quadrature LO signals.

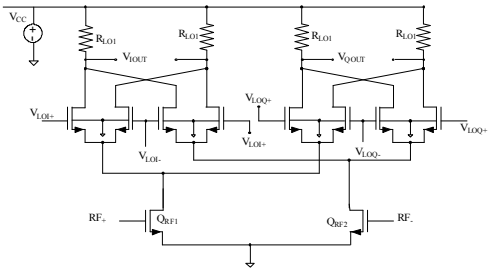


Figure 5 Quadrature mixer with single input stage.

Since the transconductor of the mixer, shown in Figure 5, drives both switch quads, the conversion gain is 3 dB lower than the basic Gilbert cell mixer of Figure 4. In adittion, complete switching requires larger LO amplitude when quadrature switch quads are driven from a single transconductor.

B. *Mixers with current boosting*

The current boosting method [4], [8]-[9] is used in the mixer and it is shown in Figure 6. The optimum bias for the input and switching stages can be optimized separately with current boosting. Due to proper gain and linearity performance, the input transconductance stage should be biased with rather higher current. However, the performance of the switch quad may require quite low current level for optimum operation. The conversion gain increases for two main reasons: the mixer requires a lower LO swing to switch completely and a larger load resistor value can be used to increase the voltage gain. Alternatively, if the load resistor value is kept unchanged, mixer design for lower supply voltages is alleviated with current boosting, since the voltage drop at the resistive load is reduced.

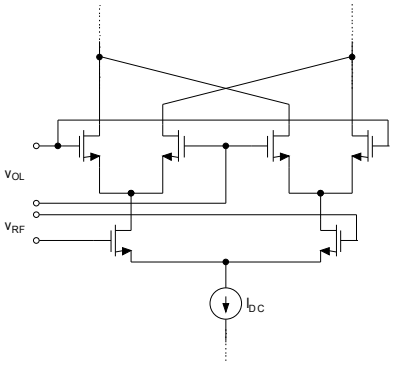


Figure 6 Current boosting with constant current source.

IV. RESULTS

A. Receiver I

Figure 7 shows a RF front-end composed by a differential common-gate shunt-peaking LNA followed by differential double balanced Gilbert mixer. The layout of the circuit, named as Receiver I, is shown in Figure 8.

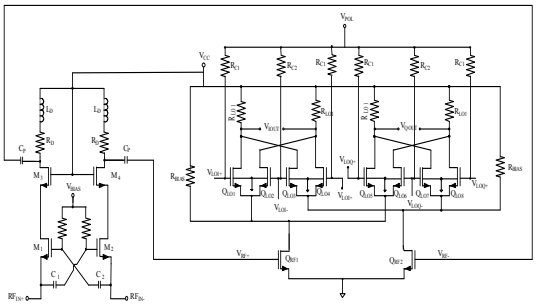


Figure 7 Schematic of the Receiver 1.

The Receiver I chip area, including the test pads, is 1410.63µm x 693.39µm. The results of post-layout simulations are summarized in TABLE I and discussed below.

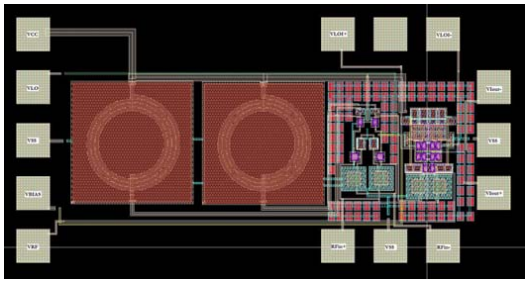


Figure 8 Layout of the Receiver1.

Conversion gain and noise figure simulation results are shown in Figure 9 and Figure 10 respectively, for a 400 MHz channel located at the center of the band. Receiver I has a conversion gain of 12.1 dB at 5.2 GHz and a noise figure of 11.2 dB (IF=200MHz).

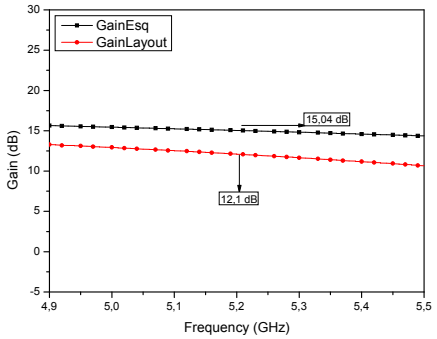


Figure 9 Simulation results of conversion gain for Receiver I.

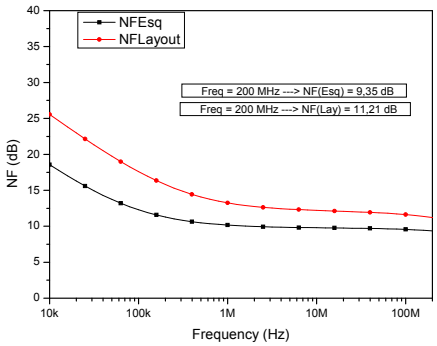


Figure 10 NF simulation results for Receiver I.

The two-tone test for third-order intermodulation distortion (IIP3) of Receiver I is shown in Figure 11. The test was performed at 5 GHz and an IIP3 of -3.3 dBm was obtained.

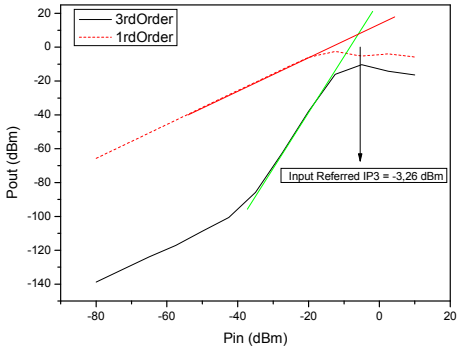


Figure 11 IIP3 simulation results for Receiver I.

B. Receiver II

Figure 12 shows an RF front-end composed by a differential common-gate resistive load LNA followed by differential double balanced Gilbert mixer with capacitive degeneration. The layout of the circuit, named as Receiver II, is shown in Figure 13.

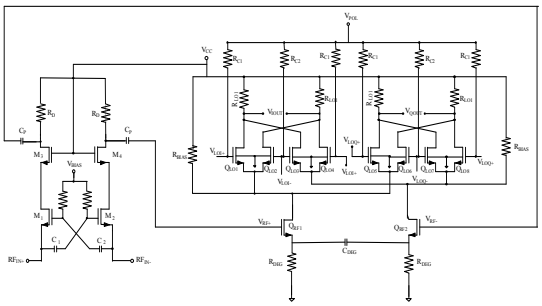


Figure 12 Schematic of Receiver II.

The Receiver II chip area, including the test pads, is 698.89µm x 744.76µm. Due to the nonexistence of inductors, the occupied area of this design is 54% lower than Receiver I.

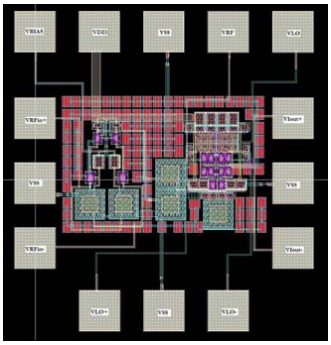


Figure 13 Layout of Receiver II.

Conversion gain and noise figure simulation results are shown in Figure 14 and Figure 15 respectively, for a 400 MHz channel located at the center of the band. Receiver II has a conversion gain of 7.2 dB at 5.2 GHz and a noise figure of 13.71 dB (IF=200MHz).

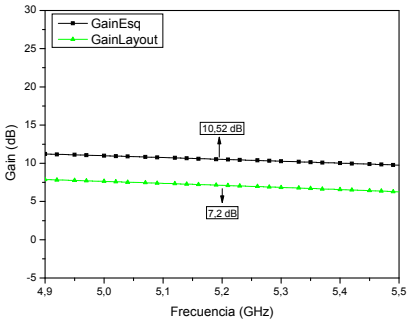


Figure 14 Conversion gain simulation for Receiver II.

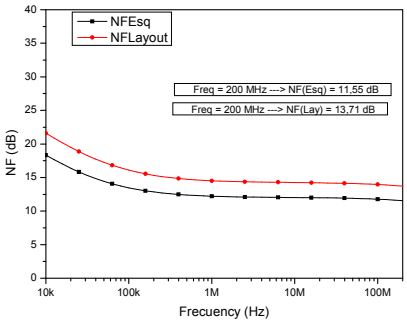


Figure 15 NF simulation for Receiver II

The linearity of the Receiver II was evaluated with two-tone IP3 test. The result is plotted in Figure 16. The IIP3 is -2.1 dBm.

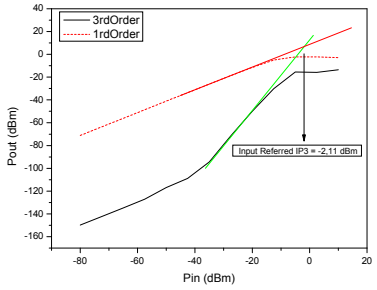


Figure 16 IIP3 simulation for Receiver II.

TABLE I FRONT-ENDS PERFORMANCE SUMMARY

	Receiver I	***Receiver II***
NF (dB)	11.2	13.7
Gain (dB)	12.1	7.2
IIP3 (dBm)	-3.3	-2.1
Consumption (mW)	16	14
Area (mm^2)	0.97	0.52

V. CONCLUSIONS

This paper describes two RF front-ends for Ultra Wideband implemented in UMC CMOS 0.18 µm process. The first one (Receiver I) uses a differential common-gate with shunt peaking LNA followed by a quadrature mixer. The second design (Receiver II), which is inductor less, uses a differential common-gate with resistive loaded LNA followed by a quadrature capacitive degeneration mixer circuit. Although the obtained specifications of this Receiver II are slightly worse than the first version, the occupied area of this design is 54% lower, also the power consumption has decreased.

REFERENCES

[1] Federal Communications Commission (FCC). "Revision of Part 15 of the Commission's Rules Regarding Ultra Wideband Transmission Systems," First Rep. and Order, ET Docket 98-153, FCC 02-48, Adopted: Feb. 2002; Released Apr. 2002.

[2] International Standard ISO/IEC 26907 "Information technology - Telecomunications and Information exchange between systems - High Rate Ultrawideband PHY and MAC Standard", Mar. 2007.

[3] International Standard ISO/IEC 26908 "Information technology - Telecomunications and Information exchange between systems - MAC-PHY Interface for ISO/IEC 26907", Apr. 2007.

[4] Jouni Kaukovuori, "CMOS Radio Frequency Circuits For Short-Range Direct-Conversion Receivers", Doctoral Dissertation, Helsinki University of Technology, Faculty of Electronics, Communications and Automation, Department of Micro and Nanosciences, 2008.

[5] T.H. Lee, "The Design of CMOS RF Integrated Circuits" Cambridge University Press, 1998.

[6] Behzad Razavi, "RF Microelectronics" University of California: Prentice Hall PTR, 1998.

[7] Behzad Razavi, "Design of Analog CMOS Integrated Circuits" Mc Graw Hill, 2001.

[8] J. del Pino, "Modelado y aplicaciones de inductores integrados en tecnologías de silicio", Tesis doctoral, Departamento de Ingeniería Electrónica y Automática, Universidad de Las Palmas de Gran Canaria, 2002.

[9] Ramesh Harjani and Liuchun Cai, "1-10GHz Inductorless Receiver in 0,13µm CMOS", IEEE Radio Frequency Integrated Circuits Symposium, University of Minnesota, Minneapolis, 2009.

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A Feedback Wideband LNA with a modified 3D inductor for UWB Applications

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Abstract— **In this paper, we propose a modified miniature 3-D inductor to implement a fully-integrated feedback wide band amplifier in a standard SiGe low cost 0.35 µm process. According to the measurements results, the proposed technique achieves a 40% of area reduction with minor performance degradation over the same circuit implemented with conventional inductors. The circuit provides a gain from 15 to 7 dB in the band between 3.1 to 10.6 GHz. In the same band the noise figure varies from 3.2 to 3.7 dB.**

Index Terms— **Amplifier noise, Low-Noise Amplifier (LNA), Noise Figure (NF), Feedback Amplifier, SiGe Amplifier, Ultrawideband (UWB), Wideband Matching.**

I. Introduction

UltraWideBand (UWB) is a new wireless technology capable of transmitting data over a wide spectrum of frequency bands with very low power and high data rates. Among the possible applications, UWB technology may be used for imaging systems, vehicular and ground-penetrating radars, and communication systems. In particular, it is envisioned to replace almost every cable at home or in an office with a wireless connection that features hundreds of megabits of data per second. UltraWideBand has bandwidth of 3.1-10.6 GHz and transmission speeds up to 400-500 Mbps [1]-[2].

Figure 1 shows the UWB zero-IF receiver architecture, which is well suited for this application [3]-[5]. The antenna signal is filtered by an external passive pre-select filter to reduce the level of out-of-band interferers. The front-end consists of a wideband LNA and a quadrature mixer that converts the signal down to zero-IF. The synthesizer provides the frequency quadrature LO signals. The baseband filter provides both filtering and variable gain. The filtered baseband signal is digitized by the ADC, which is followed by the digital baseband processor.

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The Low Noise Amplifier (LNA) is an important element due to its contribution to the noise figure.

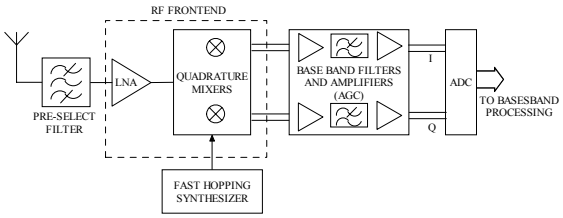


Figure 1 Schematic of a receiver for UWB.

A number of UWB LNA designs use the inductor degenerated transconductor with LC ladder input matching networks to achieve wideband impedance matching. Traditionally, the bandwidth at the output of the LNA is extended by using inductive peaking techniques. The large number of inductors in such circuits increases design complexity and silicon area. This paper focuses on the design of a LNA in a 0.35 µm SiGe technology for the receiver path of an UWB system using a modified miniature 3-D inductor.

The paper is organized as follows. In Section II, the proposed circuit is analyzed. The proposed inductor is analyzed in Section III. The final implemented circuit and the results are reported in Section IV.

II. Circuit Design

Figure 2 shows the feedback amplifier. The amplifier consists of a single stage in common-emitter configuration and an emitter follower in the feedback path. Flat frequency response and matching to 50 Ω at the input and output are achieved by shunt feedback via Q_2, R_2, R_3 and L_B.

There is often a trade-off between noise and input impedance matching in LNA designs. This trade-off reflects on the choice of transistor sizing, which is mainly dependent on the designer's objectives and priorities. A common approach used is to first determine the transistor sizing which makes the circuit be approximately noise matched to the characteristic impedance of the system, typically 50 Ω, at the

frequency range of interest. Therefore, by choosing the proper transistor size, noise matching can be achieved without signal losses or noise figure degradation [6].

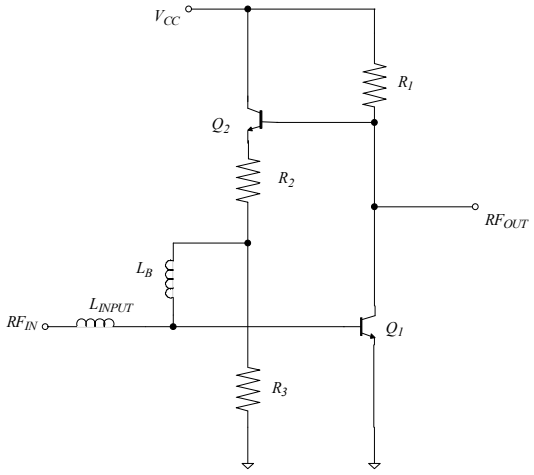


Figure 2 Schematic of the feedback amplifier for wideband.

The use of an emitter follower in the feedback path increases the collector-emitter voltage, resulting in a higher f_{max} of the transistor and improved large-signal behaviour. The emitter size of Q_1 is determined by a compromise between low noise and large bandwidth. The effective emitter area of Q_1 is 36 μm^2. The emitter follower Q_2 contributes only little to the output noise and has an effective emitter area of 1 μm^2.

The inductor L_{INPUT} is used to achieve a good response in a huge frequency range (from 0-15 GHz). This coil is in the direct path of the signal but its inductance value is low (0.5 nH). As low inductance spirals are achieved with a small number of turns, the quality factor is high and, in consequence, its contribution to the total noise figure will be low.

The inductor L_B is used to optimize the frequency response. Large values for the inductance of L_B lead to peaking in the frequency response. While this allows extending the bandwidth to higher frequencies, excessive peaking is undesirable for broadband communications systems which require a flat group delay. The quality factor Q is only of minor importance in this application, due to its low noise contribution in the signal path. Thus, L_B is realized as a modified miniature 3-D inductor.

III. Modified Miniature 3-D Inductor

Figure 3 (a) shows the typical layout of an on-chip spiral inductor. The design parameters of such structure are the outer diameter *d*, the metal width *w*, the spacing between the wiring metal *s* and the number of turns *n*. The standard lumped-element model associated to this structure is shown in Figure 3 (b). In this model, L_S and R_S represent the series inductance and resistance, C_F is the fringing capacitance between the metal traces and the overlap capacitance between the spiral inductor and the underpass metal, C_{OX} accounts for the spiral-to-substrate capacitance, and R_{SUB} and C_{SUB} models the behavior of leakage currents across the oxide and the substrate (bulk) and additional capacitive effects related to the substrate [7]-[8].

In CMOS technologies, the on-chip inductors suffer from three main loss mechanisms, namely the ohmic, capacitive and inductive losses. Ohmic losses result from the current flowing through the resistance of the metal tracks. Those losses can be reduced using a wider metal line but, it also increases the capacitive losses (in particular the metal-to-substrate capacitance) causing a decrease in the overall quality factor (*Q*) and self-resonance frequency (f_{SR}). The displacement currents conducted by the metal-to-substrate capacitance and eddy current generated by the magnetic flux penetrating into de substrate result in capacitive and inductive losses respectively.

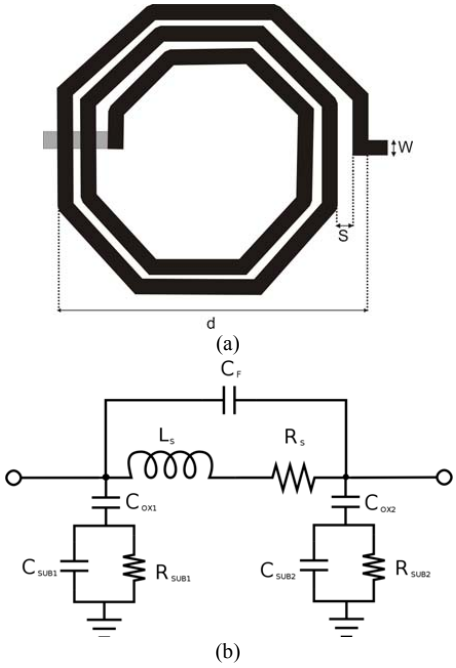


Figure 3 Layout and design parameters of the on-chip spiral inductor. (b) Simplified lumped-element inductor model.

The miniature 3-D was proposed in 2002 [8]. This structure consists of at least two or more stacked inductors by series connections, and every stacked inductor has only one turn in

every metal layer.

For example, if there are two stacked inductors with different diameters, and one of them is a one-turn stacked inductor from the metal layer 4 to the metal layer 1, and the other is a one-turn stacked inductor from the metal layer 1 to the metal layer 3, then the miniature 3-D inductor is formed by connecting two stacked inductors at the metal 1, as Figure 4 shows.

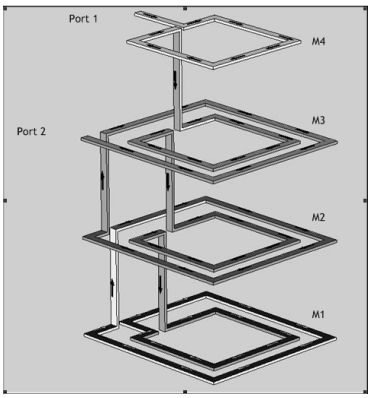


Figure 4 Miniature 3-D inductor.

The proposal structure consists in two 3-D rectangular coils connected in series, as shown in Figure 5. The objective is to share the magnetic flux generated by the coils, so that the total inductance is greater than the sum of each one of them separately, increasing the inductance of the coil without diminishing the quality factor too [7].

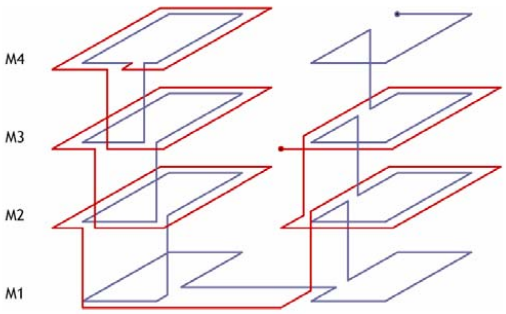


Figure 5 Modified miniature 3-D inductor.

Figure 5 shows a photograph of the modified miniature 3-D inductor, the size is 98 µm x 98 µm. The modified miniature 3-D saves about 75% area with respect to conventional spiral inductor with the same inductance. Figure 6 shows the results of the measures. The modified miniature 3-D inductor has the larger inductance due to magnetic flux, but it also suffers from low quality factor.

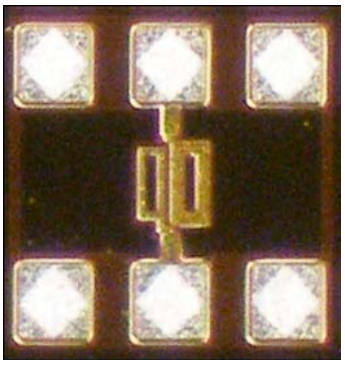


Figure 6 Photograph of the modified miniature 3-D inductor.

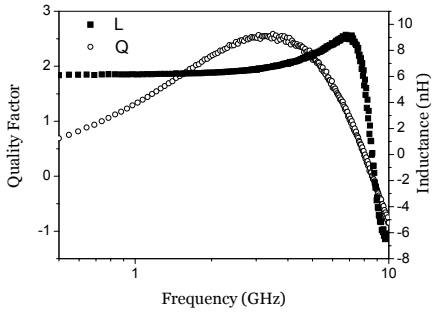
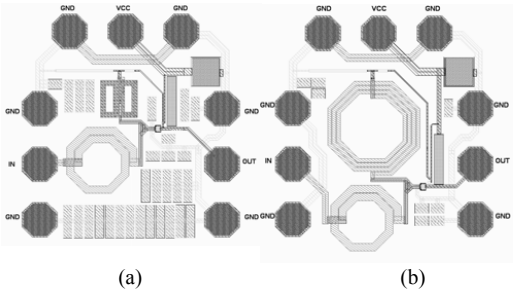


Figure 7 Measurements of the modified miniature 3-D inductor.

IV. Experimental Results

The final wideband LNA layout is shown in Figure 8 (a). The total chip size is 580 µm × 600 µm. The amplifier draws 5.1 mA from a 3.3-V supply. The proposed technique achieves a 40% of area reduction with minor performance degradation over the same circuit implemented with conventional inductors (Figure 8 (b)).



(a) (b)

Figure 8 (a) Layout with modified miniature 3-D inductor. (b) Layout with typical Spiral inductor.

The layout has been implemented for the AMS SiGe 0.35 µm BiCMOS process. The circuit was designed to be measured on wafer with a probe station. As depicted in Figure 8 the probe pads were octagonal, optimized for RF, and three ground-signal-ground (GSG) pad structures with 150 µm pitch were used.

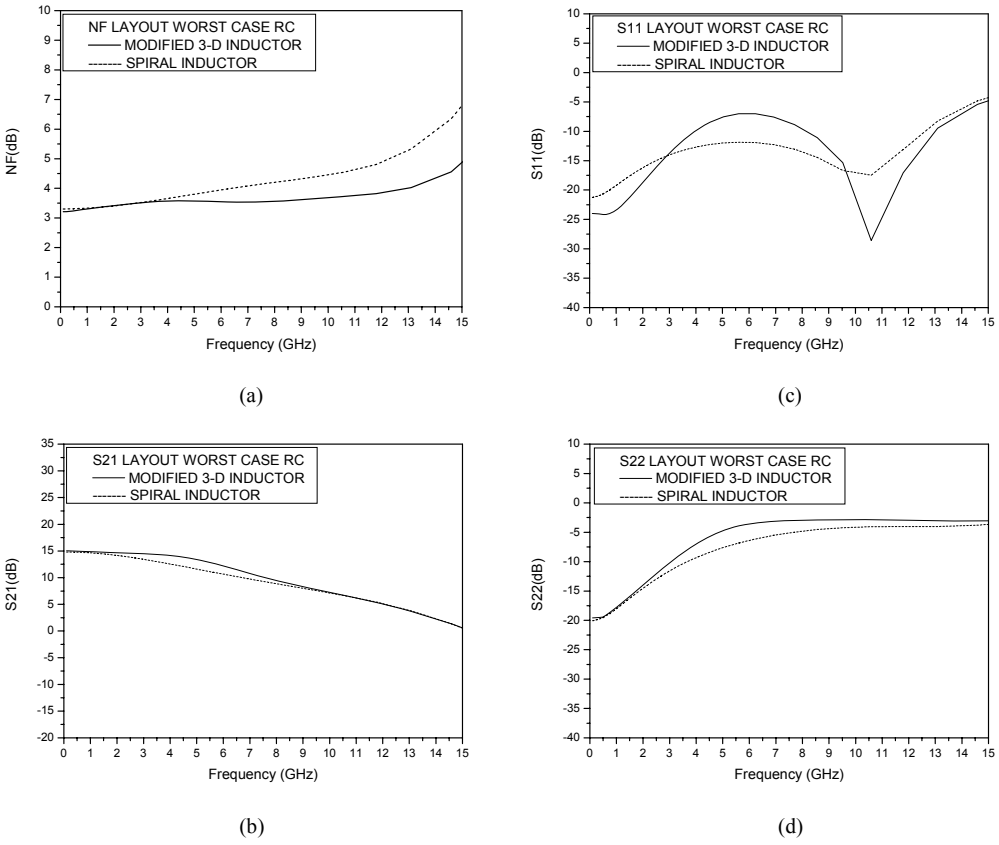


Figure 9 Post-layout results.

The layout verification and parasitics extraction were made with ASSURA. Figure 9 shows the results of the circuits. The circuit with the modified miniature 3-D inductor provides a worst case gain which varies from 15 to 7 dB in the band between 3.1 to 10.6 GHz (Figure 9 (b)), being greater than 1 dB from 0.1 to 15 GHz. The flat gain response indicates that no excessive peaking was required to obtain the desired bandwidth. Figure 9 (c) and Figure 9 (d) show the input and output return loss of the wideband amplifier, and Figure 9 (a) shows the noise figure.

Table I shows the results obtained with both the circuit with spiral inductor and the circuit with modified miniature 3-D inductor. The results obtained with both circuits are similar. The main improvement is the reduction of the area.

TABLE I
RESULTS OBTAINED WITH BOTH CIRCUITS

	With spiral inductor	With modified miniature 3-D inductor
NF_{max} (dB)	4.5	3.7
S_{21max}(dB)~S_{21min}(dB)	13~7	15~7
S_{11max} (dB)	-11	-7
S_{22max} (dB)	-4	-2
$P_{1dB\ at\ 6\ GHz}$ (dBm)	-9.9	-14.86
Effective area (µm^2)	490x355	330x310

V. Conclusions

In this paper we propose a modified miniature 3-D inductor to implement a fully-integrated feedback wide band amplifier. A description of the LNA configuration was explained emphasizing the influence of the design parameters in the circuit performance. The circuit was implemented in a standard low cost 0.35 µm process and provides a worst case gain that ranges from 15 to 7 dB in the band between 3.1 to 10.6 GHz. The noise figure ranges from 3.2 to 3.7 dB in the same band. The circuit only requires 5 mA from a 3.3-V supply. The modified miniature 3-D inductor saves about 75% area with respect to conventional spiral inductor with the same inductance.

References

[1] FCC, "Revision of Part 15 of the Commission's Rules Regarding Ultra-Wideband Transmission Systems" FCC 02-48, First Report and order, 2002.

[2] MB OFDM Alliance-SIG, "Multiband OFDM Phisical Layer Proposal for IEEE 802.15 Task Group 3a", Sept, 2004.

[3] R. Roovers, D. M. W. Leenaerts, J. Bergervoet, K. S. Harish, R. C. H. van de Beek, G. van der Weide, H. Waite, Y Zhang, S. Aggarwal, and C. Razzell, "An Interference-Robust Receiver for Ultra-Wideband Radio in SiGe BiCMOS Technology", IEEE Journal of Solid-State Circuits, vol. 40, no. 12, Dec 2005.

[4] A. Ismail and A. Abidi, "A 3.1 to 8.2 GHz direct conversion receiver for MB-OFDMUWB communication," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, San Francisco, CA, 2005, pp. 208–209.

[5] B. Razavi et al., "A 0.13 µm CMOS UWB transceiver," in IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers, San Francisco, CA, 2005, pp. 216–217.

[6] R. Pulido, H. García, J. del Pino, S. L. Khemchandani, A. Hernández, "A Feedback Wideband LNA for UWB Applications" XXI Design of Integrated Circuits and Systems Conference, 2007.

[7] Aportaciones al diseño, simulación, caracterización y modelado de inductores integrados sobre silicio / tesis doctoral presentada por Amaya Goñi Iturri ; dirigida por el Dr. D. Antonio Hernández Ballester, codirigida por el Dr. D. Francisco Javier del Pino Suárez (2007)

[8] Chih-Chun Tang, Chia-Hsin Wu, Shen-Iuan Liu, "Miniature 3-D Inductors in Standard CMOS Process" IEEE Journal of Solid-State Circuits, Vol. 37, Nº. 4, 2002.

Title	Design of a Fully Integrated DC to 8.5 GHz Distributed Amplifier in CMOS 0.35
Authors	G. Martín R. Díaz J. del Pino S.L. Khemchandani A. Hernández
Conference	XXI Conference on Design of Circuits and Integrated Systems
Date	November 2006

Design of a Fully Integrated DC to 8.5 GHz Distributed Amplifier in CMOS 0.35

G. Martín, R. Diaz, J. del Pino, S. L. Khemchandani, A. Goñi, A. Hernández

A*bstract*—A fully-integrated Distributed Amplifier was implemented in a standard 0.35 µm CMOS process up to 10 dB of gain and a bandwidth of 8.6 GHz. Octagonal inductors with no ground shield were implemented in top available metal. Design guidelines for optimizing amplifier gain are presented. Chip dimensions are 0.75 × 1 mm^2 and power dissipation is 107 mW, drawn from a 3.3 V supply.

***Index Terms*—Radio-frequency (RF) Integrated Circuit, Distributed Amplifier, Spiral Inductor, Ultra Wide Band.**

I. Introduction

The need for devices that can deliver large amounts of power without sacrificing any bandwidth has inspired researchers to develop fancy semi-compound technologies (GaAs, InP, GaN and others). One disadvantage of such technologies is the relatively high cost of integration, when compared with standard CMOS substrates. CMOS devices on the other hand, exhibit relatively low speed and passive structures with much lower quality factors, due to the lossy substrate [1]. This problem can be overcome by using a high resistivity substrate, but this usually adds more complexity and cost to the overall process. It is in the context of an SOC solution that researchers have continued their effort to demonstrate that CMOS can be used as an alternative to conventional microwave solutions.

The use of distributed amplification is proposed in this paper to push the limit of operation of an old technology (0.35 µm CMOS) to 8.6 GHz with possible applications to Ultra Wide Band (UWB) systems.

The organization of this paper is the following. In section II we present the distributed amplifier basics. Sections III is devoted to the distributed amplifier and integrated inductors design methodology. The results of the designed circuit are presented in section IV, where the layout design issues are also addressed. Finally some conclusions are given.

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II. Distributed Amplifier Basics

The frequency response of a MOS device degrades due to the pole formed by the input/output capacitance of the transistor and the resistance it sees. The MOSFET's transconductance rapidly falls with frequency and any attempt to increase the transconductance by increasing the size of the device will also increase its input/output capacitance. Thus, while low-frequency gain has been increased, the gain-bandwidth product remains about the same.

The gain-bandwidth product limits conventional circuit design to approximately 40% of the device's f_{max}.

The concept of distributed amplification has been around for over a half century [2][3]. Distributed amplifiers employ a topology in which the gain stages are connected such that their capacitances are separated, yet the output currents still combine in an additive fashion (Fig. 1). Series-inductive elements are used to separate capacitances at the inputs and outputs of adjacent gain stages. The resulting topology, given by the interlaying series inductors and shunt capacitances, forms what is essentially a lumped-parameter artificial transmission line. The additive nature of the gain dictates a relatively low gain; however, the distributed nature of the capacitance allows the amplifier to achieve very wide bandwidths.

Distributed amplification overcomes the gain bandwidth limitation absorbing the MOS input/output capacitance as part of the lumped elements of the artificial transmission line, formed with the series inductance that connects adjacent drains and gates.

As the amplified signals at each stage travels towards the load, the signal gets attenuated due to non-zero losses associated with the transmission lines. Finite Q inductors are the primary source of losses in the gate line. Losses in the drain line can be attributed to lossy inductors L_d and the drain-source resistance (r_{ds}).

The characteristic impedance (Z_0) and cut-off frequency (f_c) of lossless transmission line are given by

$$Z_0 = \sqrt{\frac{L}{C}} \tag{1}$$

$$f_c = \frac{1}{\pi\sqrt{LC}} \tag{2}$$

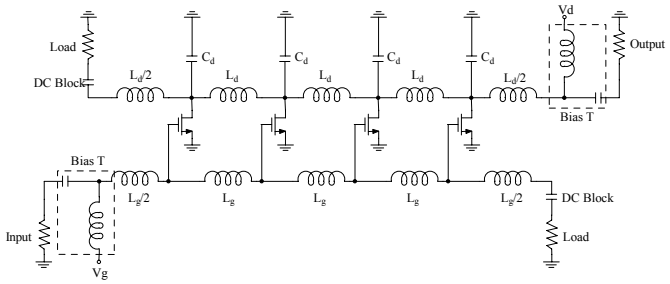

Fig. 1. Basic Distributed Amplifier schematic.

For having the same Z_0 and f_c, the capacitance and inductance on both the drain and gate lines should be the same. For a MOSFET C_{db} is usually less than C_{gs}, hence a capacitor C_d is added in shunt to the drain to make the capacitances equal.

$$L_g = L_d = L \tag{3}$$

$$C_{gs} = C_{db} + C_d = C \tag{4}$$

The gain of the DA can now be expressed as

$$A = gm \frac{Z_0}{2\sqrt{1-\left(\frac{f}{f_c}\right)^2}} \frac{e^{-N\frac{(A_g+A_d)}{2}} \sinh\left(N\frac{A_d - A_g}{2}\right)}{\sinh\left(\frac{A_d - A_g}{2}\right)} \tag{5}$$

where A_d and A_g are the attenuation of the drain and gate lines. gm is the transconductance of the MOSFET and N is the total number of stages. This equation assumes the following:

- Unilateral MOSFET model (ignores C_{gd})
- Image impedance matched terminations
- Equal gate and drain phase velocities

The optimum number of stages that maximizes the gain is simply a function of gate and drain line attenuation. As the signal propagates along the gate line towards the termination, less signal is available for each MOSFET because of attenuation. Hence, the overall gain degrades with further increase in the number of stages. Unfortunately, the optimum number of stages cannot be easily obtained since the gate and drain line attenuations are complex functions and depend on the specific MOSFET parameters and also on the operating and cut-off frequencies. The number of stages for this work is chosen as 4 which was found to be optimum in [5][6][7].

Knowing the gain, number of stages, and drain-line inductance and capacitance, the required gm can be found from the low frequency gain of (5)

$$gm = \frac{2 \cdot A}{N}\sqrt{\frac{C_d}{L_d}} \Rightarrow gm = \frac{2 \cdot A}{N \cdot Z_0} \tag{6}$$

Then, the W/L ratio can be derived from

$$\frac{W}{L} = \frac{gm}{\mu_n C_{ox}\left(V_{gs} - V_T\right)} \tag{7}$$

Finally, the device length and width can be found by combining the above equation with the following expression

$$W \cdot L = \frac{C_g}{C_{ox}} \tag{8}$$

III. Distributed Amplifier Design

Following the guidelines outlined in the previous section a distributed amplifier for a cutoff frequency of ~ 10GHz, and a voltage gain of ~8 dB was designed in a 0.35 μm technology.

One of the difficulties in realizing a fully integrated distributed amplifier is creating the high-quality inductors necessary. On-chip spiral inductor parameters from full-wave electromagnetic simulations are used to simulate accurate artificial transmission line. A commercially available planar EM simulator (Momentum©) was used to predict the broadband response of inductors in lossy silicon substrates [8].

TABLE I
INDUCTOR GEOMETRICAL PARAMETERS

	s (μm)	*n*	*r* (μm)	*w* (μm)
L1	2	2.5	100	16
L2	2	2	100	16

Fig. 2 shows the simulated quality factor and inductance of L_d=L_g inductors (see L1 in Table I). As it can be shown this inductor presents a Q and an L of 9.8 and 1.4 nH, respectively, at 10 GHz. In the same way Fig. 3 shows the simulated quality factor and inductance of the $L_d/2$=$L_g/2$ inductors (see L2 in Table I). In this case the Q and L are 11.4 and 1 nH, respectively, at 10 GHz. Although this inductor does not have half the inductance than L_d=L_g, its physical layout perfectly match with the other components in the design. Note that in such layouts, any non modelled element would imply a bad operation of the overall circuit. As it can be shown later, this issue is more important than the inductance value.

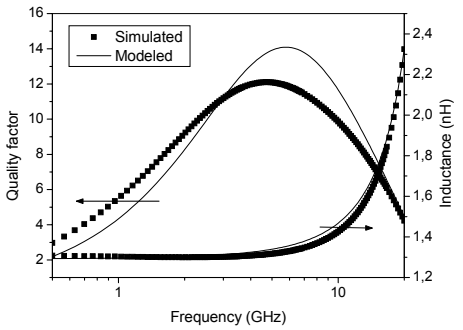

Fig. 2. Simulated and modelled Quality Factor and Inductance for $L_d=L_g$.

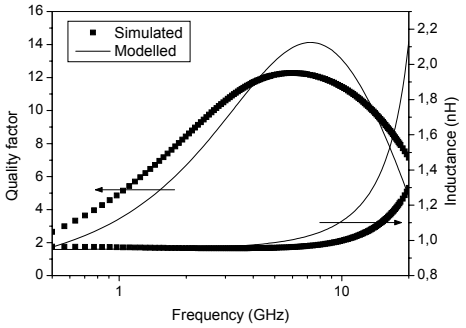

Fig. 3. Simulated and modelled Quality Factor and Inductance for $L_d/2=L_g/2$.

Both inductors were modeled using the well known pi model [9] in order to take into account its behavior in the schematics and layout simulations.

After making minor adjustments based on initial simulations, the resulting schematic, with initial component values, is shown in Fig. 4. This schematic includes the modeled inductors and also the corresponding subcircuits to take into account the effect of the pads. Note that additional capacitance has been added to the drain line to provide the required value.

Higher gain can be obtained by choosing higher characteristic impedance of gate and drain lines but the cutoff frequency will be lower, which will limit the bandwidth. On the contrary, wider bandwidth can be obtained with the tradeoff for gain. In order to investigate the tradeoffs between the gain and bandwidth with respect to the device size and drain capacitance line, two designs were simulated. The first one (DA1) utilizes a transistor size of 260 μm (equivalent to a 13 gates device with 10 μm gate width) and a capacitance C_d of 150 fF. The second one (DA2) is designed for lower frequency and higher gain with a transistor size of 380 μm (equivalent to a 19 gates device with 10 μm gate width) and a capacitance C_d of 198 fF. The frequency response of both circuits is shown in Fig. 5.

To this point, the simulated results correlate well with conventional theory, however, with the introduction of layout parasitics this will no longer hold true.

IV. Results and Discussions

Fig. 6 shows the layout of the complete distributed amplifier DA1. The circuit occupies an area of 0.75 × 1 mm^2, which include the pad frame. Due to very high frequency operation, special attention should be paid to the layout [4]. Thus, enough design accuracy can be achieved by adding accurate high-Q inductor model and optimizing parasitic effects coming from discontinuity and interconnection.

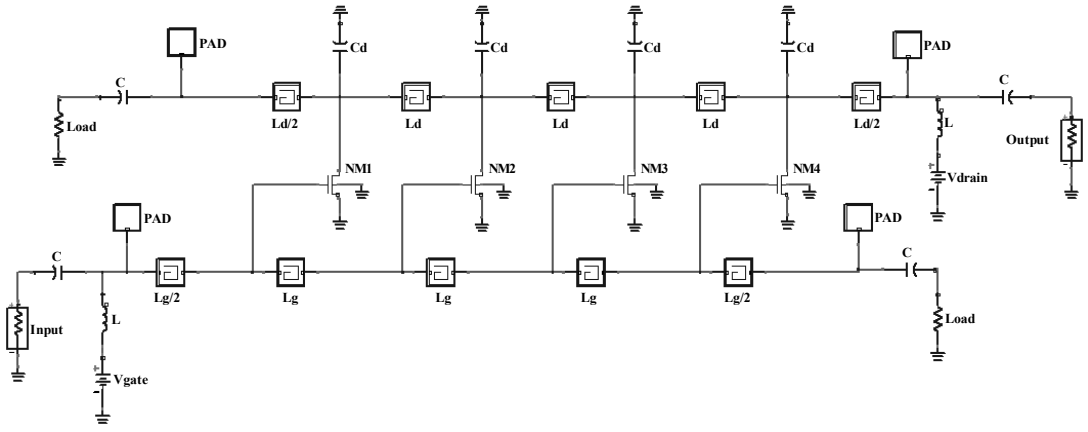

Fig. 4. Distributed Amplifier schematic.

The post-layout frequency response of the distributed amplifier is shown in Fig. 7. The gain is 8.5 dB with ± 1.2 dB flatness from 1 GHz to 5 GHz and the unity gain frequency is 8.6 GHz. The input and output match are generally much better than -10 dB over most of the bandwidth. The increase in gain in low frequency was due to the higher impedance of the blocking capacitance at low frequency. All simulations were taken under identical DC bias conditions, 3 V on the drain line and 0.8 V on the gate line; at this bias point the distributed amplifier consumed 35.64 mA for a total power dissipation of 107 mW. The phase response of this circuit is shown in Fig. 8. Result shows linear variation up to cutoff frequency.

In Fig. 9 the schematic and post-layout simulations are compared. As warned in the previous section, with the introduction of layout parasitics the simulated results differ with schematic simulations. In particular the bandwidth is reduced due to the capacitance added to the gate and drain artificial transmission lines by the routing metals. As a consequence special care should be taken on the routing metals and on the inductor layout in order to maximize the circuit performance. This is the motivation of using a $L_d/2=L_g/2$ inductors that do not have half the inductance than $L_d=L_g$ but that hold a physical layout which match with the other components in the design.

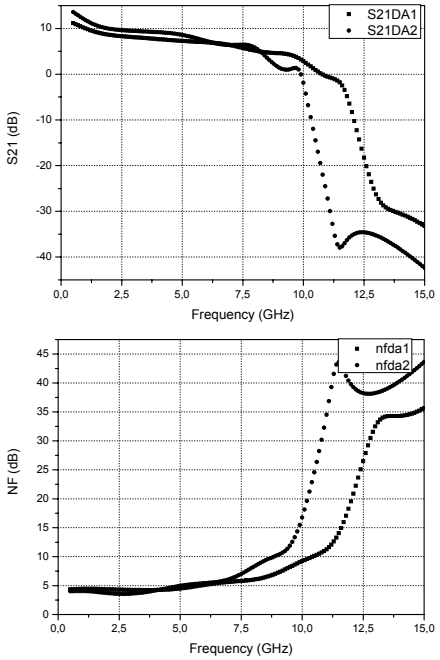

Fig. 5. The tradeoffs between the gain and bandwidth with respect to the device size and drain capacitance line. DA1: W=260 μm (ng=13), cd=150 fF and DA2 W=380 μm (ng=19), cd=198 fF.

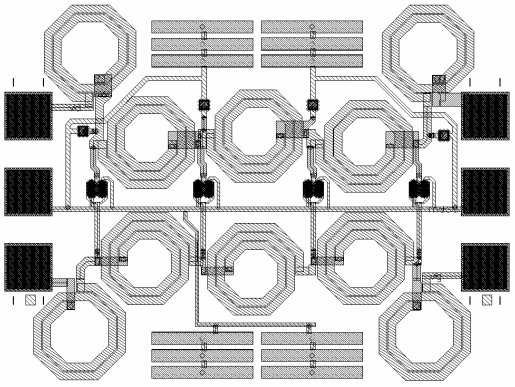

Fig. 6. Distributed Amplifier layout.

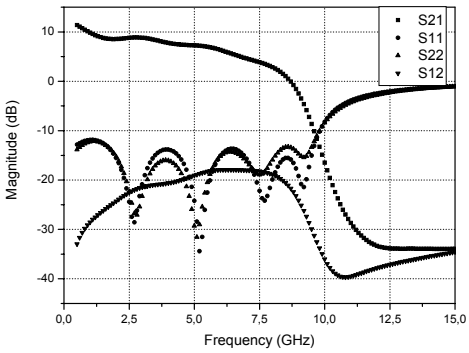

Fig. 7. Distributed amplifier post-layout S-parameter response.

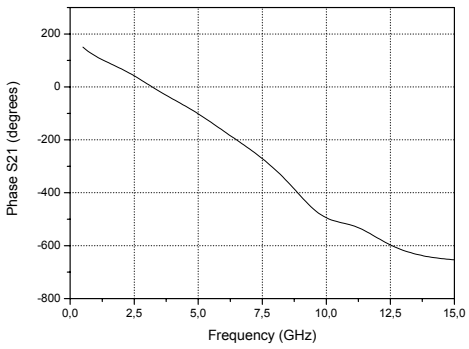

Fig. 8. Distributed amplifier post-layout phase response.

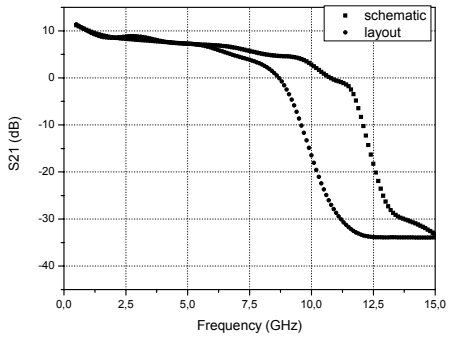

Fig. 9. Comparison between schematic and post-layout simulations.

V. CONCLUSIONS

A four-stage fully integrated CMOS distributed amplifier with 8.5 dB forward gain and 1.2 dB gain flatness over a 4 GHz bandwidth was implemented. Distributed Amplification opens the possibility for CMOS circuits to be considered as an alternative microwave solution and pushes the limit of operation of an old technology (0.35 μm CMOS) to 8.6 GHz. Since this DA was designed using a commercial CMOS technology, it can be easily integrated with other front-end circuits to build CMOS transceivers without requiring any post-processing steps.

REFERENCES

[1] Brian M. Ballweber, Ravi Gupta and David J. Allstot, "A Fully Integrated 0.5–5.5-GHz CMOS Distributed Amplifier" IEEE TRANSACTIONS ON SOLID-STATE CIRCUITS, VOL. 35, NO. 2, FEBRUARY 2000.

[2] E. L. Ginzton, W. R. Hewlett, J. H. Jasberg, and J. D. Noe, "Distributed amplification," Proc. IRE, vol. 36, pp. 956–969, Aug. 1948.

[3] W. S. Percival, "Thermonic valve circuits," British Patent 460 562, Jan. 25, 1937.

[4] Jinho Park, Kiyong Choi, and David J. Allstot "Parasitic-Aware RF Circuit Design and Optimization" IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 51, NO. 10, OCTOBER 2004.

[5] Y. Ayasli, R.L. Mozzi, J.L. Vorhaus, L D. Reynolds and R.A. Pucel, "A Mono-lithic GaAs 1-13 GHz Traveling-Wave Amplifier," IEEE Transactions on Mi-crowave Theory and Techniques, vol. 30, pp. 976–981, July 1982.

[6] Michael Ross, Investigation of Taper and Forward-Feed in GaAs MMIC Dis-tributed Amplifiers, M.E. thesis, Department of Electronics, Carleton University, June 1987.

[7] J.B. Beyer, S.N. Prasad, R.C. Becker, J.E. Nordman, and G.K. Hohenwarter, "MESFET Distributed Amplifier Guidelines," IEEE Transactions on Microwave Theory and Techniques, vol. 32, pp. 268–275, July 1984.

[8] *Momentum User's Manual*, 2004A ed., Agilent Technologies, Sept. 2004.

[9] A. Goni-Iturri S. Khemchandani, J. del Pino, J. García, B. González and A. Hernández, "Design and Modeling of an on Silicon Spiral Inductor Library Using Improved EM Simulations", SPIE's International Symposium on Microtechnologies for the New Millennium 2005 (VLSI Circuits and Systems, Sevilla, 2005.

C

Other Publications

A list of journals and conference contributions related to other works are listed in this appendix.

Journal Papers

1. Sunil L. Khemchandani, Javier del Pino, Roberto Díaz and Antonio Hernández, "A fully Integrated Single Core VCO with a Wide Tunning for DVB-H", Microwave and Optical Technology Letter, Vol. 51, Ed. Wiley, Mar 2009.

2. S.L. Khemchandani, J. del Pino Suárez, Amaya Goñi-Iturri, Roberto Díaz and Antonio Hernández, "A VCO with On-Chip Tank for IEEE 802.11a", Microwave and Optical Technology Letter, Vol. 50, Num 10, Ed. Wiley, Oct. 2008.

Conference Papers

3. H. García-Vázquez, K. Orbaiceta-Ezcurra, S.L. Khemchandani, R. Díaz, J. Arias, J. del Pino, "Analysis of Package Effects on an UWB Feedback LNA", XXVI Design of Circuits and Integrated Systems Conference (DCIS), Albufeira, Portugal, Nov. 2011.

4. R. Díaz, G. García-Saavedra, J. Arias-Pérez, S.L. Khemchandani, J. del Pino, "A Current Conveyor Based Mixer for an UltraWide Band Receiver", XXV Design of Circuits and Integrated Systems Conference, Lanzarote, Spain, Nov. 2010.

5. R. Díaz, A. Castillo, H. García, D. Ramos and S. L. Khemchandani, "Low Power Consumption Mixer Based on Current Conveyors for Wireless Systems",XXIV Conference on Design of Circuits and Integrated System, Zaragoza España, Nov. 2009.

6. G. Perez, S. L. Khemchandani, R. Díaz, R. Pulido, D. Ramos and J. del Pino, "A Multiband LNA Switched Loads and Wideband Input Matching",XXIV Conference on Design of Circuits and Integrated System, Zaragoza España, Nov. 2009.

7. J. del Pino, R. Díaz, M. Afonso, F. Cabrera, A. Iturri, S. L. Khemchandani, "A Fully Integrated Folder Mixer in CMOS 0.35 μm Technology for 802.11a WiFi Applications", SPIE Conferece on Microtechnologies for the New Millenium, Las Palmas de Gran Canaria – España, May 2007.

8. J. Pérez, N. Barrera, R. Díaz, R. Pulido, J. del Pino, S. L. Khemchandani and A. Hernández, " A SiGe Front-End for a Portable DVB-H Receiver", XXII Conference on Design of Circuits and Integrated System, Sevilla – España, Nov 2007.

9. R. Pulido, S.L. Khemchandani, A. Goñi-Iturri, R.Díaz, A. Hernández and J. del Pino, "A Fully Integrated Low Noise Amplifier in SiGe 0.35 μm Technology for 802.11a WiFi Applications", SPIE Conferece on Microtechnologies for the New Millenium, Sevilla – España, Nov. 2005.

10. R. Díaz, R. Pulido, A. Goni-Iturri, S.L. Khemchandani, B. González, J. del Pino,"A fully Integrated Mixer in CMOS 0.35 μm Technology for 802.11a WiFi Applications", Conference on Design Circuits and Integrated Systems, Burdeos – Francia, Nov 2004.