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Editorial
Embedded Systems for Portable and Mobile Video Platforms

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Video processing and coding systems are assuming an increasingly important role in a wide range of applications. These include personal communications, wireless multimedia sensing, remote video surveillance, and emergency systems, to name but a few. In such a diverse set of application scenarios, there is a real need to adapt the video processing in general, and video encoding/decoding in particular, to the restrictions imposed by both the envisaged applications and the terminal devices. This is particularly true for portable and battery-supplied devices, in which low-power considerations represent significant challenges to real deployment. The development of novel power-efficient encoding algorithms and architectures suitable for such devices is fundamental to enable the widespread deployment of next generation multimedia applications and wireless network services.

In fact, state-of-the-art implementations of handheld devices for networked electronic media are just one perspective on the actual real challenges posed by the growing ubiquity of video processing and coding on mobile devices. Significant challenges also exist in mapping processing systems developed for fading, noisy, and multipath band-limited transmission channels onto these same devices. Similarly, the requirements for scalable coding associated with networked electronic media also raise issues when handheld mobile devices are considered. A clear need therefore exists to extend, modify, and even create new algorithms, design techniques, and tools targeting architectures and technology platforms as well as addressing scalability, computational load, and energy-efficiency considerations.

The challenge of providing solutions to the requirements of the envisaged application scenarios in terms of image quality and bandwidth is well addressed by new video compression standards, such as the AVC/H.264 joint ITU-ISO/MPEG standard or the upcoming SVC standard. Unfortunately, such high performance is achieved at the expense of an even higher increase in codec complexity. To address all these challenges outlined above, all elements of the solutions have to be addressed, from the encoding algorithms themselves, seeking the best performance-complexity tradeoffs, right down to the design of all architectural elements that need to be conceived and developed with power-efficiency criteria during the design phase. Considering these challenges, this special issue targets to illuminate some important ongoing research in the design and development of embedded systems for portable and mobile video platforms.

For the special issue, we received 13 submissions covering very different areas of expertise within this broad research agenda. After an extremely rigorous review process, only 5 were finally accepted for publication. These 5 papers focused on efficient video coding methods, power-efficient algorithms and architectures for motion estimation and discrete transforms, tools for automatically generating RTL descriptions of video cores, and thermal-aware scheduler algorithms for future on-chip multicore processors. Collectively, we strongly believe that without the pretension of being exhaustive, they represent a "snapshot" of the current state of the art in the area in that they constitute a representative selection of ongoing research.

In a paper entitled "Low-complexity multiple description coding of video based on 3D block transforms", Andrey Norkin et al. present a multiple description video compression scheme based on three-dimensional transforms, where two balanced descriptions are created from a video sequence. The proposed coder exhibits low computational complexity

and improved transmission robustness over unreliable networks.

In paper "Energy-efficient acceleration of MPEG-4 compression tools", Andrew Kinane et al. present some novel hardware accelerator architectures for the most computationally demanding algorithms of MPEG-4 encoding, namely motion estimation and the forward/inverse discrete-cosine transforms, integrating shape-adaptive modes in each of these cases. These accelerators have been designed using general low-energy design approaches both at the algorithmic and architectural levels.

An application-specific instruction set processor (ASIP) to implement data-adaptive motion estimation algorithms is presented by Tiago Dias et al. in a paper entitled "AMEP: adaptive motion estimation processor for autonomous video devices". This processor is characterized by a specialized datapath and a minimum and optimized instruction set, and is able to adapt its operation to the available energy level in runtime, and is thus a suitable framework in which to develop motion estimators for portable, mobile, and battery-supplied devices.

Kristof Denolf et al. consider the design methodology itself, and in their paper entitled "A systematic approach to design of low power video codec cores", describe how a memory and communication-centric design methodology can be targeted to the development of dedicated cores for embedded systems. This methodology is adopted to design an MPEG-4 simple profile video codec using both FPGA and ASIC technologies.

K. Stavrou and P. Trancoso take a different perspective and analyze the evolution of thermal issues for future chip multiprocessor architectures in a paper entitled "thermal-aware scheduling for future chip multiprocessors". They show that as the number of on-chip cores increases, the thermal-induced problems will worsen. In order to minimize or even eliminate these problems, thermal-aware scheduler algorithms are proposed and their relative efficiency is quantified.

In conclusion, we hope that you will enjoy this special issue and the range of topics covered in this important area.

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