Single Event Transient Mitigation Techniques for CMOS Integrated Frequency Synthesizers

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***Abstract*— Single event transients (SETs) in analog integrated circuits result from the interaction of a heavy ion or high- energy proton with a sensitive p-n junction. SETs induce electron-hole pairs that can lead to current spikes, which propagate through the integrated circuit and can result in substantial transient peaks at the output voltage. This paper proposes techniques to mitigate SETs and SEU in CMOS frequency synthesizers without affecting circuit specifications. RHBD techniques are applied to redesign the blocks of the frequency synthesizer.**

Keywords-components; Radiation, Current pulse, Single Event Transients (SET), Single Event Upset (SEU), Radiation-Hardening-By-Design (RHBD), Voltage Controller Oscillator (VCO), High-Speed Divider, CMOS

I. INTRODUCTION

Currently space radiation has taken more attention due to the scalability of the electronic systems design with CMOS technology. An electronic device must often operate in environments with a significant presence of ionizing radiation, however a high energetic particle can cause systems crashes or threat the operation of electronic devices. The high-energy ionizing particles can produce three radiation effects, which are Total Ionizing Dose (TID), Displacement Damage Dose (DDD) and Single Event Effects (SEE).

The SEEs can be classifying in two main groups, the soft and hard effects. The first one may be recovered by a reset, a power cycle or a rewrite of the information and the second one are non-recoverable errors [1]. The Single Event Transients (SETs) happens when it produces a voltage glitch in circuits due of a single ion and it is considered as a soft effect. The Single Event Upset (SEU) happens in memories (SRAMs) and sequential logic such as registers implemented with flip-flops [2].

In this paper, several Radiation-Hardening-By-Design (RHBD) techniques are presented. The paper is organized as follows. Section II describes the model used for the simulation of the particle strike. Section III describes the modeling of SET and the analysis of SET in the synthesizer and finally, section IV provides some conclusions.

II. SINGLE EVENT TRANSIENT MODELING

To study of SETs in frequency synthesizers, a double exponential function was used to model the induced transient current by the particle strike [3] where *tr* is the rise time, *tf* is the fall time and *Q* is the collected charge.

$$I_{SET} = \frac{Q}{tf - tr} \cdot \left(e^{\frac{-t}{tf}} - e^{\frac{-t}{tr}} \right) \qquad (1)$$

The amount of collected charge to perform the simulation experiments ranges from several hundreds of fC up to 1200 fC, which are expected values for CMOS technology. Typically, rise times in the injected current pulse are in the order of tens picoseconds and increase almost linearly with increasing LET (*Linear Energy Transfer*), while fall times are in the order of hundreds of picoseconds [4], [5]. The simulated cases are shown in Table 1.

Table 1. *Current pulse parameters*

tr (ps)	tf (ps)	Q (fC)	LET, d=2 µm (MeV·cm^2/mg^{-1})
50	200	300	14.47
50	200	525	25.31
100	400	501	24.16
100	400	801	38.62
100	400	990	47.74
100	400	1200	57.86

To calculate the LET the expression used was:

$$LET = \frac{Q \cdot 3{,}6}{e \cdot \rho_{si} \cdot d} \qquad (2)$$

where *e* is the electron charge, ρ_{Si} is the silicon density and *d* is the sensitive depth of the charge collection. These pulses were being modelling in the software Advanced Design System (ADS) [6] to run the simulations in the circuitry. Fig. 1 shows the current pulse shape used for the different cases.

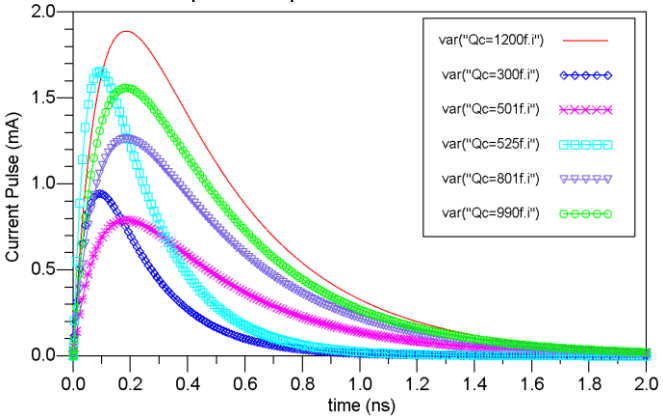

Fig. 1*. Current pulse shapes*

To analyze correctly the effect of the impacts in the synthesizer: phase shift, amplitude variation and recovery time are simulated. These magnitudes can be seen in Fig. 2. However, the amplitude variations were not considered because they were negligible.

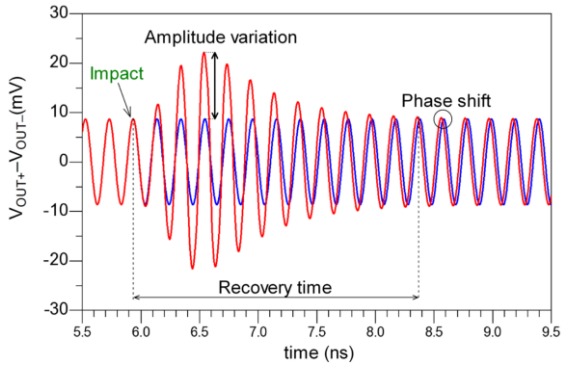

***Fig. 2**. Simulation results when a SET is applied*

III. RHBD TECHNIQUES

To improve the VCO tolerance to SETs, RHBD techniques were used. The VCO schematic with RHBD techniques is shown in Fig. 3. Resistors R7, R5 and capacitor C4 were included to increase the time constant seen from the bias transistors. While SET sensitivity has been improved, phase noise has worsened, not meeting the specifications. To improve the phase noise, we have increased the amplitude of oscillation, adding a capacitive divider (C14-C17). The combination of both techniques results in a substantial improvement on the performance of the RHBD-VCO in comparison to the unhardened design when a SET strikes one of its sensitive nodes, while still meeting the standard specifications

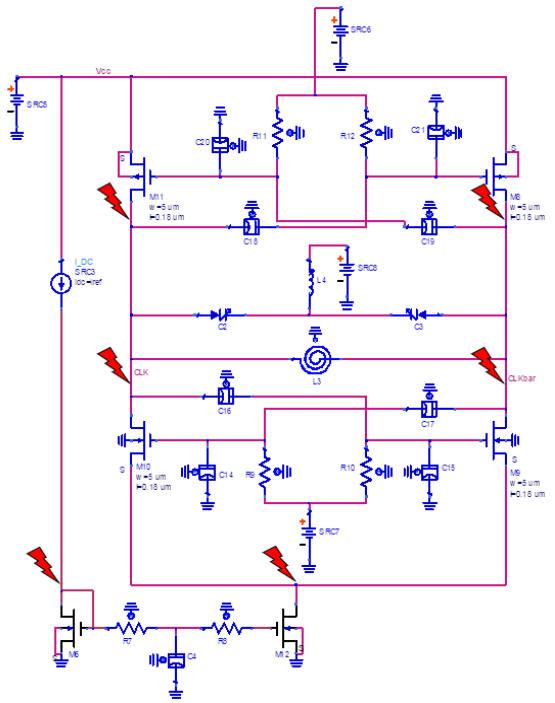

***Fig. 3.** VCO with RHBD schematic*

Regarding to RHBD techniques for the high speed divider, a Gated Feedback Cell (GFC) was used [8]. This technique is based in adding local redundancy to the circuity duplicating the latch stage to prevent the stored data passing to other parts of the circuit (see Fig. 4). At the output of the high-speed divider, a combination logic is added to secure the transmission of the data in the circuit. This combination logic was implemented with OR and AND gates. Furthermore, an increase of the time constant adding and RC network to the bias transistors was also used. This can be shown in Fig. 4 to Fig. 6.

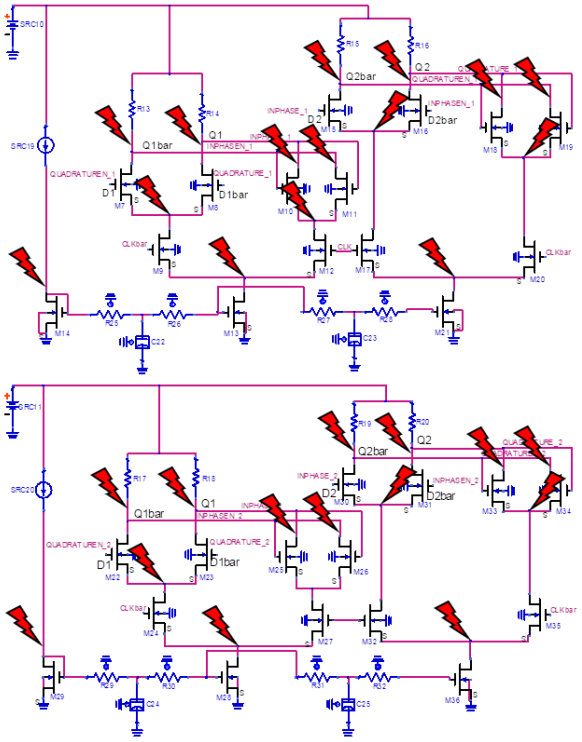

***Fig. 4**. Schematic of the high-speed divider with RHBD technique*

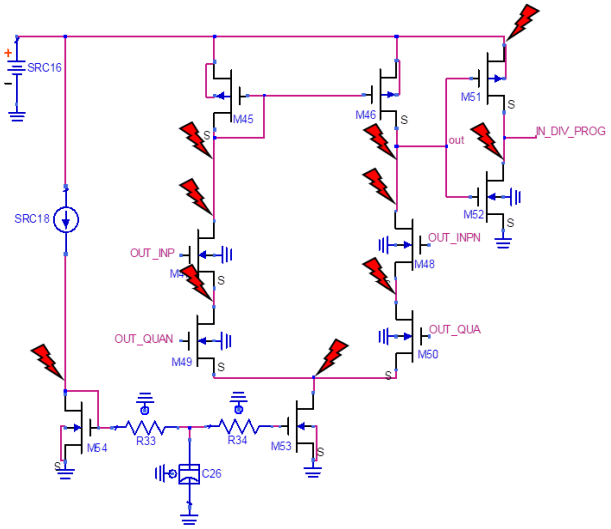

***Fig. 5.** Schematic of programmable divider buffer with RHBD technique*

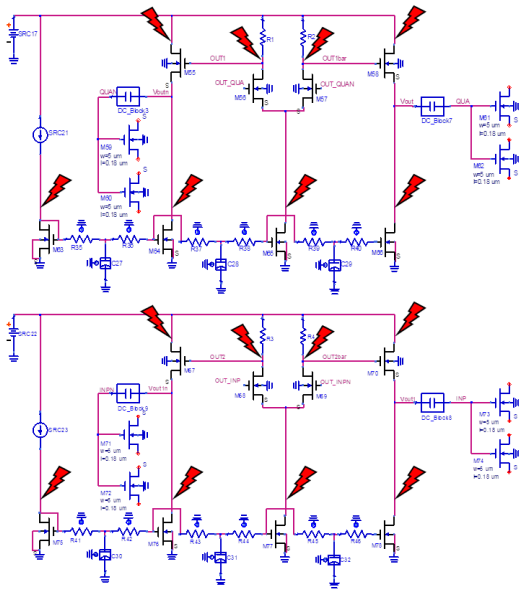

Fig. 6. *Schematic of the mixer buffer with RHBD technique*

IV. Results and Conclusions

In this paper, RHBD techniques have been proposed to minimize the impacts of SETs and SEUs in an integrated VCO and high-speed divider using 180nm CMOS technology. To test the RHBD VCO, current pulses were applied in the selected nodes (see Fig. 3) achieving an improvement by 50% in the phase shift and by 81% for the recovery time. The same procedure was followed with the divider. Simulations with the OR gate show an improvement by 81% for the phase shift and by 34% for the recovery time in the high-speed divider. For the programmable divider buffer, the recovery time improvement is by 80% while in the mixer buffer, the improvement is by 80%. With the AND gate the results are not as good as with the OR gate.

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