Design methology for extensible platforms based on Xilinx ZYNQ 7000 FPGA

Alejandro García Nieto, Antonio Núñez Ordóñez,
Pedro Hernández Fernández, Pedro Pérez Carballo
SICAD Division,
Institute for Applied Microelectronics
Las Palmas de Gran Canaria, Spain
agnieto@iuma.ulpgc.es

Abstract— **The video traffic in the mobile phone networks is growing, being coding/decoding an important factor of the video applications. In this context, the hardware accelerators to codecs are an interesting alternative. The FPGA is a possible solution for implement these accelerators. The configurable SoCs Xilinx ZYNQ 7000 series integrate a FPGA and infrastructure to execute embedded software on a ARM Cortex A9 Processor. The goal of this work is probe the Vivado Design Suite tool for logic synthesis and implementation using a Deblocking Filter H.264/SVC design already developed. Also, the design flow is execute with the Synplify Premier DP for comparing the results between both tools.**

FPGA, ZYNQ 7000, synthesis, logic synthesis, implementation, top-down, bottom-u,p utilization H.264/SVC, Deblocking Filter.

I. INTRODUCTION

Nowadays, video traffic in the mobile phone networks is growing, being the coding/decoding a key aspect of the video applications. Therefore, it is interesting to have hardware accelerators to video coding/decoding. One possibility is the implementation of these accelerators on FPGA. The SoCs Xilinx ZYNQ 7000 serie [1, 2] provide programmable logic to implement the hardware accelerator and infrastructure to embedded software execution.

Xilinx has released the Vivado Design Suite [3] to address the design flow from RTL level to the programming of the FPGA. Furthermore, Vivado Design Suite allows the user to generate an IP block of an own design and use this IP block with other available IP blocks, among others, IP blocks of AXI4 interface or the processing system. Then, it is possible emulate a complete system on chip.

In order to probe the design flow toward the extensible platform Xilinx ZYNQ 7000 by the Vivado Design Suite tool, the logic synthesis and implementation tasks are executed with two synthesis strategies, bottom-up and top-down. The design used is the Deblocking Filter H.264/SVC developed within the research project PCCMUTE [4] from RTL level. For comparison the results the same flow design is executed with the Synplify Premier DP [5] tool.

II. DESIGN REFERENCE ARCHITECTURE

The block diagram of the design is represented in Figure I. It is compound of the following main modules:

- Deblocking Filter H.264/SVC. It is composed by five modules: interface, param_bs, param_clip, luma_core and chroma_core.
- INOUT handler. Manages request related with of Deblocking Filter and read/write transfers.
- Dual Port MEMORY. It is based on BRAMs. Its function is store pixels and other parameters to be used in de DF.
- LocalLink Interface. There are two LocalLink interface, one to receive the frames to be filtered and another to transmit the frames processed.
- Two wrappers, LL2AXI4-Stream slave and master for adapt the LocalLink interface to AXI4-Stream, because the processing system of ZYQ 7000 does not support the LocalLink protocol. The two wrappers have been added in this master thesis project.

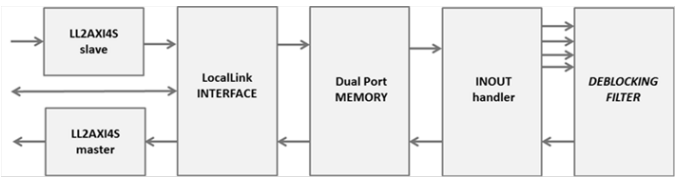

FIGURE I. BLOCK DIAGRAM DESIGN

III. RESULTS

Two synthesis strategies are used: bottom-up and top-down. The top-down strategy in Vivado Design Suite defines some modules as out-of context. Those modules defined as out-of-context are synthesized independently. This reduces the time design but also reduces the quality of results. The constraints guide the implementation of the out-of-context modules. The platform used for the implementation is the

ZYNQ 7000 ZC706 of Xilinx. The resource utilization obtained during the logic synthesis for Vivado and Synplify, for both synthesis strategies, are presented in the Table I.

TABLE I. LOGIC SYNTHESIS UTILIZATION RESULTS

	Vivado		Synplify	
	Bottom-up	Top-down	Bottom-up	Top-down
LUTs	44,785	45,049	34,075	27,043
Registers	64,390	68,275	21,944	17,730
BRAMs	128	128	106	104
DSPs	2	2	3	2

These results in Vivado for both strategies are similar due to with the top-down strategy the out-of-context modules are synthesized regardless other modules of the design. Instead, the results using Synplify Premier DP provides differences between both synthesis strategies. Synplify does not use out-of-context modules in top-down strategy. In respect of the two tools, Synplify uses fewer resources of LUTs and registers and of BRAMs, as is shown in Figure II. Each synthesis tool uses different strategies which produces different results.

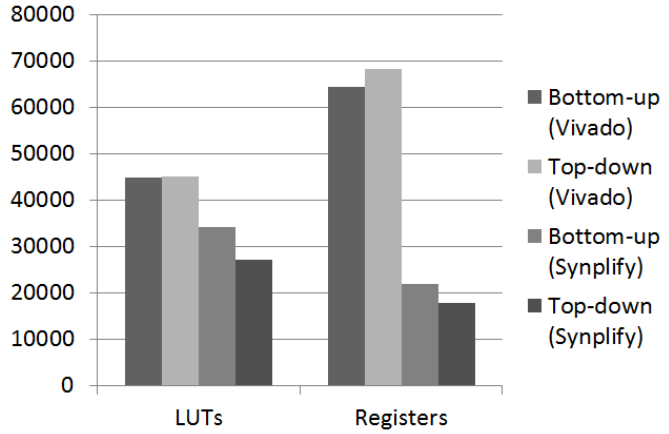

FIGURE II. LOGIC SYNTHESIS UTILIZATION RESOURCES

On the other hand, the resource utilization for Vivado implementations using bottom-up and top-down strategies are similar. Table II shown these results. Synplify Premier DP uses less consumption resources than Vivado Design Suite again. Figure III highlight the difference in resource usage (LUTs and registers) between both tools.

TABLE II. IMPLEMENTATION UTILIZATION RESULTS

	Vivado		Synplify Premier DP	
	Bottom-up	Top-down	Bottom-up	Top-down
LUTs	44,411	43,997	36,182	30,142
Registers	64,278	64,434	21,892	17,730
BRAMs	128	128	106	104
DSPs	2	2	3	2

IV. COMPARATIVE

Finally, the resources used in the implementation done using top-down strategy in PCCMUTE (1) project for the module are compared with the same module implemented using Vivado Design Suite (2) and Synplify Premier DP (3). In PCCMUTE, the design was implemented on Virtex-5 FX70T FPGA using the top-down synthesis strategy. The comparison is presented in Table III.

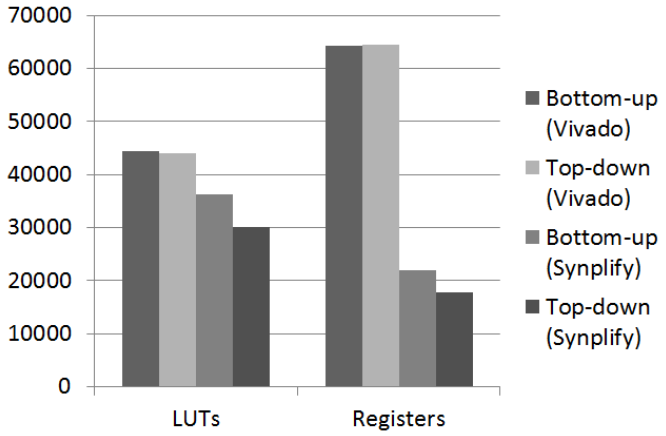

FIGURE III. IMPLEMENTATION UTILIZATION RESOURCES

.

TABLE III. COMPARATIVE OF RESOURCE UTILIZATION OF DEBLOCKIN FILTER FOR PCCMUTE (1), VIVADO (2) AND SYNPLIFY (3) IMPLEMENTATIONS

	LUTs		Registers		BRAMs		DSP	
d_filter	27,192	(1)	18,359	(1)	10	(1)	1	(1)
	39,116	(2)	60,582	(2)	0	(2)	1	(2)
	25,588	(3)	15,909	(3)	8	(3)	0	(3)
ll_interface	336	(1)	414	(1)	0	(1)	0	(1)
	339	(2)	414	(2)	0	(2)	0	(2)
	235	(3)	269	(3)	0	(3)	0	(3)
Inout_handler	6,599	(1)	3,413	(1)	0	(1)	2	(1)
	4,384	(2)	3,392	(2)	0	(2)	0	(2)
	4,244	(3)	1,546	(3)	0	(3)	2	(3)
Memory	2	(1)	0	(1)	96	(1)	0	(1)
	182	(2)	18	(2)	128	(2)	0	(2)
	75	(3)	6	(3)	96	(3)	0	(3)

The frequency constraint was 100 MHz of PCCMUTE. The maximum estimated frequency obtained is 155.7 MHz using top-down strategy using logic synthesis with Synplify Premier DP.

V. CONCLUSIONS

In this work, we have demostrate that the Synplify Premier DP can achieve better utilization resources than Vivado Design Suite. Furthermore, with this tool, the top-down and bottom-up strategies results are similar. The top-down strategy in Vivado provides worse results than Synplify but the design time is lower.

REFERENCES

[1] Xilinx Inc. Zynq-7000 all programmable SoC. Technical reference manual. 2012.

[2] Xilinx Inc. ZC706 Evaluation board for the Zynq-7000 XC7Z045 all programmable SoC user guide. 2013.

[3] Xilinx Inc. Vivado design suite tutorial. hierarchical design. 2014.

[4] P. P. Carballo, O. Espino, R. Neris, P. Hernandez-Fernandez, T. M. Szydzik and A. Nunez. Scalable video coding deblocking filter FPGA and ASIC implementation using high-level synthesis methodology. 2013.

[5] Synopsys Inc. Synopsys FPGA synthesis. user guide. 2014.