A Low-Power Fully Differential Source Compensated VGA for IEEE 802.15.4 Std in CMOS 65 nm

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***Abstract*—This paper presents the implementation of a low-power fully differential VGA for the IEEE 802.15.4 Std in CMOS UMC 65 nm technology. The designed VGA is based on the g_m/I_D methodology achieving a very low power consumption (334 µW). The proposed architecture employs two amplification stages composed by OTAs with negative feedback networks in order to adjust the gain levels from 0 to 43.7 dB in 3 dB steps. In addition, the Miller-Source Compensation technique has been used to improve the GBW product and minimize the use of capacitors in the VGA.**

Keywords-component; Variable Gain Amplifier (VGA), Programmable Gain Amplifier (PGA), CMOS, IEEE 802.15.4, Source Compensation, Miller Compensation, Constant Bandwidth.

I. INTRODUCTION

Thanks to its numerous advantages, CMOS technology continues to be the leading choice in the development of consumer-based electronic devices. Moreover, the market of Wireless Sensor Networks (WSNs) is expected to grow in the next few years as revealed recently in [1]. This implies that a high-volume production of low power, low cost transceivers will take place in the next decade. In order to achieve low power consumption, low complexity and low cost, the IEEE 802.15.4 standard is a more than adequate choice for WSNs applications. This standard defines Low-Rate Wireless Personal Area Networks (LR-WPANs) operating in the 2.4 GHz Industrial, Scientific and Medical (ISM) band and it offers a data rate varying from 20 to 250 kb/s depending on the operating frequency band.

This paper describes the design and implementation of a low-power fully differential CMOS VGA for the IEEE 802.15.4 Std. The VGA architecture is discussed in Section II. The simulation results of the implemented circuit are summarized in Section III and, finally, conclusions are given in Section IV.

II. PROPOSED VGA ARCHITECTURE

The designed VGA is integrated in a Low-IF receiver composed by an LNA, a mixer and a complex filter. The main reason of this choice is the fact that Low-IF receivers do not exhibit either a severe dc offset or 1/f noise, although it has the drawback of a restricted image rejection. However, these requirements are very relaxed in the IEEE 802.15.4 Std.

The VGA is placed after the complex filter and its function is to adjust its gain and optimize the signal level to reach the ADC dynamic range requirements. Therefore, it is desirable for the VGA to possess certain enhanced characteristics such as a wide dynamic range, a dB-linear gain control and wide and constant bandwidth. In fact, one of the mayor challenges in VGA design is to achieve constant bandwidth for all gain settings without compromising the overall performance, specially the die footprint. Although several architectures have been proposed to overcome this limitation, they often result in an increase in circuit complexity, power consumption and/or area use. That is why the Miller-Source Compensation scheme has been chosen [2].

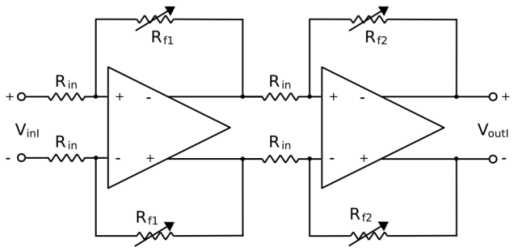


Fig. 1. Proposed VGA architecture.

The topology of the designed VGA is shown in Fig. 1. It consists of two amplification stages formed by a fully differential OTA with a negative feedback network to adjust the gain. Each stage achieves a gain range from 0 to 21 dB in 3 dB steps. The input resistor R_{in} is fixed to 6 kΩ while the feedback resistors R_{f1} and R_{f2} are varied to adjust the gain of each stage.

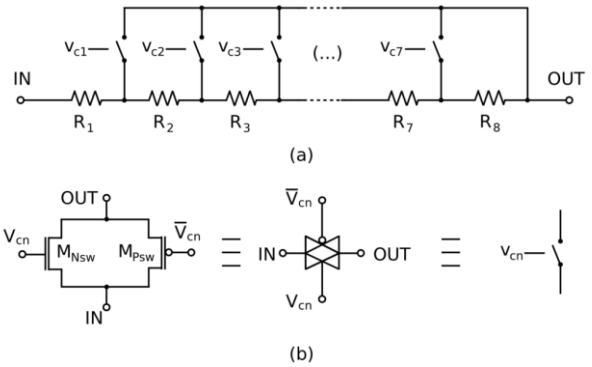


Fig. 2. Scheme of the variable resistor (a) and implementation of the switch (b).

The implementation of the variable resistor is depicted in Fig. 2 (a) and it is composed by various resistors in series and multiple switches to activate or deactivate them depending on

the control voltage, which is generated by a multiplexer. The implementation of the switches can be seen in Fig. 2 (b). Finally, the structure of the OTA [3] is presented in Fig. 3. It is composed by a differential pair with active load as the input stage. This configuration achieves high gain and CMRR while keeping a highly linear behaviour. A Class A amplifier is employed as the output stage, boosting the overall gain. Besides, a CMFB circuit is used to adjust the common-mode voltage at the Class A amplifiers and a current source is added to bias the previous stages.

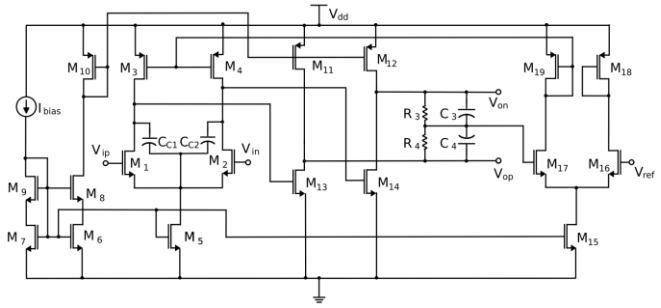


Fig. 3. Schematic of the OTA.

The layout of the VGA was developed using the Cadence Virtuoso® Layout Suite software and the models from the CMOS UMC 65 nm foundry. The resulting view of this process can be observed in Fig. 4.

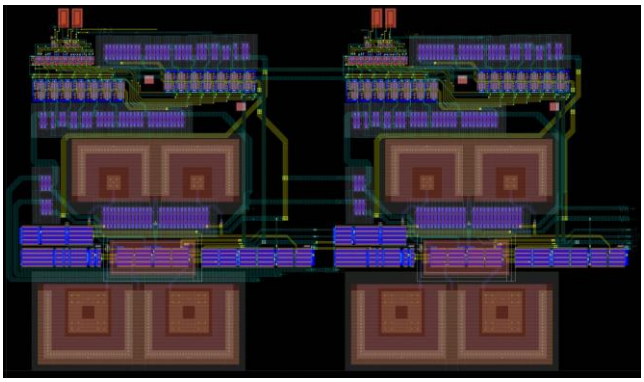


Fig. 4. Layout of the proposed VGA.

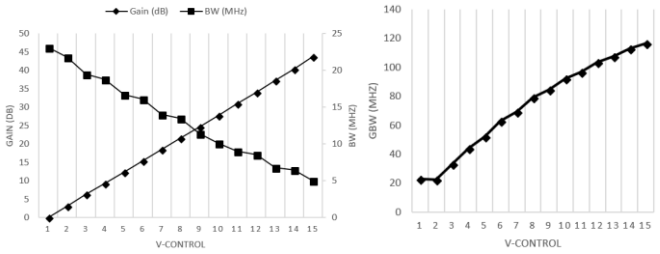
III. Simulation Results

The post-layout simulations of the proposed VGA were performed with the Cadence Virtuoso® Analog Design Environment software. The VGA total power consumption is only 334 µW with a supply voltage of 1.2 V and the area use is below 2800 µm^2.

The results of the VGA gain and bandwidth are depicted in Fig. 5 (a) and the GBW product is shown in Fig. 5 (b). Due to the parasitic extraction, the circuit shows a deviation in the gain steps from 3 to 3.1 dB resulting in a maximum gain setting of 43.7 dB. However, the gain is still approximately linear in dB and a minimum bandwidth of 5 MHz is obtained. As it can be seen, the bandwidth of the VGA decreases along with the control voltage, while the GBW product increases at the same rate. In any case, thanks to the Miller-Source Compensation scheme the VGA only needs two capacitors of 125 fF, resulting in a significant area saving.

IV. Conclusions

This paper presents the design of a low-power fully differential VGA in CMOS UMC 65 nm technology for the IEEE 802.15.4 Std. Post-layout simulations prove that the achieved performance is adequate and particularly competitive in terms of power consumption and area occupation, as it is seen in *Table 1*.



(a) (b)

Fig. 5. Gain and bandwidth of the VGA as a function of the control voltage (a) and GBW product of the proposed VGA as a function of the control voltage (b).

Table 1. *Performance comparison of different VGAs*

	[4]	[5]	[6]	[7]	*This Work*
Gain range (dB)	*-1.4 to 30.2*	*3 to 21.6*	*50*	*0 to 65*	*0 to 43.7*
Gain steps (dB)	*0.5*	*2.2*	*continuous*	*continuous*	*3.1*
Gain error (dB)	*±0.1*	*---*	*±0.5*	*±1*	*±0.1*
Bandwidth (MHz)	*3*	*10*	*15*	*3.8*	*5*
Supply (V)	*1.8*	*1.8*	*1.2*	*1.2*	*1.2*
P. Consumption (mW)	*35*	*2.8*	*2.2*	*11.5*	*0.334*
Process	*180 nm*	*180 nm*	*65 nm*	*180 nm*	*65 nm*
Area (µm^2)	*250000*	*190000*	*10000*	*750000*	*2740*

References

[1] IEEE, "The International Roadmap for Devices and Systems (IRDS): 2017 Edition: Executive Summary," 2017.

[2] J. Ramírez-angulo, E. Mirazo, J. Lemus, A. Diaz-sanchez, and A. Lopez-martín, "Source Compensated Miller Op-amps: A Simple Method to Enhance Amplifier's Bandwidth at no Cost," vol. 2, no. 1, pp. 2–5, 2010.

[3] A. Balankutty, S. Member, S. Yu, Y. Feng, P. R. Kinget, and S. Member, "A 0.6-V Zero-IF/Low-IF Receiver With Integrated Fractional-N Synthesizer for 2.4-GHz ISM-Band Applications," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 538–553, 2010.

[4] T. B. Kumar, K. Ma, K. S. Yeo, and W. Yang, "A 35-mW 30-dB gain control range current mode linear-in-decibel programmable gain amplifier with bandwidth enhancement," *IEEE Trans. Microw. Theory Tech.*, vol. 62, no. 12, pp. 3465–3475, 2014.

[5] H. Kim, Y. Park, H. Yang, and S. Kim, "A Constant Bandwidth Switched-Capacitor Programmable-Gain Amplifier Utilizing Adaptive Miller Compensation Technique," pp. 249–252.

[6] I. Choi, H. Seo, and B. Kim, "Accurate dB-Linear Variable Gain Amplifier With Gain Error Compensation," *IEEE J. Solid-State Circuits*, vol. 48, no. 2, pp. 456–464, 2013.

[7] H. Elwan, A. Tekin, and K. Pedrotti, "A Low-Noise Analog Baseband in 65nm CMOS," *Proc. Cust. Integr. Circuits Conf.*, pp. 2–5, 2010.