A 46.8 µW wake-up receiver for WSN with -78 dBm sensitivity using uncertain-IF architecture

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***Abstract*—This paper presents an 868 MHz wake-up radio using uncertain-IF architecture for wireless sensor network. It is designed to receive data modulated with on-off-keying in UMC 65nm CMOS technology and employs uncertain-IF architecture to reduce the oscillator design constraints and reduce power consumption. The wake-up radio consists of a single-ended dual-gate mixer, a five stage IF-amplifier and a differential envelope detector biased in weak inversion. The wake-up radio has been designed with a trade-off between sensitivity and power consumption The obtained sensitivity and power consumption is -78 dBm and 46.8 µW, respectively, with 1.2 V power supply.**

Keywords—component: uncertain-IF, IF amplifier, wake-up, low power, envelope detector.

I. INTRODUCTION

Gradually, things around us have sensors that communicate with each other. In this context, Wireless Sensor Networks (WSN) play a major role in the advent of the so called Internet of Things (IoT) with applications in fields such as smart buildings, medicine and health care, precision agriculture, industrial process control, military, disaster relief operations, intelligent buildings or bridges. Typically, WSNs are composed of a large number of minimal capacity sensing, computing, and communicating devices and various types of actuators operating in a complex and noisy real-time environment. Their hardware should be power-efficient, small, inexpensive, and reliable to maximize node lifetime, add flexibility, facilitate data collection and minimize the need for maintenance. Lifetime is particularly critical for most applications, and its key limiting factor is the energy consumption of the nodes. This paper deals with this issue and focuses on extending the node battery life thanks to the use of low-power wake-up radios.

In WSNs, periodic wake-up is a convenient mean to avoid idle listening to the channel and to prolong the node lifetime. In this paper we propose going one-step further adding a wake-up receiver to the node. The node will have two radios, one main radio which transfers raw-data from sensors to the WSN, and a wake-up radio which is an ultra-low power radio intended to activate the main radio only when it is ready to transmit or when the node receives a wake-up signal from the network [1]. Using this two radio terminal configuration, the main radio, which typically is very power consuming, remains turned off most of the time and only turns on when it is necessary to transmit.

In this work, we present the design of a wake-up radio for WSNs using uncertain-IF architecture. The paper is organized as follows. Section II gives an overview of the node block diagram, including the description of the two terminal radio and the uncertain-IF architecture used in the wake-up radio. This radio is composed of one active mixer, one IF amplifier, and one envelope detector. The design of these circuits is explained in Section III. The simulation results of the circuit are reported in Section IV and finally some conclusions are given in Section V.

II. RECEIVER ARCHITECTURE

The main components of the wireless sensor node are the microcontroller, the transceiver, the battery and the sensors. As shown in Figure 1, a solution to reduce the power consumption of the node is to incorporate a wake-up radio. The wake-up radio is composed of a mixer with input matching network, a set of IF amplifiers, a differential envelope detector to demodulate the input signal and a pattern recognizer

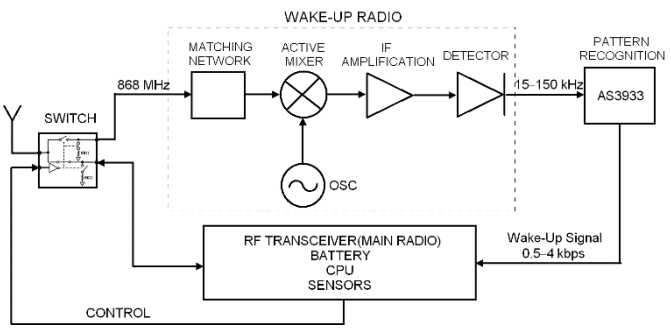

Figure 1. Block diagram of a wireless sensor node.

Thus, the node has two receiving paths: one for processing a wake-up signal and other for communicating with the other nodes. Which path is activated depends on the antenna switch, situated directly behind the antenna. It is controlled via an output port of the microcontroller. The wake-up radio listens continuously the input signal to detect the node addressed bit sequence. In case of a valid wake-up signal and a positive correlation of the sent address with an internal saved bit

sequence, the correlator interrupts the microcontroller from its sleep mode. When entering active mode the controller toggles the antenna switch and can establish a regular communication link with the nodes main radio.

The correlator used in this paper is the AS3933 from AMS [2]. This circuit accepts a low frequency wake-up (0.5-4 kbps) signal modulated on a high frequency carrier (15-150 kHz). In order to use the same antenna than the main radio, this carrier is modulated again with an 868 MHz carrier.

The wake-up radio uses the uncertain-IF architecture [4]-[6] to downconvert the 868 MHz signal to an undefined IF frequency which can be in the interval between 4.3 to 67.3 MHz using a free running oscillator (LO) and a mixer (see Figure 2). The proposed architecture use a free running LO instead of a PLL to reduce considerably the power consumption, Frequency variation of the LO simply becomes visible as IF frequency variation, to which the envelope detector is insensitive.

The performance of this architecture is similar to any downconversion receiver but with considerably increased gain before envelope detection, improving the sensitivity compared to wake-up receivers using only RF gain or passive detectors [7].

However, as any downconversion receiver, the main drawback of the uncertain-IF architecture is its susceptibility to interferers, therefore, a narrow and accurate RF bandpass or very selective matching network at the input is required to improve robustness to interferers.

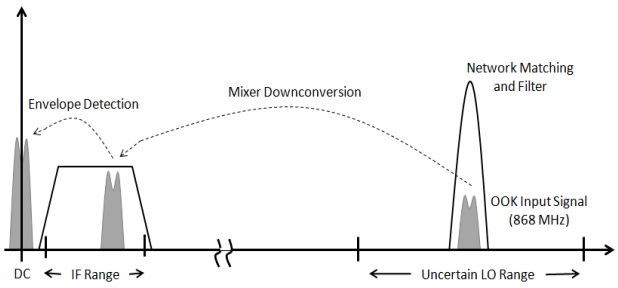

Figure 2. Uncertain IF frequency.

An important frequency planning consideration is the trade-off between LO accuracy and IF bandwidth. If the LO can be tuned very close to the channel frequency, the required bandwidth of the IF amplifier can be narrowed and its power reduced proportionately. If the LO is kept within a smaller frequency range, the vulnerability to oscillator frequency drift increase [6]. As shown in Figure 2, for this implementation, an IF bandwidth of about 63 MHz is chosen to maximize tolerance of LO frequency drift, without requiring excessive power in the IF amplifier.

III. Circuit Design

The simplified schematic of the wake-up radio is shown in Figure 3 and it is composed of a single-ended active mixer whit an input matching network to maximize the power transfer from the antenna , a five stage cascade IF amplifier with 4.3 MHz to 67.3 MHz frequency range, and a differential detector working in weak inversion.

A. Mixer

The input matching network consists of two capacitors C_{M1} and C_{M2}, and an inductor, L_{M1}. It must supply a stable impedance matching similar to the antenna (50 Ω) at the desired frequency band (868 MHz).

The mixer is designed to achieve minimum power consumption, maximum conversion gain and minimum LO drive requirements. As shown in Figure 3, a single-ended dual gate configuration is used as a mixer because the LO port can be driven from a single-ended oscillator, reducing in this way the wake-up radio power consumption. The dual-gate mixer is simply a cascade connection of two NMOS transistors in series, M1 and M2. This configuration is well suited to CMOS since the drain and source of the two devices can be shared thus reducing capacitance at this node by a factor of two.

The input signal is fed to the gate of M1, which is in common source and the f_{LO} signal is connected to the gate of transistor M2. The f_{RF} signal varies the drain-source current of M1, and the switching operation of M2 multiplies this variation by the f_{LO} signal coming from the local oscillator. Then the signals are multiplied obtaining an IF signal in M2 drain.

The load network, composed of R_L and C_L, acts as a low-pass filter. f_{RF} and f_{LO} feedthrough to IF, which are intrinsic to the single-balanced design, are filtered by the load network and the IF amplifier stages, before arriving at the envelope detector.

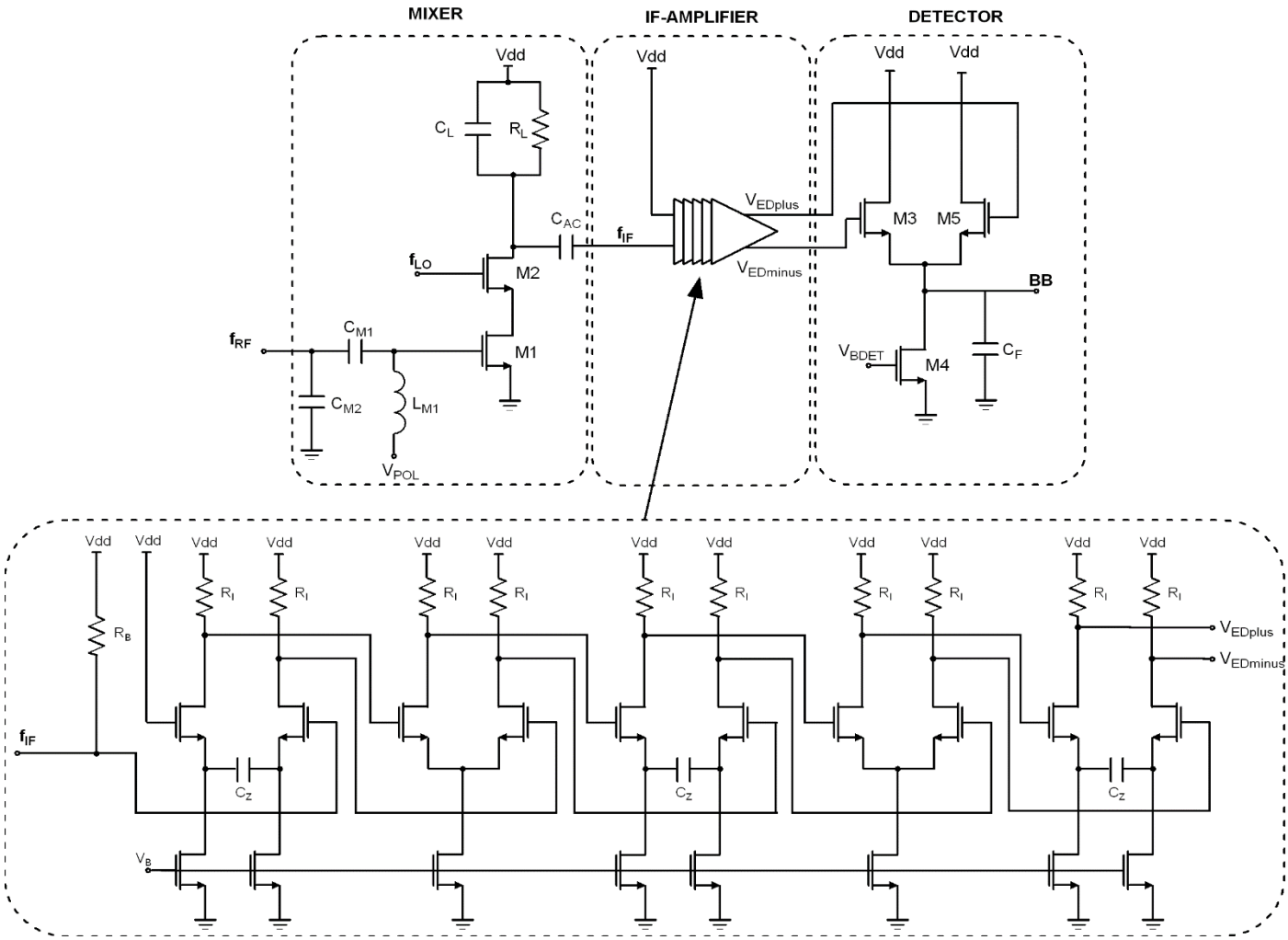

Figure 3. Wake-up radio simplified schematic.

B. IF Amplifier

The IF amplifier must provide a gain for 67 MHz bandwidth approximately. A differential amplifier with resistive loads has been used to meet the wideband specification. The typical configuration for this type of amplifiers is composed of two transistors that share the same source connection, whereby a current is applied to bias the transistors. The input of each stage is the gate of the transistors, while the drains are the amplifier outputs. As shown in Figure 3, the use of identical stages and resistive loads simplifies biasing and allows simple DC coupling between stages.

To achieve the required bandwidth and maximize the gain with the lowest power consumption, we have used five stages. The odd stages have an independent current source in each branch and the even stages have a single current source common to both transistors. The bias currents of all five stages are matched and controlled simultaneously via a single voltage (V_B), which is common to all stages.

In the odd stages, the tail current source is split into two branches with a coupling capacitor C_Z of 1.5 pF, introducing a zero at DC in the differential transfer function [6]. On the other hand, the transistor size and the load resistor condition the high frequency limitation.

C. Envelope Detector

The envelope detector is shown in Figure 3 and has a differential configuration. For signals inside the detector's baseband bandwidth, the differential topology rejects the differential mode, but common mode signals pass through.

M3·and M5 are biased in weak inversion to reduce the power consumption and generate an output that is an exponential function of the input voltage [8][9]. For CMOS analog circuits, when the transistors operate in weak inversion region, gm/I_D ratio is higher compared to strong inversion, hence the minimum power consumption can be achieved due to the small quiescent current at the expense of large silicon area and slow speed. When MOS transistors operate in strong inversion, however, although good frequency response and small area are obtained, non-optimum larger power is consumed, and V_{DS} (sat) is high [10].

M4 is working as a current source to drive M3 and M5. The output impedance of the detector with capacitor C_F form a 125 kHz low pass filter.

The output of the detector is connected to the AS3933, which can detect a minimum signal of 80 µVrms (113 µVp) and has an input impedance of 2 MΩ.

IV. Simulation Results

The circuits were implemented with Cadence using UMC CMOS 65 nm technology and simulated in Advanced Design System (ADS) through RFIC Dynamic Link. A complete layout of the wake up radio can be shown in Figure 4. Figure 5 shows the wake-up receiver output, which is a 125 kHz frequency signal and with 148.6 μV_{peak}, enough to drive the AS3993.

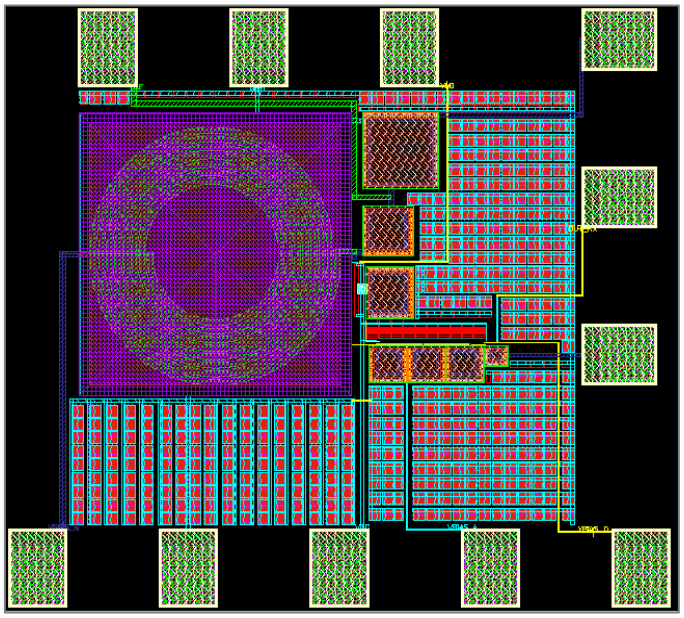

Figure 4. Wake-up radio layout.

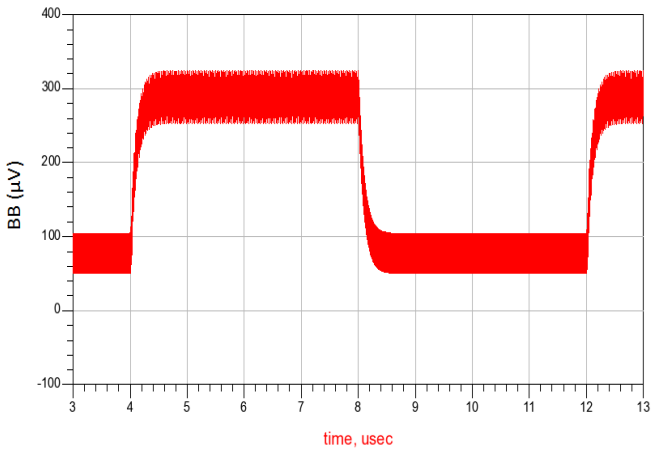

Figure 5. Receiver output.

Table I summarizes the wake-up radio performance and compares the results with [6]. The obtained values are similar, but in this work the sensitivity has been improved at the expense of increased power consumption.

Table I. Summary results

Parameter	[6]	This work
Supply voltage	0.5 V	1.2 V
Carrier frequency	2 GHz/OOK	868 MHz/OOK
Power Cons.	32 µW	46.8 µW
Data rate	100/200 kbps	0.5-4 kbps
Sensitivity	-72/-70 dBm	-78 dBm

V. Conclusions

In this work, a wake-up radio for WSN has been designed to extend the battery life of a node. The radio architecture use an uncertain-IF architecture with an IF frequency from 4.3 to 67.3 MHz. Using this architecture, a free running oscillator instead of a PLL is used, decreasing the radio power consumption. The circuit was implemented in UMC CMOS 65 nm process and it is composed of a mixer, a five-stage cascade differential amplifier and a detector biased in weak inversion. Complete simulation of the wake-up receiver has been done obtaining a sensitivity of -78 dBm with a power consumption of 46.8 µW with a 1.2 V power supply. The circuits have been designed to optimize power consumption and sensitivity.

Acknowledgment

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