Design of a Programmable Phase Shifter for Phased Array Antennas

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***Abstract*—This paper presents the implementation of an 8 bits programmable active phase shifter for phased array antenna applications. This circuit is designed to operate in the bandwidth that goes from 27.5 GHz to 30 GHz and it has been implemented in SiGe_1K5PAx technology of Global Foundries. The phase shifter has a vector sum phase structure, generating 360° phase shifts. Also, is composed by of a quadrature generator formed by a polyphase filter. In the same way, is composed by of an amplifier based on a Gilbert cell, considering the current of the Digital/Analog Converter (DAC), that will perform as current mirror of the net mentioned.**

Keywords-component; Programmable Phase Shifter, Phased Array Antenna, SiGe, Vector Sum, 360° Phase Shifts, Quadrature Generator, Polyphase Filter, Gilbert's Cell, Digital/Analog Converter.

I. INTRODUCTION

The Global Foundries (GF) 5PAx and 1K5PAx processes are the latest additions to the GF SiGe family of technologies, also composed of 5PAe and 1KW5PAe. The four processes make up a family that provides significant performance, ease of integration and acceptable price for customers currently using alternatives based on Gallium Arsenide (GaAs). The latest offers, 5PAx and 1K5PAx, are optimized to meet the rigorous demands of evolving mobile standards such as 802.11ac, which requires data performance three times faster than the previous generation of standards. These processes allow to implement power amplifiers (PA), low noise amplifiers (LNA) and switching circuits optimized for energy efficiency, improved noise figure and insertion losses, allowing to implement next-generation Wi-Fi and cellular solutions more efficient in power consumption and allowing faster access to data and uninterrupted connections [1].

The design of the electronic phase shifter, object of this paper was carried out using the GF 1K5PAx SiGe process. The SiGe 1K5PAx process, like its predecessor 1KW5PAe, is built on a high resistivity substrate and is optimized to maximize circuit integration and performance.

II. PROPOSED PHASE SHIFTER ARCHITECTURE

Currently, the electronic phase shifters that are used for phased array antennas have a vector sum phase structure, being able to generate 360° phase changes. In addition, they consist of a quadrature generator made up of polyphase RC filters and quadrature all-pass filters, as well as the effects of load capacities. In the same way, they consist of an amplifier based on a Gilbert cell, in which the current of the Digital/Analog Converter (DAC) must be taken into account, which will act as a current mirror for the said network [2].

A. First Orden Polyphase Filter

The quadrature generator is the circuit responsible for the generation of two pairs of differential outputs in phase and quadrature from a differential input. Two typical implementations of quadrature generators are RC Polyphase Filters (PPF) and RLC Quadrature All-Pass Filters (QAF). RC Polyphase Filters are widely used in image rejection reception architectures [3] and are constructed from RC-CR networks that generate two voltages with 45 ° and -45 ° phases at a central frequency, so that the difference between exits phases is 90 °.

Figure 1 shows the scheme of a first order polyphase filter designed and simulated in the Cadence software for a center frequency of 28.75 GHz. In this case, to generate the differential input signal, an ideal balun is used. Due to the excessive size that a circuit of these characteristics can present and the complexity of the electromagnetic simulations necessary for its design, it is estimated that this component will be external and is not the object of this work.

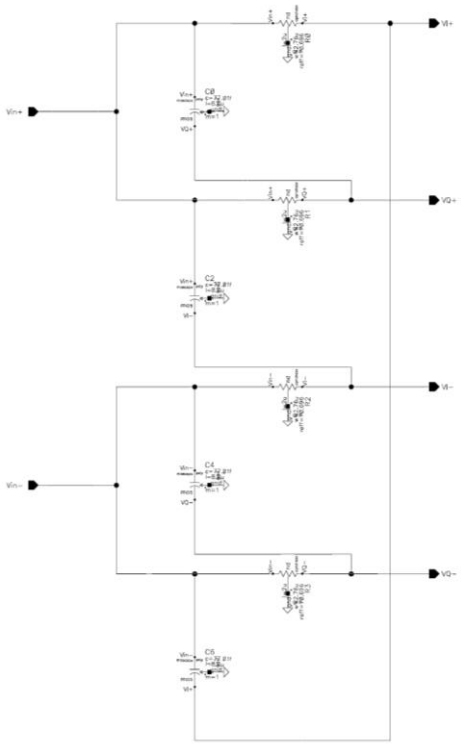

Fig 1. First order polyphase filter.

B. Phase Shifter

A detailed schematic of the phase shifter can be seen in Figure 2. In this scheme we can see how the first order polyphase filter mentioned in the previous section would be connected to the input of the network of differential amplifiers based on Gilbert cells, whose current sources and its active load is composed of transistors. The outputs of the differential pairs are connected to the output buffer. Finally, the circuit output is delivered to the next circuit in the chain through an adaptation network.

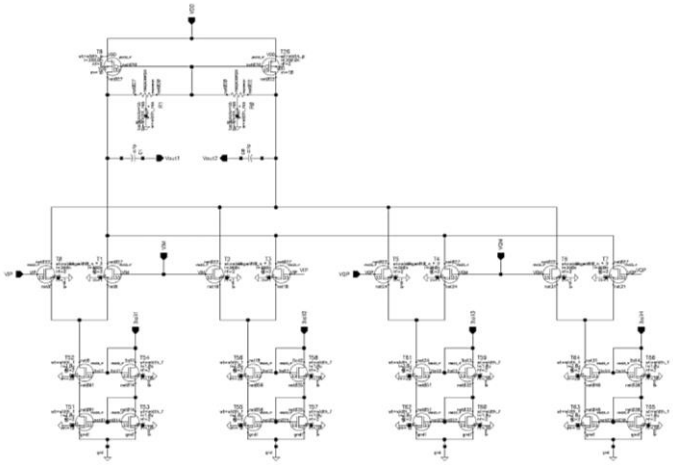

Fig 2. Phase shiter.

To access the four quadrants of the unit circle, only one of the differential pairs is enabled at a time. In this case, the control is implemented by applying a voltage on the gate or gate terminal of the phase amplifiers, as in quadrature amplifiers. For example, to access the first quadrant, the positive amplifiers of both I and Q are activated, so they are connected to the bias voltage respectively, while the negative amplifiers are connected to ground. The gain of each amplifier is controlled by varying the bias voltages.

The phase change in this topology is made thanks to the current that passes through each branch. If, for example, we want to provide an output signal that is in the first quadrant (phase between 0° and 90°), we must conduct the current through $I_{TAIL\,1}$ and $I_{TAIL\,3}$ and keep $I_{TAIL\,2}$ and $I_{TAIL\,4}$ at 0 mA. Varying their values and ensuring that the magnitude of the sum of both currents is constant will provide different phase changes [4].

C. Digital/Analog Converter

The current DAC is designed to allow 8-bit digital control of phase changes. This circuit acts as a current mirror of the circuit discussed above and is responsible for providing the different tail currents that give rise to the different phase changes. In order to provide the tail currents necessary for each phase step, the current source must be carefully designed. To do this, the architecture shown in Figure 3 will be implemented.

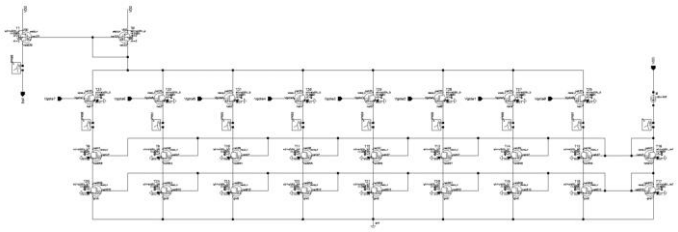

Fig 3. Current DAC**.**

In this architecture the transistors must have the correct size to provide the necessary tail currents. The principle of operation of this circuit is simple: The current generator located to the right of the schematic (reference branch of the DAC) establishes a constant tail current that is divided between routes I and Q. The tail current then passes to through a series of NMOS (Negative-channel Metal-Oxide Semiconductor) transistors controlled by a *Vgate* voltage that is associated with each of the 8 bits that make up the DAC. In this topology, the control of the unit circle quadrant is established using the combinational logic that gives rise to the different bit configurations that are implemented by activating or deactivating the NMOS transistors by applying or not applying the *Vgate* voltage on them. Due to the fact that the necessary currents have very specific values, each bit branch is connected to several transistors connected in parallel to regulate the current flow. On the left of the schematic (output branch of the DAC) there is a current mirror formed by PMOS transistors (Positive-channel Metal-Oxide Semiconductor), which will be responsible for making the copy of the current from the bit branches with in order to guarantee the correct functioning of the circuit.

III. Simulation Results

Once the polyphase filter, phase shifter and DAC were successfully implemented, to complete the design, the complete phase shifter including the DAC was simulated.

The objective that was sought in this final part of the design was to obtain the different lags for the four quadrants taking into account the current values generated by the DAC and the phase step (5.625°) established in the specifications. For this, the complete phase shifter was simulated using the setup shown in Figure 4, where it can be seen that the four DACs that replace the four current sources present in the previously designed phase shifter are located at the top of the schematic.

As a result of the simulations of the complete phase shifter, Table 1 and Table 2 show the currents obtained for the first and second quadrants since the values of the first quadrant are equal to those of the third and those of the second are equal to those of the fourth . Table 1 and Table 2 show the current and phase errors between the phase shifter without DAC and the simulated full phase shifter. Since these errors are not significantly large and we comply with the initially established specifications, it can be stated that the objective of the specified phase step is achieved.

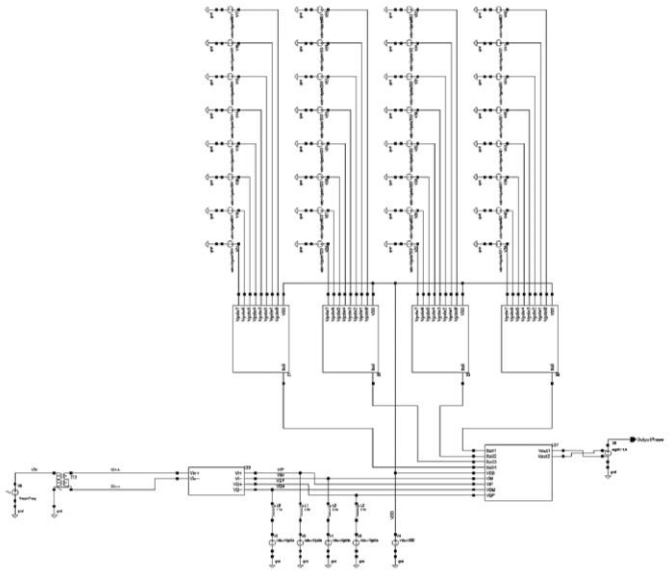

Fig 4. Complete phase shifter simulation setup.

Tab 1. First and third quadrant currents obtained from the complete phase shifter.

Full Phase Shifter Simulation (1° y 3 ° Quadrant)																																
I_{TAL1}DAC												I_{TAL3}DAC																Phase Results		
B7	B6	B5	B4	B3	B2	B1	B0	I_{TAL} (µA)	Ref (µA)	I_{TAL1} Error		B7	B6	B5	B4	B3	B2	B1	B0	I_{TAL} (µA)	Ref (µA)	I_{TAL3} Error						Phase (°)	Ref (°)	Phase Error
1	1	0	1	0	1	0	1	1000	1000	0		0	0	0	0	0	0	0	0	1,627	0	1,627						38,046u	0	38,046u
1	1	0	1	0	0	1	1	991,7	992,932	1,232		0	0	0	0	0	0	0	1	6,803	7,068	0,265						5,5714	5,625	0,0536
1	1	0	1	0	0	0	0	978,9	980,815	1,915		0	0	0	0	0	0	1	1	18,82	19,185	0,365						11,13688	11,25	0,11312
1	1	0	0	1	1	0	0	961,8	961,481	0,319		0	0	0	0	0	1	1	1	41,25	38,519	2,731						17,50881	16,875	0,63381
1	1	0	0	0	1	0	1	931,8	932,484	0,684		0	0	0	0	0	1	1	0	68,12	67,516	0,604						22,59175	22,5	0,09175
1	0	1	1	1	0	1	1	888,7	888,985	0,285		0	0	0	1	0	1	0	0	109,8	111,015	1,215						27,9983	28,125	0,1267
1	0	1	0	1	1	0	0	823,2	821,856	1,344		0	0	1	0	0	0	1	0	180,6	178,144	2,456						33,89419	33,75	0,14419
1	0	0	1	0	0	1	1	712,4	714,615	2,215		0	0	1	1	0	1	1	1	284	285,385	1,385						39,34496	39,375	0,03004
0	1	1	1	0	0	0	0	553,2	552,242	0,958		0	1	0	1	1	0	0	1	446,2	447,758	1,558						45	45	0,0395
0	1	0	0	1	0	0	0	365,7	365,971	0,271		1	0	0	0	0	0	1	0	635,7	634,029	1,671						50,6484	50,625	0,0234
0	0	1	0	1	0	1	0	220,3	221,664	1,364		1	0	1	0	0	0	1	0	779,1	778,336	0,764						56,3094	56,25	0,0594
0	0	0	1	1	0	0	0	130,3	131,295	0,995		1	0	1	1	0	1	1	0	867	868,705	1,705						61,9444	61,875	0,0694
0	0	0	0	1	1	1	0	78,66	76,0542	2,6058		1	1	0	0	0	0	1	1	923,2	923,9458	0,7458						67,1821	67,5	0,3179
0	0	0	0	0	1	1	1	41,25	41,7576	0,5076		1	1	0	0	0	1	0	1	957,6	958,2424	0,6424						73,22161	73,125	0,02839
0	0	0	0	0	0	1	1	18,82	20,1541	1,3341		1	1	0	1	0	0	0	0	978,9	979,8459	0,9459						79,2048	78,75	0,4548
0	0	0	0	0	0	0	1	6,803	7,22079	0,41779		1	1	0	1	0	0	0	1	991,7	992,77921	1,07921						84,51682	84,375	0,14182
0	0	0	0	0	0	0	0	1,627	0	1,627		1	1	0	1	0	1	0	1	1000	1000	0						89,68878	90	0,31122

Tab 2. Second and fourth quadrant currents obtained from the complete phase shifter.

Full Phase Shifter Simulation (2° y 4° Quadrant)																																
I_{TAL3}DAC												I_{TAL2}DAC																Phase Results		
B7	B6	B5	B4	B3	B2	B1	B0	I_{TAL} (µA)	Ref (µA)	I_{TAL3} Error		B7	B6	B5	B4	B3	B2	B1	B0	I_{TAL} (µA)	Ref (µA)	I_{TAL2} Error						Phase (°)	Ref (°)	Phase Error
1	1	0	1	0	1	0	1	999,603	0,397			0	0	0	0	0	0	0	0	1,627	0,397	1,23						89,68878	90	0,31122
1	1	0	1	0	0	0	1	991,7	991,157	0,543		0	0	0	0	0	0	0	1	6,803	8,843	2,04						94,64241	95,625	0,98259
1	1	0	0	1	1	1	1	974,6	975,81	1,21		0	0	0	0	0	1	0	0	24,56	24,19	0,37						101,3657	101,25	0,1157
1	1	0	0	1	0	0	1	949	951,009	2,009		0	0	0	0	1	0	0	0	46,71	48,991	2,281						106,4608	106,875	0,4142
1	1	0	0	0	0	0	1	914,6	913,051	1,549		0	0	0	1	0	0	0	0	89,12	86,949	2,171						112,7393	112,5	0,2393
1	0	1	1	0	0	1	1	853,9	854,546	0,646		0	0	0	1	1	0	1	1	145,5	145,454	0,046						118,1294	118,125	0,0044
1	0	0	1	1	1	1	0	761,5	761,84	0,34		0	0	1	0	1	1	1	0	240	238,16	1,84						123,8307	123,75	0,0807
0	1	1	1	1	1	1	0	617,4	616,974	0,426		0	1	0	0	1	1	0	0	384,7	383,026	1,674						129,4098	129,375	0,0348
0	1	0	1	0	1	1	0	432,1	431,981	0,119		0	1	1	1	0	0	1	1	567	568,019	1,019						135	135	0,01423
0	0	1	1	0	1	0	0	269,4	271,185	1,785		1	0	0	1	0	1	1	1	730,3	728,815	1,485						140,69766	140,625	0,07266
0	0	0	1	1	1	1	1	165,7	165,716	0,016		1	0	1	0	1	1	1	1	836,4	834,284	2,116						146,26677	146,25	0,01677
0	0	0	1	0	0	1	0	99,5	101,005	1,505		1	0	1	1	1	1	0	1	897,4	898,995	1,595						152,03316	151,875	0,15816
0	0	0	0	1	0	1	1	62,81	60,3987	2,4113		1	1	0	0	0	1	1	1	940,4	939,6013	0,7987						157,09898	157,5	0,40102
0	0	0	0	0	1	1	0	35,75	34,2286	1,5214		1	1	0	0	1	1	0	1	966,1	965,7714	0,3286						162,724	163,125	0,401
0	0	0	0	0	0	1	1	18,82	17,3053	1,5147		1	1	0	1	0	0	0	1	983,2	982,6947	0,5053						168,1041	168,75	0,6459
0	0	0	0	0	0	0	1	6,803	6,58644	0,21656		1	1	0	1	0	0	1	1	991,7	993,41356	1,71356						174,1312	174,375	0,2438
0	0	0	0	0	0	0	0	1,627	4,47618E-05	1,62695524		1	1	0	1	0	1	0	1	1000	999,999955	0,000045						180	180	0

IV. Conclutions

In order to record compliance with the requirements throughout the design process, Table 3 shows the results of the phase shifter obtained at the conclusion of the procedure carried out. In this table a comparison is made between the specifications required for the implementation of the programmable phase shifter and the complete design. In addition, Table 1 and Table 2 show how the simulation results reflect that the currents generated by the complete phase shifter are similar to those obtained in the phase shifter simulation without DAC, which denotes the satisfactory development of the design.

Tab 3. Comparison between specifications and results.

	Specifications			Complete Phase Shifter	
Parameter	Min.	Tip.	Máx.	Results	Units
Frequency Range	27.5	--	30	27.5 – 30	GHz
Phase Range	0	--	360	0 – 360	°
Precision/Step Phase Control	1.40625	--	5.625	1.40625 – 5.625	°
Phase Error Throughout the Frequency Band	--	--	5	4.93595	°
Amplitude Flatness for Phase Change	--	--	1	-0.00728	dB
Profit Flatness @ Entire Band	--	--	2	-1.42665	dB
Input/Output Adaptation (S_{11})	--	--	-12	-7.8660/-27.1454	dB
Output Port Isolation	--	-24	--	-67.7695	dB
Operating Temperature Range	-40	--	85	-40 – 25 – 85	°C

References

[1] E. McGill, “GlobalFoundries broadens SiGe power amplifier portfolio, enhancing RF performance and efficiency for wireless devices”, GlobalFoundries, March 2016.

[2] S. Ituah, “High frequency receiver front – end module for active antenna applications”, Thesis presented to the University of Waterloo, pp. 36 – 58, 2015.

[3] F. Behbahani, Y. Kishigami, J. Leete, and A. Abidi, “CMOS mixers and polyphaser filters for large image rejection", IEEE Journal of Solid – State Circuits, vol. 36, no. 6, pp. 873 – 887, June 2001.

[4] M. San Miguel and D. Mayor Duarte, “Beamformer topology analysis”, eScan – ESA preliminary antenna design, Ref. CTGUK-ESA-PhaseShifter-002, April 2019.