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ANÁLISIS DE LOS EFECTOS DE LA RADIACIÓN ESPACIAL EN CIRCUITOS INTEGRADOS DE RADIOFRECUENCIA EN TECNOLOGÍAS NANOMÉTRICAS COMERCIALES BASADAS EN SILICIO

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DOCTORAL PROGRAMME IN
TELECOMMUNICATIONS TECHNOLOGIES
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PhD DISSERTATION

RADIATION EFFECTS ANALYSIS OF RF INTEGRATED CIRCUITS IMPLEMENTED IN NANOMETRIC TECHNOLOGIES BASED ON SILICON

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ABSTRACT

Radiation tolerance in electronic circuits has become a relevant field of study in the design of nanonelectronic systems. Specifically, the analysis of the impact of radiation in circuits that compose wireless sensor networks (WSNs) has become of major importance. This type of network has changed the way of communicating, allowing the interconnection of a wide variety of devices and playing a major role in the development of the Internet of Things (IoT). However, there still exist certain applications in which the presence of high radiation discourages the use of this kind of network. Taking this into account, the development of devices that allow the deployment of WSNs in high radiation environments is seen as a hot topic in the field of electronic systems. Specifically, in aerospace applications, the use of WSNs would reduce the weight and volume of spacecrafts by reducing the wiring used for intra-satellite communications. This is of major importance, since it reduces the cost of launching the spacecrafts into space.

The main issue in the use of WSNs in high radiation environments is how the circuits and electronic components are affected by the high energy ionizing particles present in this kind of environment. These particles can produce negative effects such as total ionizing dose (TID) or single event effects (SEEs).

In order to mitigate the damages produced by TID and SEEs, there are several strategies that can be followed. One of them consists in using lightweight shielding. However, this shielding cannot fully prevent the ionizing particles from reaching the circuits. Furthermore, the use of this shielding will increase the weight of the spacecraft and, in turn, increase the cost of launching it into space. Another strategy is focused on the design of radiation hardened devices and circuits that are inherently robust against radiation. This dissertation follows this strategy and focuses on the design of radio-frequency (RF) circuits that are robust against radiation. In this case, radiation hardening by design (RHBD) techniques are employed.

In this work, complementary metal-oxide-semiconductor (CMOS) technologies have been used to develop these circuits. These technologies represent a cost-effective solution when compared to III-V technologies, which are typically used in space applications. This cost reduction is achieved by using low cost devices with minimum size and weight, as well as operating at low power. However, CMOS technologies are vulnerable to radiation effects, which means that designing radiation hardened circuits using these technologies can be stated as a challenging task.

In order to achieve the goal of designing radiation hardened RF circuits, a thorough study of the effect of radiation in this type of circuit must be carried out. To do so, a complete analysis from the basic elements of RF circuits, which are the semiconductor devices, to complete RF systems is performed.

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LIST OF ACRONYMS

ACRONYM	MEANING
AC	Alternating Current
ADS	Advanced Design System
BER	Bit Error Rate
BPF	Band Pass Filter
CCVS	Current Controlled Voltage Source
CG	Common-Gate
CMEs	Coronal Mass Ejections
CMOS	Complementary Metal-Oxide-Semiconductor
COTS	Commercial-Off-The-Shelf
CS	Common-Source
CSOIC	Ceramic Small Outline Integrated Circuit
DC	Direct Current
DICE	Dual Interlocked Cell
DIP	Dual In-line Package
DRAM	Dynamic Random Access Memory
FPGAs	Field Programmable Gate Arrays
GaN	Gallium Nitride
GCRs	Galactic Cosmic Rays
GEO	Geostationary Orbit
GSM	Global System for Mobile communications
HBTs	Heterojunction Bipolar Transistors
HEMTs	High Electron Mobility Transistors
HEO	Highly Elliptical Orbit
IF	Intermediate Frequency
IIP2	Second-order Input Intercept Point
IIP3	Third-order Input Intercept Point
LEO	Low Earth Orbit
LET	Linear Energy Transfer
LNA	Low Noise Amplifier
LO	Local Oscillator
LPF	Low Pass Filter
MBU	Multiple Bit Upset
MEO	Medium Earth Orbit
MIM	Metal-Insulator-Metal
NF	Noise Figure
PCB	Printed Circuit Board
PLL	Phase-Locked Loop

ACRONYM	MEANING
RC	Resistor-Capacitor
RF	Radio Frequency
RHBD	Radiation Hardening By Design
RHBP	Radiation Hardening By Process
RHBR	Radiation Hardening By Reconfiguration
SAA	South Atlantic Anomaly
SDE	Sentaurus Device Editor
SDEVICE	Sentaurus Device
SEB	Single Event Burnout
SEEs	Single Event Effects
SEFI	Single Event Functional Interrupt
SEGR	Single Event Gate Rupture
SEL	Single Event Latchup
SET	Single Event Transient
SEU	Single Event Upset
SiGe	Silicon Germanium
SOA	Safe Operating Area
SOI	Silicon-On-Insulator
SRAM	Static Random Access Memory
SRIM	Stopping and Range of Ions in Matter
TCAD	Technology Computer Aided Design
TF	Transfer Function
TIA	Transimpedance Amplifier
TID	Total Ionizing Dose
TOI	Third-Order Intercept
VCCS	Voltage Controlled Current Source
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network
WSNs	Wireless Sensor Networks

Parte I

Dissertation

Chapter 1

INTRODUCTION

1.1 Motivation

Wireless Sensor Networks (WSNs) have allowed the deployment of electronic systems that are sensitive and responsive to the presence of people in a wide number of fields such as industry, environmental applications or medicine. However, there are certain applications in which the presence of high radiation obstructs the use of this kind of technology. Specifically, aeronautics, aerospace, nuclear, health and particle accelerator sectors will benefit from its use. For example, in aerospace applications, the use of WSNs will reduce the wiring, thus reducing the weight and volume. This is of high importance in satellites, since it reduces the cost of launching them into space. Simultaneously, the flexibility of the communication networks is enhanced since less time is required for assembly, integration and testing.

The main concern in the use of WSNs in high radiation environments is its impact on the circuits and electronic systems. In this type of environment, high energy ionizing particles can produce damaging effects such as total ionizing dose (TID) or single event effects (SEEs). The former may progressively degrade the operation of circuits by an accumulative process of charge generation. The latter generates data corruption in digital circuits and transitory perturbations in analog circuits. Even high peak currents that can destroy the circuitry could be produced due to SEEs. If these effects are not considered during the design process and from a technological point of view, SEEs can produce an interruption in the proper functioning of devices and even fatal errors. This problem becomes more pronounced with technology scaling, where the number of integrated devices increases and the transistor gate lengths decrease. In these cases, SEEs can be produced by particles with less energy.

In order to mitigate the damages produced by TID and SEEs in electronic circuits and systems, lightweight shielding can be employed. However, the shielding cannot fully stop the high energy particles from reaching the electronics. Additionally, this shielding (even lightweight) will add weight on a spacecraft, thus increasing the cost of launching it into space. Therefore, it is a major goal in the radiation effects research community to develop radiation hardened devices, robust circuits and systems that can operate in high radiation environments. Radiation hardening techniques can be implemented at different levels. Radiation-hardening-by-design

(RHBD) is the most extended solution since it meets specified radiation performance criteria without modifying the existing technology process and maintaining the device electrical behaviour [1].

Taking this into consideration, radiation tolerance in circuits has become a relevant topic in the field of nanoelectronic system design. Circuits used in space applications have conventionally been implemented in radiation hardened technologies such as III-V technologies, silicon germanium (SiGe) or silicon on insulator (SOI). However, thanks to complementary metal-oxide-semiconductor (CMOS) technologies, cost reduction can be achieved by using cheap devices with minimum size and weight, besides operating at low power [2]. Indeed, a special hot topic nowadays is using commercial-off-the-shelf (COTS) parts to enable low-cost missions [3]. Despite these advantages, CMOS technologies are vulnerable to radiation effects even at terrestrial level, thus affecting circuits that are used in many applications apart from space-intended devices, such as medical and military equipment, nuclear plant control systems, etc.

As mentioned previously, SEEs are one of the greatest liabilities in electronic systems and in CMOS devices in particular [4]. These effects are generated when an energetically charged particle strikes a sensitive region in an integrated circuit. The resulting electron-hole pair generation caused by these strikes can produce transient pulses that could propagate to other areas of the circuit, generating single event upsets (SEUs). This temporary voltage or current disturbance at a circuit node is called a single event transient (SET).

This effect has been mainly analysed in digital circuits [4]-[11], with considerably less attention paid to analog and mixed-signal circuits in high radiation environments. This is explained by the fact that digital circuits are generally implemented with minimum transistor sizes, while transistors in analog circuits tend to be larger. However, analog circuits have been receiving more attention in recent years due to device scaling. This work focuses on the study of SETs in analog radio-frequency (RF) circuits, as well as proposing techniques which mitigate the effects of radiation.

Usually, in order to carry out SET analyses, experimental measurements are performed in laboratories equipped with laser beam testing and other ion-inducing devices [2], [12]. However, this equipment will mean high costs both financially and time-wise. As an alternative, simulation tools provide the means to predict the behaviour of analog circuits in harsh environments. A practical way to analyse the effect of SETs in circuits is to perform transient simulations. Despite the time required for this kind of studies [2], these simulations give an approximation of how the circuit's parameters are affected without needing to perform expensive experimental measurements using heavy ion or laser strikes.

In CMOS circuits, the effects of SETs are usually simulated with a current source connected at the reverse-biased *n-p* junction of the transistor (which corresponds to the drain). Typically, the current pulse generated by this source follows a double exponential function, such as the one shown in Equation 1.1:

$$I_{rad} = \frac{Q}{t_f - t_r} \cdot \left(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}} \right) \tag{1.1}$$

where Q is the collected charge, while t_f and t_r are the fall and rise time, respectively. This current pulse is introduced in an electrical circuit domain simulation tool, where transient simulations are performed.

In order to obtain a more accurate model of this double exponential function, a technology computer aided design (TCAD) physics-based software can be used [13]. It is known that these tools provide the means to simulate the effects of radiation on physics parameters of semiconductor devices and are widely used to predict the response of these devices to incident radiation.

In [14], a review of techniques for physics-based device level simulation of SEEs in silicon based microelectronic devices and integrated circuits is given. It is known that the simulation of radiation effects can be approached at different levels:

1. Interaction of ionising particles with matter.
2. Physical device simulators that estimate the response of devices to incident radiation.
3. Circuit simulators that model circuit response to a single event effect.
4. Codes that predict the error rate that will be observed.

The physics-based device simulators typically follow the drift diffusion model, where the Poisson and the current continuity equations are discretized and solved on a mesh using finite-element techniques. Due to the computational efficiency of these models, the physics-based simulators have become a popular simulation tool, even for deep submicron devices.

For example, in [15] TCAD simulations are performed to investigate the effects of SETs in SOI RF CMOS technologies. In this case, the *Sentaurus* TCAD tool by *Synopsys* is used to calibrate the device models and verify the results obtained in laser inducing experiments.

Studies on silicon germanium (SiGe) heterojunction bipolar transistors (HBTs) have proliferated in recent years [16], [17]. Similarly as in Si CMOS transistors, both conventional bulk and silicon on insulator (SOI), TCAD tools are also used to simulate the effects of radiation in SiGe HBT devices.

These same studies can be replicated in non-silicon-based devices, like the one performed in [18], where the electrical behaviour of COTS gallium nitride (GaN) transistors under heavy ion irradiation is studied using the *Sentaurus* TCAD tool.

In this work, the *Sentaurus* TCAD tool is used to model CMOS semiconductor devices and perform ion strike simulations. The results obtained in these simulations will then be used to refine the circuit simulations performed in an electrical circuit domain simulator. In this case, the *Advanced Design System* (ADS) software by *Keysight Technologies* has been used. This way the accuracy of the device solver is combined with the fast simulations performed in the circuit simulator. This methodology has been proven by [17], where a close agreement between the simulation and experimental results is obtained. Therefore, it can be stated that the methodology presented in this reference can be applied for any other RF circuits.

1.2 Objectives

The aim of this research is to analyse how analog radio-frequency (RF) circuits behave in radiation environments. The results of the present work are integrated in the research project named Design of Communication Circuits under Radiation (ComRad). This project has been partially funded by the Spanish Ministry of Economy and Competitiveness (TEC2015-71072-C03-01), by the Spanish Ministry of Science, Innovation and Universities (RTI2018-099189-B-C22), by the Canary Agency for Research, Innovation and Information Society (ACIISI) of the Canary Islands Government (ProID2017010067) and the "Programa Predoctoral de Formación del Personal Investigador" of the ULPGC.

In order to achieve the main aim, the following milestones have been established and achieved:

- **Understanding the effect of radiation on semiconductor devices**. It is important to fully understand the different radiation sources and their effects on electronic systems before analysing RF circuits under radiation.
- **Analysing the effect of radiation on CMOS technologies**. As it has been mentioned previously, the RF circuits studied in this work have been designed using CMOS technologies. Therefore, CMOS devices must be studied under the effect of radiation.
- **Modelling of the transistors**. In order to study the effects of radiation in RF circuits, first the basic elements of such circuits must be studied. To do so, TCAD tools are used to model the transistors and analyse their response to ionizing particle strikes.
- **Analysing the effects of radiation on individual RF circuits**. In this case, low noise amplifiers are studied under the effects of radiation. Additionally, the effect on down-conversion mixers is also studied.

- **Analysing the effects of radiation on RF systems**. It is important to analyse how the effects of radiation in an analog RF circuit impacts the performance of a whole RF system, such as a RF receiver. One approach to perform this study is to analyse the distortion produced in the constellation diagram of an RF system under the effects of radiation [19]. However, in order to be able to perform this study, the symbol period of the system and the duration of the radiation effect must be in the same order of magnitude. This is not always the case, as it will be demonstrated in this work, which leads to the necessity of using some other kind of study. In this dissertation, a procedure focused on the analysis of the voltage signal at critical nodes of the system, checking for possible variations of the signal, is proposed.

1.3 Outline of the research

This work is organized in seven chapters. The first and current chapter introduces the motivation of this research and establishes the research objectives. *Chapter 2* presents an overview of radiation effects in microelectronic systems. The different radiation sources are studied and their effects on semiconductor devices explained. In *Chapter 3*, the effect of radiation on transistors of different technologies are studied. To do so, a TCAD tool has been used to model the transistors and to study the effect of a heavy ion striking the device. The information obtained in these simulations is then used for the analysis of the effects of radiation in analog RF circuits. This is done in *Chapter 4*, where low noise amplifiers are studied under the effect of radiation. Additionally, radiation hardening by design (RHBD) techniques have been applied at the most vulnerable nodes of the designed low noise amplifiers. After radiation effects have been studied in analog RF circuits, the next step consists in analysing a microelectronic system. In this case, RF receivers are considered. In *Chapter 5*, the designed receivers are presented and some of the design decisions taken during the process are discussed. *Chapter 6* is devoted to analysing these RF receivers under the effects of radiation. Finally, some conclusions and areas of further research are presented in *Chapter 7*.

Chapter 2

RADIATION EFFECTS OVERVIEW

In this chapter, a background of radiation and its effects on microelectronic systems that operate in harsh radiation environments is presented. Firstly, the different radiation sources present in space are studied. Secondly, the effects that these sources have on electronic devices is analysed. Total ionizing dose and displacement damage effects are briefly addressed, since this research focuses on single event effects and how to mitigate them. A special attention is given to these effects on analog circuits. Finally, a review of mitigation techniques is presented.

2.1 Radiation sources

In this section, a brief description is given of the different radiation sources present in space environments, which can be divided into two major groups: radiation trapped in the magnetic fields of most planets and the transient radiation environment [20]. Additionally, the environment that a spacecraft or satellite will face depends on different variables such as the solar cycle, the orbital path and the duration of the orbit. In this regard, there are four different types of earth orbits: low earth orbit (LEO) which is encountered below an altitude of 10,000 km, medium earth orbit (MEO) which can be found between 10,000 to 20,000 km, geostationary orbit (GEO) at 36,000 km and highly elliptical orbit (HEO). The particle sources, types and intensities found in these orbits varies depending on the type of orbit. To make sure that a satellite can operate in this harsh environment, the different space radiation sources and their interactions with electronic devices must be studied [21].

2.1.1 Van Allen Belts

The Van Allen belts represent an area of the magnetosphere with a high density of trapped ionizing particles. These particles are ejected from the sun in the form of solar winds and are confined by the Earth's magnetic field, forming what can be approximated as a toroid around the Earth's surface, with the Earth at the centre and the Earth's magnetic pole defining the toroidal axis [20], as shown in Figure 2.1. This environment is mainly composed of electrons, protons and low energy heavy ions which spiral around the magnetic field lines.

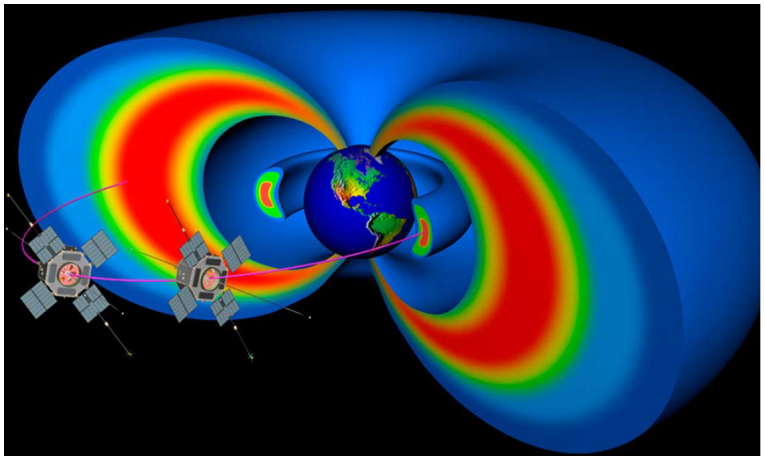


Figure 2.1. An illustration of the Van Allen radiation belts [3].

The electrons of the Van Allen belts can be divided into two main areas: the inner belt and the outer belt. The former is found at an altitude between approximately 1,000 and 15,000 km over the Earth's surface, while the latter includes a zone that ranges from about 17,000 to 60,000 km above the surface [21].

A special region of the Van Allen belts is the one known as the "South Atlantic Anomaly" (SAA) [22]. This region can be found off the coast of Brazil and is formed by a depression of the Earth's magnetic field. This represents a troublesome characteristic since in this zone the trapped proton particles can be found at altitudes as low as 200 km above the Earth's surface. As a consequence, this must be considered specially for LEO applications.

2.1.2 Transient radiation environment

As opposed to the particles trapped in the Earth's magnetic field, there is another radiation source formed by particles which are traversing through space. This is known as the transient radiation environment. There are many types of radiation sources that compose the transient environment. However, the two main contributors to this environment are the galactic cosmic rays (GCRs) and particles emitted during solar events [20].

Galactic cosmic rays originate from outside our solar system and are mainly composed of protons, with electrons, alpha particles and heavy ions also present. The spectral distribution of elements in GCRs is shown in Figure 2.2. The energy of these ions peaks around 1 GeV/nucleon near the Earth. Taking into account their high energies, these particles can be particularly harmful for electronic systems. Therefore, it is not possible to use aluminium plating with reasonable thickness as shielding.

Regarding the radiation produced by the sun, two different events can be distinguished: coronal mass ejections (CMEs) and solar flares. CMEs are events that

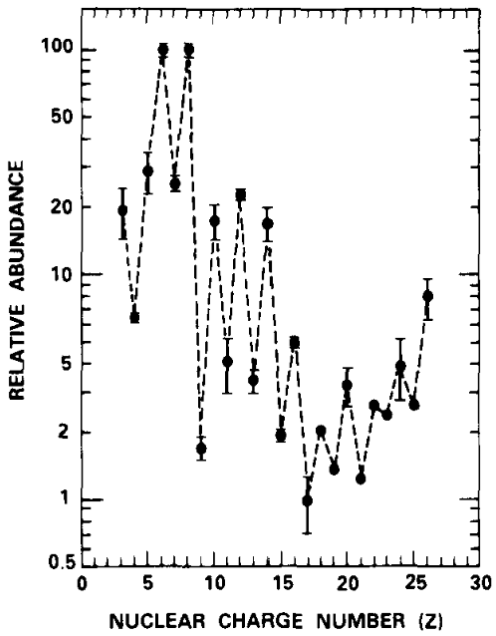


Figure 2.2. Relative distribution of elements contained in galactic cosmic rays [23].

have a high probability of producing protons that reach the Earth. Regarding solar flares, they are characterised by having a high density of heavy ions. These events occur periodically, following the solar cycles which have a peak of maximum activity roughly every 11 years [20].

2.2 Radiation effects

Radiation effects can be divided in three main categories: activation by nuclear reactions, displacement damage effects and ionizing effects [24]. All of these effects should be taken into account when designing electronic systems for radiation environment applications. However, as mentioned previously, this thesis is focused on the analysis of single event effects in analog circuits. Therefore, in this chapter only a brief overview of the rest of the phenomena is presented.

2.2.1 Activation by nuclear reaction

This effect is produced when stable nuclei are exposed to a flux of energetic particles, becoming unstable and radioactive due to nuclear reactions. This effect can be produced by proton fluxes, electrons, neutrons and ions. Nonetheless, the most common reaction produced in space radiation environments is due to high energy protons. Specifically, the major source of this type of reaction is located at altitudes of the equator of the inner Van Allen belt, with energies that go from 30 to 400 MeV. For other altitudes, GCRs become the most important source of activation [25].

2.2.2 **Displacement damage effects**

This phenomenon occurs when particles pass through a semiconductor device. This leads to elastic collisions of the particle with atoms in the crystal lattice, which can result in displacement damages. This displacement of a lattice atom leaves a vacancy, which affects the periodicity of the crystal structure. This allows new energy states or energy traps in the band gap of electrons in the semiconductor, which in turn affects the charge carriers mobility [25].

2.2.3 **Ionizing effects**

When an ionizing particle strikes a semiconductor device with sufficient energy, the particle penetrates the device. As the particle traverses the bulk of the semiconductor device, the particle loses energy and doing so, creates electron-hole pairs (see Figure 2.3). This electron-hole pairs generation is the source of both total ionizing dose (TID) and single event effects (SEEs), which will be covered in the following sections.

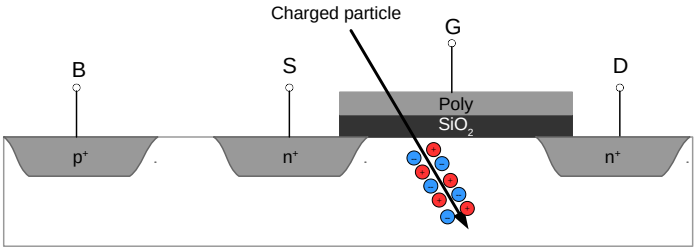


Figure 2.3. Illustration of an ionizing particle creating electron-hole pairs as it traverses a semiconductor device.

2.2.3.1. Total ionizing dose effects

The generated electron-hole pairs quickly recombine as they are transported by drift-diffusion mechanisms. However, charge generated in dielectric layers and interfaces remains trapped for long periods of time. This leads to total ionizing dose (TID) effects appearing when semiconductor devices are exposed to radiation for a long period. The total dose absorbed in the device is usually given in units of *rads* and is related to the amount of ionization [1].

In CMOS devices, the aging and degradation of the electrical performance is primarily produced by the charge generated in the gate oxide. The accumulated charges eventually impact the CMOS performance by decreasing the threshold voltage (V_{th}) and in an increase of the leakage current between the source and the drain of CMOS transistors.

It should be noted that for modern CMOS processes, where the gate lengths have been considerably reduced, the gate oxide is thin enough to prevent trapped charge from appearing due to the quantum tunnel effect. This translates into processes becoming inherently more robust against TID [1], [25].

2.2.3.2. Single event effects

Single event effects are another type of radiation effect generated by the ionization produced by a particle traversing a semiconductor material. In this case, they occur when a heavy ion impacts a semiconductor device. There are two different mechanisms that cause SEEs: charge deposition and charge collection.

The first mechanism is produced when an incident particle deposits charge in a semiconductor device. This charge deposition can be generated in two different ways: direct ionization and indirect ionization. Both of them can generate single event effects [26].

Direct ionization takes place when an ionizing particle (e.g. heavy ion or proton) traverses a semiconductor device and loses energy in the process. This frees electron-hole pairs, until it loses all its energy in the device. The total number of charges are proportional to the linear energy transfer (LET) of the impacting ion and to the density of the material (silicon in this case). LET is defined as the amount of energy deposited per unit of distance as the particle passes through the device. It is commonly expressed as MeV·cm^2/mg. LET is obtained by normalizing electronic stopping power S, by the specified material density (see Equation 2.1)[22]. Additionally, the LET of a particle is related to the charge deposition per unit path length. For example, in silicon, a LET of 97 MeV·cm^2/mg corresponds to a charge deposition of 1 pC/μm [27].

$$LET = \frac{S}{\rho} = \frac{\frac{-\mathrm{d}E}{\mathrm{d}x}}{\rho} = \frac{MeV/cm}{mg/cm^3} = \frac{MeV \cdot cm^2}{mg} \tag{2.1}$$

Direct ionization caused by heavy ions is the primary charge deposition mechanism that causes single event upsets (SEUs). Nonetheless, protons and lighter particles can cause SEUs by direct ionization in modern technologies due to them becoming more sensitive with process scaling [26], [27].

Regarding indirect ionization, it can be produced by light particles such as protons and neutrons. When high-energy protons or neutrons strike a semiconductor device, they interact with its lattice and suffer elastic or inelastic collisions with a target nucleus. This results in the possible generation of several nuclear reactions. The products from these reactions are able to deposit energy along their paths by direct ionization. These particles are considerably heavier than the original proton

or neutron. Therefore, they deposit higher charge densities as they travel, so they are capable of causing SEUs [27].

The second mechanism that can cause SEEs is charge collection. When a heavy ion strikes a semiconductor device, they impact the lattice structure of the semiconductor, transferring energy to it and leaving free electron-hole pairs in the process. It becomes specially problematic when the reverse-biased junctions of a semiconductor device are struck. In the case of NMOS transistors, this corresponds to the *n*-*p* junction of the drain to substrate, while for the PMOS transistors it is found in the *p*-*n* junction of the drain to substrate. This phenomenon can be explained by the fact that electron-hole pairs are separated due to the electric field before they are able to recombine. This electric field is generated from the reverse-biased *n*-*p* junction voltage potential, which causes electrons to be carried to the n-diffusion region and holes to be swept to the bulk contact in NMOS transistors. This is known as charge collection [1].

Figure 2.4 shows an illustration of an NMOS transistor when impacted by a heavy ion. Figure 2.4 (a) shows how the energetic particle passes through the drain of an NMOS transistor and generates electron-hole pairs. The generated charges are absorbed by the potential of the drain and bulk nodes of the NMOS transistor, as it can be seen in Figure 2.4 (b). This leads to the generation of a transient current pulse that flows from the drain to the bulk in NMOS transistors (Figure 2.4 (c)). This translates into the transient current pulse charging or discharging the potential on a critical node of an electronic circuit, thus modifying the logic level of these nodes [1].

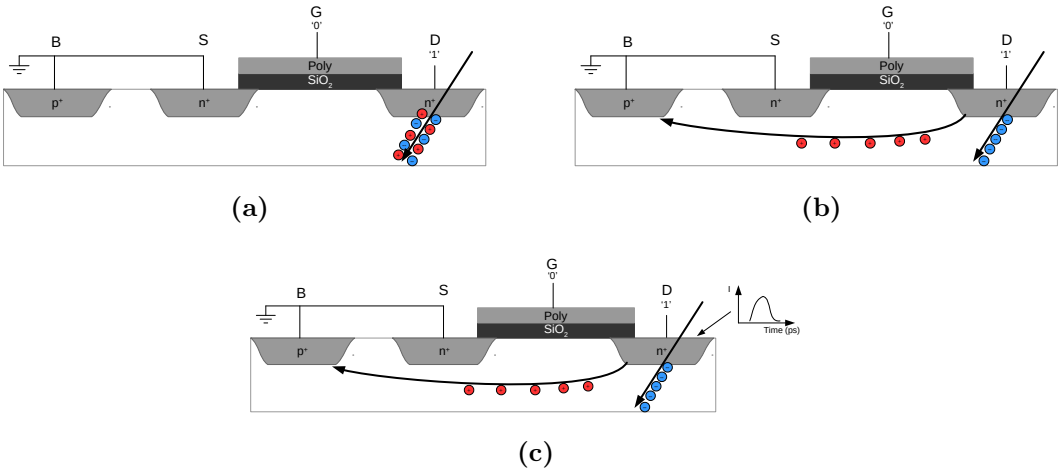


Figure 2.4. Illustration of SEE generation process: (a) Charge generation (b) Charge collection (c) Circuit response.

As it was mentioned previously, TID effects cause a gradual degradation of the performance of a semiconductor device. However, single event effects have an instantaneous impact on circuits. SEEs are usually referred to as soft errors, since they typically do not inflict a permanent damage to circuits [1]. SEEs can be divided into two main types of effects: non-destructive and destructive effects. The

most important single event effects that fall under the category of non-destructive are [26], [22]]:

- **Single Event Upset (SEU):** This effect is produced when the information stored in a memory cell is corrupted due to the strike of a high energy particle. Memory cells and latches in logic devices are typically the circuits affected by SEUs.
- **Multiple Bit Upset (MBU):** It is produced when several memory elements are corrupted by a single strike. This effect has become more problematic due to down-scaling in modern processes.
- **Single Event Functional Interrupt (SEFI):** This effect appears when there is an ion strike in an integrated circuit test mode, reset mode or some other mode that leads to the temporarily loss of the IC's normal operation. It affects complex devices with built-in state machine/control sections.
- **Single Event Transient (SET):** It is described as a transient response corruption of certain amplitude and duration that can cause errors or failures in subsequent circuits. They are of major concern for analog and mixed/signal circuits. This effect will be studied in further detail in the following section.

Regarding destructive single event effects, they include:

- **Single Event Gate Rupture (SEGR):** This effect occurs when there is a breakdown of the gate dielectric of a MOSFET due to an ion strike. This creates a conducting path through the gate oxide, which leads to an increase in gate leakage current and can result in device degradation or complete failure.
- **Single Event Latchup (SEL):** It is produced by a high-current state that causes a digital component to malfunction.
- **Single Event Burnout (SEB):** SELs that result in overcurrenting and catastrophic failure are called SEBs. As a result, the device operation ends in a damaging burnout.

2.3 Single event effects in analog circuits

In analog circuits, SETs are the most problematic SEE that need to be mitigated [1]. In digital circuits, SETs need to overstep the gate threshold to propagate. However, in analog circuits even a small pulse induced by a SET can produce a considerable degradation of the circuits' performance. As an example, a small pulse in a current mirror can significantly modify the performance of a circuit. Accuracy

in current mirrors is really important since they provide the current bias of the circuit. Taking this into account, a slight variation of the bias current can lead to a modification of the circuit response due to the transistors being deviated from their operating point. This leads to a degradation of the circuit performance, affecting parameters such as voltage gain, bandwidth, voltage swing or noise [1].

Additionally, the propagation of SETs in analog circuits and fault generation in this type of circuit depends more on the interpretation of the signal than in digital circuits. This can be explained by the fact that an incorrect logic state is defined in digital circuitry. However, for analog circuits there is no metric for analog SEEs. Thus, the severity of the phenomenon is only known once it propagates until the end of the signal processing chain [28].

Nevertheless, it can be established that both the frequency characteristic and the absolute magnitude of SETs are relevant to the severity of the system response. However, the severity is application-dependent. As an example, a short pulse in the time domain that has a large voltage magnitude peak may be filtered and, thus, have a smaller impact on the system performance than a wider pulse and smaller voltage peak. However, in another application a long pulse with small voltage peak may not surpass the noise tolerance of a receiver, resulting in a smaller importance in the system response.

Taking this into account, it is common practice to study the effect of SETs in analog circuits by generating *amplitude/pulse-width* scatter plots. This type of plot shows the signal in a critical node in terms of peak amplitude and disturbance duration. As mentioned previously, both of these metrics are important to analyse the SET response of analog circuits. In this plot, a designer-defined safe operating area can be defined in order to establish *upset* thresholds for SETs in analog circuits [28], as shown in Figure 2.5.

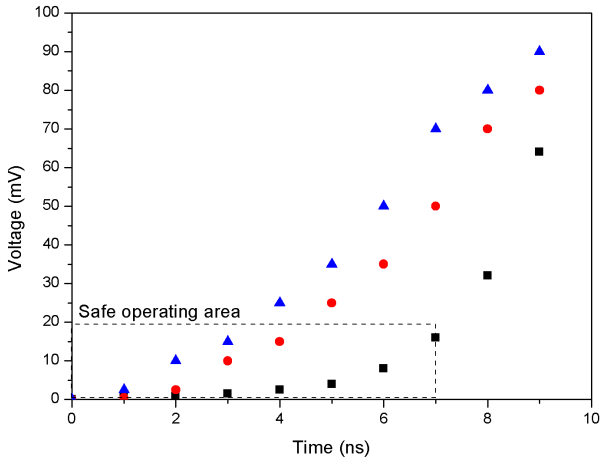


Figure 2.5. Example of pulse duration versus peak voltage magnitude scatter plot for an analog/mixed signal circuit.

2.4 Mitigation techniques

Conventionally, there are three hardening techniques which can be applied to develop extreme environment electronics: radiation hardening by process (RHBP), radiation hardening by reconfiguration (RHBR) and radiation hardening by design (RHBD). A combination of these three techniques can be implemented in order to design robust against radiation circuits [29].

An example of an RHBP technique consists of fabricating electronic devices with specific materials that posses a higher tolerance to high radiation environments. This results in what is known as rad-hard technologies. RHBP techniques have the benefit of being considerably reliable in order to obtain hardened devices. However, they have the drawback of high manufacturing costs, low yield and process instability [29].

In RHBR approaches, reconfigurable devices such as field programmable gate arrays (FPGAs) are employed. For example, when device parameters are altered due to radiation conditions, new parameter values for a new circuit design will be mapped into the system to restore the original circuit performance. The use of this type of technique may result in an increase of the size and complexity of the system.

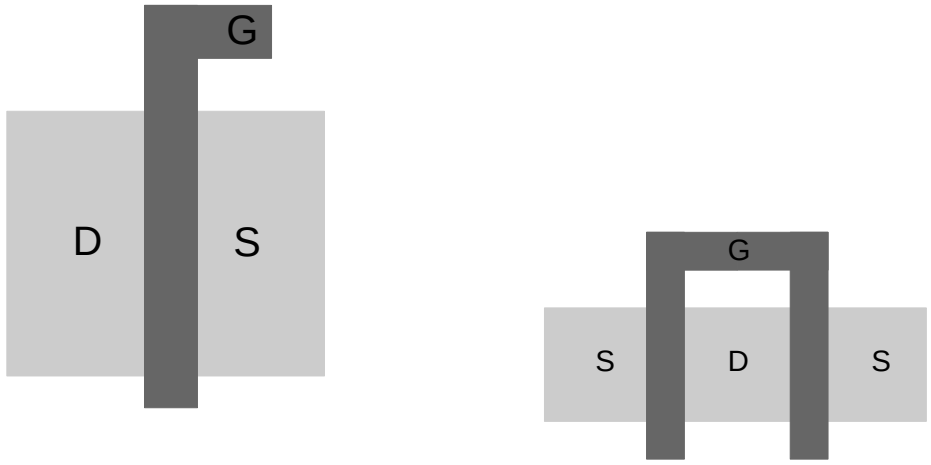
Regarding RHBD techniques, they can be applied both at transistor or circuit level. RHBD techniques at transistor level consist on modifying the structure of a standard transistor, while at circuit level implies the use of a special design or compensation mechanism. RHBD techniques have been thoroughly studied in digital circuits as a cheaper alternative compared to the other approaches. However, in analog RF circuits these techniques are less covered in the literature.

Some of the most common RHBD techniques include [30]:

- **Reducing the cross section of generated SETs:** Cross section is an area measurement of the region where an ion passing through the region can generate a SET. The cross section is the area of the semiconductor seen from the top of the device. The first RHBD approach to reduce the SET cross section is to minimise the semiconductor area of the transistor. The second method is to employ transistor folding, as shown in Figure 2.6. This way the area of the drain is halved, even though the W/L ratio is the same in both transistors.

  The third approach consists in having a low resistance contact to the body of the transistor. This low resistance contact allows the potential in the body to remain constant and facilitates a path to remove the excess current.

- **Reducing the duration of generated SETs:** Short SETs have a lower probability of being captured in a memory circuit. A way to reduce the length of SETs is to reduce the collected charge. Thus, the techniques presented for



(a) **(b)**

Figure 2.6. Top view of a transistor layout (a) Conventional transistor (b) Folded transistor.

the reduction of cross section will also reduce the duration of SETs. Another approach to reduce the duration of SETs is to increase the capacitance of nodes. This means that more charge is required to overcome the stored charge in the capacitance to start the transient.

- **Mitigating SETs in propagating circuits:** The first RHBD technique to mitigate the SETs duration during propagation in combinational circuits consists in placing a high resistance between the combinational logic nodes to create a low pass filter. This reduces the impact of high frequency voltage transients. The second approach is to use a guard gate, which is simply a two input inverter. If the output of a combinational logic circuit is introduced in both inputs of the guard gate (one with a direct input and the other with a controlled delay) the SET must be longer than the delay to propagate through the guard gate.

- **Mitigating SETs in memory circuits:** Most of the RHBD techniques implemented to mitigate SETs in memory circuits follow the same principles as the ones exposed for the previous cases. In general, the idea is to increase the minimum voltage duration that is considered an acceptable signal. For example, inserting resistors in the memory storage element will require inputs to last longer for the storage cell to be overwritten.

- **Mitigating SEUs through redundancy:** Taking into account that SEUs affect memory elements by changing a memory state, the redundancy can be of two types: spatial or temporal.

  Spatial redundancy consists of having more than one storage node for the

memory. An example would be to duplicate a dynamic random access memory (DRAM) cell and program both in the same way. For static random acces memory (SRAM) cells, there are two spatial redundancy techniques. The first is named Dual Interlocked Cell (DICE), where the number of transistors for the memory storage is doubled. This technique is effective against single event effects that affect only one node, but are vulnerable against single events that affect multiple nodes. The second spatial redundancy approach is triple modular redundancy. In this technique, the circuit design is tripled and majority voting is used to choose the correct output.

In temporal redundancy techniques, three copies of the desired digital state are created in time. An example of this technique is the circuit known as temporal latch, where three copies of the data are created in time and majority voting is used to select the data.

2.5 Conclusion

In this chapter, an overview of radiation and its effects on microelectronic systems has been presented. Firstly, the different radiation sources present in space have been analysed. Radiation sources can be divided into two main groups: radiation trapped in the magnetic field of planets and transient radiation environment. The Van Allen belts represent the ionizing particles trapped in the magnetic field of the Earth. The South Atlantic Anomaly represents a problematic region of the Van Allen belts, since it can be found at smaller altitudes form the Earth's surface compared to the rest of the belts. Regarding transient radiation, the two main contributors are galactic cosmic rays and particles emitted during solar events.

Once the radiation sources were studied, the different radiation effects on semiconductor devices have been analysed. There are three main categories: activation by nuclear reaction, displacement damage and ionizing effects. The latter is the aim of this research, which occur when an ionizing particle strikes a semiconductor device with enough energy to penetrate the device. As the particle passes through the device, electron-hole pairs are generated, which are the source to both single event effects and total ionizing dose effects. In this work, special attention has been given to single event effects rather than to total ionizing dose effects. The different types of single event effects have been presented in this chapter.

Finally, some common mitigation techniques were presented, with focus on radiation hardened by design techniques.

In the following chapters, the effect of single event transients in RF analog CMOS circuits is further studied. To do so, first the effect on a CMOS transistor is analysed in the following chapter before analysing complete circuits and RF receivers.

Chapter 3

RADIATION EFFECTS IN SEMICONDUCTOR DEVICES

In this chapter, the effects of radiation in semiconductor devices are studied. As mentioned in previous chapters of this document, the main aim of this research is to analyse how analog radio-frequency (RF) circuits behave in radiation environments. To do so, the first step is to study the effect of radiation on the basic elements of such circuits, the transistors. As explained in *Chapter 1*, a widely used methodology to study the effect of radiation in semiconductor devices is to employ a technology computer aided design (TCAD) physics-based software. This type of tool provides the means to simulate the effects of radiation on physics parameters of semiconductor devices and are widely used to predict the response of these devices to incident radiation.

The circuits designed in this research, which will be presented in following chapters, are based on a complementary metal-oxide-semiconductor (CMOS) technology. Therefore, a TCAD tool has been used to model semiconductor devices of the 0.18 μm CMOS technology by UMC. Once the transistors have been correctly modelled, the effect of a heavy ion striking the device has been studied with the TCAD tool. The information obtained in these simulations will be used later on in the analysis of the effects of radiation in analog RF circuits.

As explained previously, the main aim of the research is to examine the effect of radiation in CMOS technologies. However, in the course of the research, a high performance gallium nitride (GaN) technology became available for the research group. This represents a unique opportunity to complement the analysis performed on CMOS devices in this research. Hence, the study of the effects of radiation on GaN devices has also been included in this chapter.

3.1 Analysis of CMOS technology

3.1.1 Transistor modelling

The *Sentaurus Structure Editor* (SDE) tool by *Synopsys* was used to model the 0.18 μm CMOS technology transistors. This tool provides a graphical user

interface which aids the design of 2D and 3D devices. The geometric shape and device parameters, such as doping concentration, can be defined with this tool [31]. The transistor dimensions were obtained from the UMC documentation and the layout masks. Figure 3.1 shows the dimensions for a minimum gate length NMOS transistor. This information is used in the modelling performed in this section.

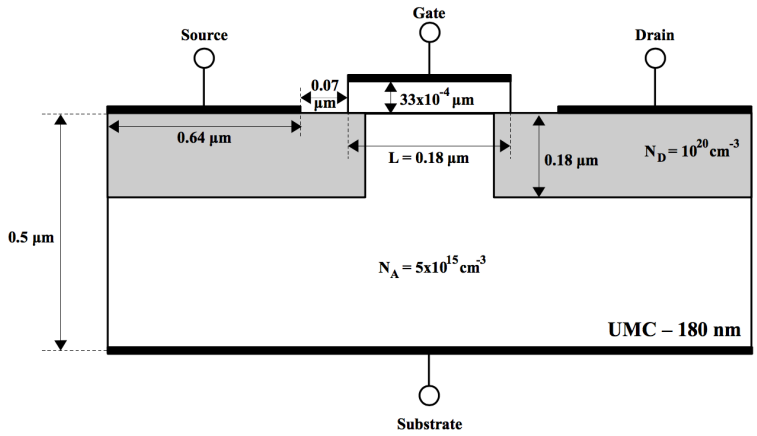


Figure 3.1. Dimensions of the transistor used in the modelling.

This transistor dimensions must be transferred to the *Sentaurus Structure Editor* tool. To do so, the different regions of the transistor have been defined by coordinates. In this case, the origin has been set in the middle of the device, since it is symmetrical with respect to the y-axis. The contacts must also be defined in the model. These are the gate, drain, source and bulk contacts. A structure like the one shown in Figure 3.2 is obtained at this point.

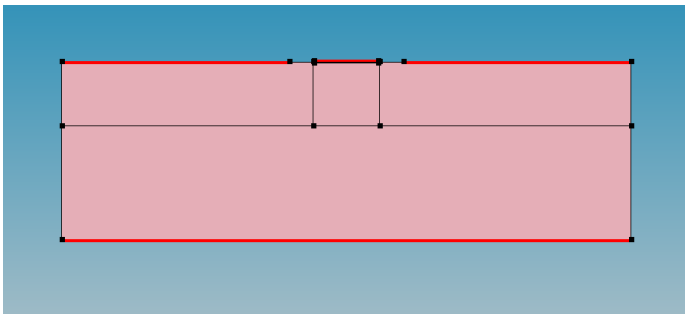


Figure 3.2. Regions and contacts of the transistor defined in the *Sentaurus Structure Editor* tool.

Once the geometry of the transistor has been defined, the doping concentration of the different regions and the mesh were specified. In this case, the substrate had a boron doping concentration of 5×10^{15} cm^{-3}. It is worth noting that the value of this parameter is not provided by the technology. Therefore, the parameter was swept until the performance of the model matched that of the transistor provided by the technology. For the sake of simplicity, only the final value is shown. This parameter is introduced in the SDE tool in a dialog box like the one shown in Figure 3.3. It should be noted that for this technology the material of the substrate must be set to silicon (Si).

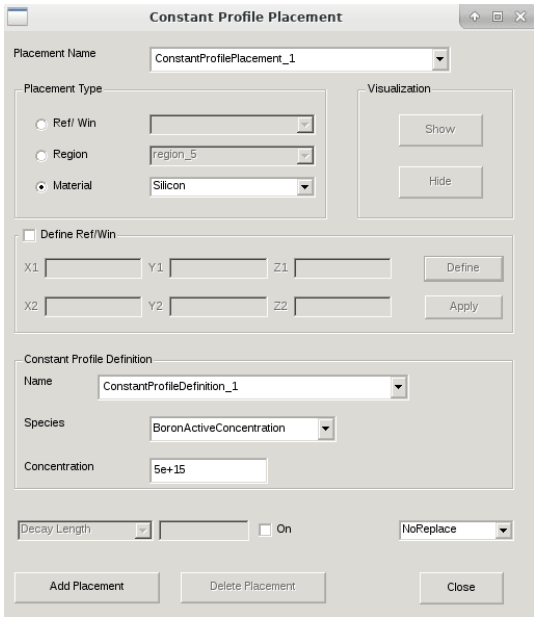
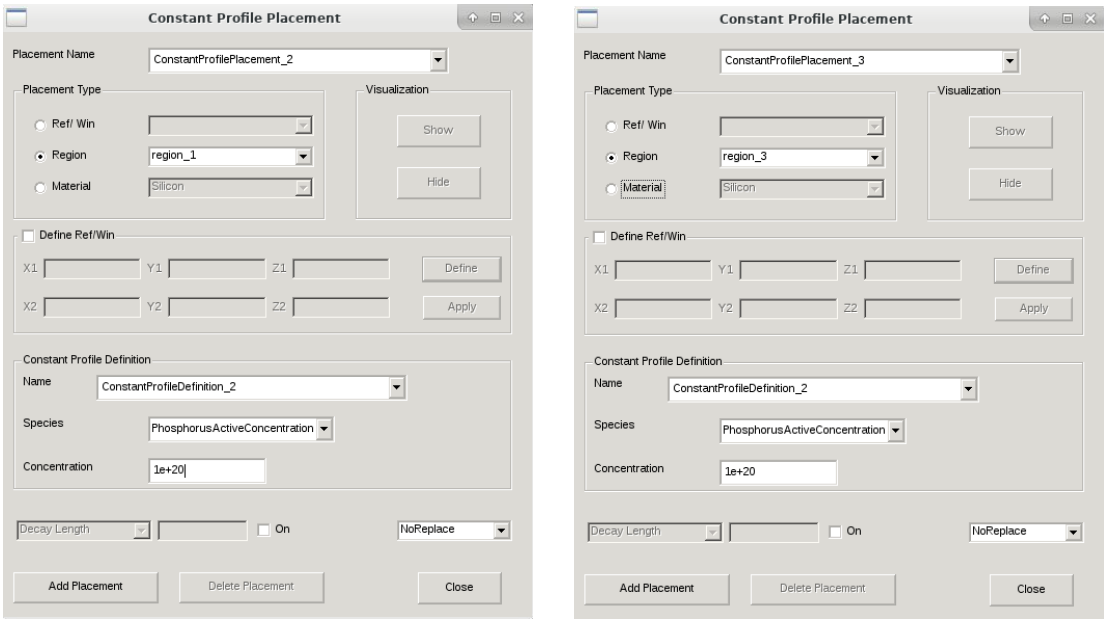


Figure 3.3. Substrate doping definition.

In a similar way, the doping of the source and the drain is set. In this case, they were doped with a phosphorus concentration of 1×10^{20} cm^{-3}. Figure 3.4 shows the dialog boxes where the source and drain dopings are defined.



(a) **(b)**

Figure 3.4. Doping definition for the (a) Source (b) Drain.

Until this point the doping has been set as constant in the whole region. However, a Gaussian distribution has to be defined in the source and drain regions. To do so, a reference line must be defined in each of these regions. This simulates the effect of the diffusion of the doping which allows the channel formation. Figure 3.5 shows the dialog boxes where the Gaussian distributions are set.

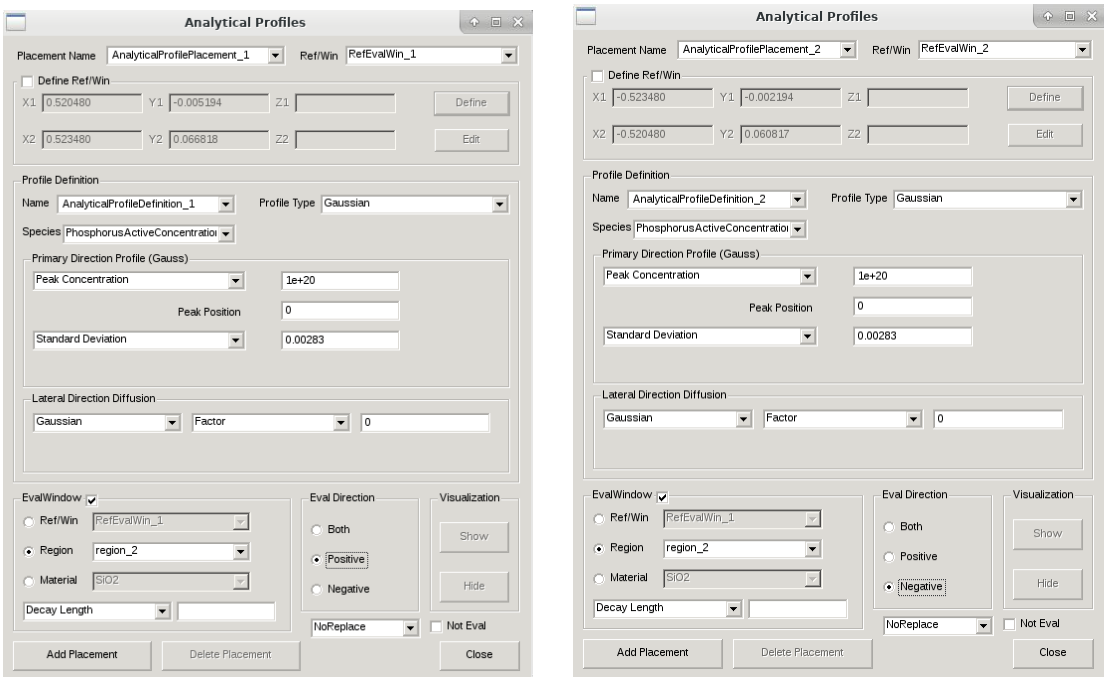


Figure 3.5. Gaussian distribution definition for the (a) Source (b) Drain.

Finally, the meshing of the device is performed. Refinements of the Gaussian distribution, the electrostatic potential in silicon and the concentration of electrons in the channel were performed, as shown in Figure 3.6.

Once the meshing conditions have been defined, the model can be generated. Figure 3.7 (a) shows the obtained meshing of the modelled transistor, while Figure 3.7 (b) shows the the electron density in the 2D extruded model of the transistor generated with the SDE tool.

In order to calibrate the designed model, the characteristic *I-V* curves have been calculated and compared to those given by the technology, which have been obtained from the UMC design kit for ADS. To perform these electrical simulations at device level, the *Sentaurus Device* (SDEVICE) tool has been used. Figure 3.8 shows the drain current against the gate voltage for two different drain voltages, both in a linear and a logarithmic scale. As it can be seen, the curves generated with *Sentaurus* match those provided by the technology. In the logarithmic scale it can be seen that the curves slightly differ at sub-threshold voltages. However, this difference is not problematic if the transistors of a specific circuit are biased with higher voltages in order to operate at moderate or strong inversion regions. This is the case of the circuits presented in the following chapters.

To achieve these results, parameters like the doping concentration, electron mobility and hole mobility had to be modified. First, the threshold voltage is fixed by modifying the work function of the gate and the doping concentrations of the substrate. As mentioned before, the substrate had a boron doping concentration of 5×10^{15} cm^{-3}, while the source and drain of the transistors were doped with a

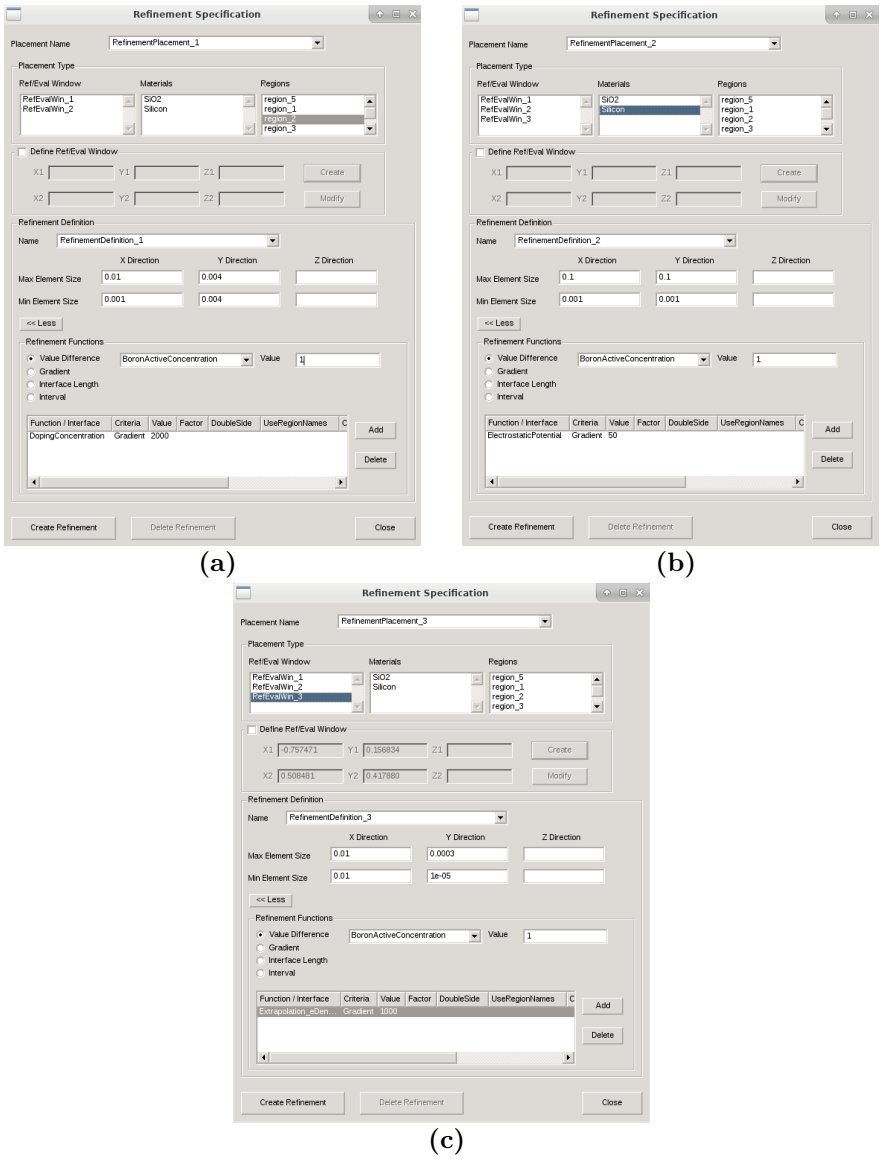


Figure 3.6. Meshing refinement of the (a) Gaussian distribution (b) electrostatic potential in Si (c) electron concentration in the channel

phosphorus concentration of 1×10^{20} cm^{-3}. In order to modify the work function of the gate, the parameter *Barrier* is used. Once the threshold voltage has been set, the transconductance must be modified to adjust the gradient of the curve. To do so, the Lombardi and Canali models were used to define carrier mobilities at low and high fields, respectively. After several simulations, an electron mobility of 500 cm^2/Vs and a hole mobility of 200 cm^2/Vs were obtained. Regarding the Canali model, the parameters β_0 and v_{sat} are used to model the transition from linear to saturation regions and the saturation velocity, respectively. In this case, a β_0 of 1.15 and a v_{sat} of 1.4×10^7 cm/s were obtained [32].

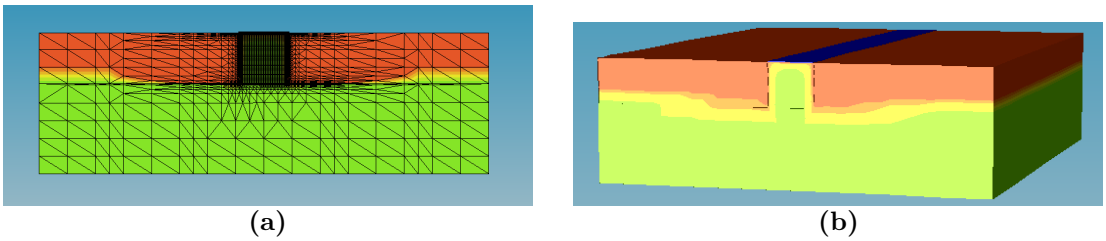


Figure 3.7. (a) Meshing of the model (b) 2D extruded model of the NMOS transistor.

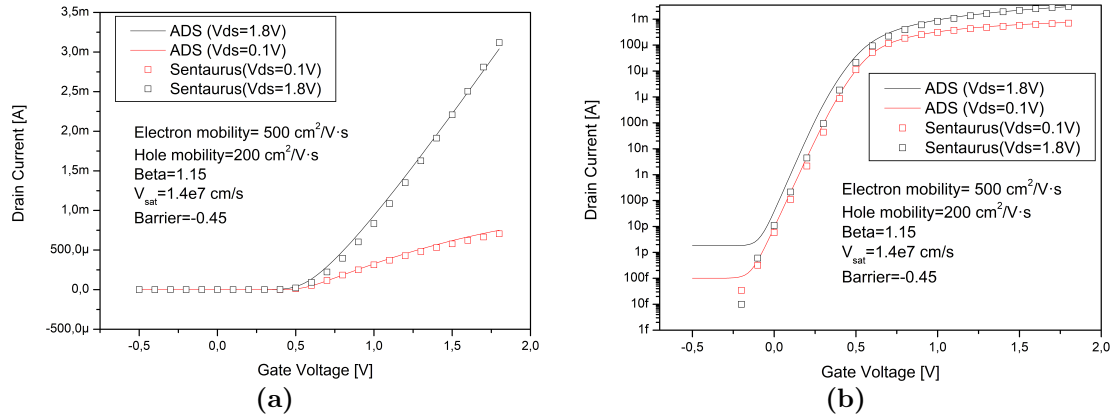


Figure 3.8. Gate voltage versus drain current in Sentaurus compared to the ADS model (a) linear scale (b)logarithmic scale.

3.1.2 Radiation effects in CMOS technology

Once the NMOS transistor of the 0.18 μm UMC CMOS technology has been correctly modelled, an analysis of the effects of a heavy ion impacting the device is performed. The SDEVICE tool presents many different radiation models which simulate the effect of a high-energy particle penetrating a semiconductor device. A commonly used model to perform SET simulations is the heavy ion model [15], [33], [34]. When a heavy ion passes through a device, it loses energy and creates electron-hole pairs. These pairs could generate large enough currents which can translate into SETs.

Some important factors that should be considered in this model are the energy of the ion, the angle of penetration or the relation between the linear energy transfer (LET) and the number of pairs created.

Figure 3.9 shows a simple model for the heavy ion penetration process. The generation rate caused by the pass of the ion through the device follows Equation 3.1:

$$G\left(l,w,t\right)=G_{LET}\left(l\right)\cdot R\left(w,l\right)\cdot T\left(t\right), \tag{3.1}$$

where $R(w,l)$ and $T(t)$ describe the spatial and temporal variations of the generation rate, respectively. $G_{LET}(l)$ is the LET generation rate density, which represents the

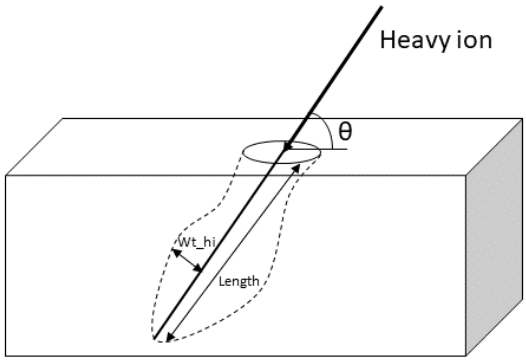


Figure 3.9. Heavy ion penetrating in a semiconductor device.

energy loss of a charged particle due to ionisation and excitation. $T(t)$ is defined as a Gaussian function:

$$T(t) = \frac{2 \cdot e^{-\left(\frac{t-t_0}{\sqrt{2}\cdot s_{hi}}\right)^2}}{\sqrt{2} \cdot s_{hi}\sqrt{\pi}\left(1 + erf\left(\frac{t_0}{\sqrt{2}\cdot s_{hi}}\right)\right)}, \tag{3.2}$$

where t_0 is the instant of the heavy ion impact, s_{hi} is the characteristic value of the Gaussian and *erf* is the Gauss error function.

The spatial distribution $R(w, l)$ can be defined as an exponential function(Equation 3.3) or a Gaussian function (Equation 3.4):

$$R(w, l) = e^{-\frac{w}{w_t(l)}} \tag{3.3}$$

$$R(w, l) = e^{-\left(\frac{w}{w_t(l)}\right)^2} \tag{3.4}$$

where w is the perpendicular distance from the track and w_t is the characteristic distance, which can be a function of the length. In this case, the Gaussian function is used.

The parameters from the heavy ion model that can be modified in the SDEVICE tool are shown in Table 3.1.

Transient simulations were performed for different length, LET and direction values, keeping the characteristic distance and the location constant. Regarding the location of the impact of the heavy ion, it is known that the most sensitive areas of an NMOS transistor to ion impacts are the reverse-biased junctions, which corresponds to the *n-p* junction between the drain and substrate [1]. In this case, the LET ranges from 1 to 30 MeV·cm^2/mg, since LETs as low as 3 MeV·cm^2/mg are

Table 3.1: Heavy ion model parameters

Parameter	Description
Length	Penetration depth of the heavy ion on the device
LET_f	Linear energy transfer function
Wt_{hi}	Characteristic distance
Location	Point where the heavy ion enters the device
Direction	Direction of motion of the ion
Time	Time at which the ion penetrates the device

capable of generating significant transients in a 0.18 μm technology [5]. Regarding the length, simulations were run for values ranging from 0.05 to 0.5 μm. Finally, the angle of incidence from the surface of the device (θ) ranges from 15° to 90°, for the cases of an ion angled towards the gate and away from the gate.

Figure 3.10 shows the current pulse generated at the drain of the modelled transistor due to the impact of a heavy ion. Specifically, the pulse shown corresponds to a LET of 3 MeV·cm^2/mg, a length of 0.18 μm and an angle of incidence θ of 90°.

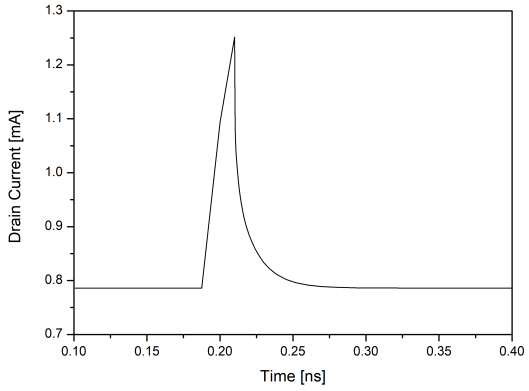


Figure 3.10. Current pulse in the drain of the transistor due to a heavy ion impact.

As it can be seen, the generated pulse has the shape of a double-exponential, which is in concordance with a model for SETs extensively used in the literature, where sensitive nodes are injected with double exponential current pulses that follow Equation 3.5 [1], [13], [26]:

$$I_{rad} = \frac{Q}{t_f - t_r} \cdot \left(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}} \right) \tag{3.5}$$

In this case, the obtained drain current has a maximum peak over the DC offset of less than 1 mA. It should be noted that the current has a DC offset of approximately 0.8 mA because the transistor has been biased with a gate voltage of 1 V and a drain voltage of 1.8 V.

Figure 3.11 shows how the current pulse changes for different values of length and LET, with $\theta = 90°$. It can be seen that as the LET value increases so does the drain current. This can be explained by the fact that an increase in LET means that the number of generated electron-hole pairs increases, translating into a higher current. Similarly, the drain current increases as the length increases.

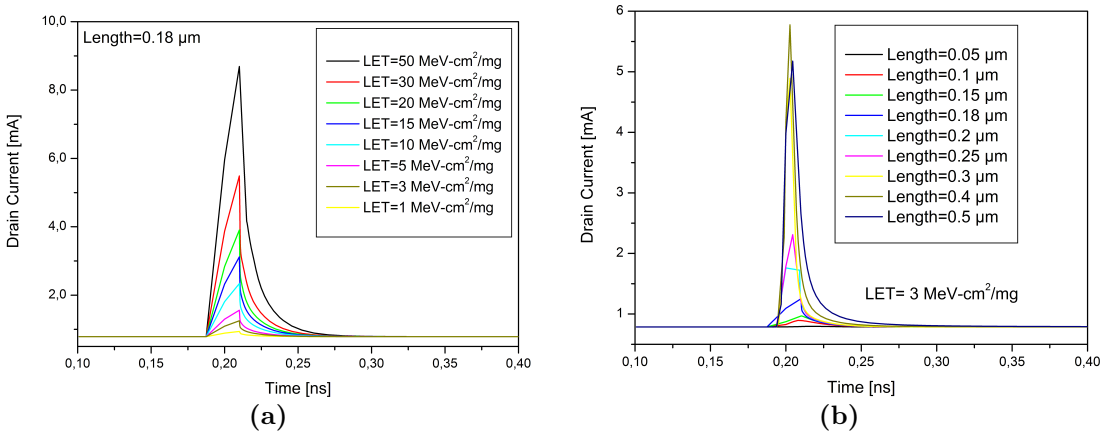


Figure 3.11. Drain current for (a) different values of LET for a constant length (b) different values of length for a constant LET.

Regarding the angle of incidence, Figure 3.12 shows the electron-hole pair generation when θ ranges from 15° to 90°, while the length and the LET are kept constant to 0.18 μm and 3 MeV·cm^2/mg, respectively. It should be noted that a positive value of θ corresponds to a heavy ion angled towards the gate of the transistor, while a negative value represents an angle towards the edge of the device.

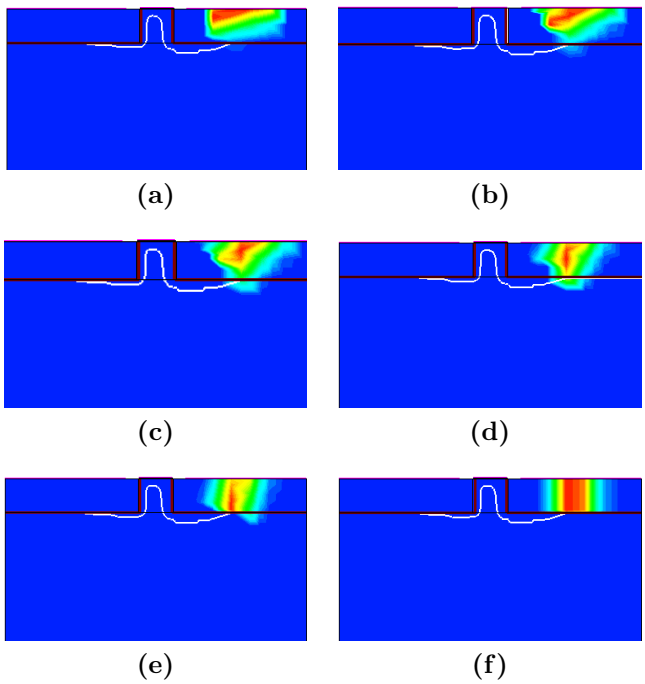


Figure 3.12. Electron-hole pair generation rate for different angles of incidence (a) θ=15° (b) θ=30° (c) θ=45° (d) θ=60° (e) θ=75° (f) θ=90°.

The obtained drain current of the device depends on the penetration depth and the angle of incidence of the impact of the heavy ion. A higher current will be achieved when the track of the heavy ion, as it passes through the device, lands on a *n-p* junction. These regions are typically the most sensitive due to the presence of high fields. The electric field causes the holes to drift into the p-region and the electrons into the n-region. This phenomenon can be observed in Figure 3.13, where the maximum drain current is obtained for smaller positive angles ($\theta = 30°$ or $45°$) and for $\theta = -60°$. In the case of positive angles, the track of the heavy ion enters the region under the gate of the transistor, where the channel is formed. Regarding the case of the negative angles, it must be taken into account that at smaller angles the ions exit through the side of the transistor, leading to a reduced electron-hole pair generation. Therefore, for $\theta = -60°$ the maximum number of electron-hole pairs is generated along the reverse-biased *n-p* junction between drain and substrate.

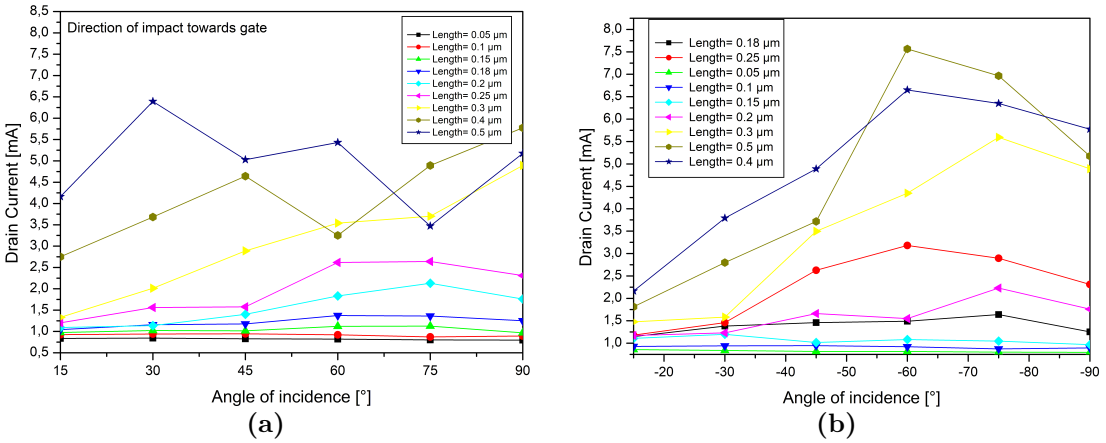


Figure 3.13. Maximum drain current for different angles (a) Angles towards gate (b) Angles away from gate.

3.2 Analysis of GaN technology

In this section, high electron mobility transistors (HEMTs) based on an AlGaN/GaN on sapphire process are analysed under the effect of radiation. These transistors had been previously modelled by other members of the research group [35]. In this document, the model is merely presented before analysing the effect of heavy ions in this technology, which is the aim of this research [36].

3.2.1 Transistor modelling

In a similar way as in the case of the CMOS transistors, the AlGaN/GaN transistors were modelled with the *Sentaurus* TCAD tool. The AlGaN/Gan HEMTs structure used in this study is shown in Figure 3.14.

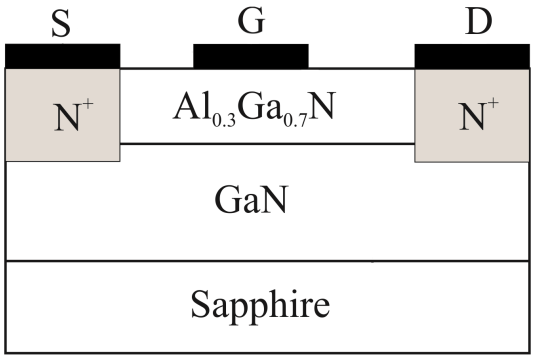


Figure 3.14. Device structure of the AlGaN/GaN HEMT.

The transistor consists of a 3 μm thick GaN buffer and a 19 nm thick AlGaN barrier, unintentionally doped. The 2DEG concentration in the channel is modulated by a Schottky gate, which is 2 μm long and 300 μm wide. The sapphire substrate is 330 μm thick.

The source and drain terminals each have a donor concentration of 10^{20} cm^3 extended down to the GaN channel. These terminals are distanced from the gate borders 4 and 10 μm, respectively.

In order to be able to take into account effects such as gate-lag and modulation of the ON resistance of the transistor, due to the presence of traps in different locations, two main trapping centres have been considered. Firstly, traps on the top of the AlGaN barrier with a donor sheet concentration of 2.3×10^{13} cm^{-2} and an activation energy from the centre of the band gap of 0.4 eV. Secondly, acceptor traps in the GaN buffer, with a concentration of 5×10^{16} cm^{-3} and an activation energy from the valence band maximum of 0.368 eV [37].

For the HEMT under consideration, a layer 2 nm deep of donor traps just below the gate terminal, with an activation energy from the conduction band minimum of 0.2 eV and capture cross-section of 10^{-15} cm^{-2}, is assumed. All of these considerations result in the simulated curves shown in Figure 3.15, compared with the measured output and transfer characteristics.

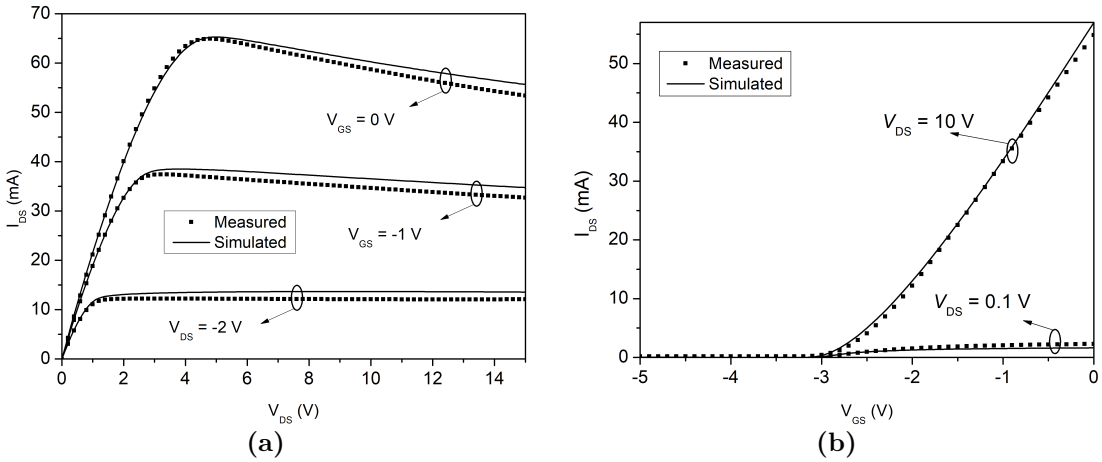


Figure 3.15. Measured and simulated (a) output characteristics (b) transfer characteristics.

3.2.2 **Radiation effects in GaN technology**

In order to perform the single event simulations, it is important to know how the ion behaves as it penetrates the device. To do so, the stopping and range of ions in matter (SRIM) code has been used. This is a collection of software packages which calculate many features of the transport of ions in matter [38]. This way, the track created by the ion is obtained. This information has been later on imported into the TCAD tool.

3.2.2.1. SRIM simulations

The impact of an oxygen ion with different energies on an AlGAN/GaN device has been simulated. It should be noted that, in this case, a target device composed of three layers (Si_3N_4, AlGaN and GaN) has been generated, following the dimensions of the AlGaN/GaN transistor presented in the previous section. Figure 3.16 shows the dialog box from SRIM where the layers of the transistor have been defined.

As it can be seen, three layers have been defined: *Silicon Nitride*, *AlGaN* and *GaN*. Both *Silicon Nitride* and *GaN* are included in the *Compound Dictionary*. However, the *AlGaN* is not included. Therefore, this layer had to be created manually. Aluminium, gallium and nitrogen elements have been included in the layer following the proportion $Al_{0.3}Ga_{0.7}N_1$. This results in a layer stack like the one shown in Figure 3.17.

The SRIM tool allows the simulation of the impact of different elements with different energies on a target device. In this case, oxygen ions with an energy of 2 MeV are simulated, as seen in Figure 3.16. The total number of simulated ion impacts can also be defined.

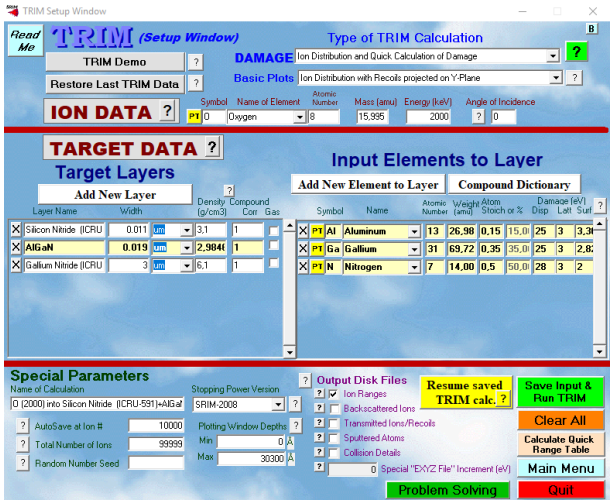


Figure 3.16. Definition of the transistor layers in SRIM.

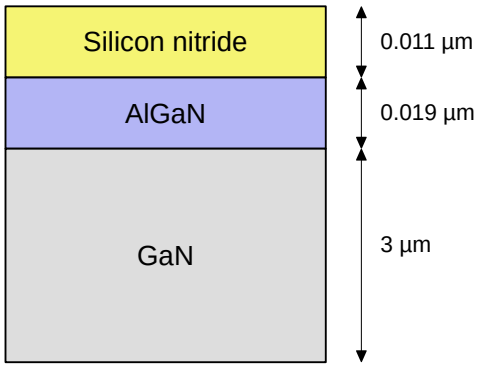


Figure 3.17. Layer stack of the device generated with SRIM.

One important feature of this tool is that the penetration depth on the device of an ion of a certain element with a particular energy can be calculated. Figure 3.18 shows the results of simulating the impact of oxygen ions with an energy of 2 MeV on the AlGaN/GaN device.

In this case, a penetration depth of almost 2 μm is obtained. This is confirmed by the results shown in Figure 3.19, where the distribution of the obtained penetration for all of the simulated ion impacts is depicted. It can be seen that most of the simulated ions reach a penetration depth of 1.71 μm.

The LET can also be calculated with the SRIM tool considering the energy loss in the device due to ionization and the density of the target material. Figure 3.20 shows the energy lost by the oxygen ions with an energy of 2 MeV before the impact as they traverse through the device. It should be noted that all of the parameters that have been calculated with the SRIM tool have been later on introduced in the TCAD simulations.

As mentioned previously, this tool allows us to simulate the impact of different elements on a target device. Thus, a study of how different elements impact an

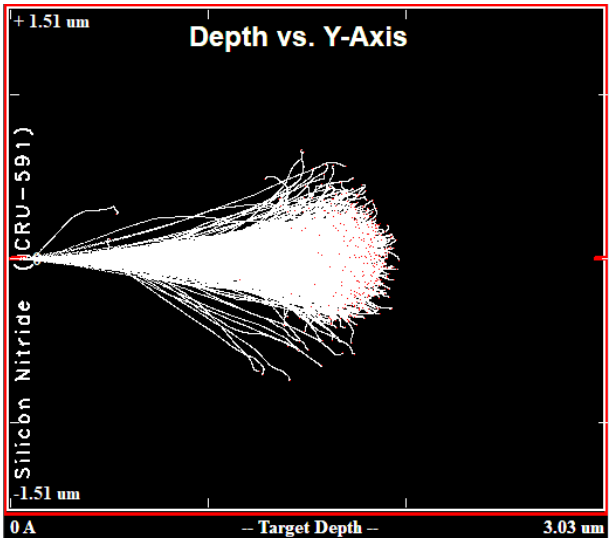


Figure 3.18. Penetration depth of oxygen ions with an energy of 2 MeV in an AlGaN/GaN device, calculated with the SRIM tool.

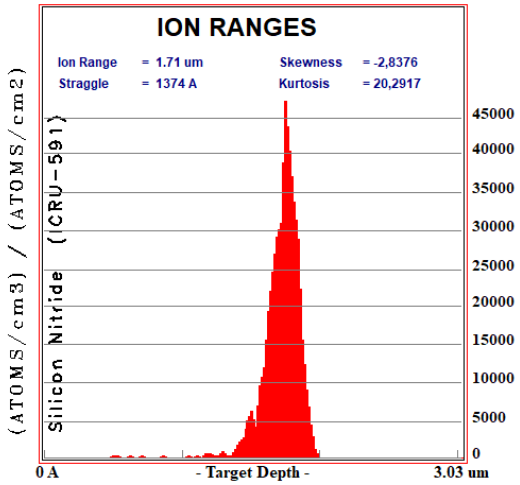


Figure 3.19. Distribution of the obtained penetration depth of oxygen ions with an energy of 2 MeV in an AlGaN/GaN device, calculated with the SRIM tool.

AlGaN/GaN device has been performed. Their LET versus depth curves are shown in Figure 3.21 (a).

Considering that all strikes have been simulated with the same ion energy (2 MeV), it can be seen that the penetration depth is inversely proportional to the atomic number. This can be explained by the fact that a smaller ion results in less collisions with the lattice structure of the device, which slow down the ion.

Regarding the effect of the ion energy, the LET versus depth curves for different energies of oxygen ions are shown in Figure 3.21 (b). It is known that a high-energy heavy-ion track can be modelled with a constant LET, while the LET of low-energy ions varies significantly along their track, which are shorter [39]. This is confirmed by the curves displayed in Figure 3.21 (b), where it can be seen that for low energies (2 and 5 MeV) the LET varies with the depth, while for higher energies (10, 20 and

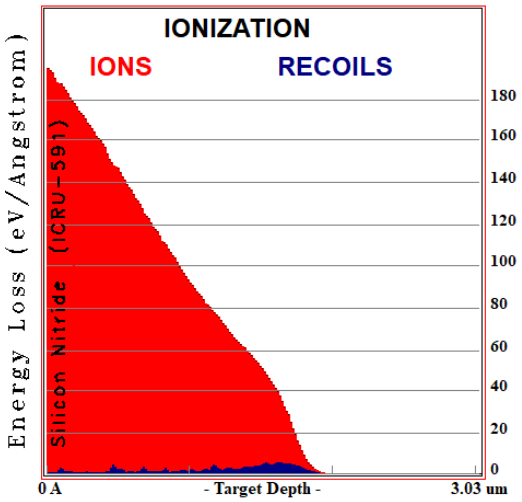


Figure 3.20. LET of oxygen ions with an energy of 2 MeV in an AlGaN/GaN device, calculated with the SRIM tool.

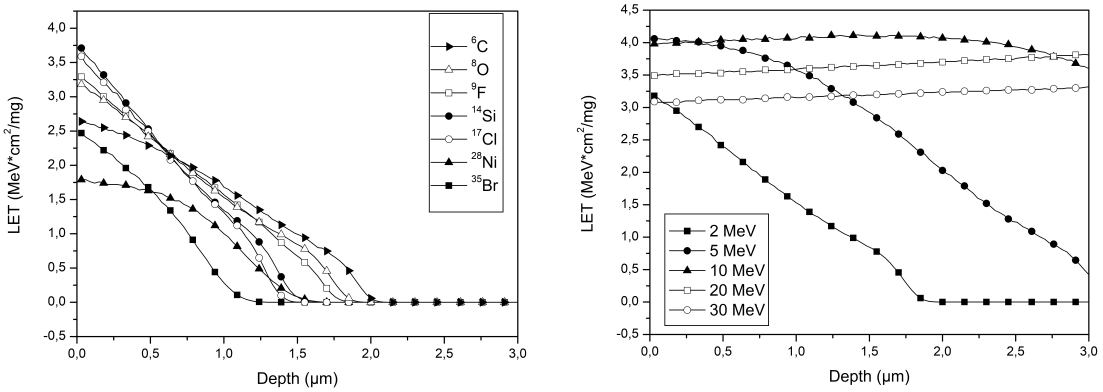


Figure 3.21. LET versus depth for (a) different elements in GaN (b) different energies of oxygen ions in GaN.

30 MeV) the LET remains almost constant. Additionally, it can be observed that the maximum LET value is achieved for an energy of 10 MeV, when a Bragg peak appears if LET is represented against the energy the ion has before the impact, as shown in Figure 3.22.

Additionally, the effect of the angle of incidence has been studied using the SRIM tool. The angle θ corresponds to the angle of incidence from the normal. As seen in Figure 3.23, the penetration depth is deeper for smaller angles of incidence. Regarding the LET, the area under each curve should be the same since the same ion energy is used for each case. Therefore, for bigger angles the ionization occurs in the first micrometers of the device while for smaller angles the same ionization is distributed along the depth of the device.

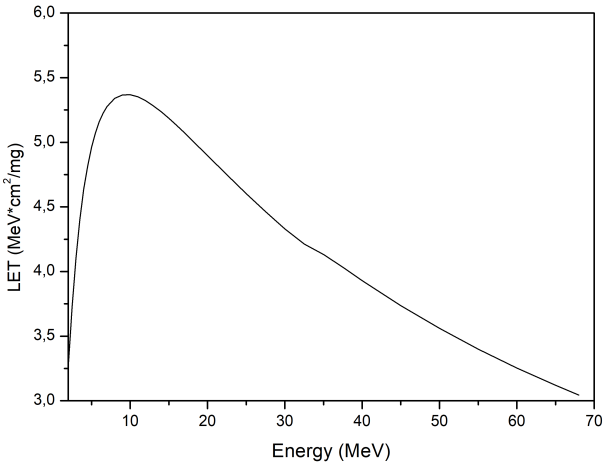


Figure 3.22. LET versus energy for oxygen ions in GaN.

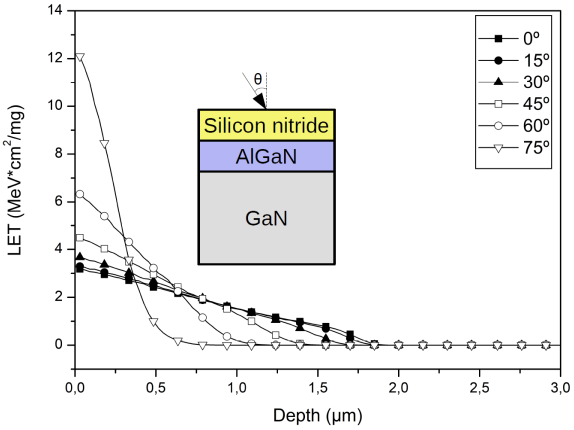


Figure 3.23. LET versus depth for different angles of incidence of oxygen ions in GaN.

3.2.2.2. TCAD simulations

Similarly as in the case of the CMOS transistors, the heavy ion model of the *Sentaurus* TCAD tool has been used to simulate effects of single event transients in an AlGaN/GaN HEMT.

In this case, transient simulations have been performed for different locations, depths, LET and direction values, keeping the characteristic distance and instant of impact constant, with the transistor operating in saturation region (with $V_g = 0V$ and $V_d = 20V$, which are typical bias values for RF circuits). In this section, all simulations have been performed using the track information obtained in the SRIM simulations when the target device is impacted with an oxygen ion. Specifically, the LET function, penetration depth of the heavy ion in the device and characteristic distance parameters are obtained from the SRIM simulations.

Figure 3.24 shows the drain current density for ion strikes at different points of the transistor. It can be seen that the highest drain current density is obtained when there is a strike at the drain, as expected. The lowest current is achieved when there is a strike at the source of the transistor. This can be explained by the fact

that this is the contact further away from the drain and, therefore, the generated electron-hole pairs due to the strike recombine before reaching the drain. Taking this into account, it would be expected for the drain current density to be larger when there is a strike in the gate-to-drain region compared to a strike in the gate. However, the opposite occurs since the generated current due to the strike at the Schottky gate reaches the drain through the transistor's channel.

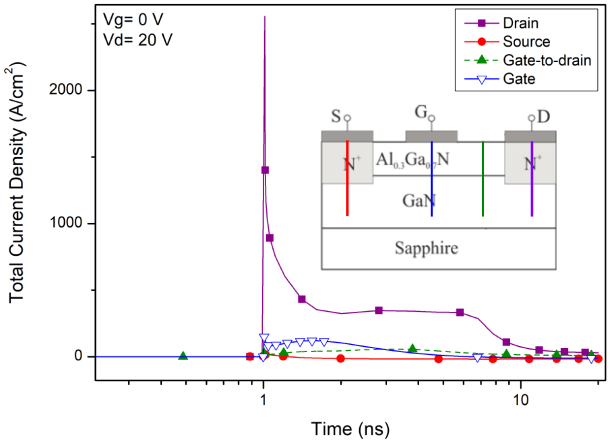


Figure 3.24. Drain current density over time of heavy ion strikes at different positions.

Regarding the penetration depth of the particle in the device, the energy of the ion before impacting the device must be considered. The bigger the energy, the deeper the ion will penetrate in the device. Figure 3.25 shows the drain current density for ion strikes on the gate-to-drain region with different penetration depth (d).

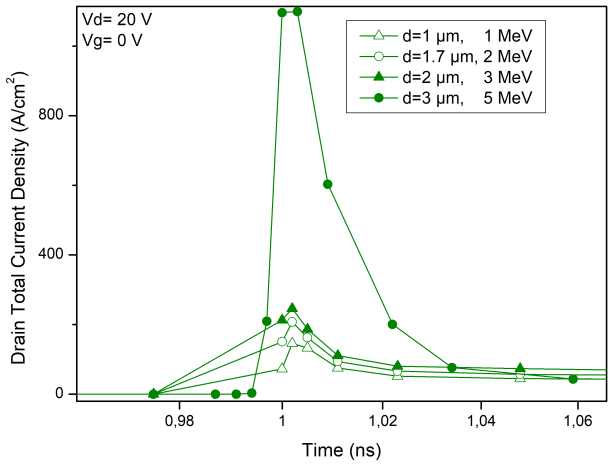


Figure 3.25. Drain current density over time for ion strikes on the depletion region with different penetration depth.

It can be seen that the drain current density increases as the ion penetrates further in the device. This is explained by the fact that a higher energy ion results in more ionization produced in the transistor, including in the 2DEG zone, as shown in Figure 3.26.

In a similar way as in the SRIM simulations, the effect of the angle of incidence was studied with the TCAD tool. To do so, the direction of the heavy ion model

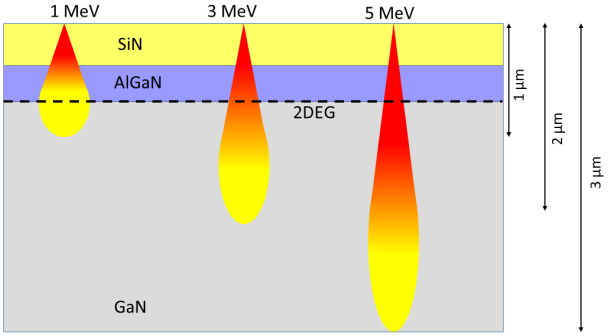


Figure 3.26. Illustration of different energy ions impacting on a GaN device.

was modified. The angle of incidence from the normal (θ) ranges from 0° to 60°. Figure 3.27 shows the electron-hole pair generation rate for different θ values, when a 5 MeV oxygen ion strikes on the gate-to-drain region.

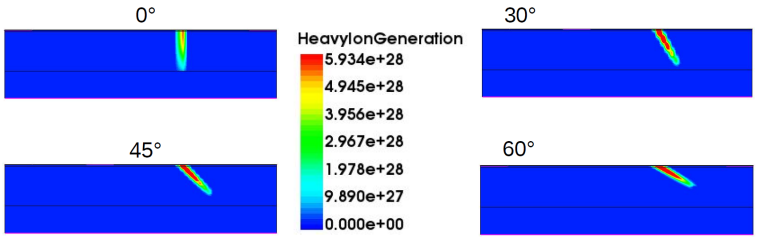


Figure 3.27. Electron-hole pair generation rate for different angle values.

The curves in Figure 3.28 depict an inversely proportional relationship between drain current density and angle of incidence. Hence, the drain total current density decreases for bigger angles, when the recombination of electron-hole pairs enhances. In the case of a vertical strike ($\theta = 0°$), the longitudinal electric field produces non-coincident carrier trajectories. However, as the angle of incidence increases, the carrier trajectories coincidence grows and recombination is augmented.

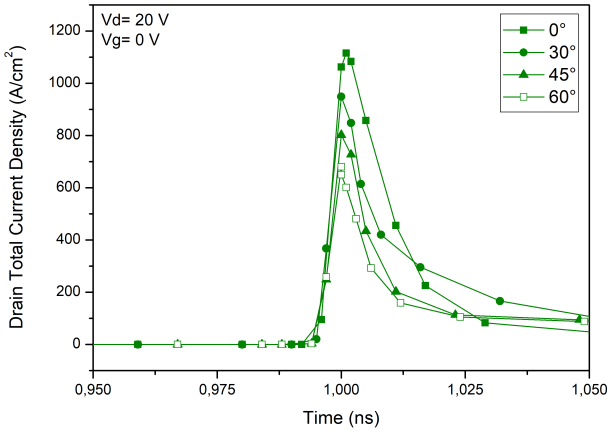


Figure 3.28. Drain current density over time for ion strikes with different angles of incidence.

In all of the drain current density over time curves shown in this section, the curves can be modelled following a function based on the sum of three exponential functions. This can be clearly identified by observing the drain current density when

there is a strike at the drain, as shown in Figure 3.24. In the other graphs this fact can not be seen so clearly since the represented time in the x-axis is considerably lower. In the following pages, a discussion on the modelling of this phenomenon is addressed.

Equation 3.6 shows the equation used to model the drain current of the AlGaN/-GaN HEMT transistor when there is an ion impact:

$$I_D = \sum_{n=1}^{3} \frac{Q_n}{t_{fn} - t_{rn}} \cdot \left(e^{-\left(\frac{t}{t_{fn}}\right)} - e^{-\left(\frac{t}{t_{rn}}\right)} \right), \tag{3.6}$$

where Q_n represents the collected charge, t_{fn} the fall time and t_{rn} the rise time. The model is composed of three exponential functions. The first of them simulates the effect of a heavy ion striking the device, which results in the generation of electron-hole pairs. The electrons are collected quickly at the drain (due to a drain voltage of 20 V) and is modelled by the first term ($n = 1$). This leads to an excess of holes in the GaN buffer layer. It should be noted that a parasitic bipolar transistor appears due to the $n - p - n$ junction formed by the source, the excess of holes and the drain. These positive charges lower the potential barrier between the source and the channel, leading to additional injections of electrons, which are collected at the drain. Thus, a diffusion-mechanism from the source (the emitter of the parasitic bipolar transistor) to the excess of holes (the base of the parasitic bipolar transistor) is originated. The derived current is modelled by the second term ($n = 2$). Additionally, a long-term drift-mechanism from the source to the channel (back-channel effect) produces the current modelled by the third term ($n = 3$) [40]. Figure 3.29 shows the model compared to the curves generated with *Sentaurus*, previously presented in Figure 3.25.

The effect of the energy of the ion on the collected charge can be studied using this model. The curves shown in Figure 3.25 have been replicated and the resulting values of the model parameters are shown in Table 3.2.

Table 3.2: Model parameter values for different energies.

Energy (MeV)	1	2	3	5
Q_1 (nC)	3.75	9.5	16.5	28
Q_2 (nC)	130	150	175	220
Q_3 (nC)	120	120	120	120

In order to correctly study the effect of the energy on the collected charge, all rise and fall times, t_{f1}, t_{r1}, t_{f2}, t_{r2}, t_{f3} and t_{r3}, are kept constant and equal to 0.0115, 0.005. 0.65, 2, 0.1 and 90 ns, respectively. Taking this into account, it can be seen that both Q_1 and Q_2 increase as the energy increases, as expected. If the ion impacts the device with higher energy, more electron-hole pairs are generated, which results in higher collected charges Q_1 and Q_2. However, regarding Q_3, as it is related

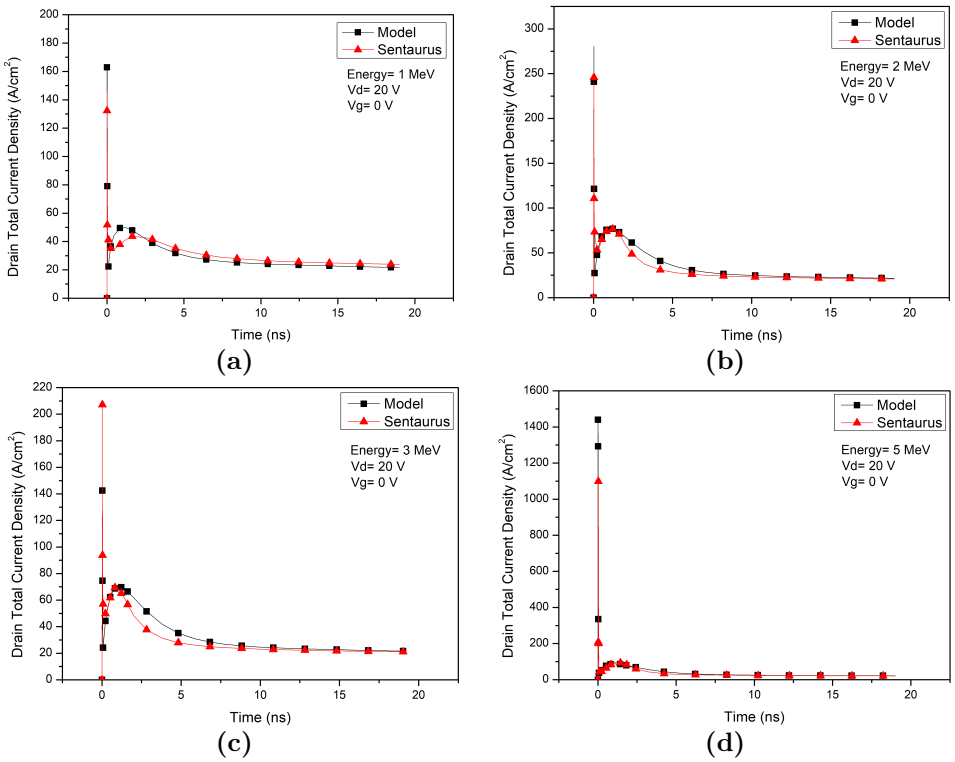


Figure 3.29. Modelling of different energy ion strikes on the gate-to-drain region (a) 1 MeV (b) 2 MeV (c) 3 MeV (d) 5 MeV.

to the back-channel, which is a long-term charge enhancement, it can be assumed constant and small [40]. Figure 3.30 shows how Q_1 and Q_2 increase linearly with the energy. The obtained Q_1 and Q_2 values are transistor dependant, since the doping and dimensions of the transistor affect the collected charge and current generated by a heavy ion strike.

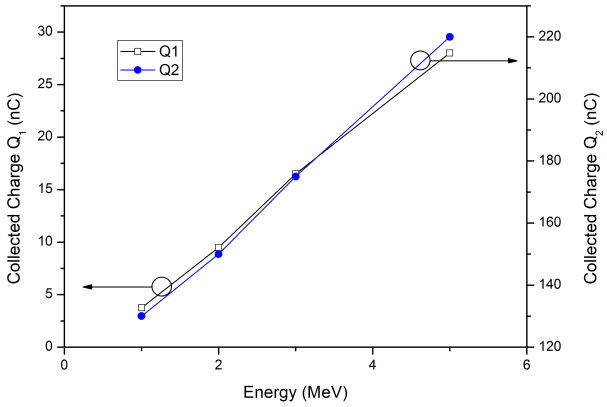


Figure 3.30. Q_1 and Q_2 versus energy ion strike.

Regarding the effect of angled strikes on the collected charge, for an energy of 5 MeV, Table 3.3 shows the resulting model parameter values for different angles once the curves in Figure 3.28 have been replicated. As in the previous case, all rise and fall times are kept constant and with the same values.

Table 3.3: Model parameter values for different angles.

Angle (°)	0	30	45	60
Q_1 (nC)	28	20	18	14
Q_2 (nC)	220	260	285	310
Q_3 (nC)	120	120	120	120

Figure 3.31 shows how Q_1 and Q_2 behave for different angles of incidence. As it can be seen, Q_1 decreases as the angle of incidence increases. This is in agreement with the results shown previously (Figure 3.28). However, Q_2 follows the opposite behaviour, since the base of the parasitic bipolar transistor (the excess of holes) is located deeper as the angle of incidence decreases, thus reducing the diffusion-mechanism transport. Therefore, the second charge collection mechanism is larger in the case of larger angles of incidence.

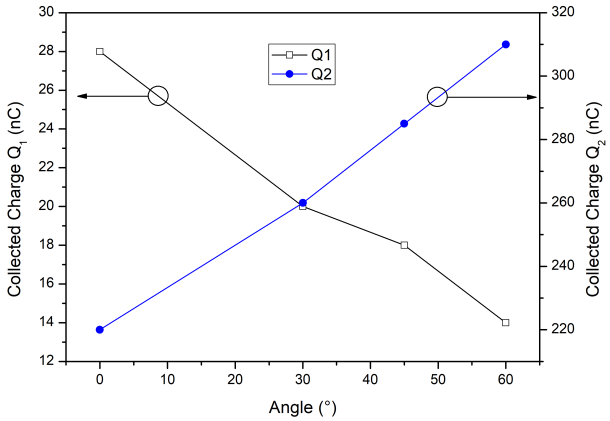


Figure 3.31. Q_1 and Q_2 versus angle of incidence.

3.3 Conclusion

In this chapter, an analysis of radiation effects on semiconductor devices has been performed. To do so, the *Sentaurus* TCAD tool has been used. Considering that the main goal of this research is to study the effects of radiation on CMOS technologies, a 0.18 μm CMOS process has been examined.

The first step consisted on modelling a NMOS transistor of this process. Once the adequate electrical performance of the transistor was verified and compared with the information given by the technology, the NMOS transistor was studied under the effects of a heavy ion impacting the device. In this case, the heavy ion model provided by *Sentaurus* was used to simulate the effect of a charged particle striking the modelled transistor. These simulations showed that an increase in LET and penetration depth of the heavy ion in the semiconductor implies an increase in the drain current. Regarding the angle of incidence, higher currents are obtained for angles where the maximum number of electron-hole pairs is generated along the reverse-biased *n-p* junction.

As mentioned previously, a high performance GaN technology has also been studied under the effects of radiation. This was not in the original aim of the research, but since devices fabricated in an AlGaN/GaN on sapphire process became available to the research group during the process of this research, this study has been included. The methodology used was very similar as the one followed for the CMOS devices. First, the devices were modelled using the *Sentaurus* TCAD tool. Then, oxygen ion impacts were simulated for different locations, depth, LET and direction values. Simulation results show that the drain current density increases as the ion penetrates further in the device. This can be explained by the fact that a higher energy ion results in a deeper penetration and more ionization produced in the transistor, including the 2DEG zone. Additionally, the total drain current density decreases for bigger angles since as the angle of incidence increases, so does the recombination of electron-hole pairs.

In the following chapter, the TCAD generated current pulses in the CMOS transistor will be introduced in the critical nodes of analog RF circuits. Specifically, low noise amplifiers will be studied under the effects of radiation.

Chapter 4

RADIATION EFFECTS IN LOW NOISE AMPLIFIERS

In this chapter, the effects of radiation in analog RF circuits is studied. Specifically, low noise amplifiers (LNA) are considered. These circuits are the first elements of a receiver chain. Therefore, the current pulses generated in these circuits due to heavy ion strikes could affect the subsequent circuits in the receiver chain. These pulses could propagate to other circuits and generate errors. This phenomenon will be studied in following chapters.

The LNAs presented in this chapter have been designed for the IEEE 802.15.4 standard using CMOS technologies. Specifically, two well-known LNA topologies, the common-source (CS) and the common-gate (CG) cascodes, have been analysed when heavy ions strike the most sensitive nodes of these structures. In order to simulate these strikes, the TCAD-generated current pulses studied in the previous chapter are introduced in the critical nodes of the LNAs. To do so, the electrical circuit domain simulator *Advanced Design System* (ADS) has been used. This way, the physics information given by the TCAD tool is combined with the fast transient simulations performed in circuit simulators.

Once the effect of radiation has been studied in these LNAs, radiation hardening by design (RHBD) techniques have been applied at the most vulnerable nodes of both LNAs.

4.1 Schematic design of the low noise amplifiers

4.1.1 Common-source cascode low noise amplifier

The main goals of the low noise amplifier are low noise figure (NF), high gain to sufficiently reduce the NF contribution of the subsequent stages, and high linearity to accommodate high input signal and strong interferences. In addition, the LNA should have a 50-Ω input impedance to match with the output impedance of the off-chip components such as an RF bandpass filter or a transmission/reception switch.

Figure 4.1 shows the schematic of the CS LNA. A single-ended topology has been chosen because it dissipates lower DC current than a differential one and the required input second-order input intercept point (IIP_2) performance of the IEEE 802.15.4 standard is not as high compared with other wireless communication standards [41].

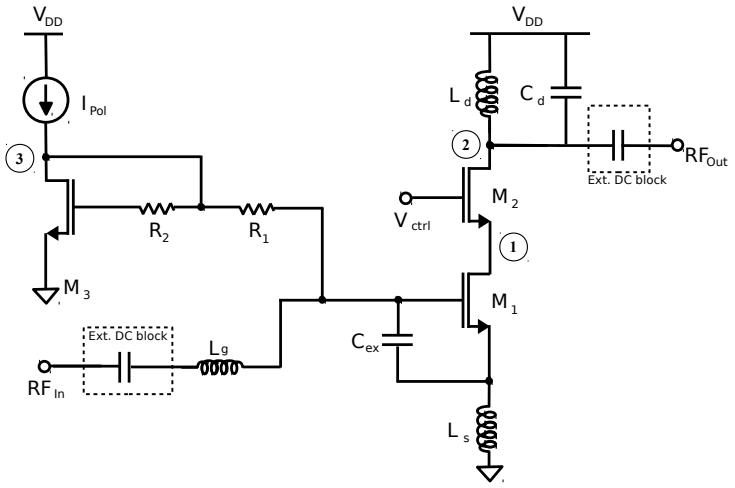


Figure 4.1. Schematic of the common-source cascode LNA.

As shown in Figure 4.1, an inductive degenerated cascode LNA topology is used. This topology is known to provide high gain, low noise and high/output isolation. In order to achieve simultaneously low noise and input matching, the inductive degeneration technique is used. The addition of L_s generates a real part at the input impedance which reduces the discrepancy between the optimum noise impedance and the LNA input impedance. This is due to the fact that the optimum noise impedance has a real part, while without degeneration there is no real part at the input impedance. However, under low power consumption the inductance value needed to obtain both noise and input matching is very large. This results in a minimum achievable noise figure of the LNA significantly higher than its NF_{min}. This can be solved by including the capacitor C_{ex}, as it is shown in Figure 4.1. By adding this capacitance, one can use lower values of the inductance L_s to achieve simultaneous noise and input matching.

The input impedance of the LNA is given by Equation 4.1:

$$Z_{in} = s \cdot (L_s + L_g) + \frac{1}{s \cdot C_t} + \frac{g_M \cdot L_s}{C_t} \tag{4.1}$$

where C_t is the total capacitance between the gate and the source of M_1, which is $C_{gs} + C_{ex}$. From Equation 4.1 it can be seen that by including the capacitor C_{ex} the imaginary part of the input impedance changes, allowing smaller values for L_s and L_g. This also reduces the parasitic resistance, thus improving the noise figure of the LNA.

In this design, the inductors L_s, L_g and L_d are implemented on-chip in order to reduce the off-chip components. This can be done because the noise figure required by the standard is relaxed. Additionally, in this topology the gain control function is implemented by adjusting the bias voltage V_{ctrl}.

4.1.2 **Common-gate cascode low-noise amplifier**

The low input impedance of the common-gate (CG) stage makes it an attractive topology for LNA design. Figure 4.2 shows the schematic of a CG cascode LNA. In this case, the input impedance is approximately $1/g_{m1}$.

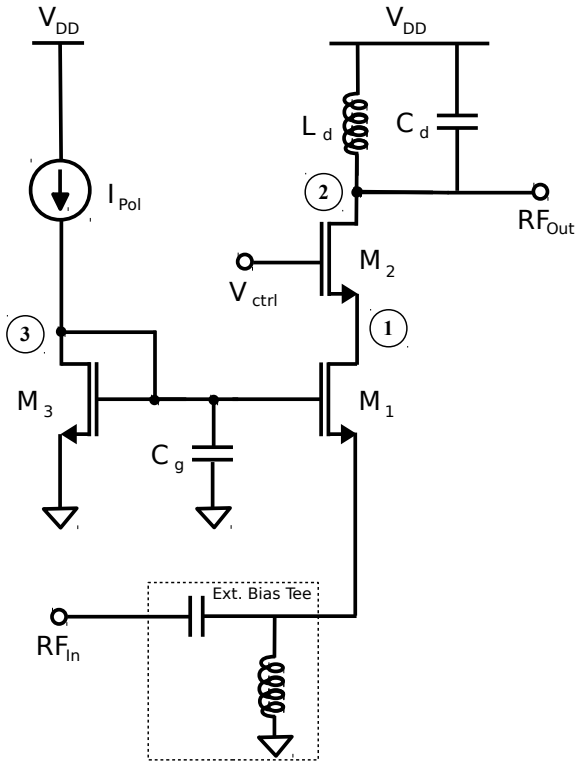


Figure 4.2. Schematic of the common-gate cascode LNA.

As it can be seen in Figure 4.2, the implemented CG LNA has an inductorless topology except for the required L_d inductor, which is part of the load tank of the circuit. This results in a considerably smaller area size in comparison to the CS LNA previously presented. Additionally, it is known that the CS LNA's input matching network is series resonant, while the CG LNA's is parallel resonant. Because of this, the input matching network of the CG has a lower quality factor and, as a consequence, it provides a more wideband input matching and it is more robust against typical production process, voltage and temperature variations.

4.1.3 RF performance comparison

Both LNA structures have been designed using a 0.18 μm CMOS technology by UMC for the 2.4 GHz band specified by the IEEE 802.15.4 standard. The design of the circuits has been performed looking for good trade-offs between low power consumption, high gain and low noise.

Figure 4.3 shows the performance of both LNA topologies. As it can be observed, the CS has a gain of approximately 18.2 dB while the CG achieves 10.4 dB. Regarding the noise figure (NF), Figure 4.3 shows that the CS offer a better performance (3.2 dB against 5 dB). However, the CG provides a superior input matching than the CS at the desired 2.4 GHz frequency, as expected (-28.7 dB against -11.3 dB). Considering the achieved results, it can be stated that both LNAs meet the IEEE 802.15.4 standard specifications.

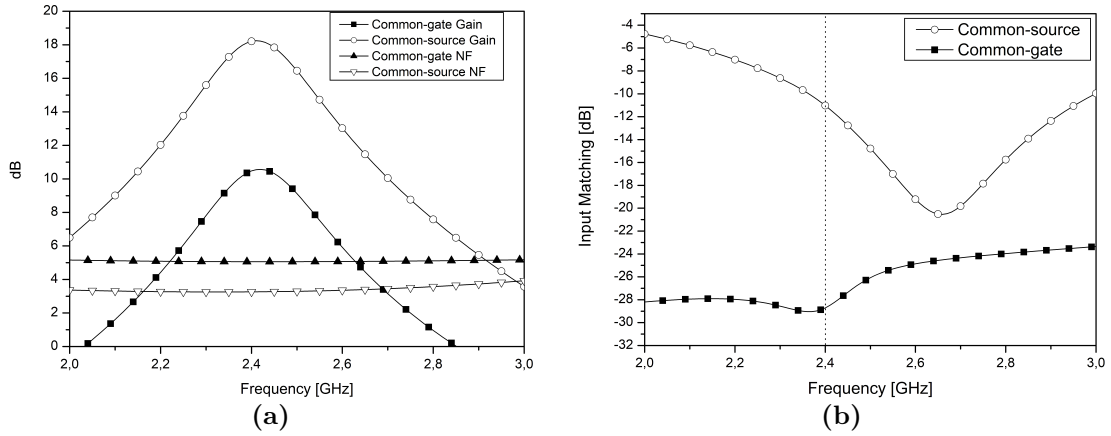


Figure 4.3. RF performance comparison between the CS and CG LNAs: (a) gain and NF, (b) input matching.

4.2 Single Event Transient response of the low noise amplifiers

In the previous section, the two LNA structures were studied regarding their RF and electrical performance. Despite the fact that both LNAs perform favourably according to the standard specifications, it is yet to be analysed how these amplifiers operate in harsh radiation environments. To do so, an investigation on the effect of SETs has been performed.

The current pulses generated with the *Sentaurus* TCAD tool (presented in the previous chapter) were introduced in a circuit domain simulator through current sources that were applied at the most vulnerable nodes of both LNAs (nodes 1, 2 and 3 as seen in Figure 4.1 and Figure 4.2). This way, the semiconductor physics information obtained from the TCAD tool is combined with the fast electrical simulations performed in a circuit domain simulator. As stated previously, the ADS

simulator has been used, where transient simulations have been performed with the current sources connected at the drain of each transistor of both LNAs.

In order to assess the SET behaviour of both circuits, the maximum voltage peak and the recovery time of the output signal have been calculated for each case. The output signal is considered to be recovered when the difference between the output voltage signal when the SET strikes and the voltage signal when there is no strike is below 5%. In this section, the results shown correspond to current pulses with different LET and length values, while the angle of incidence remains at a constant value of $\theta = 90°$. This corresponds to a heavy ion impacting the transistor perpendicularly, which is a widely used approach in this kind of studies [15], [16].

Figure 4.4 shows the obtained maximum voltage peak against the recovery time of the output signal for both LNAs. A safe operating area (SOA) can be defined, setting the boundaries for acceptable SETs. The events that occur inside this area have amplitudes and durations that do not affect the functionality of adjacent circuits. This SOA is specified by the designer and is application-dependent [42]. In this case, a maximum voltage peak of 20 mV and a recovery time of 7 ns have been defined as the boundaries of the SOA. Table 4.1 shows the percentage of SETs that are inside the SOA for each node of both circuits. From these results it can be stated that node 3 is the most critical node in both circuits.

Table 4.1: Percentage of SETs inside the SOA for the CG and CS LNAs.

	LNA	
Node	CG	CS
1	80%	80%
2	65%	60%
3	50%	40%

Additionally, it can be seen that the largest voltage peaks at the output are obtained when a strike occurs at node 2 in both LNAs. This is because this node is directly connected to the output of the LNAs. Regarding the recovery time, it can be observed that both circuits take longer to recover when there is a strike in node 3 compared to the other nodes. This can be explained since bias circuits, which are responsible for setting the operating voltage for the transistors, are known to be very sensitive to SETs. Therefore, any voltage variation induced by an ion strike in the bias circuit will result in a deviation of the circuit response [1].

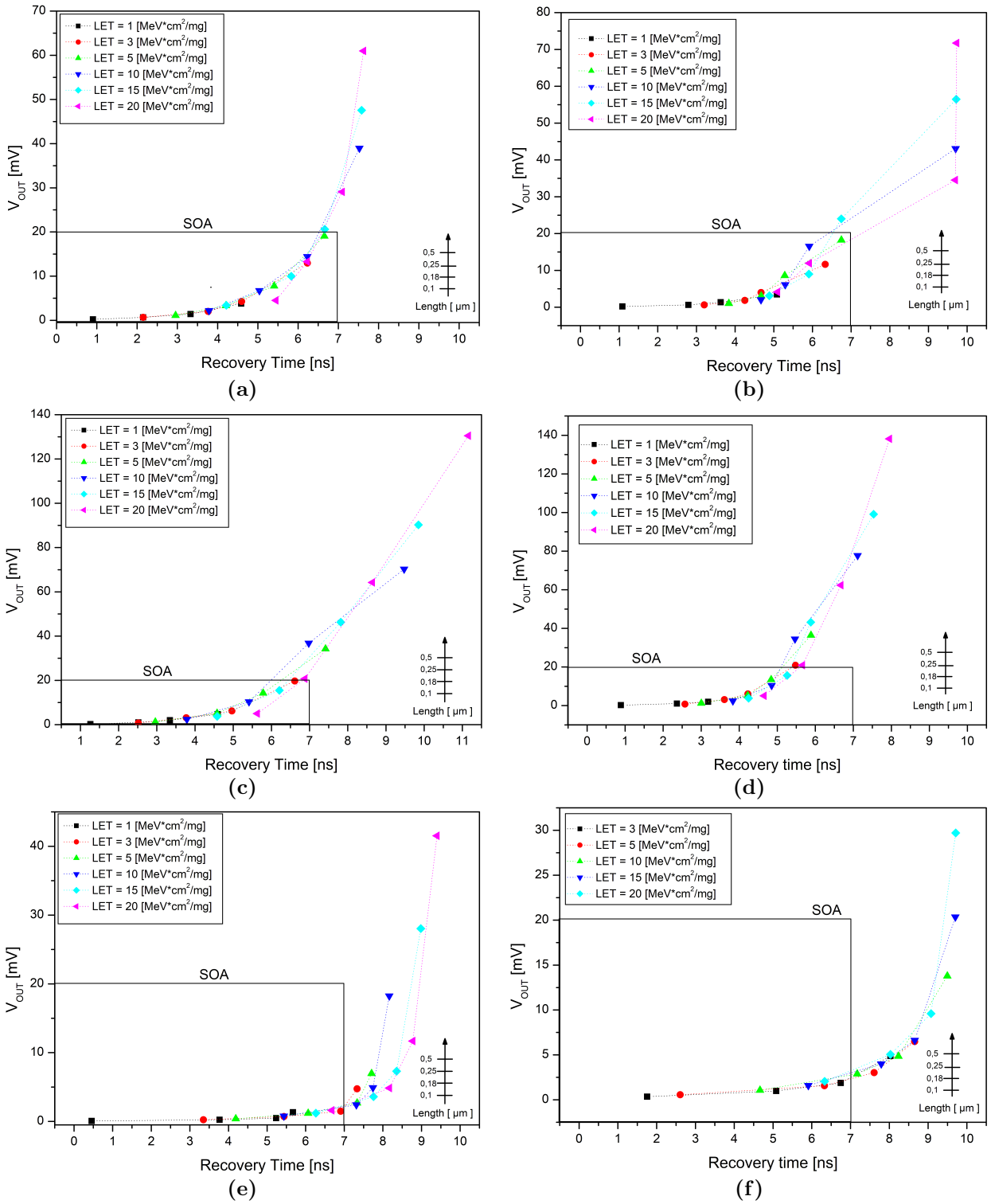


Figure 4.4. Maximum voltage peak against recovery time of the output signal (a) Strike at node 1 of the CG (b) Strike at node 1 of the CS (c) Strike at node 2 of the CG (d) Strike at node 2 of the CS (e) Strike at node 3 of the CG (f) Strike at node 3 of the CS.

4.3 Radiation hardening techniques

Once the effects of SETs have been analysed for both LNAs, several mitigation techniques can be applied to reduce the effect of these events.

As seen in the previous section, node 3 is the most critical node in both LNAs. Therefore, the mitigation techniques proposed in this case are focused on this node. These RHBD techniques should improve the SET performance of the LNAs without affecting their RF performance.

In this case, resistor-capacitor (RC) filtering is implemented to achieve RHBD LNAs. Increasing the capacitance of node 3 lowers the impedance and increases the time constant ($\tau = R \cdot C$), hence the resulting voltage deviation due to the SET is much lower. Therefore, since the peak is now smaller, the time it takes for the signal to get back within the threshold is shorter, resulting in a smaller recovery time. Taking this into account, the biasing networks of both LNAs have been modified. As seen in Figure 4.5, the capacitor C_g has been included at node 3 of the CS. This way the amplitude and duration of the peaks caused by the strikes is reduced by the capacitor, since more charge is required to overcome the stored charge in the capacitor to initiate the transient [30]. Therefore, a large capacitor results in a bigger reduction of the voltage peaks. However, area constraints must also be considered. In this case, the capacitor has a value of 1.45 pF, which is the same value as the C_g present in the CG LNA.

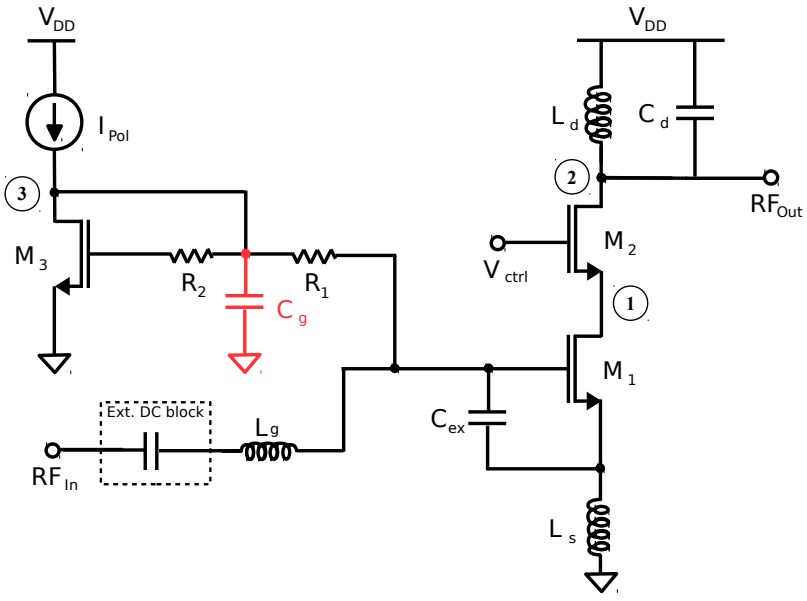


Figure 4.5. Radiation hardened by design common-source cascode LNA.

Regarding the CG, resistances R_1 and R_2 have been included to reduce the voltage peak by increasing the time constant at node 3. These resistances should be large enough so that the AC signal is forced to go through the gate of the M_1 transistor. Taking this into account, it can be assumed that a high resistance value should be chosen for these resistors. However, it should be noted that increasing

the resistance will result in a larger area consumption. Therefore, two 2 kΩ resistors have been chosen. Figure 4.6 shows the schematic of the RHBD CG LNA.

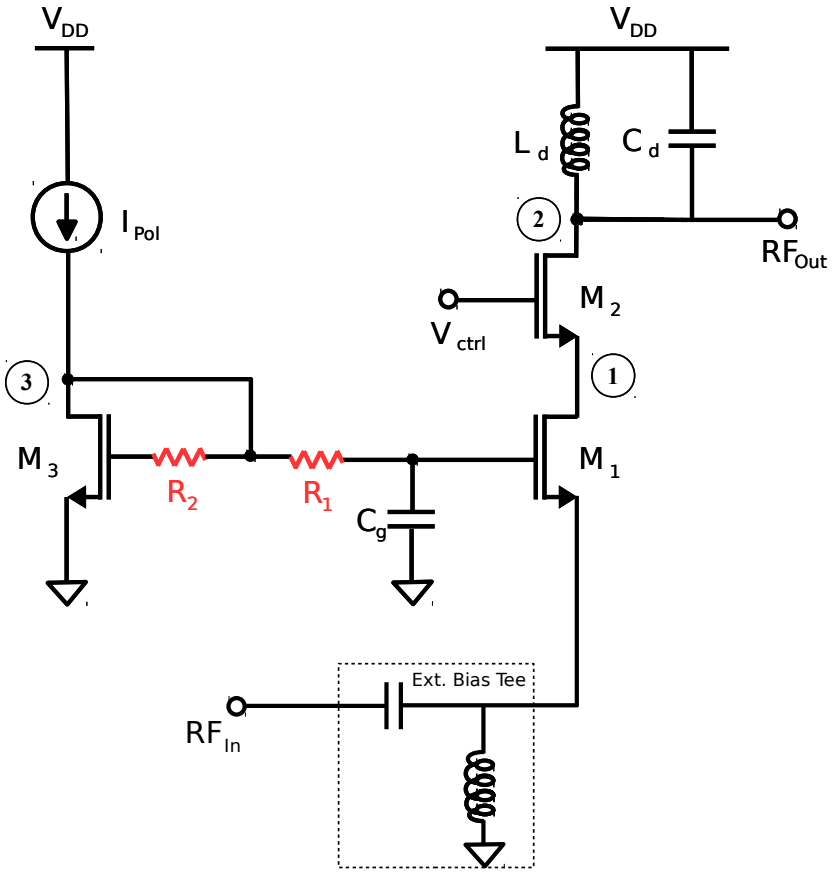


Figure 4.6. Radiation hardened by design common-gate cascode LNA.

Figure 4.7 shows the maximum voltage peak against the recovery time of the output signal for the two RHBD LNAs when there is a strike at node 3. It can be observed that both the recovery time and the maximum voltage peak of the output signal have been considerably reduced. In fact, now 100% of the SETs are inside the SOA for both LNAs.

As seen in the previous section, nodes 1 and 2 are less vulnerable to SETs compared to node 3 in both LNAs. Still, the SET performance of the circuits when there is a strike at these nodes could be further improved by increasing the time constant including resistances and capacitances, similarly as for node 3. However, this approach is not advisable since the RF performance of the LNAs will be worsened by introducing noise and shifting the frequency response of the circuit.

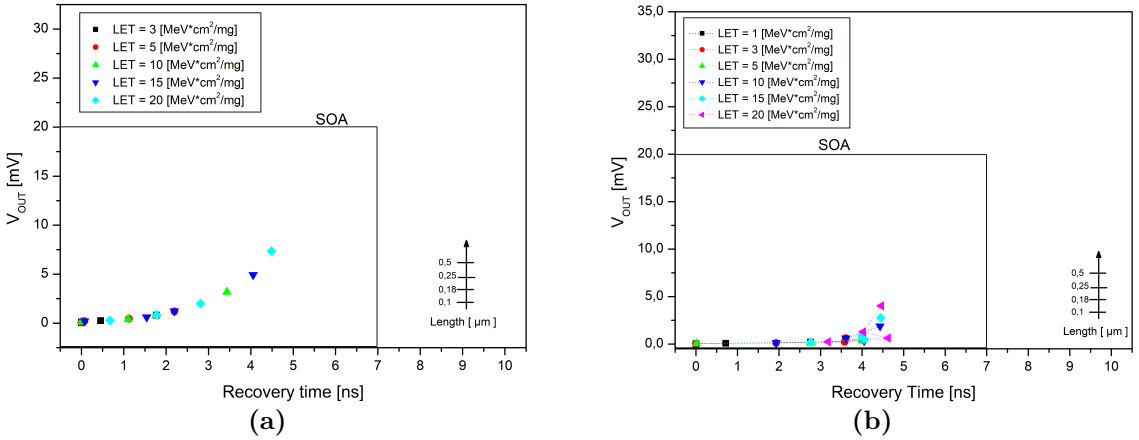


Figure 4.7. Maximum voltage peak against recovery time of the output signal (a) Strike at node 3 of the RHBD CS (b) Strike at node 3 of the RHBD CG.

4.4 Layout design of the low noise amplifiers

The layout of both LNAs was designed using the Virtuoso software tool by Cadence and implemented in the 0.18 μm UMC CMOS technology. The *Assura* extractor was used to obtain the parasitic resistances and capacitances which are introduced by the metal lines that connect the different elements.

4.4.1 Common-source cascode low noise amplifier

Figure 4.8 shows the designed layout of the CS LNA. As it can be seen, the three inductors used in this circuit occupy a great percentage of the total area of the circuit. The circuit occupies a total area of approximately 789 μm x 957 μm.

The extracted parasitic resistances and capacitances have been taken into account and the capacitor present in the tank circuit has been modified. This capacitor is responsible, together with the L_d inductor, of centering the frequency response of the LNA at the desired 2.4 GHz frequency. Therefore, the designed value of the capacitor in schematic had to be decreased in order to compensate for the extracted parasitic capacitances.

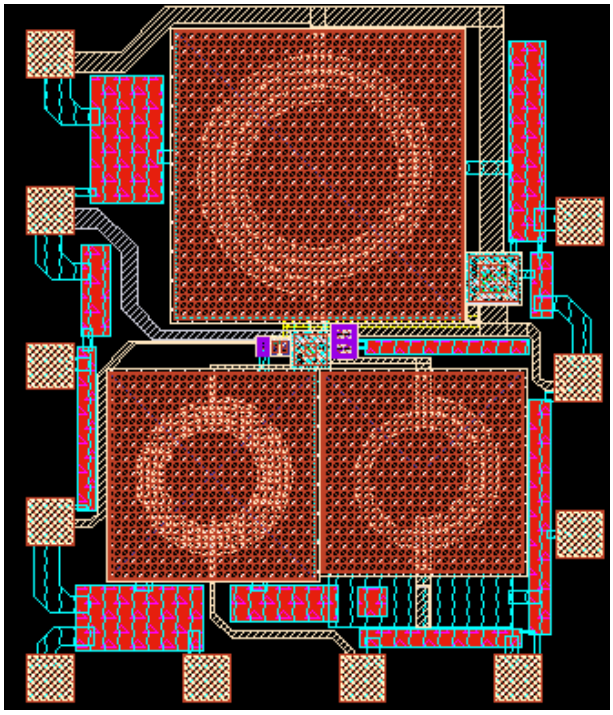


Figure 4.8. Layout design of the common-source cascode LNA.

4.4.2 Common-gate cascode low noise amplifier

Figure 4.9 shows the designed layout of the CG LNA. As it can be seen, this circuit only has one inductor. In this case, the total area of the CG LNA is 730 μm x 1049 μm. However, it should be noted that in this case an output buffer stage has been designed to match the output of the LNA to 50 Ω. A source follower circuit has been implemented as this output buffer stage (as seen in Figure 4.10). The reason for the inclusion of this stage is that it is paramount for measuring the fabricated LNA and, as it will be explained in the following section, only the CG LNA has been fabricated and measured.

In a similar way as in the case of the CS LNA, the capacitor of the tank circuit of the CG LNA had to be modified to compensate the effect of the parasitic capacitances. Additionally, the bias current of the LNA had to be slightly increased to compensate for the losses due to the parasitic resistances.

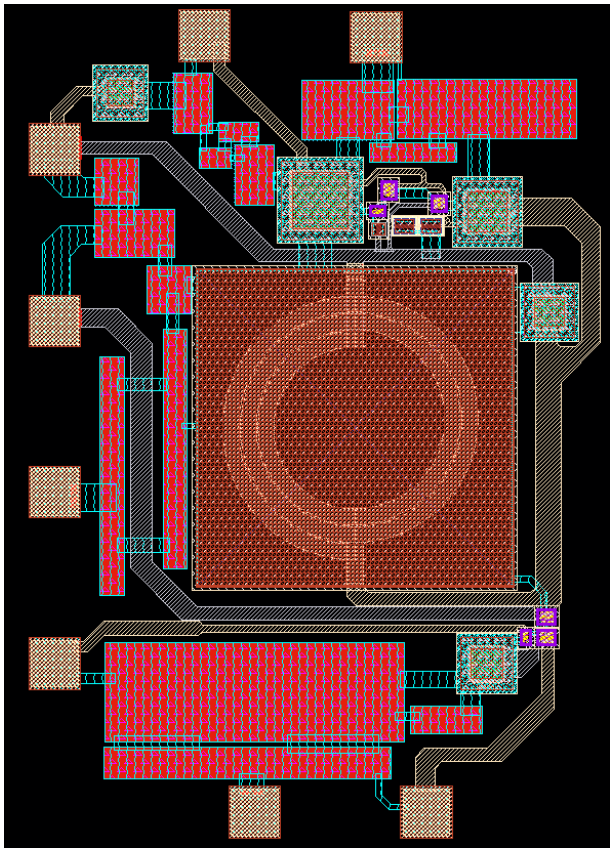


Figure 4.9. Layout design of the common-gate cascode LNA.

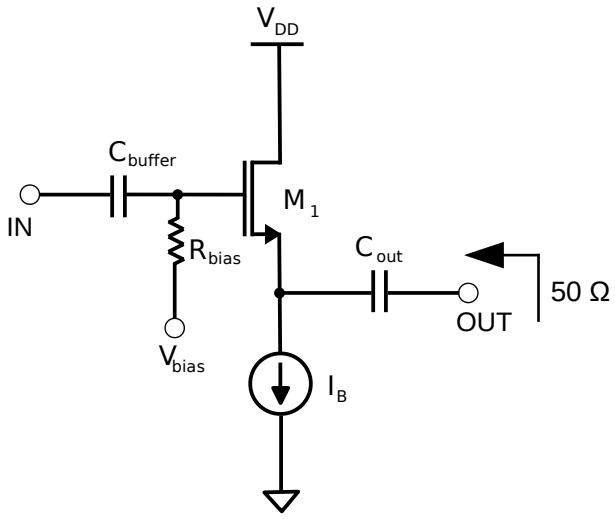


Figure 4.10. Output stage of the CG LNA implemented with a source follower structure.

4.5 Measurements of the low noise amplifiers

Once the SET response of both LNAs has been analysed and the layout has been designed for both of them, the next step corresponds to the fabrication and measurement of these circuits. However, due to funding limitations, it was only possible to fabricate one of the LNAs. In this case, the CG LNA was chosen for fabrication since it has a slightly better response against radiation than the CS. Additionally, as mentioned previously, the CG LNA has a slightly smaller area occupation, if the output buffer stage is not taken into account.

Figure 4.11 shows the layout of the CG LNA prior to fabrication. As it can be seen, both the CG LNA (on the left) and the RHBD version of this LNA (on the right) have been implemented in the same chip. Figure 4.11 also shows that the corresponding pads for bonding have been included.

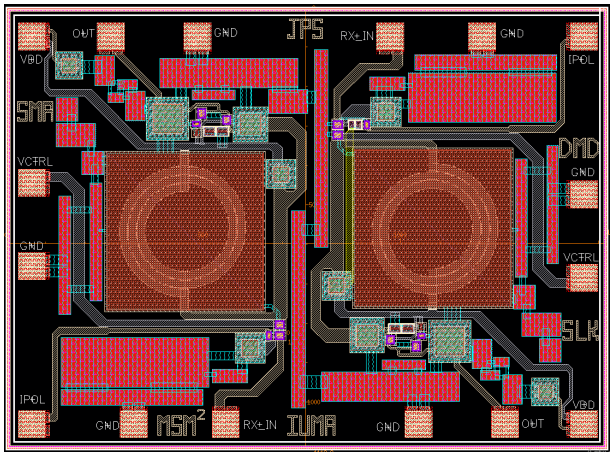


Figure 4.11. Layout design of the common-gate cascode LNA and the RHBD version.

In this case, a 16-pin ceramic small outline integrated circuit (CSOIC) package was chosen. This type of packaging is typically used in RF applications. Additionally, the lid of the package has been designed in a way that it can be removed easily. This is particularly interesting since it allows the performance of laser testing on the circuits in order to assess their radiation response. Figure 4.12 shows the bonding schematic of the circuit and the CSOIC-16 packaging.

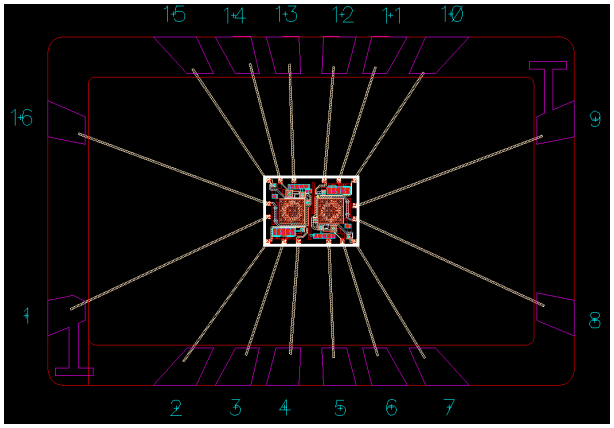


Figure 4.12. Bonding of the common-gate cascode LNA and the RHBD version with the CSOIC-16 packaging.

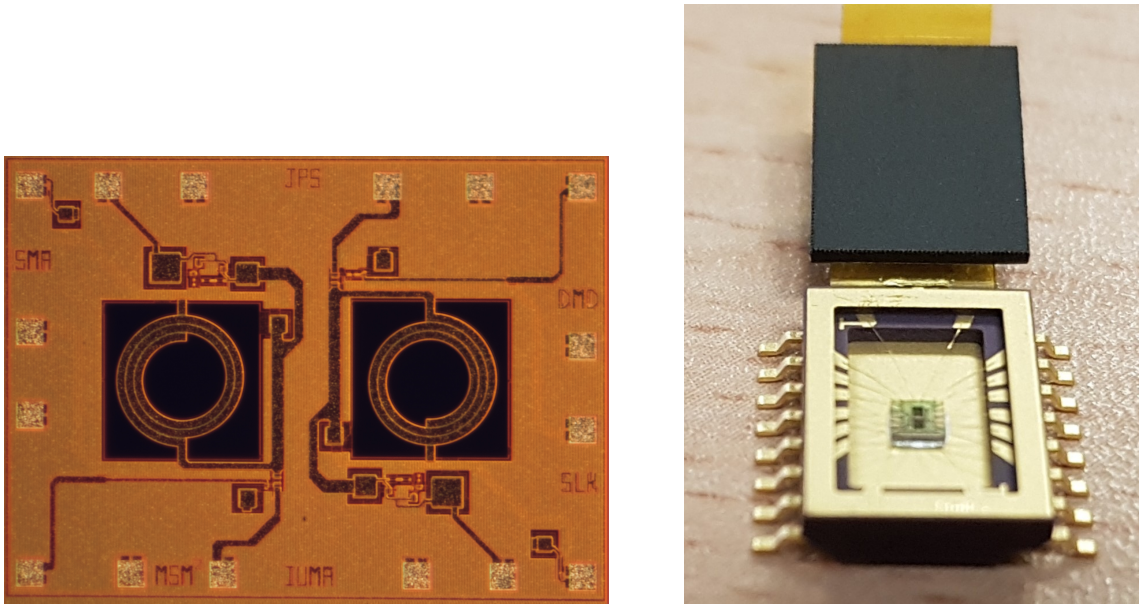
In order to estimate the associated inductance of the wire bonding, and its effect on the performance of the circuit, it is assumed that a wire with a length of 1 mm introduces an inductance of 1 nH. In this case, the longest bonding wires are approximately 1 mm to 1.5 mm long. Taking this into account, the LNAs have been simulated with two 1 nH inductors, one at the input and another at the output. Simulation results show that the wire bonding slightly worsens the S_{11} and S_{22} parameters, but the LNA still performs adequately (see Table 4.2).

Table 4.2: Effect of the wire bonding on the LNAs performance.

	CG		RHBD	
	Without wire bonding	With wire bonding	Without wire bonding	With wire bonding
Gain [dB]	9.5	9.2	9.4	9.2
NF [dB]	5.8	5.6	5.6	5.5
S_{11} [dB]	-24.8	-13.4	-21.3	-14.2
S_{22} [dB]	-15.2	-13.6	-14.5	-13.4

Figure 4.13 (a) shows the microphotograph of the designed circuit. As it can be seen, the circuit on the left corresponds to the CG LNA, while the one on the right corresponds to its RHBD counterpart. Figure 4.13 (b) shows the CSOIC-16 package with the lid removed. The circuits and the bonding can also be identified.

The chip has been mounted on a custom printed circuit board (PCB) with SMA connectors for the RF signals and BNC connectors for the supply voltages and currents, as seen in Figure 4.14.



(a) **(b)**

Figure 4.13. (a) Microphotograph of the fabricated LNAs (b) CSOIC-16 package of the fabricated LNAs.

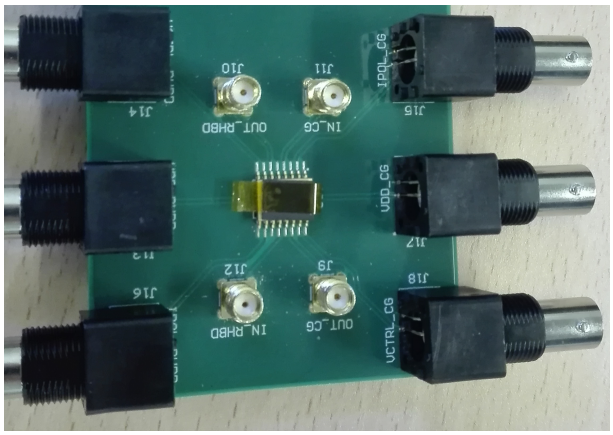


Figure 4.14. Chip mounted on the PCB.

In order to measure the S-parameters of the fabricated LNAs, the setup shown in Figure 4.15 has been employed. In this case, the *8720ES S-Parameter Network Analyzer* from *Agilent* has been used. The input and the output of each LNA are connected through the SMA ports to Port 1 and Port 2 of the network analyser, respectively. It should be taken into account that an external bias tee is required at the input of the circuit. The supply voltages and currents are generated using the *B1500 Semiconductor Device Analyzer* from *Agilent*. In order to perform the measurements, the setup must be previously calibrated. This has been done for both the CG LNA and the RHBD CG LNA.

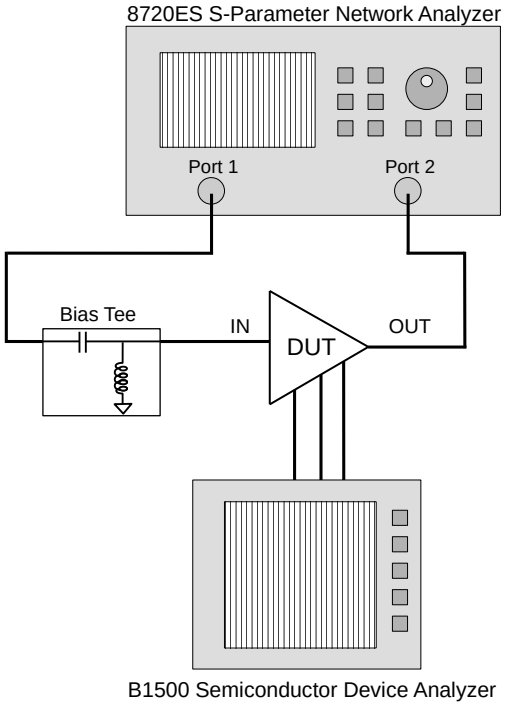


Figure 4.15. Setup for S-Parameters measurements.

Table 4.3 shows the values of the different parameters used in this setup. It should be noted that the control voltage is set to 1.8 V in order to set the LNA at maximum gain.

Table 4.3: S-Parameters measurement setup parameters.

Parameter	Value
Bias current [μA]	700
Supply voltage [V]	1.8
Control voltage (V_{ctrl}) [V]	1.8
Input Power [dBm]	-40
Frequency range [GHz]	2-3

Regarding the NF measurements, Figure 4.16 shows the employed setup where the *E440A PSA Series Spectrum Analyzer* has been used. In order to perform the NF measurements, the input of the LNA is connected to the noise source (*Agilent 346C*), while the output of the LNA is connected to the spectrum analyzer. In the same way as for the S-parameters measurements, the supply voltages and current are provided by the *B1500* device.

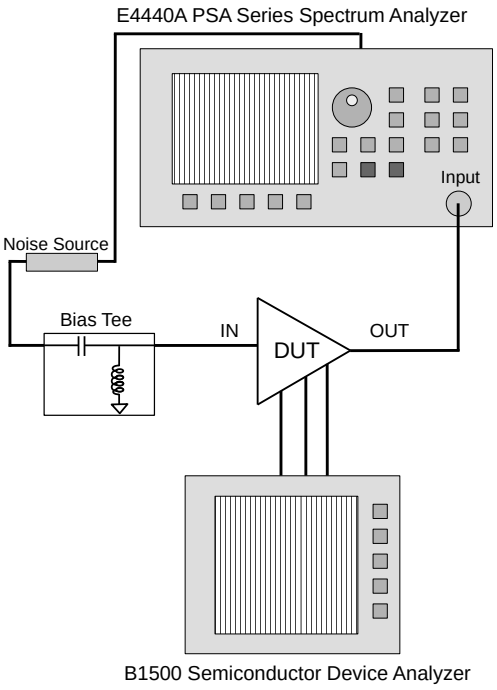


Figure 4.16. Setup for the NF measurements.

Figure 4.17 shows the S-Parameters and NF measurement results for both the CG LNA and the RHBD CG LNA.

If these results are compared with the simulation results of the post-layout simulations of the LNAs, it can be seen that the operating frequency of the amplifier has shifted from 2.4 GHz to approximately 2.2 GHz. This is due to the fact that there is a long metal strip that connects the inductor and the capacitor that form the tank circuit of the LNA. This metal strip increases the inductance at this node, which causes the mentioned frequency shift. Additionally, the parasitic capacitances that appear during the fabrication process further increase this frequency shift.

It can also be observed that the gain has considerably decreased due to the parasitic resistances inherent to the fabrication process. In order to compensate this gain loss, the supply current which feeds the current mirror of the LNA is increased. Figure 4.18 shows the measurement results for a current of 1 mA.

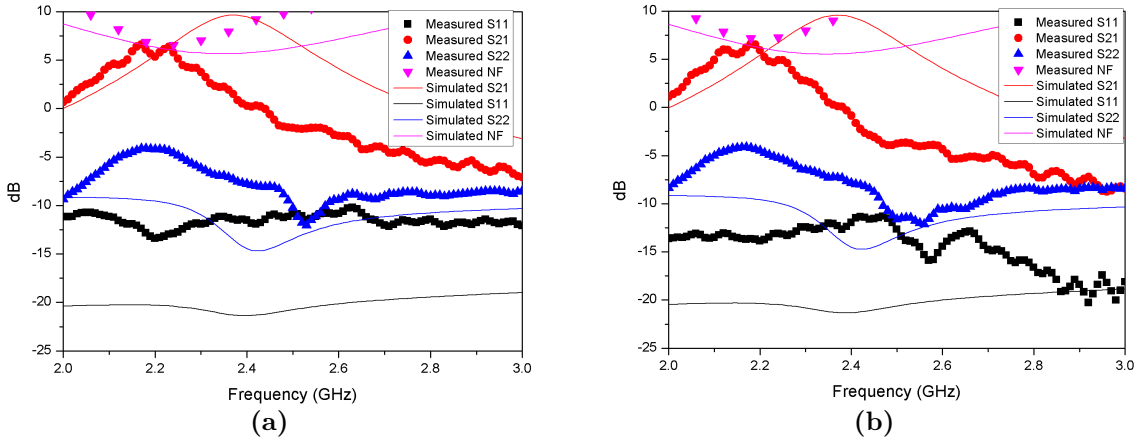


Figure 4.17. Measurement results (a) Common-gate LNA (b) Common-gate RHBD LNA.

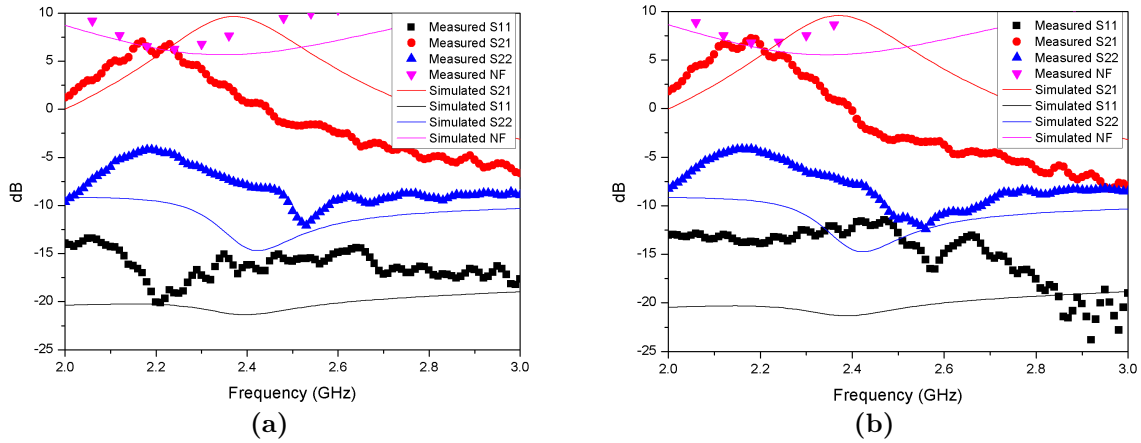


Figure 4.18. Measurement results (bias current = $1mA$) (a) Common-gate LNA (b) Common-gate RHBD LNA.

It can be observed that the gain and the NF have slightly improved, as well as the S_{11} and S_{22} parameters in the case of a current of 1 mA. However, the NF has almost the same value as the gain at a frequency of 2.2 GHz. Nevertheless, until this point the losses due to the PCB and the package have not been considered. Taking into account that the test board was fabricated using the *RO4003C* material from *Rogers*, the losses due to the test board are approximately 0.04 dB. This value is obtained from the fact that the *RO4003C* material has an insertion loss of 0.044 dB/inch at a frequency of 2.5 GHz. Considering that both the input and output paths of the RF singal in the board have a length of approximately 0.5 inches, the total loss due to these paths is the 0.04 dB mentioned previously. Additionally, the voltage standing wave ratio (VSWR) of the SMA connectors has a maximum value of 1.3, which translates to an insertion loss of 0.07 dB. Therefore, it can be stated that the package is responsible for a great part of the losses. In fact, this type of package generally has a great signal attenuation. For example, [43] obtains a 1.5 dB loss in the gain of a distributed amplifier using a 16-pin dual in-line package (DIP)-style ceramic small-outline IC (SOIC) mounted on a test board. This result

is in concordance with the results obtained in [44], where the S-parameters of two small-outline packages are measured. The packages studied have 8 and 28 pins, respectively. At 2.4 GHz the 8-pin package has an S_{21} parameter of -2.5 dB, while the 28-pin package obtains -1.25 dB. Therefore, a 16-pin package, like the one used in this work, can be assumed to have a loss of approximately 2 dB.

Regarding the NF, it has increased due to the decrease in gain mentioned previously. This can be proved by analysing the Friis formula (Equation 4.2), where it can be seen that a decrease in gain produces an increase in noise.

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \cdots + \frac{F_n - 1}{G_1 G_2 \cdots G_{n-1}} \tag{4.2}$$

To sum up, the combination of the parasitic elements of the integrated circuit and the losses due to the package result in the decrease in the performance of the LNA presented previously. Figure 4.19 shows the measurement results for a current of 1 mA, with these losses taken into account.

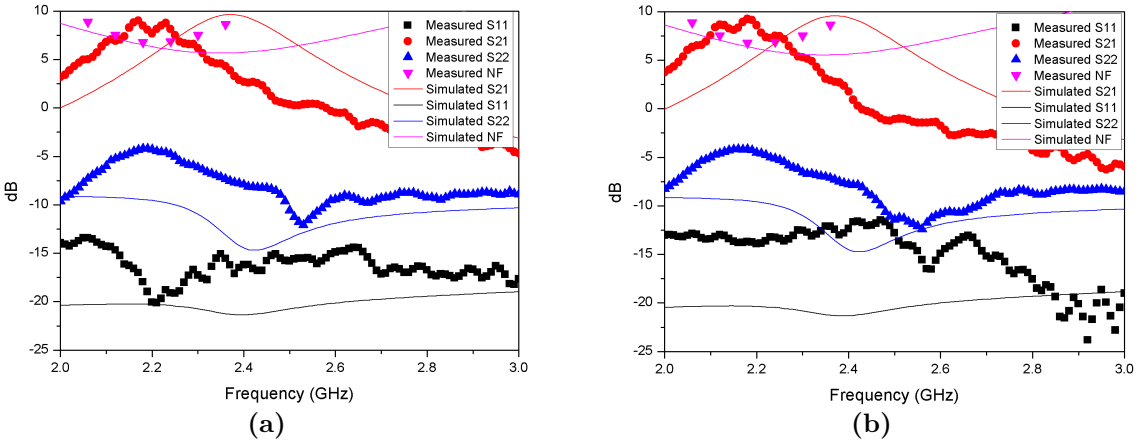


Figure 4.19. Measurement results (bias current = $1mA$ and 2 dB losses not taken into account) (a) Common-gate LNA (b) Common-gate RHBD LNA.

4.6 Conclusion

In this chapter, the effects of radiation in low noise amplifiers has been studied. This analysis is interesting since LNAs are generally the first element in a receiver chain, and their SET response will define the response of the whole receiver.

Two different LNAs have been designed following two well-known topologies, the common-source and the common-gate cascode. Once an adequate performance of these amplifiers was obtained and they met the requirements of the IEEE 802.15.4 standard, the effect of SETs in these LNAs was analysed. To do so, the TCAD-generated curves studied in the previous chapter were introduced in the circuit

domain simulator ADS to analyse the most vulnerable nodes of the CS and the CG LNAs. Simulation results show that the SET performance of both LNAs is considerably more sensitive to strikes at the biasing networks of the circuits. In light of these results, radiation hardening by design techniques were applied at these nodes in order to reduce the effect of SETs, without modifying the RF performance of the LNAs. The main approach was to reduce the voltage peaks by increasing the time constant of the sensitive nodes by including resistances and capacitances. These RHBD techniques considerably reduce the recovery time and the maximum voltage peak of the output signal of both LNAs. The proposed modifications make both LNAs more robust against SETs since 100% of the generated SETs are inside a defined SOA for both the CS and CG.

Due to funding limitations, only the CG LNA was fabricated and measured. Specifically, a CG LNA and its RHBD counterpart were integrated in one chip. A CSOIC-16 package was implemented and the chip was mounted on a custom PCB. The package was designed in a way that the lid can be removed for laser testing to assess the SET response of the circuit. Unfortunately, funding and time limitations made it impossible to test the circuits with laser. This will be further detailed in the conclusions chapter.

The next step consists in analysing the SET response on a whole RF receiver. In the following chapter, several designed low-IF receiver are presented before they are analysed under the effects of radiation.

Chapter **5**

DESIGN OF RF RECEIVERS

In this chapter, the design of different RF receivers is covered. All the receivers presented in this chapter use CMOS technologies and are designed for the IEEE 802.15.4 standard. The first receiver that has been designed follows a low-IF conventional architecture, while the other two have a current-reuse topology. The second of these current-reuse receivers employs a balun-LNA-Mixer (Blixer) topology. The main aim of this chapter is to present the designed receivers and discuss some of the design decisions taken during the process. The receivers presented in this chapter are explained in greater detail in other bachelor and masters dissertations written within the design group [45]-[47]. The performance of these receivers under the effect of radiation will be addressed in following chapters of this document.

5.1 Low-IF conventional architecture

Direct conversion architectures (Zero-IF and Low-IF) are known for their suitability for making radios in a single chip. Zero-IF receivers directly down-convert the RF input signal to baseband needing only a few components. However, some drawbacks appear: dc offset, *1/f* noise, I/Q mismatch, even order distortion and local oscillator (LO) leakage. Alternatively, the low-IF architecture does not exhibit either a severe dc offset or *1/f* noise, but still possesses the drawback of a restricted image rejection which is carried out by a complex filter. The order of the filter depends on the blocking profile imposed to the receiver.

Figure 5.1 shows the blocking profile in the 2.4 GHz band for the IEEE 802.15.4 standard. In this case, the interferers surrounding the desired signal are relatively weak compared with the environment of other radio technologies (WLAN, GSM, WCDMA, etc.). Additionally, the specifications of the image rejection filter are quite loose. As a consequence, a number of IEEE 802.15.4 receivers in the literature use a low-IF receiver architecture [41], [48]-[50].

The proposed receiver architecture is shown in Figure 5.2. The RF input signal is amplified by an LNA and down-converted by a current-mode I/Q mixer. Then, the output current signal is converted to voltage by a transimpedance amplifier (TIA) and filtered by a complex filter to improve the image rejection sensitivity.

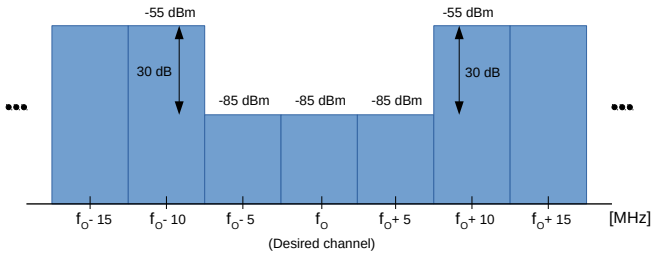


Figure 5.1. Blocking profile in the 2.4 GHz band for ZigBee radio.

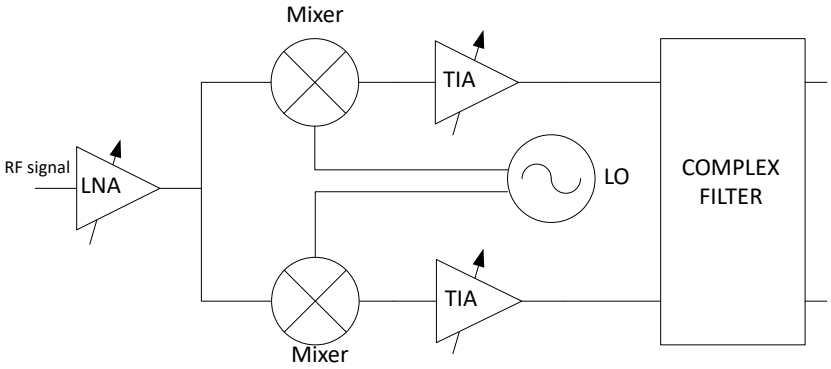


Figure 5.2. Architecture of the proposed low-IF conventional receiver.

5.1.1 Low Noise Amplifier

As mentioned in previous chapters, the main goals of the LNA are low noise figure (NF), high gain to sufficiently reduce the NF contribution of the subsequent stages, and high linearity to accommodate high input signal and strong interferences. In addition, the LNA should have a 50-Ω input impedance to match with the output impedance of the off-chip components such as an RF bandpass filter or a transmission/reception switch.

Figure 5.3 shows the schematic of the LNA. As it can be observed, this circuit corresponds to the common-source LNA studied in the previous chapter. In order to read the description and performance of this circuit, please refer to the common-source LNA section of the previous chapter.

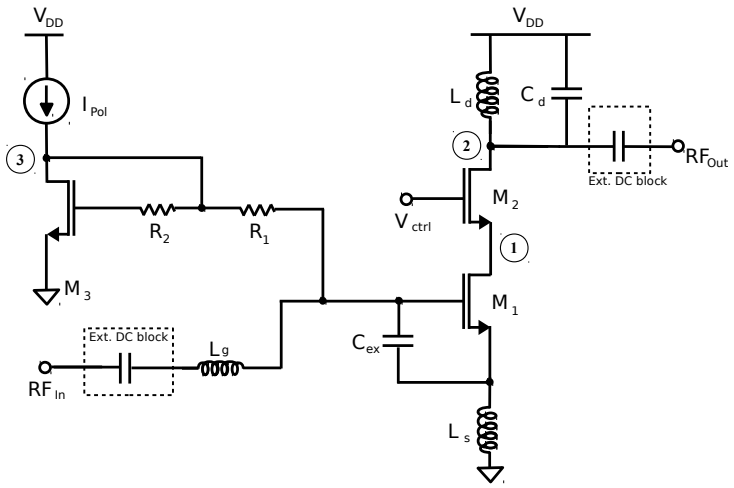


Figure 5.3. Schematic of the Low-Noise Amplifier.

5.1.2 Down-conversion mixer

Figure 5.4 shows the schematic of the down-conversion mixer. A passive double-balanced mixer has been chosen because it dissipates no DC current, provides high linearity and reduces the LO leakage. Also, as no DC current flows through the transistors, the *1/f* noise contribution from the mixers is minimised [51].

The output of the LNA is connected to one terminal of the differential input of the mixer via the coupling capacitor C_d, while the second input terminal of the mixer is connected to AC ground through the bypass capacitor C_{bp}. This approach maintains most of the advantages of the differential circuitry such as the second-order distortion and the LO leakage, with a negligible gain penalty [48].

There are two parameters that can be modified in this mixer to obtain the best possible performance: the device size and the LO signal characteristics. When low noise performance is desired, the width of the transistors should be large enough to provide a low on-resistance. Also, there is a trade-off between the mixer noise performance and the gain of the LNA, which has to be considered when sizing the switches. The LNA has a load impedance which is a parallel resonance circuit that consists of a capacitance and an output inductor. In this case, the inductance must be decreased if the switch capacitance increases. This has to be done so that the resonance frequency does not change, which would decrease the gain of the LNA. Also, the DC level of the LO signal will affect the mixer performance because it controls the switching performance.

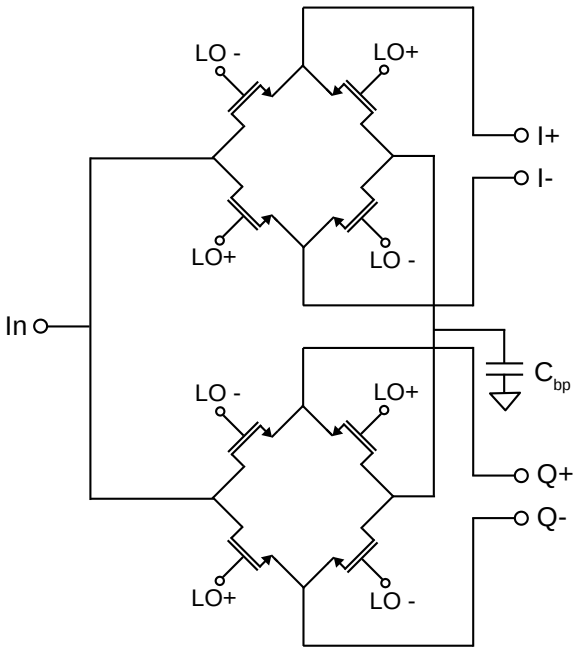


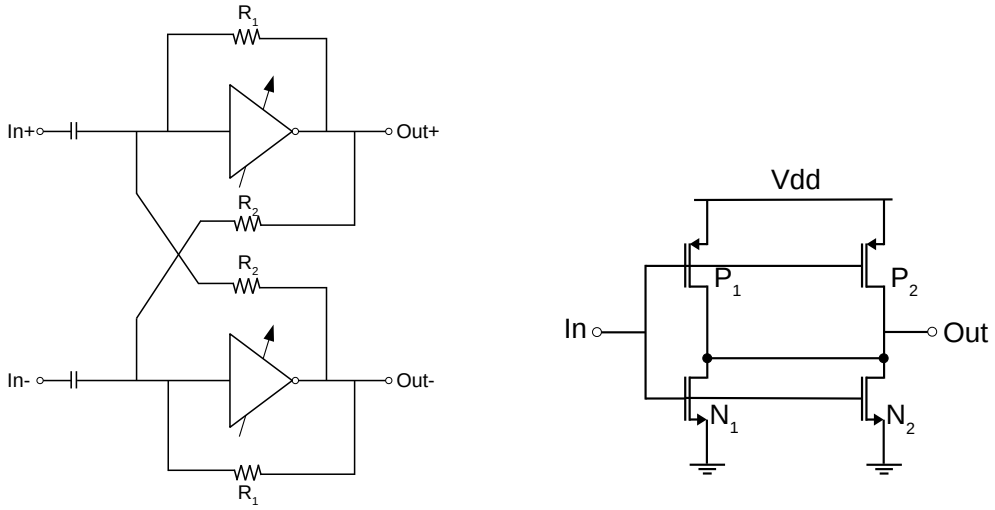
Figure 5.4. Schematic of the down-conversion mixer.

5.1.3 Transimpedance amplifier

The current signal from the mixer is converted to voltage by a TIA. As it can be seen in Figure 5.5 (a), this amplifier consists of two inverters in parallel (Figure 5.5 (b)) and resistive feedback loops. In order to maintain common-mode voltage stability, the resistors R_1 and R_2 are used. These resistors produce an effective resistance for differential signals of $R_1 \cdot R_2/(R_2 - R_1)$. The elimination of the DC offsets produced by the mixer is carried out by a high pass filter formed by this effective resistance and the capacitor C. The high value of this effective resistance allows the input blocking capacitor to be smaller and, as a consequence, both the noise and area are reduced. In Equation 5.1 the voltage gain of the amplifier is shown:

$$A_v = \frac{v_{out}}{v_{in}} = 1 - (g_{MN} + g_{MP}) \frac{R_1 \cdot R_2}{(R_2 - R_1)} \tag{5.1}$$

As it can be seen, by adjusting the g_M of the inverters, the voltage gain can be modified. To allow the TIA to operate at high and low gain modes, the switches SW_1 and SW_2 are used to activate or ground the inverters. The two inverters have been designed with different size ratios. Therefore, depending on which inverter is activated and which is grounded, the high or low gain mode will be achieved.



(a) **(b)**

Figure 5.5. (a) Schematic of the TIA (b) Inverter used in the TIA.

5.1.4 Complex filter

The IEEE 802.15.4 standard requires 0 dB rejection at the adjacent channel (5 MHz) and 30 dB rejection at the alternate channel (10 MHz). This can be accomplished by a Butterworth third order g_m-C complex filter. The main advantage of this topology is that the inherent insertion loss of passive filters can be compensated by the transconductance of the input stage. Also, a good trade-off in terms of power, operating frequency and noise can be achieved [52], [53].

The topology of the complex filter is shown in Figure 5.6. It consists of two Butterworth third order gm-C low-pass filters for the I and Q paths and two crossing extra signal paths per integrator to transform the low-pass prototypes to their bandpass complex counterparts.

In order to reduce the power consumption, inverter based transconductors have been used in the I and Q paths (Figure 5.7(b)). The main issue with this kind of transconductors is the difficulty of setting the DC levels. To maintain the output common-mode voltage stability, Nauta's transconductors (Figure 5.7(a)) have been used in the crossing signal paths that connect the I and Q branches [54]. In this type of transconductors, inverters Inv3, Inv4, Inv5 and Inv6 are used to maintain the common-mode stability and enhance the DC gain. Common-mode stability follows if the common-mode gain (A_{CM}) is less than unity. Moreover, if the width of the transistors in Inv4 and Inv5 are designed slightly smaller than those of Inv3 and Inv6, the differential mode gain (A_{DM}) is boosted [55].

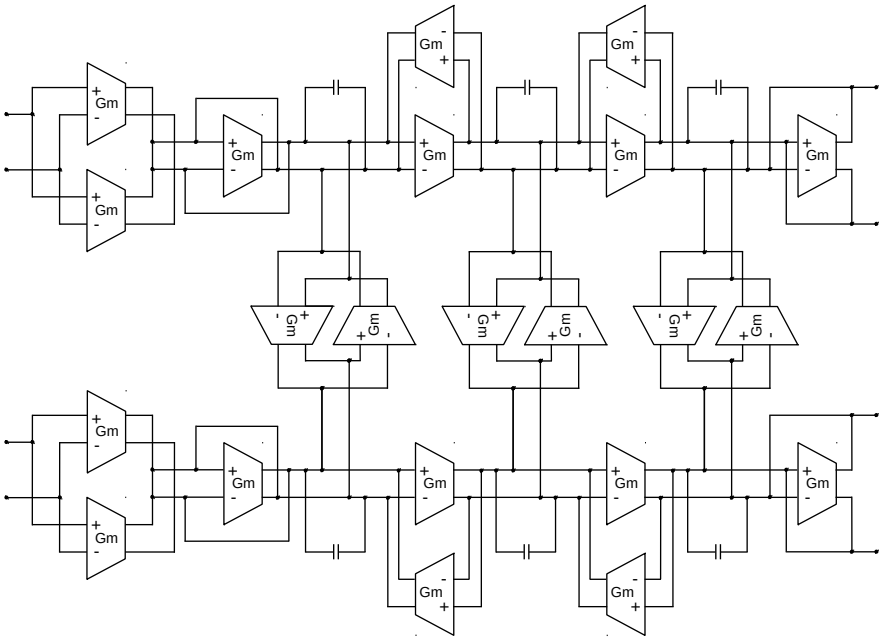


Figure 5.6. Schematic of the complex filter.

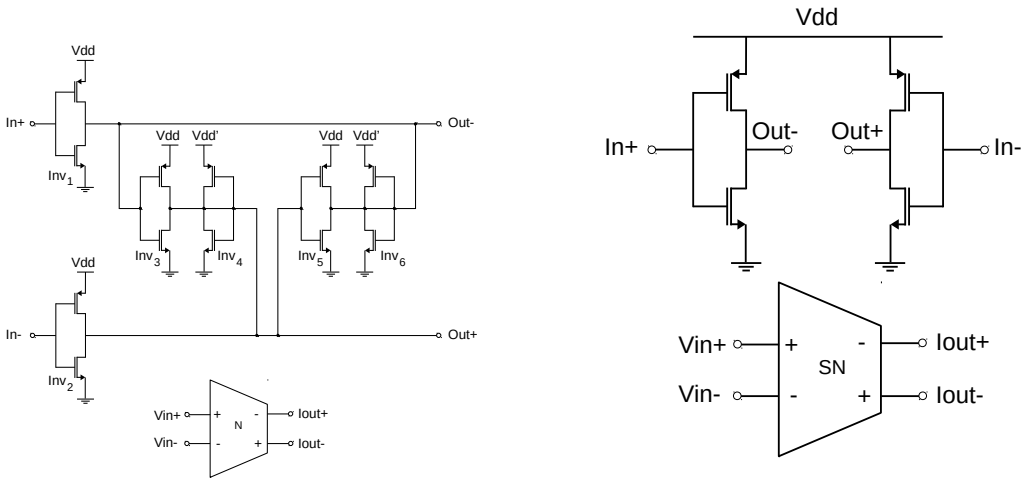


Figure 5.7. (a) Nauta's transconductor (b) Simplified Nauta's transconductor.

The frequency response of this filter is shown in Figure 5.8. As a consequence of both dispersions in the process of fabrications and variations of the voltage power supply, this frequency response may suffer variations. These deviations can be compensated by controlling the voltage supply of the transconductors with a tuning circuit that controls the voltage supply of both the TIAs and the complex filter transconductors. For this reason, these circuits have been designed to work with a 1.4 V supply voltage instead of 1.8 V, which is the supply voltage for the rest of the

receiver. In the Nauta's transconductors, the voltages Vdd and Vdd' are used for frequency tuning and quality factor tuning, respectively.

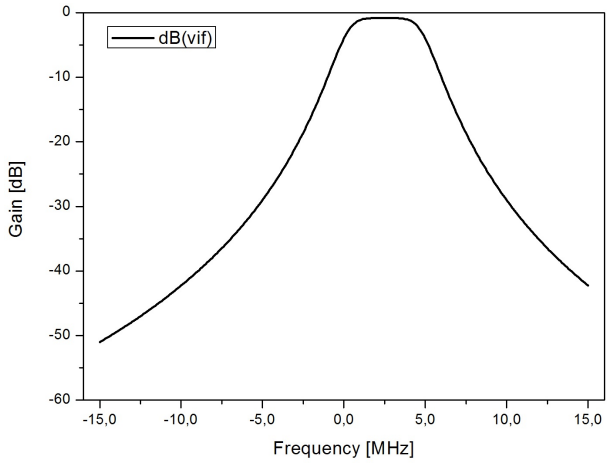


Figure 5.8. Complex filter frequency response.

5.1.5 Layout design of the low-IF conventional receiver

The layout of the conventional low-IF receiver was designed using the Virtuoso software tool by Cadence and implemented in the 0.18 μm UMC CMOS technology. Figure 5.9 shows the designed layout of the receiver front-end, formed by the LNA, mixer and TIA. The receiver front-end occupies a total area of 855 μm x 840 μm. It can be seen that the elements which restrict the total area of the circuit are the inductors present in the LNA [56].

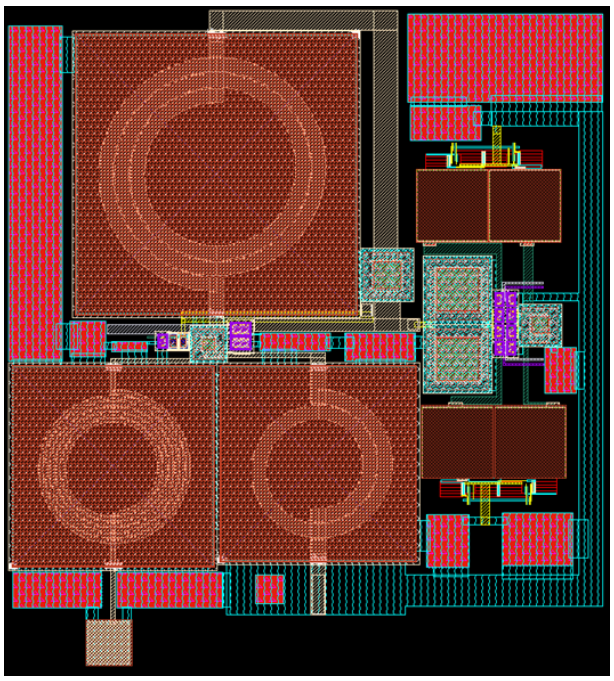


Figure 5.9. Layout of the low-IF conventional receiver.

Figure 5.10 shows the designed layout of the complex filter. It can be seen that the elements which occupy the biggest area are the capacitors. The whole complex filter occupies an area of 300 μm x 262 μm [57].

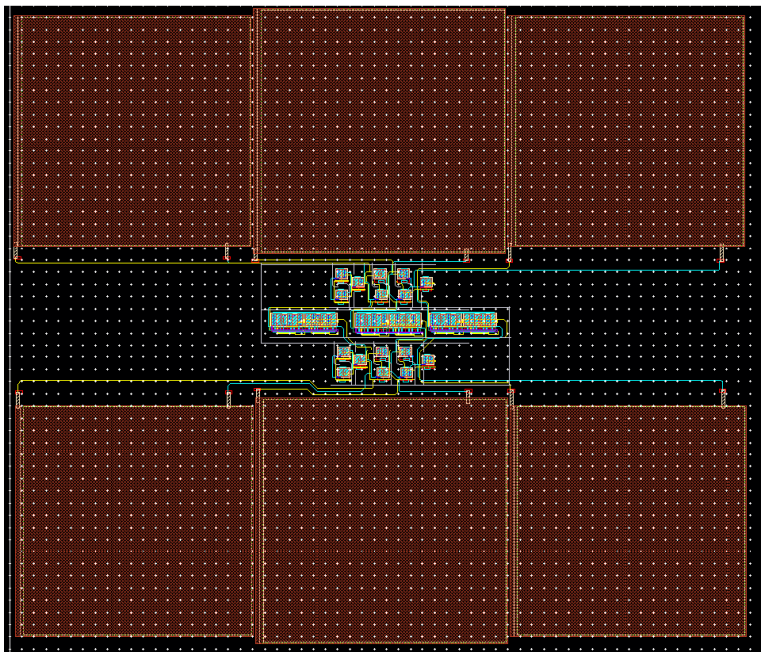


Figure 5.10. Layout of the complex filter.

5.1.6 **Low-IF conventional receiver simulation results**

The performance of the proposed receiver has been simulated using Advanced Design System (ADS) software. The total power consumption of the receiver is 4.19 mW (1.7 mA at 1.8 V for the LNA, 60 μA at 1.4 V for the mixer and TIA, and 0.85 mA at 1.4 V for the complex filter [57]).

The input matching of the receiver is shown in Figure 5.11 (a). It can be observed that for 2.4 GHz the S_{11} parameter is below -10 dB, resulting in an adequate input matching. The gain and NF for the entire IEEE 802.15.4 standard band are shown in Figure 5.11 (b). The noise figure varies from 10.3 dB to 12 dB over the whole band, while the gain fluctuates between 41.7 and 43.7 dB. The simulated value of the receiver's NF for one channel is shown in Figure 5.11 (c). The simulation shows a constant value of approximately 10.3 dB, with a high rise at low frequencies due to the *1/f* noise. Figure 5.11 (d) shows the frequency response of the receiver. It can be observed that the maximum gain is over 43 dB, while the rejection of the adjacent channel is 29 dB. Finally, the simulated value of the third-order input intercept point (IIP_3) at high gain mode is shown in Figure 5.11 (e). A 0 dBm IIP_3 is obtained when two tones at a 500 kHz offset from the centre of the designed channel are applied at the input.

It is worth mentioning that the LNA has a maximum gain of almost 19 dB and a minimum gain of 4 dB. This is controlled by the LNA's control voltage pin (V_{ctrl}).

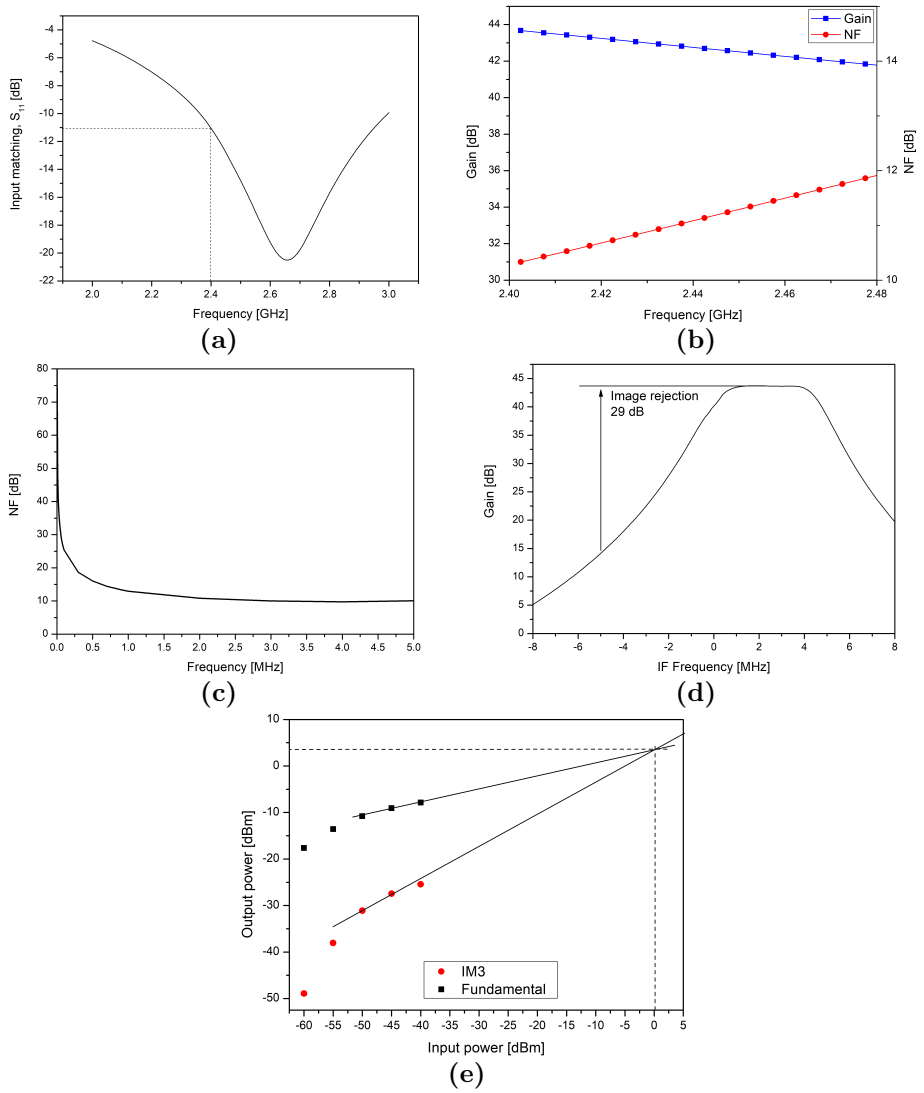


Figure 5.11. Simulation results of the low-IF conventional receiver (a) input matching (b) gain and NF over the entire IEEE 802.15.4 band (c) NF for one channel of the IEEE 802.15.4 standard (d) frequency response (e) IIP_3.

As shown in Figure 5.12, as V_{ctrl} increases, the gain of the LNA also increases, while the NF decreases. In addition, the TIA has a high gain mode of 24 dB and a low gain mode of 1 dB. This is achieved thanks to the switches included in each inverter.

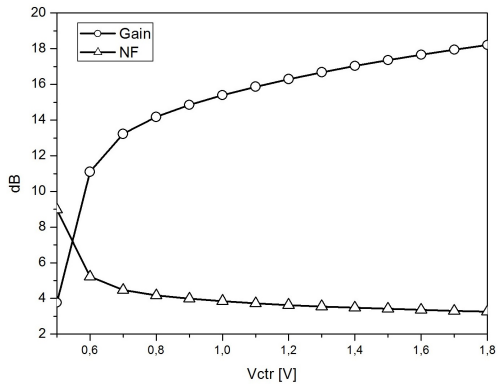


Figure 5.12. Simulated gain and NF of the LNA depending on V_{ctr} of the low-IF conventional receiver.

In Table 5.1, the total gain and NF of the receiver are shown depending on the gains of the LNA and the TIA. The total gain can be varied from 5 to 43 dB, while the NF changes between 10.3 and 43 dB. This increase of the NF at low gain values is acceptable because as the input power increases, so does the tolerable NF. This can be seen in Figure 5.13, where the tolerable system NF of an IEEE 802.15.4 standard receiver versus the received signal power is shown [58]. According to the standard, the input signal ranges from a minimum value of -85 dBm and a maximum value of -20 dBm, which imposes a maximum NF ranging from 15.5 to 78 dB.

Table 5.1: Receiver gain and NF for different gain setups.

LNA gain [dB]	TIA gain [dB]	Receiver gain [dB]	Receiver NF [dB]
4	1	5	43
19	1	20	28
4	24	28	25
19	24	43	10.3

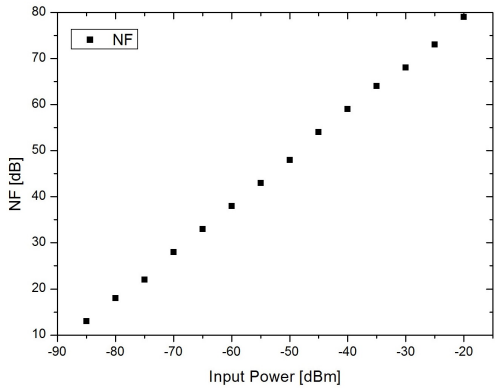


Figure 5.13. Tolerable NF versus received input power for the IEEE 802.15.4 standard.

5.2 Current-reuse architecture

The proposed receiver front-end current-reuse architecture is shown in Figure 5.14. As it can be seen, it follows a differential low-IF architecture. The differential RF input signal is amplified by an LNA and down-converted by an active I/Q mixer. In this case, the bias of the LNA and mixers are stacked in order to reuse the DC current and minimise the power consumption of the entire front-end [59], [60]. The proposed receiver front-end is implemented in the UMC 65 nm CMOS technology.

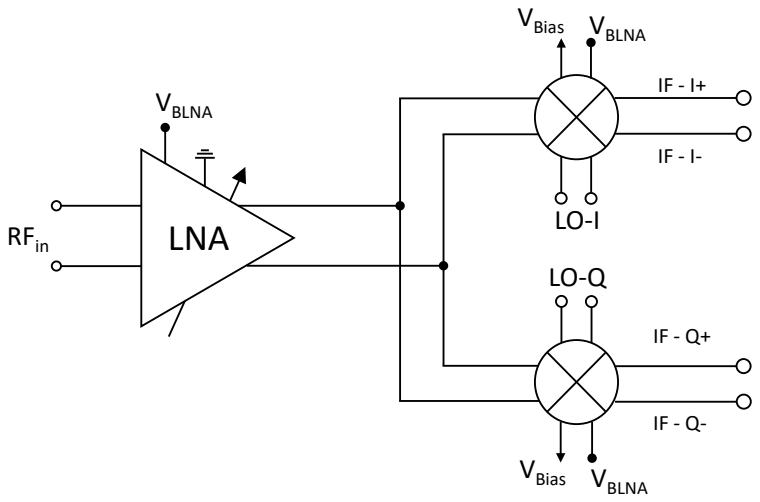


Figure 5.14. System architecture of the current-reuse receiver.

The purpose of this configuration is to minimise the power consumption of the entire front-end by reusing the bias current. To do so, the circuit had to be set up in the way shown in Figure 5.15. The LNA output is connected to the mixer input via capacitors C_7 and C_8, which isolate the DC level that biases the LNA from the input of the mixer. Capacitors C_5 and C_6 are used to maintain the DC voltage level at the tank circuit of the LNA. The front-end is biased with a supply voltage of 1.2 V.

5.2.1 Low Noise Amplifier

For the LNA design, the differential common gate (CG) topology shown in Figure 5.15 was chosen. The CG provides a better input matching than other topologies like the common source (CS) without the need of inductors, which considerably reduces the area of the circuit [61]. In this case, the input impedance is approximately $1/g_{\mathrm{m1}}$, with g_{m1} being the input transistor's transconductance. Regarding the linearity, differential LNAs achieve better performance at the cost of an increase in area and power consumption [61]. This LNA also includes a capacitive cross coupling input, which boosts the g_{m}, increasing the gain and input matching of the circuit [59]. Another advantage of using this input stage is that the noise figure of the LNA can be minimised compared to a conventional CG [62]].

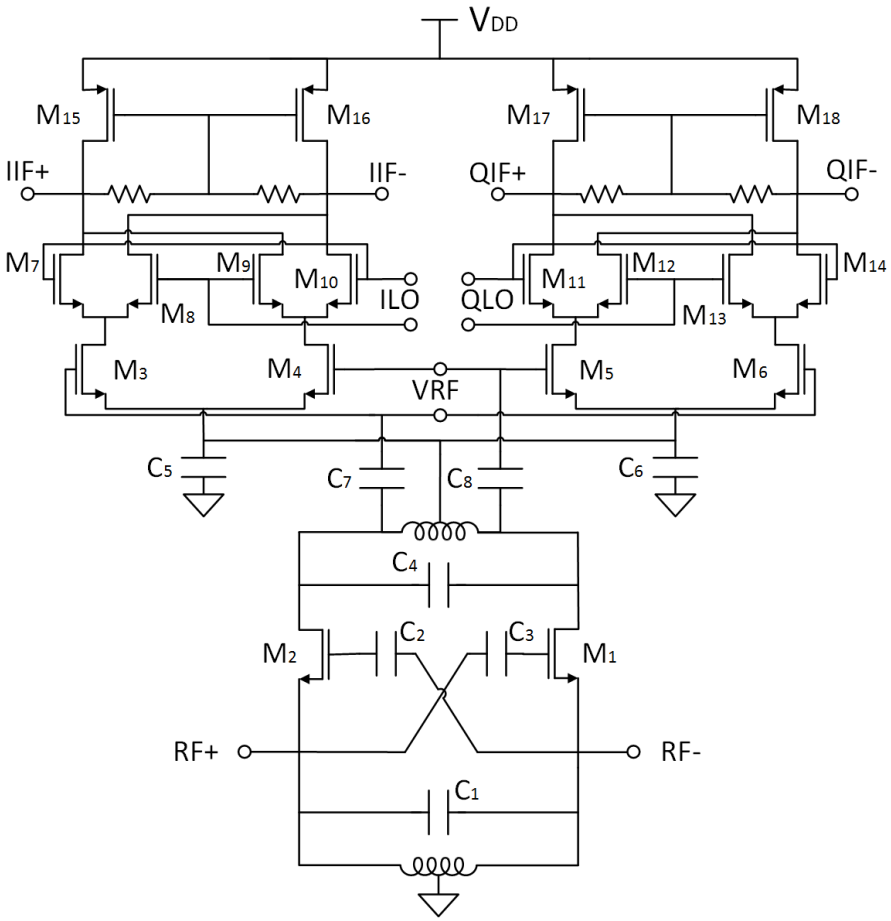


Figure 5.15. Schematic of the current-reuse receiver front-end.

The LC parallel input matching circuit of the LNA is composed of a center-tap inductor and a metal-insulator-metal (MIM) capacitor. Its function is to isolate the DC bias current and the RF input signal. The achieved input matching (S_{11}) of this circuit is shown in Figure 5.16, where the effects of the pad capacitance and the inductance of the wire bonding on the circuit are also taken into account. Considering a fixed pad capacitance (the default value given by the technology) and varying the inductance value for the bonding, the figure shows the range of possible values where the S_{11} is lower than -10 dB. It can be seen that the obtained inductance values range from 0 to 1.4 nH. Therefore, it can be stated that the input matching is considerably robust against the variation of the bonding inductance.

The LC tank circuit at the load of the differential CG LNA also uses a center-tap inductor (L_1) and a MIM capacitor. The center-tap allows having the same inductance value at both branches of the LNA and reducing the size of the tank simultaneously. The sizes of the inductor and capacitor were optimised to have the best tank quality factor for the desired RF frequency. In this case, the capacitor has a value of 0.3 pF while the inductance has a value of 4.5 nH.

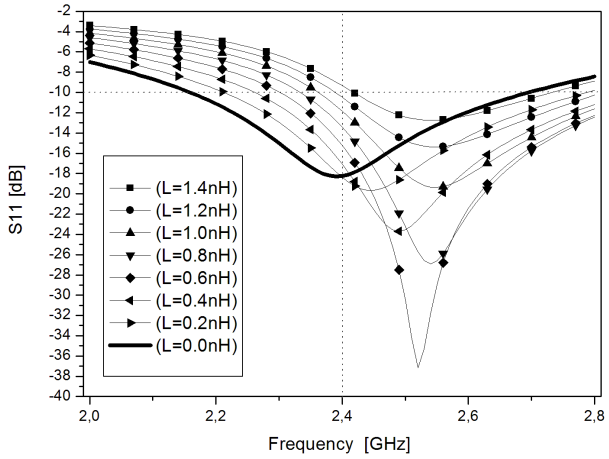


Figure 5.16. Effects of bonding inductance on S_{11}.

5.2.2 Down-conversion mixer

The down-conversion mixer shown in Figure 5.15 is a double-balanced Gilbert cell with active load. This configuration is widely used for the design of RFICs due to its compact structure, good port isolation and high gain. As a downside, it has higher noise figure and power consumption than passive mixers [63]. This down-conversion mixer differentiates between phase and quadrature, with a 90° phase difference between the LO signal injected to each path.

This mixer uses NMOS transistors operating in the saturation region as transconductors and they stack a switching quad to commute the output signals of the two paths. In this case, transistors M_3 to M_6 were optimised to achieve a high transconductance which, in turn, will boost the gain of the mixer. To do so, the transistors were sized by changing their number of fingers. Transistors M_7 to M_{14} are responsible for the commutation of the output signals. Their sizes were fixed to achieve low noise figure and high gain. The active load consists of PMOS transistors that set a reference voltage at the output nodes.

Each transistor of the mixer was biased to achieve maximum gain. A DC voltage was added to the LO signal to bias the switching transistors and control the switching performance.

5.2.3 Current boosting

A typical single-balanced mixer, as the one shown in Figure 5.17 (a), is considered. In order to achieve an adequate gain and linearity performance, the transconductance of the input transconductor formed by transistor M_1 must be sufficiently large. Therefore, it must be biased with a large current. However, the switching stage requires a much lower current to achieve optimum performance. Having a

lower quiescent current reduces the flicker noise of the switching transistors and allows to increase the conversion gain of the circuit. This increase can be caused either by a reduction of the required LO swing to switch the transistors or by increasing the voltage gain with a larger load resistor (R_L) value. If the load resistor value is not changed, the mixer performance for lower supply voltages can be increased with current boosting [63], [64].

The boosting technique consists in applying a current in the transconductor formed by M_1. Injecting current in the transconductor allows maintaining a low current in the switching stage while improving the performance of the mixer in terms of gain and NF. The current injection at the transconductor node can be performed by using a constant current source or a transconductor implemented with a PMOS transistor, as shown in Figure 5.17 (b) and (c).

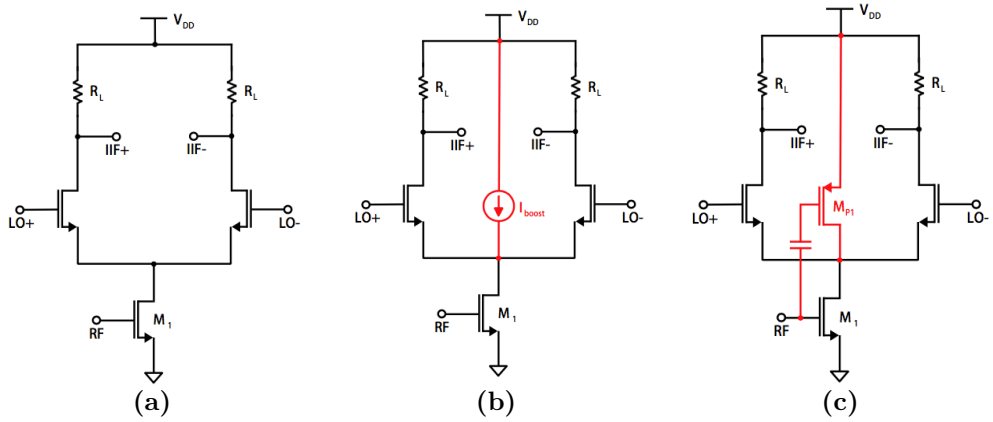


Figure 5.17. Boosting techniques applied in a single balanced mixer (a) None (b) with current source (c) with PMOS transistor.

While a constant current source directly increases the current at the node, which translates into an increase of the transconductance of M_1 (g_{m1}), the PMOS boost source is used as an additional transconductor. This way, the effective transconductance (g_T) of the mixer input stage is the combination of the transconductances g_{m1} and g_{mp1}, with $g_T = g_{m1} + g_{mp1}$. The capacitor is added to let the AC signal from the input pass to both transistors.

Figure 5.18 (a) and (b) show the effect of changing the boost current of the constant source on the gain, NF and third-order intercept point (TOI). As it can be seen, for boost currents between 130 and 160 μA, the performance of the mixer increases. However, if the boost current is too large, the performance deteriorates, with a gain and TOI decrease and a NF increase.

The effect of changing the effective transconductance can be analysed by varying the size of the PMOS transistor. In Figure 5.18 (c) and (d), the size of the PMOS was modified by changing the number of fingers of the transistor. As it can be seen, there is an improvement both in gain and noise figure for a number of fingers between 15 and 22.

In this work, both current boosting techniques have been implemented in the design of the current-reuse receiver at schematic level. In the following section, the simulation results of both design options will be discussed.

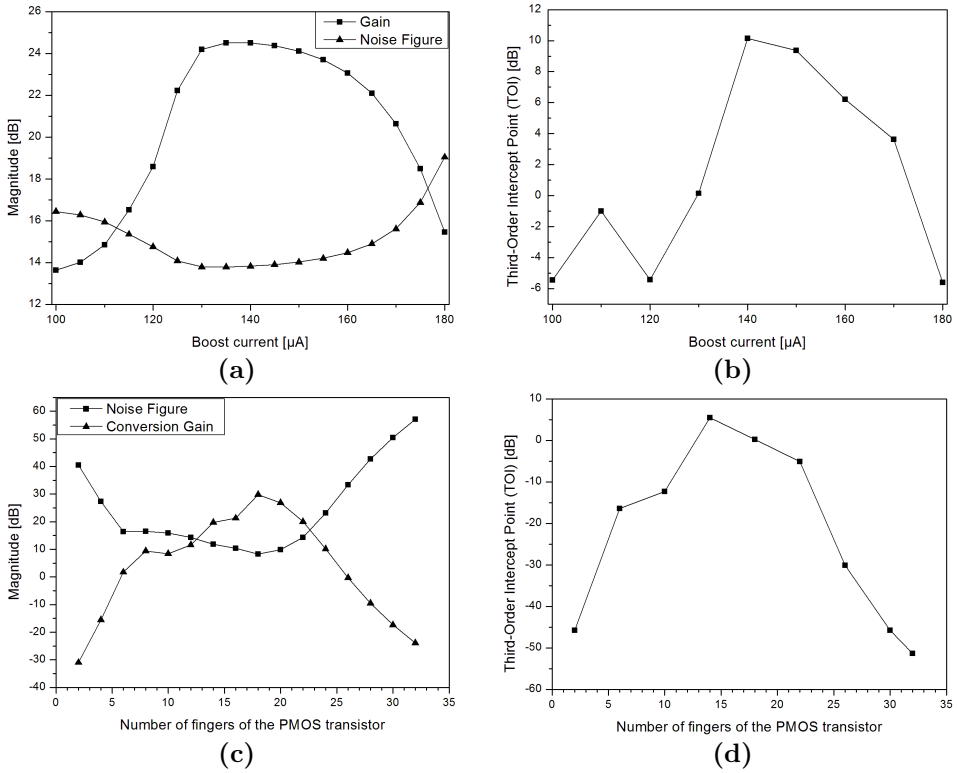


Figure 5.18. Results of simulating boosting with current source and PMOS transistor: (a) Gain and NF with current source (b) TOI with current source (c) Gain and NF with PMOS transistor (d) TOI with PMOS transistor.

5.2.4 **Layout design of the current-reuse receiver**

In the same way as for the low-IF conventional receiver, the layout of the current-reuse receiver was designed using the Virtuoso software tool by Cadence. As discussed earlier, the inductors are the key elements when trying to obtain a compact design since they occupy the largest area. Figure 5.19 shows the layout design of the current-reuse receiver formed by the LNA and the mixer stacked on top. The current-reuse receiver front-end occupies a total area of 484 μm x 221.2 μm [65].

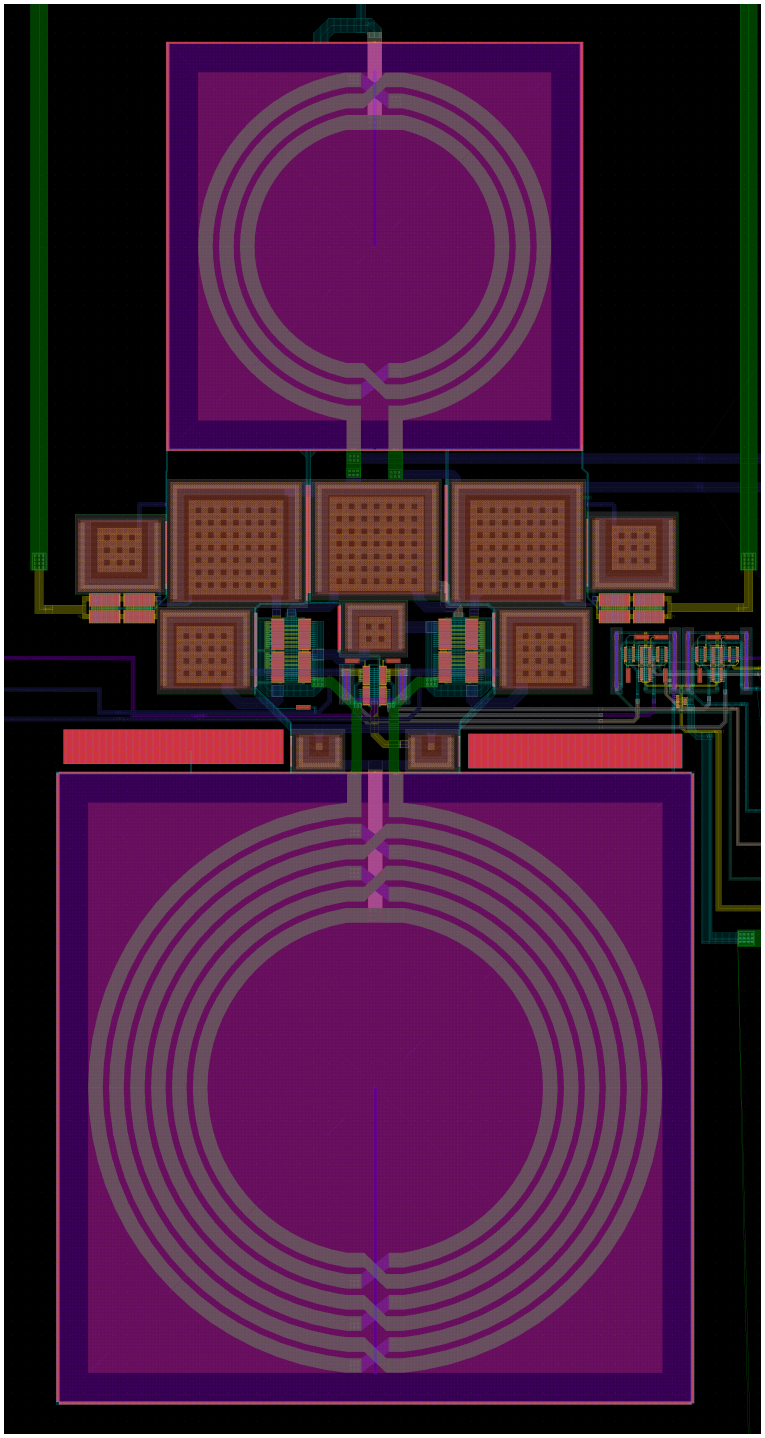


Figure 5.19. Layout of the current-reuse receiver.

5.2.5 Current-reuse receiver simulation results

A summary of the simulation results of the current-reuse receiver is shown in Table 5.2. It can be seen that the current-reuse receiver front-end provides a gain of approximately 25.5 dB and a noise figure of almost 12.4 dB at the desired frequency of 2.4 GHz. However, if the current boosting technique is applied, the performance of the circuit is considerably enhanced, proving this technique to be an adequate solution in this type of architectures. Table 5.2 shows simulation results for both cases studied previously. This is, applying the current boosting technique with a current source and with a PMOS transistor acting as a transconductor. For the current injection with a current source, the power consumption is 2.2 mW (1.83 mA at 1.2 V) with a total conversion gain of 31.02 dB and a NF of 10.75 dB. When the current boosting is performed with an additional transconductor, the obtained power consumption is also around 2.2 mW (1.83 mA at 1.2 V) with a gain of 31.3 dB and a NF of 10.74 dB.

Table 5.2: Simulation results of the current-reuse receiver with different current boosting implementations.

Used architecture	Current-reuse	Current-reuse w/ Current source	Current-reuse w/ PMOS transistor
Power consumption [mW]	2.14	2.2	2.2
LNA gain [dB]	14.55	14.48	13.48
Mixer gain [dB]	10.9	16.54	17.82
Total gain [dB]	25.45	31.02	31.3
Noise Figure [dB]	12.37	10.75	10.74
IIP3 [dBm]	-19	-24	-22

The gain and NF of the front-end for the entire IEEE 802.15.4 standard band are shown in Figure 5.20. The noise figure ranges from 10.7 to 10.81 dB when boosting with the current source and from 10.74 to 10.95 dB when boosting with the PMOS transistor. The gain, presented in Figure 5.20 (b), varies from 31 to 30.8 dB when using the current source and from 31.3 to 30.7 dB with the PMOS transistor.

The simulated value of the third-order input intercept point (IIP_3) at high gain mode is shown in Figure 5.21. This parameter is obtained by applying at the input of the circuit two tones with a 500 kHz offset from the centre of the designated channel. Taking this into account, a -24 dBm and -21 dBm IIP_3 are obtained when the current boosting is applied with a current source and a PMOS transistor, respectively.

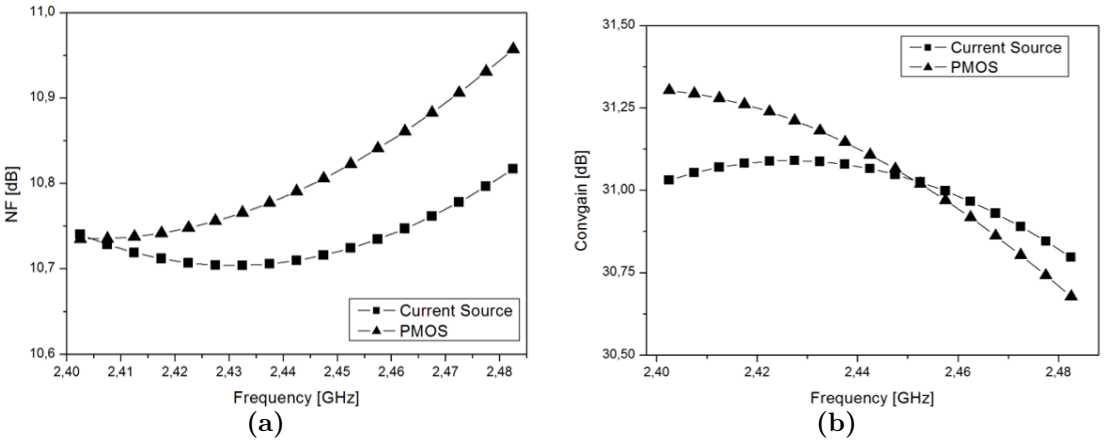


Figure 5.20. Simulated results of the current-reuse receiver over the entire IEEE 802.15.4 band: (a) Gain (b) NF.

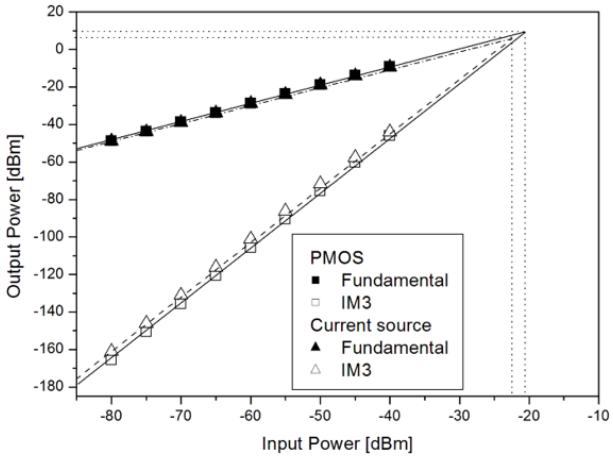


Figure 5.21. Simulated IIP_3 of the current-reuse receiver.

5.3 Blixer architecture

The third receiver front-end that has been designed is presented in this section. The narrowband receiver employs a balun-LNA-Mixer (Blixer) topology, which is formed by a noise-cancelling balun-LNA and a double-balanced I/Q mixer stacked on top of it. The output current signals of the mixer are filtered by a current-mode biquadratic filter (Biquad) which is also stacked on top. The filtered output currents are converted into voltage signals by the complex load, which performs both image rejection and channel selection [60]. The architecture of the receiver is shown in Figure 5.22.

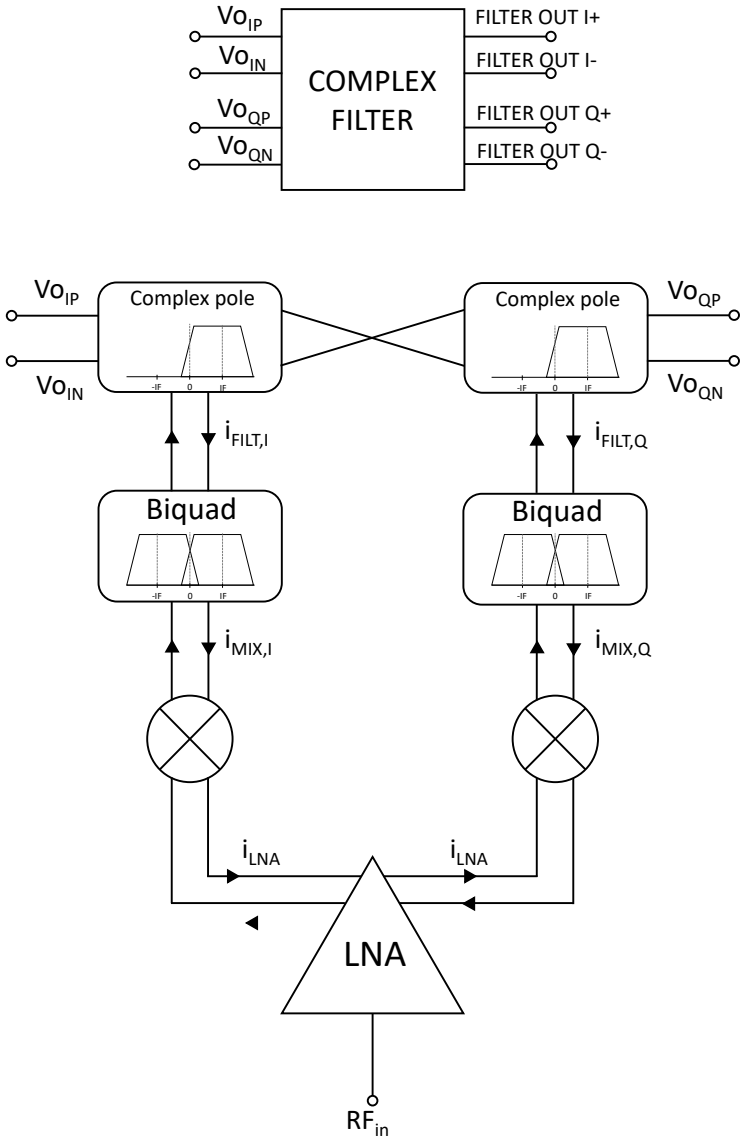


Figure 5.22. System architecture of the current-reuse Blixer receiver.

This Blixer topology is a solution that performs favourably in terms of linearity, input matching, power consumption and area [60], [66]. By comprising all of these elements in a single circuit, the area reduction is considerable. The Blixer also improves the balancing of the output signal, if the output load network is made completely symmetrical. Another attractive property of the Blixer topology is that the bias current of the balun-LNA is reused to perform the mixing. When an I/Q mixer is used, a receiver with high conversion gain can be obtained by reusing the power provided by the balun-LNA [66].

5.3.1 **Low Noise Amplifier**

The designed LNA uses a common-gate common-source (CG-CS) balun-LNA configuration. In this type of configuration there are different design approaches

regarding the noise figure. Figure 5.23 shows the schematic of the basic CG-CS topology.

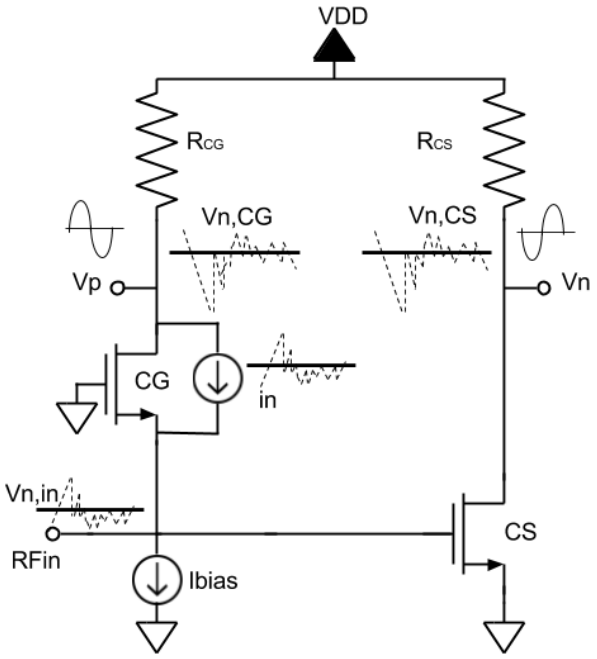


Figure 5.23. Basic CG-CS topology.

There are three design options for the CG-CS topology depending on the value of the transconductances of the CG and CS transistors:

1. The first option considers the transconductances of both transistors to be equal. The load resistors are also equal. Therefore: $g_{mCS} = g_{mCG}$ and $R_{CS} = R_{CG}$. In this case, the noise of the CG transistor is fully cancelled, but this effect is not exploited to achieve a NF below 3 dB. The low transconductance of the CS stage ($g_{mCS} = 1/R_S$) needed for input matching translates into a significant noise generation. Furthermore, the noise contribution is aggravated by the voltage being divided in half by the input resistance and the source resistance [67].

2. In the second design option, the CS transconductance is n times bigger than the CG transconductance, and the load resistors are equal. Thus: $g_{mCS} = n{\cdot}g_{mCG}$ and $R_{CS} = R_{CG}$. In this option, as n increases so does the voltage gain, but the NF decreases. Although these effects are very beneficial, this option presents the disadvantage of an increase in gain imbalance. An increase in n means that the voltage gain of the CS-stage also increases while the voltage gain of the CG-stage remains constant [67]. This can be solved by introducing a differential current balancer (DCB) at the output [68].

3. The third option also considers a CS transconductance n times bigger than the CG transconductance, but differs from the second option in that in this case the CS resistor is n times smaller than the CG resistor, so: $g_{mCS} = n \cdot g_{mCG}$

and $R_{CS} = R_{CG}/n$. This approach shows an even faster decrease of NF than in the previous option. This can be explained by the fact that the noise of the CG transistor is fully cancelled in this case. Additionally, the contribution of the CS transistor is inversely proportional to n. In other words, it decreases with a factor of $1/n$ when n increases. In the second option, the contribution of this transistor decreases at a slower rate. Regarding the voltage gain, it remains constant in this approach. The gain of the CS stage remains constant because the transconductance and the resistance of this stage are scaled simultaneously. Therefore, there is no gain imbalance in this design option [67].

Apart from these three options, a gain boosting amplifier can be used to improve the NF, as shown in Figure 5.24 [60], [68]. Taking this into account, the first design option has been used in the designed LNA. This means that the transconductances of the CS and CG transistors are equal, as well as the load resistors, thus: $g_{mCS} = g_{mCG}$ and $R_{CS} = R_{CG}$. This way both transistors can be biased with the same current so no scaling of load is required for output balancing, thus improving the output linearity and gain. The NF reduction can be explained by studying the noise transfer function (TF) of the CG transistor to the differential output (V_p-V_n), which has the expression shown in Equation 5.2 when the input impedance is matched:

$$TF_{in} = -\frac{1}{2}\left(R_L - R_{in}G_{mCS}R_L\right) \tag{5.2}$$

where $G_{mCS} = g_{mCS} + g_{mAGB}$. Considering this, the noise contribution of the CG transistor can be fully cancelled if $R_{in}G_{mCS} = 1$. Therefore, by including the gain boosting circuit, the needed transconductance of the CS transistor is lower. This means that the current required to achieve the desired transconductance is lower, hence decreasing the NF [60].

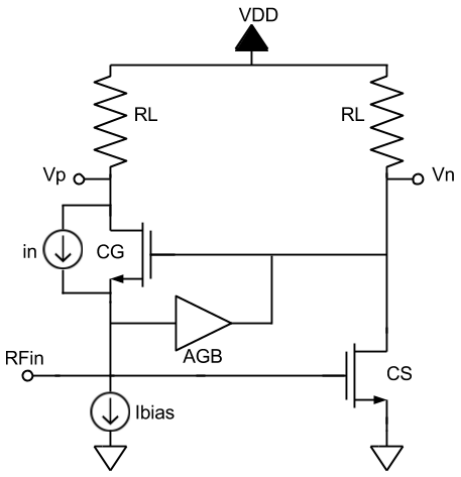


Figure 5.24. Basic CG-CS topology with gain boosting.

Figure 5.25 shows the schematic of the designed balun-LNA, with and without the gain boosting amplifier (A_{GB}). The input matching network is formed by inductor L_M, capacitor C_M and resistor R_P. L_M also sets the bias of the M_1 transistor.

Capacitors C_2, C_3 and C_4 are used for AC coupling. The gain boosting amplifier has a self-biased inverter topology, as seen in Figure 5.26.

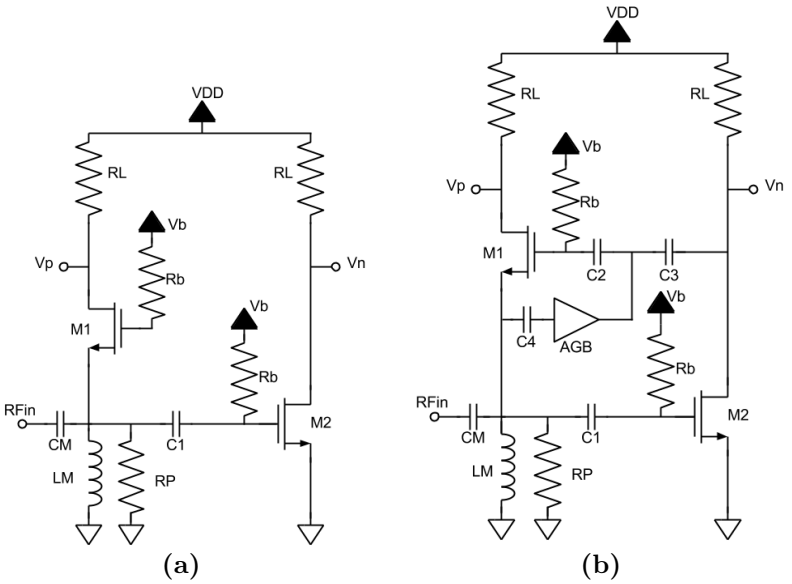


Figure 5.25. Schematic of the balun-LNA (a) without gain boosting amplifier (b) with gain boosting amplifier.

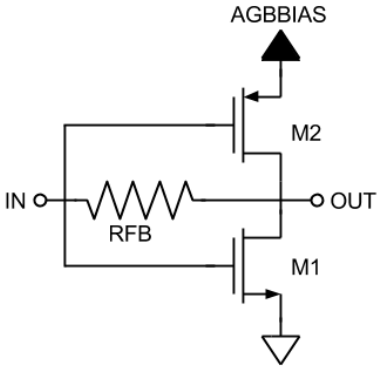


Figure 5.26. Schematic of the gain boosting amplifier.

Figure 5.27 shows the influence of the A_{GB} on the performance of the balun-LNA. Regarding the gain, it can be seen that it considerably increases from a value of almost 13 dB at the desired frequency of 2.4 GHz when there is no A_{GB}, up to a value of 19.5 dB when the A_{GB} is included. As it was explained earlier in this section, the A_{GB} significantly decreases the NF of the balun-LNA. In this case, there is a decrease of more than 5 dB (from 10 dB to 4.7 dB) when the A_{GB} is included. The linearity of the balun-LNA decreases by including the A_{GB} (from an IIP_3 of approximately 2 dBm to -8 dBm), but still performs favourably.

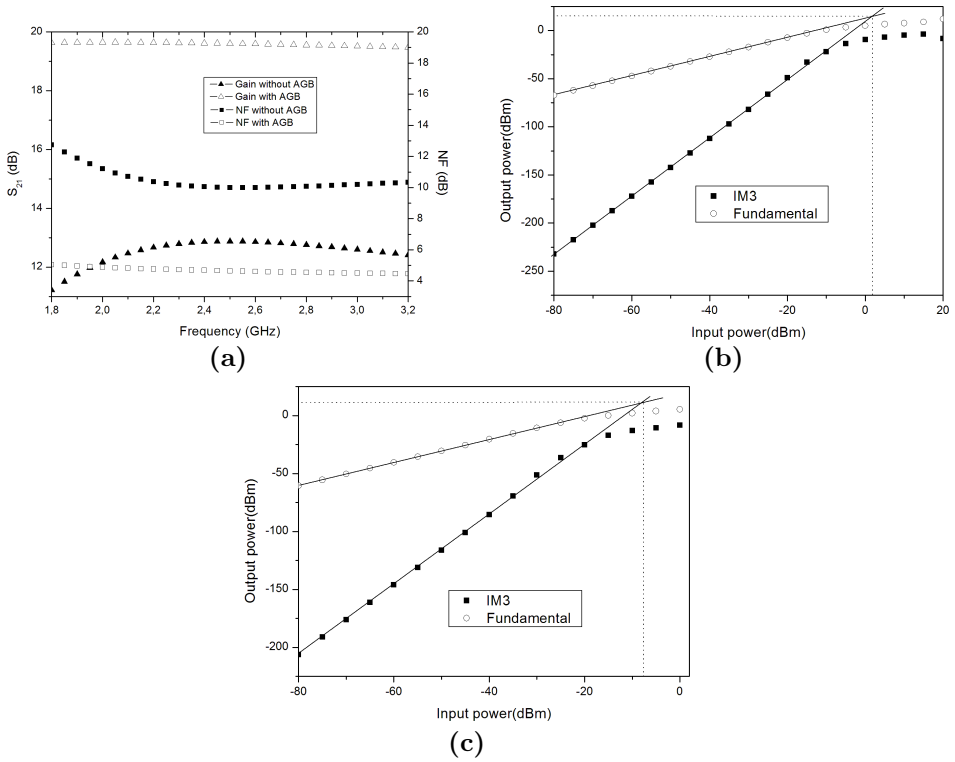


Figure 5.27. Effect of the A_{GB} on the performance of the balun-LNA (a) gain and NF (b) IIP_3 without A_{GB} (c) IIP_3 with A_{GB}.

5.3.2 Down-conversion mixer

The designed double-balanced I/Q mixer is shown in Figure 5.28 stacked on top of the balun-LNA. The mixer distinguishes between I and Q paths due to a 90° shift of the local oscillator signal introduced in each path. As it was explained before, a good output balance is achieved thanks to the equal transconductances and load resistors in the output branches of the balun-LNA.

The switching is done by the $M_{3\text{-}6}$ and $M_{9\text{-}12}$ NMOS transistors. These transistors were sized to obtain the best performance both in gain and NF. A DC voltage level was introduced in the LO signal to bias these NMOS transistors.

In Figure 5.28, the mixer is depicted with an active load formed by the $M_{7\text{-}8}$ and $M_{13\text{-}14}$ PMOS transistors and R_{IF} resistors that set the reference voltage at the output nodes. This load will be replaced later on by the filtering stage which is stacked on top of the mixer.

An important factor to be taken into account when designing a receiver based on a Blixer topology is the duty-cycle of the local oscillator (LO) signal injected in the mixer to perform the down-conversion of the RF signal. Using a 25% duty-cycle LO instead of a 50% duty-cycle results in a better performance in gain (3 dB higher). Also, in current driven I/Q mixers clocked with a 25% duty-cycle LO, all of the current will go to one of the two paths (I or Q) at one instant in time, thus

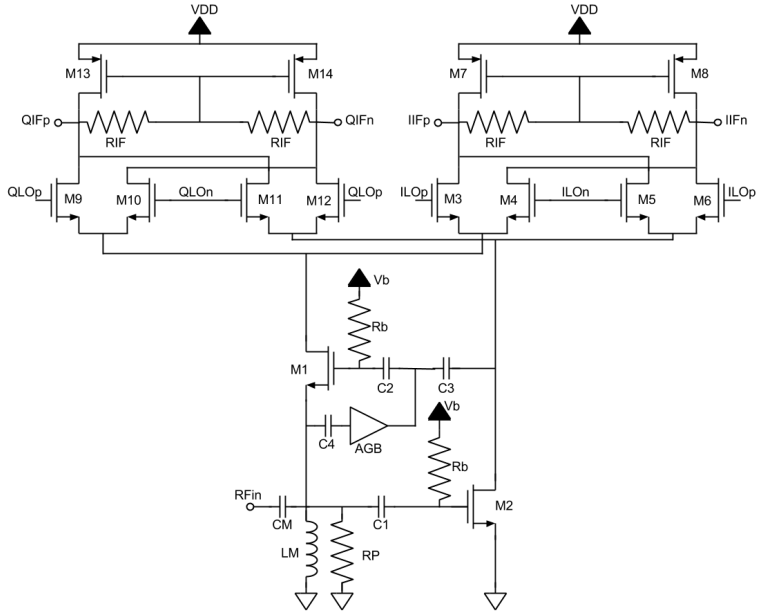


Figure 5.28. Schematic of the proposed Blixer circuit.

improving the power consumption performance [69]. In order to clarify the benefits of using a 25% duty-cycle LO, a theoretical explanation of this concept is presented.

The Fourier series representation for a 50% duty-cycle LO signal can be represented as shown in Equation 5.3:

$$F_{50\%}(t) = \frac{4}{\pi}\left[cos(\omega_{LO} \cdot t) - \frac{1}{3}cos(3 \cdot \omega_{LO} \cdot t) + \frac{1}{5}cos(\omega_{LO} \cdot t) + \cdots\right] \tag{5.3}$$

Whereas the Fourier series representation for a 25% duty-cycle LO can be represented as:

$$F_{25\%}(t) = \frac{2\sqrt{2}}{\pi}\left[cos(\omega_{LO} \cdot t) + \frac{1}{3}cos(3 \cdot \omega_{LO} \cdot t) - \frac{1}{5}cos(\omega_{LO} \cdot t) + \cdots\right] \tag{5.4}$$

Considering the input current as:

$$i_{RF}(t) = G_M \cdot v_{RF} \cdot sin(\omega_{RF} \cdot t) \tag{5.5}$$

the output current $i_{IF}(t)$ is obtained by multiplying the LO signal with this input current. Taking into account that the IF is the difference between the RF and the LO frequency, the output current for duty-cycle d can be written as:

$$i_{IF}(t) = \left(\frac{2}{\pi} \cdot sin(\pi d)\right) \cdot \frac{1}{2d} \cdot G_M \cdot v_{RF} \cdot sin(\omega_{IF} \cdot t) \tag{5.6}$$

The $1/2d$ term introduces a compensation for the increase in the mixer output current given by the $\left(\frac{2}{\pi} \cdot sin(\pi d)\right)$ term as the duty-cycle increases. In practice, this makes the conversion gain for a 25% duty-cycle greater than for a 50% duty-cycle. Given that $v_{IF}(t) = i_{IF}(t) \cdot R_F$ and the conversion gain of a mixer is v_{IF}/v_{RF}, then the difference in gain between using a 25% duty-cycle instead of a 50% duty-cycle is:

$$\Delta G = 20log\left(\frac{2\sqrt{2}}{\pi} \cdot G_M \cdot R_F\right) - 20log\left(\frac{2}{\pi} \cdot G_M \cdot R_F\right) = 3dB \tag{5.7}$$

Moreover, the output balancing is further improved by the mixer under a 4-phase 25% local oscillator signal [60].

5.3.3 Filtering stage

The filtering stage of the Blixer can be divided into two main parts. The first is formed by a biquadratic filter (Biquad) and the second is formed by a complex load, which synthesizes a first order-complex pole at the positive IF for channel selection and image rejection.

The Biquad employs a low-pass RLC structure. However, in order to reduce the area consumption, an active inductor is used. An additional active inductor is included at the source of transistors $M_{2,1}$ and $M_{2,2}$ in order to shift the frequency response of the Biquad to the desired IF. Figure 5.29 shows the complete schematic of the Blixer receiver front-end with the filtering stage stacked on top of the balun-LNA and the mixer.

5.3.4 Blixer receiver simulation results

The proposed Blixer receiver front-end was implemented in a conventional 65 nm CMOS technology. The power consumption of the proposed receiver is only 1.25 mW (a 1.045 mA current consumption with a bias voltage of 1.2 V).

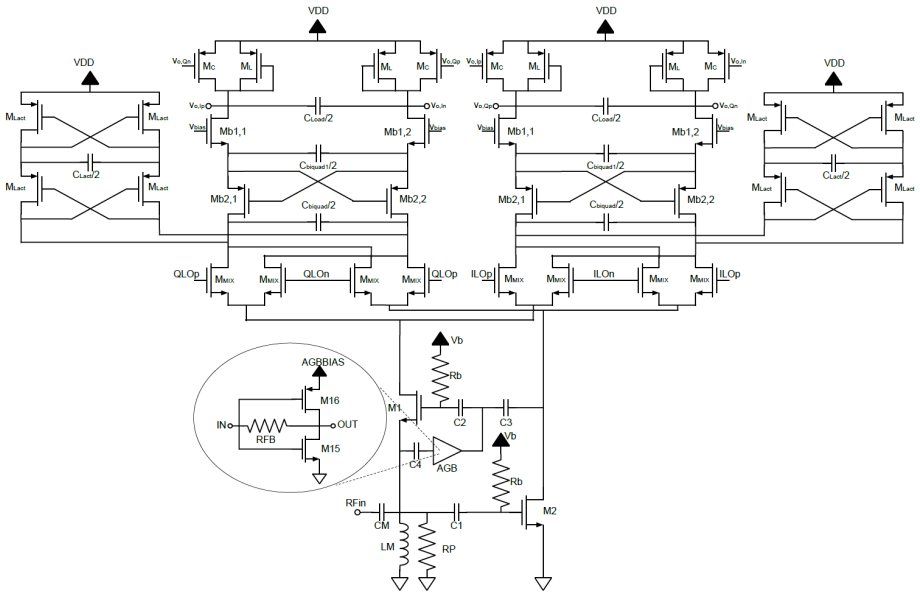


Figure 5.29. Schematic of the receiver-front end current-reuse Blixer topology.

Figure 5.30 shows the frequency response of the Blixer receiver front-end. It can be seen that the gain at the centre frequency (2.5 MHz) is approximately 40 dB. Regarding the bandwidth, it can be seen that the gain drops almost 3 dB at 1.5 MHz and 3.5 MHz, resulting in a bandwidth of 2 MHz. In this case, the receiver has an adjacent channel rejection of 16.4 dB and an image rejection of 13.7 dB.

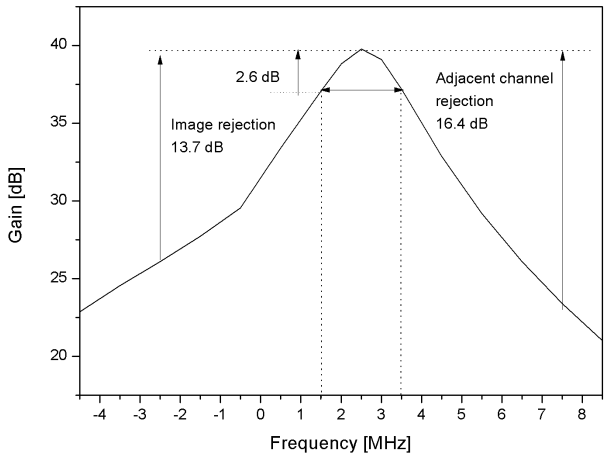


Figure 5.30. Frequency response of the Blixer receiver.

Regarding the gain and NF for the entire IEEE 802.15.4 band, Figure 5.31 shows that the gain is almost constant at a value of 40 dB while the NF has a value of 8.5 dB for the whole band.

Finally, the linearity of the Blixer receiver has been simulated by calculating the IIP_3 parameter. Figure 5.32 shows the IIP_3 obtained in a similar way as for the previously discussed receivers. It can be seen that an IIP_3 of approximately -16 dBm is obtained.

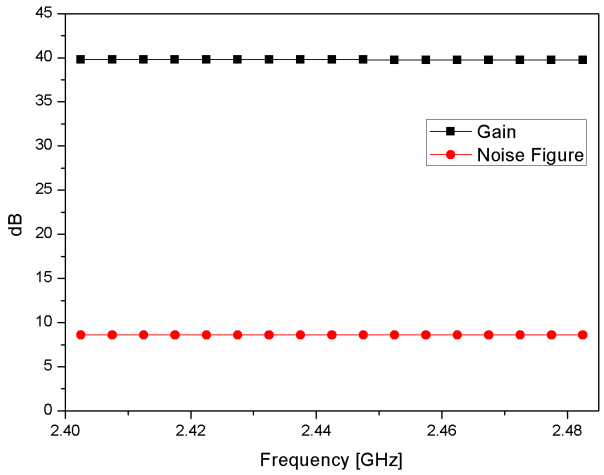


Figure 5.31. Gain and NF of the Blixer receiver over the entire IEEE 802.15.4 band.

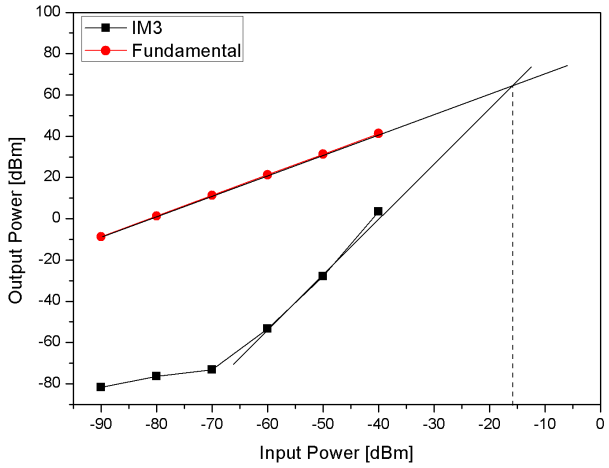


Figure 5.32. Simulated IIP_3 of the Blixer receiver.

5.4 Conclusion

In this chapter, three different low-IF receiver front ends for the IEEE 802.15.4 standard, designed using CMOS technologies, have been presented. The first receiver follows a conventional architecture, while the other two employ a current-reuse structure. The conventional receiver has been implemented using a 0.18 μm CMOS technology by UMC, while the current-reuse receivers have been designed with a 65 nm CMOS technology by the same foundry.

The conventional low-IF receiver is formed by a low noise amplifier with a common-source inductive degenerated cascode topology, a double-balanced passive down-conversion mixer, with a transimpedance amplifier to convert the current signal to voltage, and a complex filter.

The first of the current-reuse receivers is composed of a differential common-gate LNA and a Gilbert cell based double-balanced active down-conversion mixer. The mixer is stacked on top of the LNA in order to reuse the bias current, thus reducing the power consumption of the receiver front end.

Finally, a current-reuse front end based on the Blixer topology was designed. This receiver includes a noise-cancelling balun-LNA and a double-balance I/Q mixer stacked on top of it. A current-mode Biquad filter is also stacked on top, which filters the mixer's output currents that are then converted into voltage by a complex load. This load performs both image rejection and channel selection.

A summarised comparison of the performance of the three receivers is shown in Table 5.3. All of them meet the requirements of the IEEE 802.15.4 standard and perform favourably in terms of high level of integration and low power consumption.

Table 5.3: Summarised comparison of the performance of the desinged receivers.

	Conventional architecture	Current-reuse architecture	Blixer architecture
Power consumption (mW)	4.19	2.2	1.25
Gain (dB)	43	31.3	40
NF (dB)	10.3	10.74	8.5
NF variation in band (dB)	1.7	0.25	0
S_{11} (dB)	-11	-17	-40
IIP_3 (dBm)	0	-21	-16
Technology	0.18 μm	65 nm	65 nm

It is worth noting that the highest gain is achieved by the conventional receiver, but with a considerably higher power consumption. The main drawback of the current-reuse architectures is the linearity, which is worsened by stacking elements on top of each other.

Chapter 6

RADIATION EFFECTS IN RF RECEIVERS

In this chapter, the receivers presented in *Chapter 5* will be studied under the effects of radiation. The main focus of this chapter is to present a procedure to analyse how RF receivers behave under the effects of SETs. To do so, it is paramount to understand how current pulses generated in the low noise amplifier, which is typically the first element of a RF receiver, propagate through the different circuits that form the receiver. These generated pulses have already been studied in *Chapter 4*. First, the propagation of pulses through mixers is studied, followed by the analysis of the effect of filters in such pulses. To do so, ideal structures are implemented in order to perform this theoretical study. Once the behaviour of pulses has been studied, the analysis of single event transients on receivers is performed. The conventional and the two current-reuse receivers explained in *Chapter 5* are considered.

As mentioned in *Chapter 1*, a possible approach is to analyse the distortion produced in the constellation diagram of an RF system under the effects of radiation. However, the symbol rate specified in the IEEE 802.15.4 standard is 62.5 KHz, which means that there is a symbol every 16 μs. Taking into account that the pulses analysed in this work last only a few nanoseconds, the effect of the pulse will have disappeared when the symbol is sampled. Therefore, in this chapter, a procedure where the voltage signal is analysed at the critical nodes of the receiver chain, searching for possible variations in the signal, is proposed.

6.1 Single Event Transients in Mixers

In this section, a thorough study of the effect of single event transients on down-conversion mixers is performed. First, a theoretical study on a single-balanced mixer is carried out. Secondly, a similar study is replicated on a double-balanced mixer. Finally, some real circuits are tested for single events.

Figure 6.1 (a) shows the diagram of an ideal mixer. As it can be seen, the mixer is formed by three main stages: transconductance, switching quad and load. The first is in charge of the voltage to current conversion at the input of the circuit. The current signal is then mixed in the switching quad, which is driven by a local

oscillator (LO) signal. This produces an output signal with a frequency equal to the difference between the RF input frequency and the LO frequency, in the case of down-conversion mixers. This output signal is then converted to voltage in the load of the mixer.

A typical implementation of this ideal structure is the Gilbert cell, which is shown in Figure 6.1 (b). As mentioned previously, the current-reuse receiver presented in the previous chapter implements this kind of structure. The transconductance stage is formed by transistors M_1 and M_2 acting as transconductors, while transistors $M_{3\text{-}6}$ commutate the RF input to the outputs. The load can be implemented in several ways (resistive load, active load, etc.). In this case, the load is depicted as a resistive load for simplicity.

Another implementation of the ideal mixer is shown in Figure 6.1 (c). In this case, a double-balanced passive mixer is shown, where the load is implemented as a transimpedance amplifier (TIA). The main aim of this amplifier is to convert current into voltage, which must be achieved in the load of the mixer. As mentioned previously, the conventional low-IF receiver presented in the previous chapter employs this type of mixer. Taking this into account, the results obtained in the theoretical study of single event transients on ideal mixers can be transferred to any other mixer implementation, such as those implemented in the RF receivers discussed in the previous chapter.

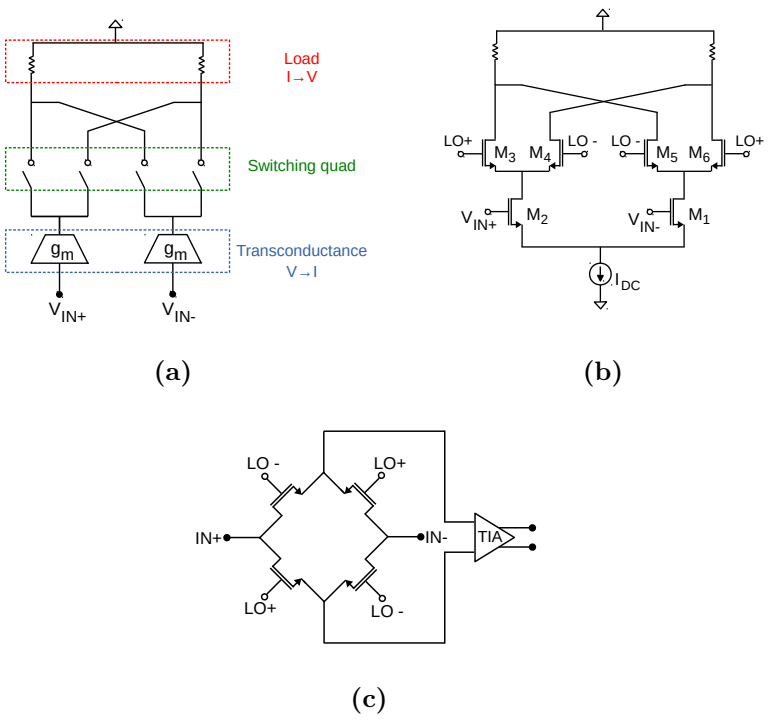


Figure 6.1. Schematic of a: (a) ideal mixer (b) Gilbert cell (c) double-balanced passive mixer plus TIA.

6.1.1 **Single-balanced mixers**

In order to perform a theoretical study of single event transients on a single-balanced mixer, a mixer with ideal components has been designed. Figure 6.2 shows the schematic of such mixer.

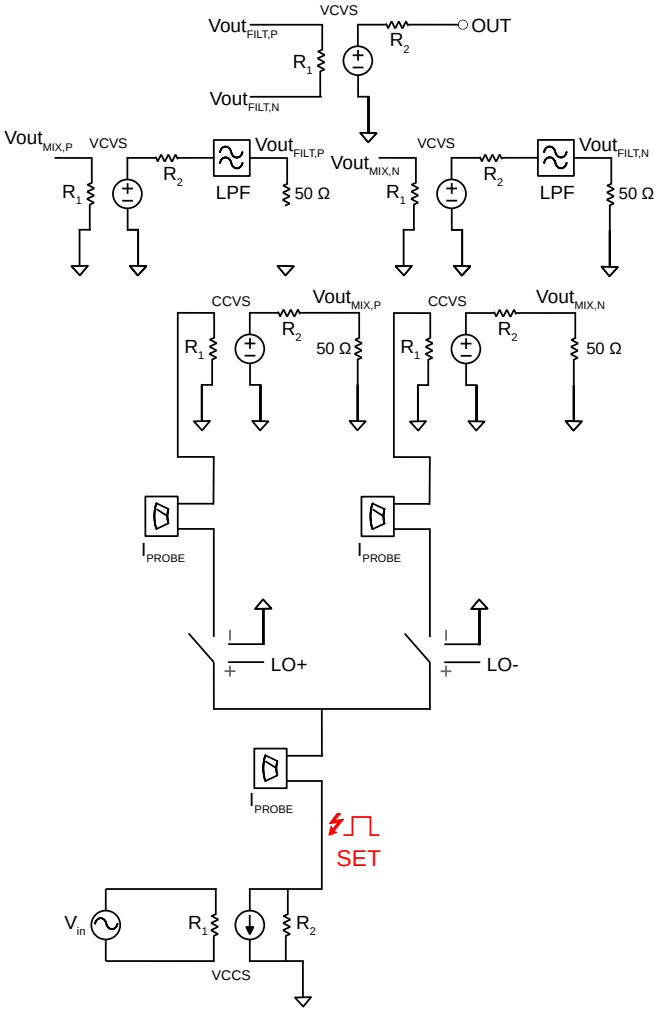


Figure 6.2. Schematic of the single-balanced mixer.

As it can be seen, the RF input signal is introduced as a sinusoidal signal with a P_1Tone. This voltage signal is converted into current with an ideal voltage controlled current source (VCCS). Therefore, this component acts as a transconductor. In this case, the gain of the transconductor is set to 1 S. The differential pair that commutates the RF with the LO signal is implemented with ideal switches (SwitchV model from ADS). These switches are driven by the LO signal and there must be a phase shift of 180° in the LO signal that drives each one of them. Then, the output currents are converted to voltage with ideal current controlled voltage sources (CCVS), whose transresistances are set to 1 Ohm. Finally, the output signals are filtered using ideal Butterworth filters. It should be noted that each branch is filtered

independently from the other. Figure 6.3 shows that, in this case, the LO signal is a pulse wave (with 180° phase shift between + and - signal, as mentioned before) with a peak voltage of 1 V. Table 6.1 shows the frequencies used in this study.

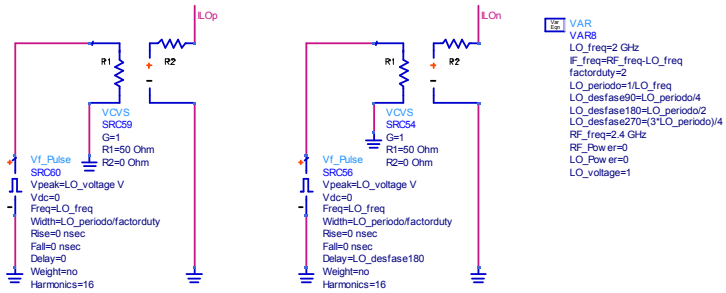


Figure 6.3. LO signal generation.

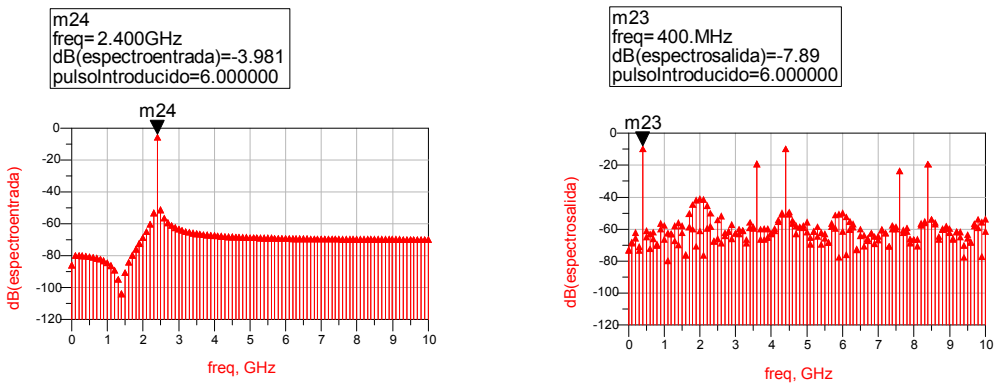
Table 6.1: Frequencies for the single balanced mixer.

RF	2.4 GHz
LO	2 GHz
IF	400 MHz

Well-known mixer theory states that the conversion gain of a single-balanced mixer follows Equation 6.1 [61]:

$$G_c = \frac{2}{\pi} \cdot g_m \cdot R_L \tag{6.1}$$

In this case, both g_m and R_L are equal to 1, so the gain is equal to $2/\pi$ (which is approximately -4 dB). This can be seen in Figure 6.4, where the input and the output signal are represented in the frequency domain.



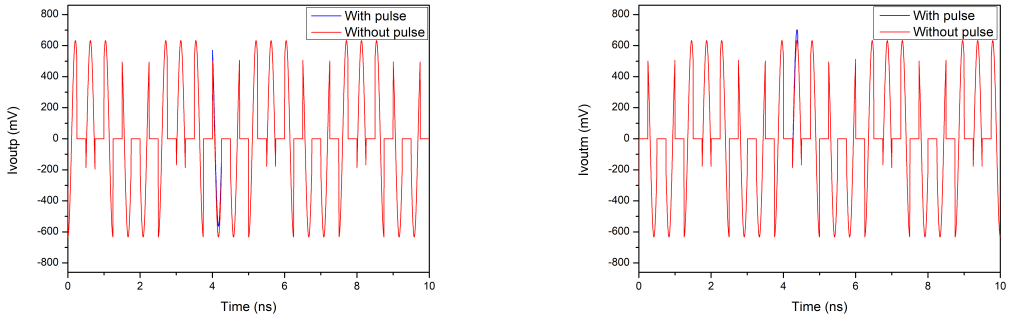
(a) **(b)**

Figure 6.4. Single-balanced mixer (a) Input signal (b) Output signal.

It can be seen that the input signal has -3.981 dB at 2.4 GHz, while the output signal has -7.92 dB at 400 MHz (f_{RF}-f_{LO}), which results in the expected gain of approximately -4 dB.

Once the correct performance of the designed ideal mixer has been confirmed, we can proceed with the study of SETs in this mixer. To do so, current pulses are introduced in the mixer. As mentioned in previous chapters, it is known that in CMOS circuits the effects of SETs are usually simulated with a current source connected at the drain of the transistors. Since in this mixer only ideal components are used, the current pulses will be introduced at the "drain" of the transconductor, as seen in Figure 6.2. The current pulses are generated with an ideal current source. For the moment, they are considered to have an ideal rectangular shape.

In this particular case, the pulse width is $\tau = 400ps$, which is in the order of pulses applied in similar studies [13]. In order to understand how this pulse will be propagated to the output of the circuit, it should be noted that the switches are changing from the ON-state to the OFF-state rapidly with the frequency of the LO signal. In this case, the LO frequency is 2 GHz. At a particular instant, one of the switches is in the ON-state and the other in the OFF-state. Consequently, the transient current finds a path to the output of the mixer. At another time instant, the opposite happens (the switch that was in the ON-state is now in the OFF-state, and vice versa). This occurs periodically, with the period of the LO signal. Taking this into account, it can be considered that the switches are sampling the transient current at each instant [12]. Therefore, the pulse will propagate to the output of the circuit. This can be seen in Figure 6.5, where the single-ended outputs of the mixer (*Ivoutp* and *Ivoutm*) are shown. It should be noted that these signals are before the filtering stage.



(a) **(b)**

Figure 6.5. Single-ended outputs of the mixer when there is a pulse at the input (a) Positive branch (b) Negative branch.

The blue line represents the case when a pulse is introduced and the red line the case when there is no pulse. Figure 6.6 shows the difference between both cases for each branch.

It can be observed that the pulse has been propagated to the single-ended outputs of the mixer. It should be noted that neither of the pulses seen at the single-ended

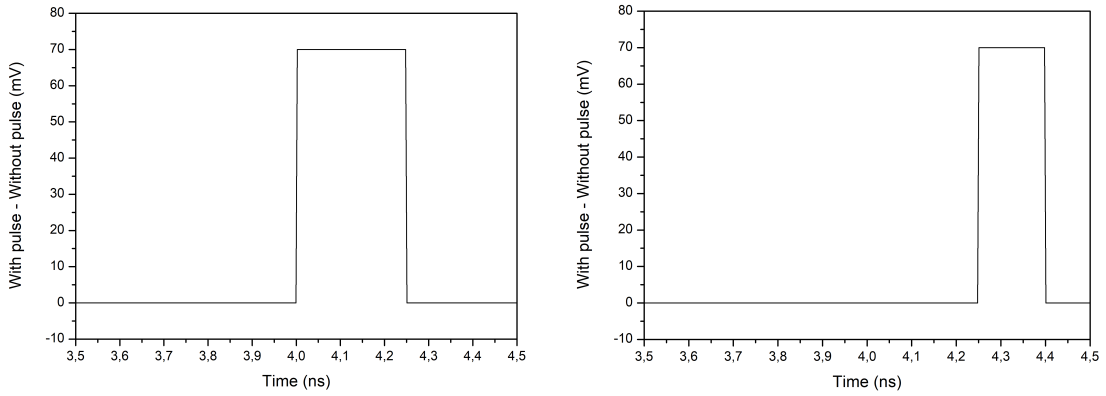


Figure 6.6. Effect of the pulse on single-ended outputs (a) Positive branch (b) Negative branch.

outputs has the same pulse width as the pulse introduced at the input of the circuit. This is due to the behaviour of the mixer where the switches are not simultaneously ON all of the time. However, if these two pulses that appear at the single-ended outputs are added, the original pulse width would be obtained.

Figure 6.7 shows the single-ended outputs after the filtering stage. It can be seen that the period of the signal is approximately 2.5 ns, which corresponds to the inverse of the intermediate frequency (IF) of 400 MHz.

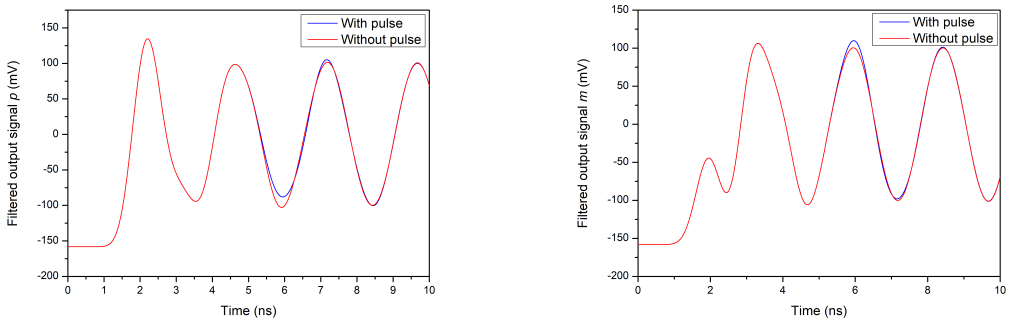


Figure 6.7. Filtered single-ended outputs of the mixer when there is a pulse at the input (a) Positive branch (b) Negative branch.

The blue line represents the case when a pulse is introduced and the red line the case when there is no pulse. Figure 6.8 shows the difference between both cases for each branch.

It can be observed that, after the filtering stage, there is a voltage disturbance, but the original shape of the pulse has not propagated to the output of the circuit. In order for this to happen, the following condition must be met [12]:

$$f_{LO} > \frac{2}{\tau} \tag{6.2}$$

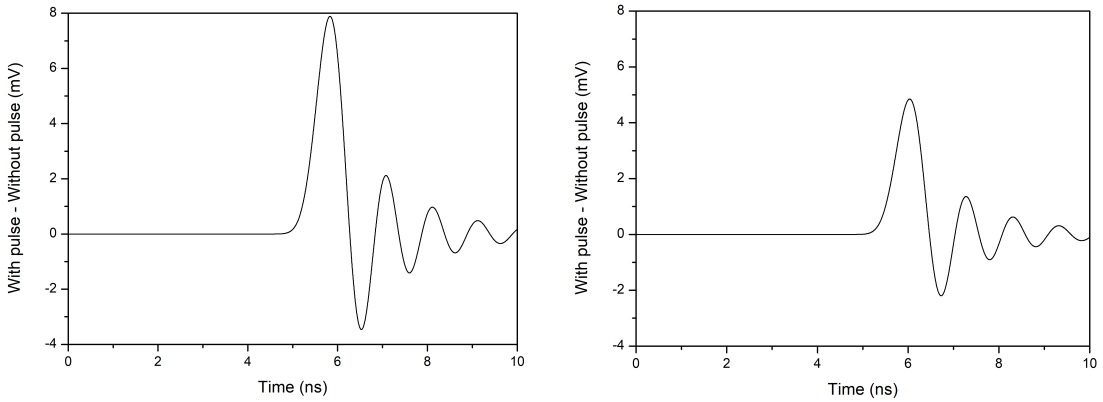


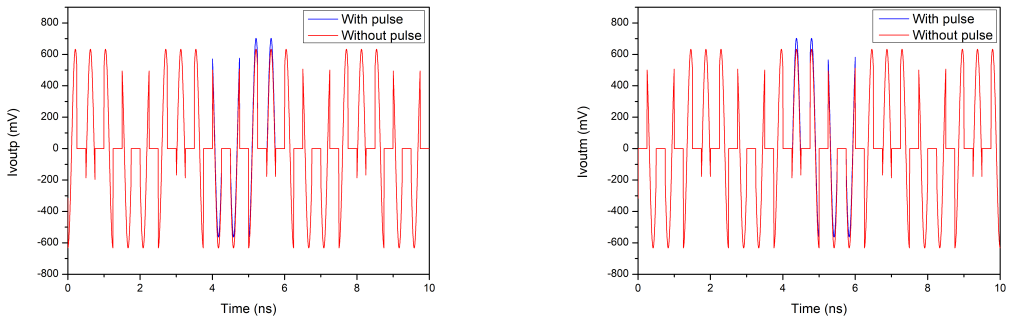
Figure 6.8. Effect of the pulse on filtered single-ended outputs of the mixer when there is a pulse at the input (a) Positive branch (b) Negative branch.

In this case, this condition is not met, considering that the pulse width is $\tau = 400ps$ and f_{LO} is 2 GHz, so:

$$2GHz \not> \frac{2}{400ps} = 5GHz \tag{6.3}$$

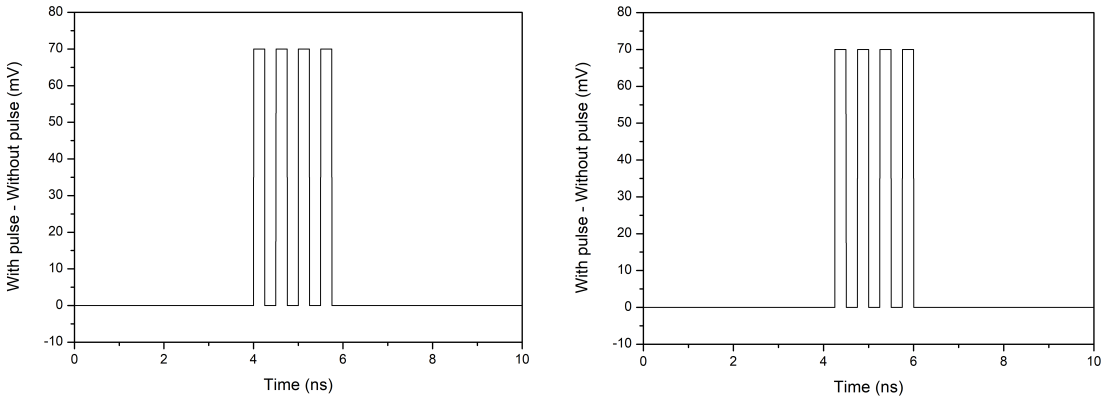
Furthermore, it can be seen in Figure 6.8 that the resulting pulse at the output is larger in the positive branch than in the negative one. This can be explained by the combination of two factors: the instant at which the pulse occurs and the pulse width. In this particular case, with the pulse width being $\tau = 400ps$ and the period of the output signal being T= 2.5 ns, the output pulse will not affect at least one period of the signal. Therefore, the instant at which the pulse occurs is extremely relevant, since it could affect a peak, a valley or a transition of the output signal. Additionally, it should be taken into account the fact that the switches are changing from the ON-state to the OFF-state, so part of the pulse is sampled by one branch and the rest is sampled by the other branch, which can also lead to the discrepancies seen in Figure 6.8.

In order to meet the condition shown in Equation 6.2, the pulse width must be increased. Hence, the same simulations performed earlier are repeated with a pulse width $\tau = 2ns$. Figure 6.9 shows the single-ended outputs before the filtering stage, while Figure 6.10 shows the difference between the case of a strike occurring and the case of no strike, for each branch.



(a) **(b)**

Figure 6.9. Single-ended outputs of the mixer when there is a pulse at the input ($\tau = 2ns$) (a) Positive branch (b) Negative branch.



(a) **(b)**

Figure 6.10. Effect of the pulse on single-ended outputs ($\tau = 2ns$) (a) Positive branch (b) Negative branch.

It can be seen that the phenomenon observed for a pulse width of $\tau = 400ps$ can also be observed for the case of 2 ns. This is that if both branches are added we would obtain the original pulse. Figure 6.11 shows the single-ended outputs after the filtering stage, while Figure 6.12 shows the difference between the case of a pulse and the case of no pulse, for each branch.

As it can be seen, the obtained pulse resembles the original pulse introduced at the input of the circuit. It must be noted that the ideal pulse shape is not seen since part of the information is discarded during the filtering process.

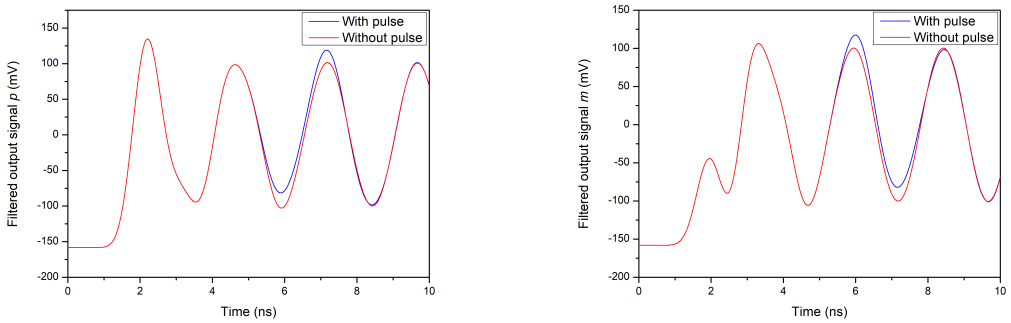


Figure 6.11. Filtered single-ended outputs of the mixer when there is a pulse at the input ($\tau = 2ns$) (a) Positive branch (b) Negative branch.

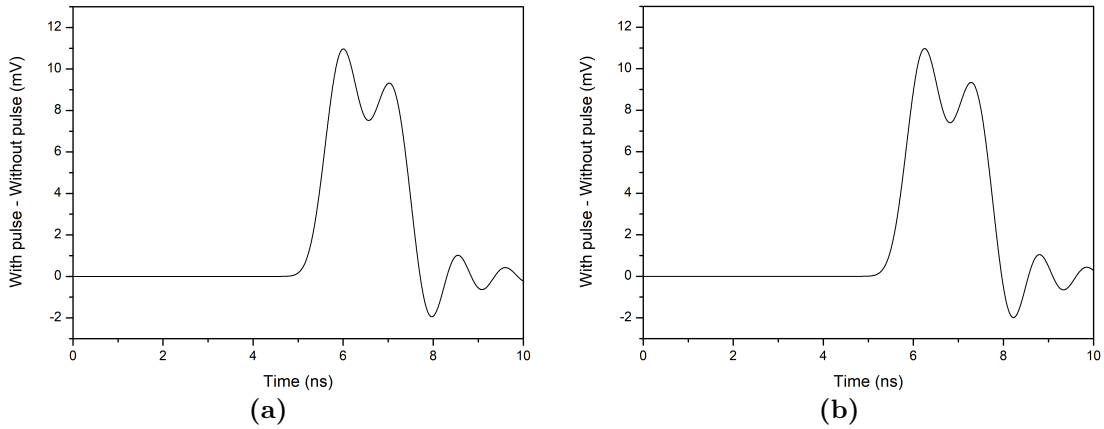


Figure 6.12. Effect of the pulse on filtered single-ended outputs ($\tau = 2ns$) (a) Positive branch (b) Negative branch.

6.1.2 Double-balanced mixers

Once the performance of a single-balanced mixer has been studied when a current pulse is introduced at the input of the circuit, a similar study has been performed in this section for a double-balanced mixer. Figure 6.13 shows the schematic of the tested double-balanced mixer.

In a similar way as for the single-balanced mixer, the input signal is a 2.4 GHz sinusoidal signal. However, in this case there is a differential input, where each single-ended input is converted into current with an ideal VCCS. The differential pairs that commutate the signal are also implemented using ideal switches (SwitchV model). The LO signal used to translate from the RF to the IF is the same as the one used for the single-balanced mixer (see Figure 6.3).

It is known that for double-balanced mixers the conversion gain follows the same expression as for the single-balanced mixer:

$$G_c = \frac{2}{\pi} \cdot g_m \cdot R_L \tag{6.4}$$

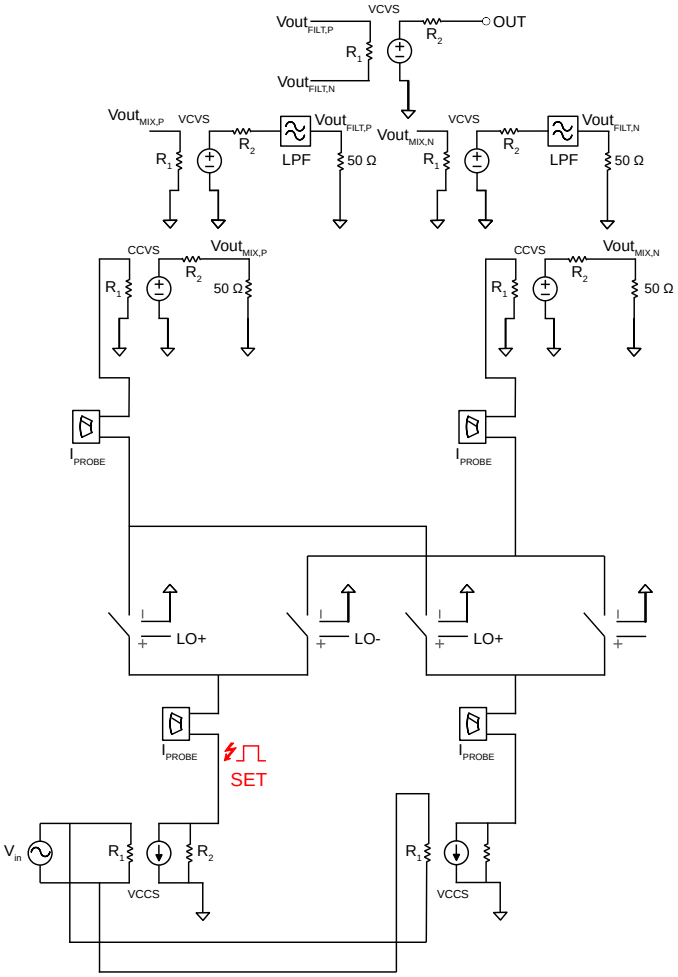
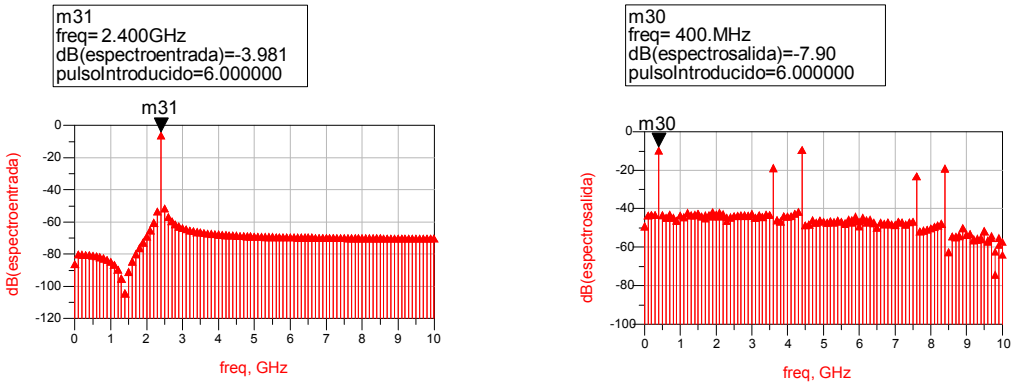


Figure 6.13. Schematic of the double-balanced mixer.

As in the previous case, both g_m and R_L are equal to 1, so the gain is equal to $2/\pi$ (which is approximately -4 dB). Figure 6.14 confirms this statement, as it can be seen that the input signal has -3.981 dB at 2.4 GHz, while the output signal has -7.92 dB at 400 MHz (f_{RF}-f_{LO}), which results in the expected gain of approximately -4 dB. It should be noted that in the case of the double-balanced mixer there is no LO feedthrough to the IF [61]. It can be seen that at $f_{LO} = 2$ GHz there is no peak at the output, such as the one that appears for the single-balanced mixer (see Figure 6.4).

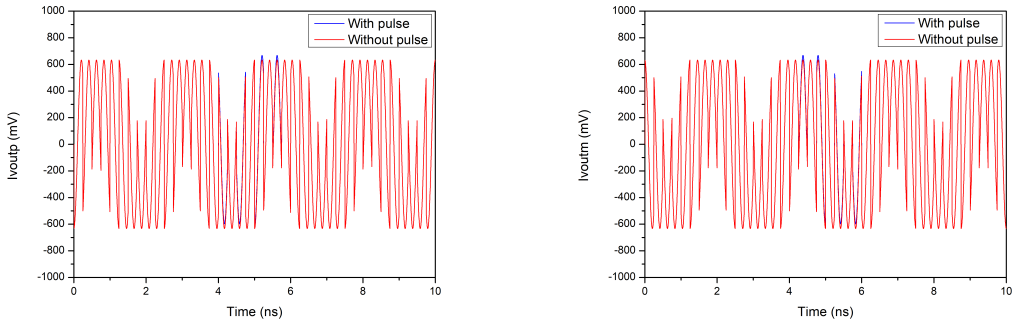


(a) **(b)**

Figure 6.14. Double-balanced mixer (a) Input signal (b) Output signal.

Following the same procedure as in the case of the single-balanced, the SET study was performed by connecting an ideal current source at the input of the circuit, as shown in Figure 6.13. In this case, the pulse width is $\tau = 2ns$.

Figure 6.15 shows both single-ended outputs before their filtering stage, while Figure 6.16 shows the difference for each branch between the case of a strike occurring or not.



(a) **(b)**

Figure 6.15. Single-ended outputs of the double-balanced mixer when there is a pulse at the input $\tau = 2ns$ (a) Positive branch (b) Negative branch.

It can be observed that the same effect seen in the single-balanced mixer also appears for the double-balanced mixer. If both branches are added, the original pulse would be obtained.

The results obtained for the study of the propagation of the pulse through the filtering stage are shown in Figure 6.17 and Figure 6.18.

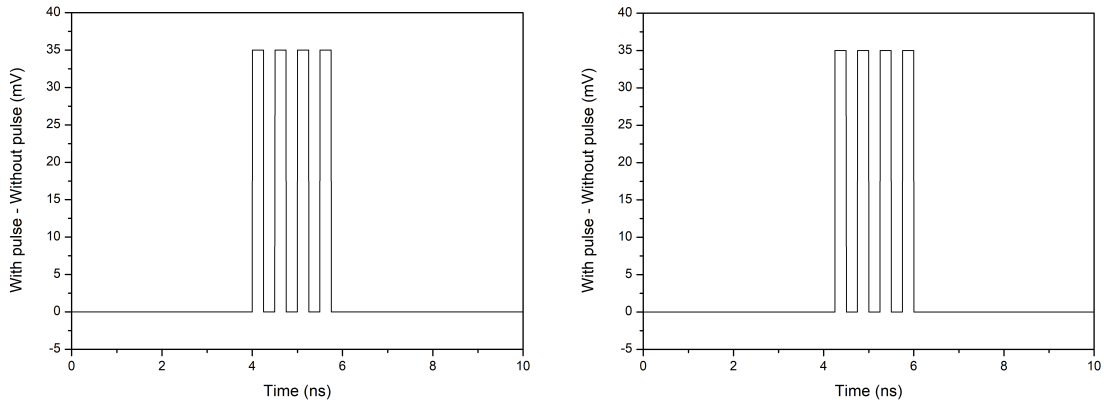


Figure 6.16. Effect of the pulse on single-ended outputs of the double-balanced mixer ($\tau = 2ns$) (a) Positive branch (b) Negative branch.

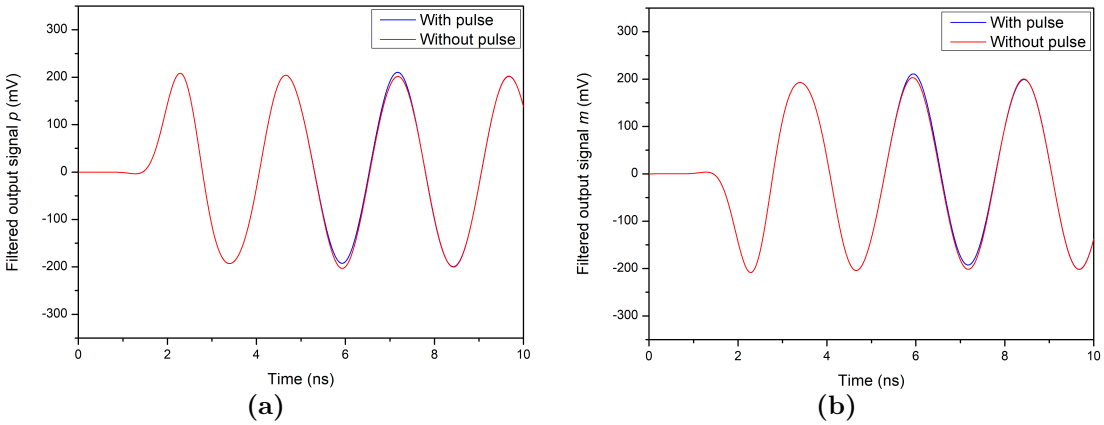


Figure 6.17. Filtered single-ended outputs of the double-balanced mixer when there is a pulse at the input ($\tau = 2ns$) (a) Positive branch (b) Negative branch.

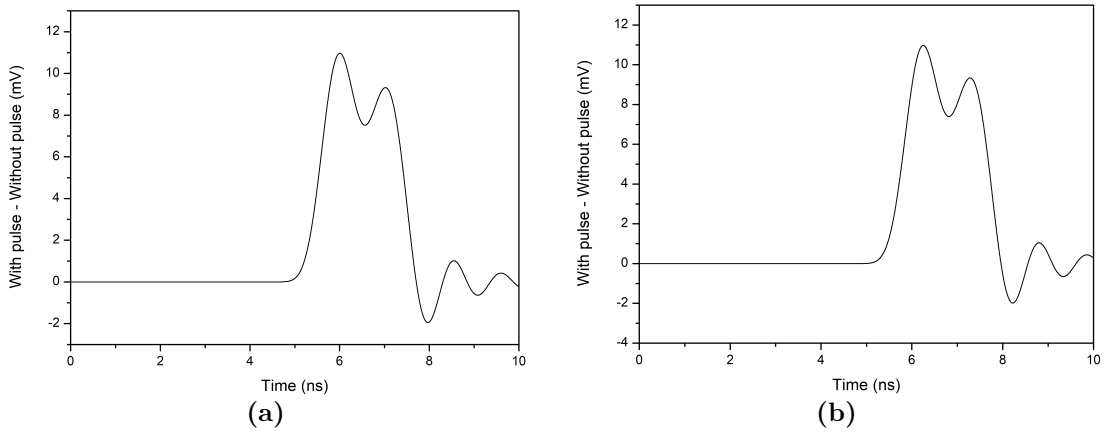


Figure 6.18. Effect of the pulse on filtered single-ended outputs of the mixer when there is a pulse at the input ($\tau = 2ns$) (a) Positive branch (b) Negative branch.

From these results it can be stated that the double-balanced mixer has the same SET performance as the single-balanced mixer, since the obtained pulse resembles the original pulse introduced at the input of the circuit.

However, if the differential output is considered, it can be seen that the pulse is considerably reduced. This result is in line with the statement made in [12], which is that the differential signal suppresses the transient current at the output considerably. This implies that using fully differential architectures is an adequate solution in order to suppress the transient pulses generated in the transconductor stage of the mixer. Figure 6.19 shows the effect of the pulse on the differential output signal.

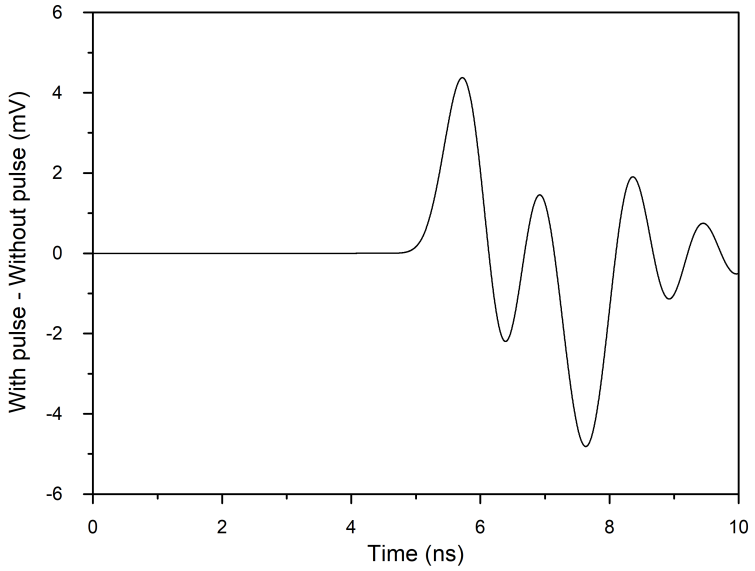
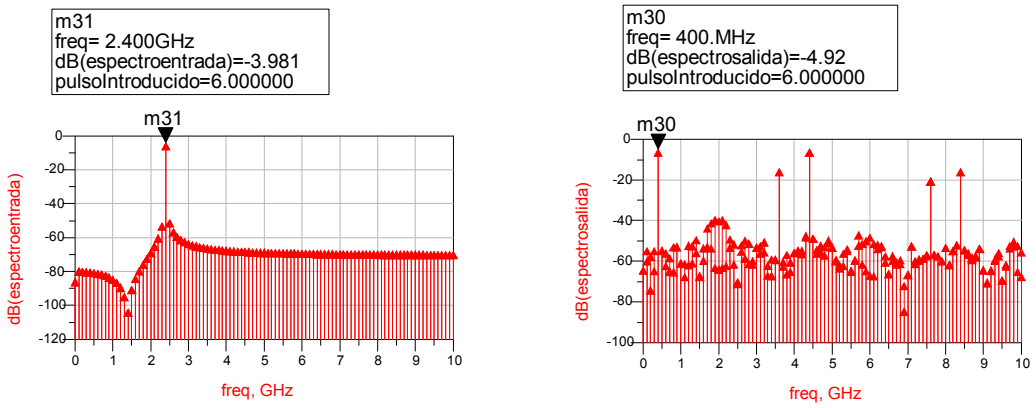


Figure 6.19. Effect of the pulse on the filtered differential output of the double-balanced mixer.

6.1.2.1. Effect of duty cycle

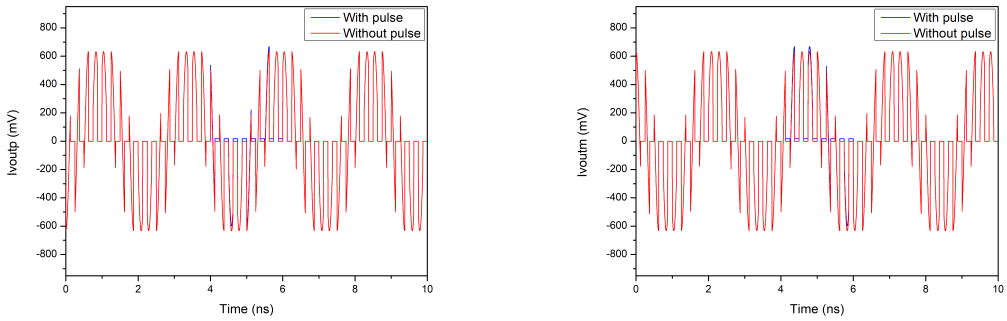
In the studies performed in both the single-balanced and the double-balanced mixers, the duty-cycle of the LO signal was set to the conventional value of 50%. However, it is known that employing a 25% duty-cycle enhances the gain of a mixer by approximately 3 dB [61]. Figure 6.20 proves this statement, since it can be seen that the gain is now approximately -1 dB, instead of -4 dB.

The SET performance of the double-balanced mixer has also been analysed when the duty-cycle of the LO signal is set to 25%. Figure 6.21 depicts both single-ended outputs of the mixer before the filtering stage, while Figure 6.22 shows the effect of the pulse on these outputs.



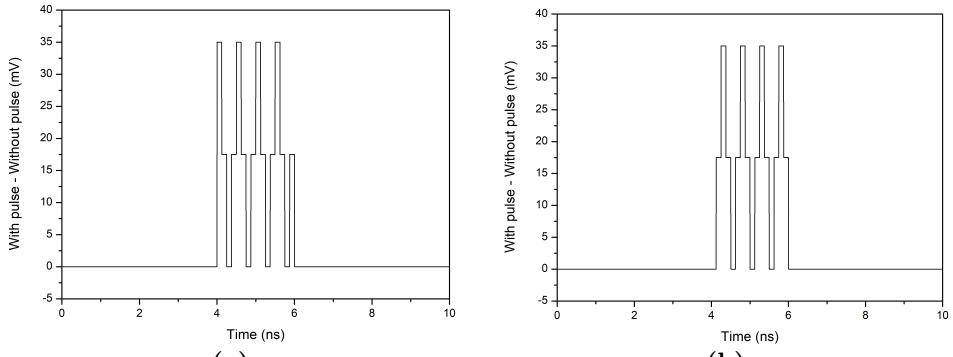
(a) **(b)**

Figure 6.20. Double-balanced mixer with 25% duty cycle (a) Input signal (b) Output signal.



(a) **(b)**

Figure 6.21. Single-ended outputs of the double-balanced mixer with 25% when there is a pulse at the input (a) Positive branch (b) Negative branch.



(a) **(b)**

Figure 6.22. Effect of the pulse on single-ended outputs of the double-balanced mixer with a 25% duty-cycle (a) Positive branch (b) Negative branch.

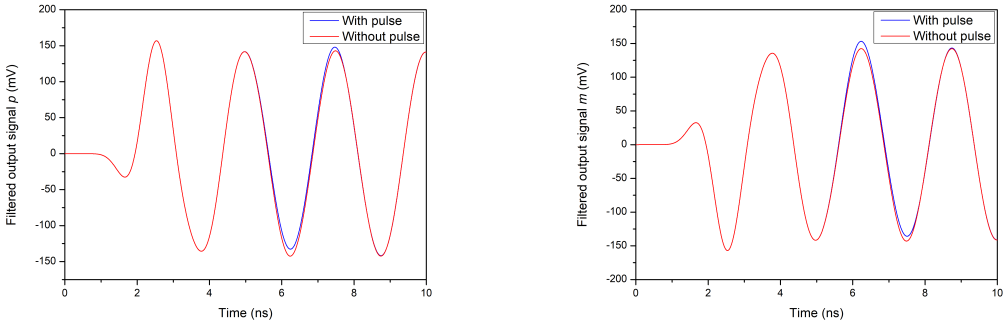
The results obtained still show the phenomenon observed in the previous cases, which is that if the effect on each branch is added, the original pulse is obtained. However, it can be seen that there is a slightly different behaviour compared to the previous cases. This can be explained by studying the quadrature LO waveforms shown in Figure 6.23.

(a) **(b)**

Figure 6.23. Quadrature LO waveforms with (a) 25% duty-cycle (b) 50% duty-cycle.

It can be observed that for a 25% duty-cycle there are instants when none of the switches are in the ON-state. In this case, all of the current goes through the OFF resistance (which is the same for all switches), leading to a divider that reduces the output voltage by half. Hence, the output signals shown in Figure 6.22.

Regarding the propagation of the pulse through the filtering stage, Figure 6.24 and Figure 6.25 show the obtained results. It can be seen that the double-balanced mixer with 25% duty-cycle behaves similarly as for the case of 50% duty-cycle when the SET performance is analysed.



(a) **(b)**

Figure 6.24. Filtered single-ended outputs of the double-balanced mixer when there is a pulse at the input ($\tau = 2ns$) (a) Positive branch (b) Negative branch.

If the differential output is considered, the same effect as for the case of 50% duty-cycle is observed, as shown in Figure 6.26.

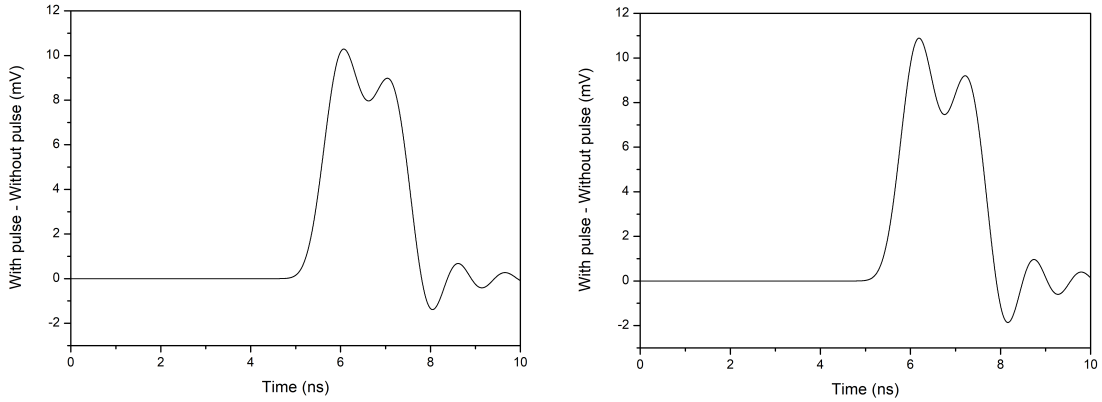


Figure 6.25. Effect of the pulse on filtered single-ended outputs of the mixer with 25% duty-cycle when there is a pulse at the input (a) Positive branch (b) Negative branch.

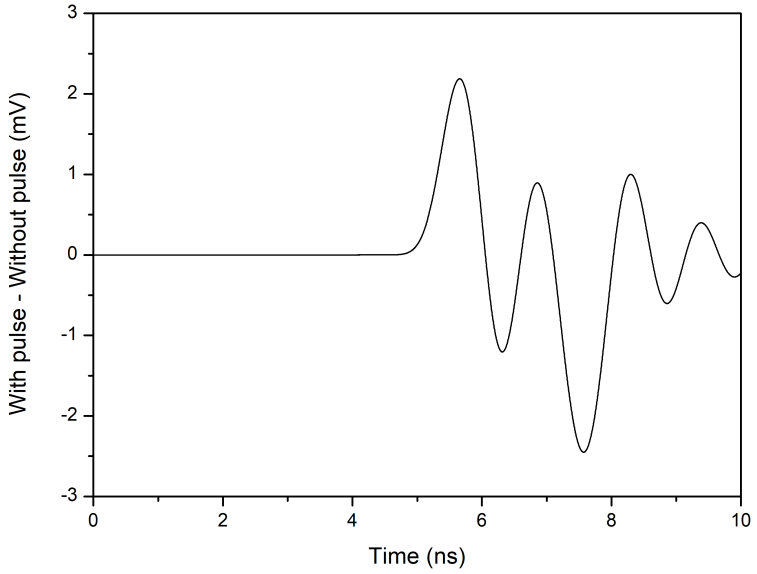


Figure 6.26. Effect of the pulse on the filtered differential output of the double-balanced mixer with 25% duty-cycle.

As a conclusion, once the SET performances of the single-balanced mixer and the double-balanced mixer with 50% duty-cycle and 25% duty-cycle have been studied, it can be stated that in all cases a pulse introduced in the input of the circuit will propagate to the output under certain conditions (see Equation 6.2). In order for the shape of the pulse to appear at the output, the LO frequency must be greater than $2/\tau$, being τ the pulse width. If this condition is not met, a disturbance will appear at the output, but not with the same shape as the introduced pulse. It must be noted that this remains true when considering the single-ended outputs of the mixer. If the differential output is analysed, it can be seen that the pulse is reduced considerably, which encourages the use of differential topologies in order to minimise the effect of SETs.

6.2 Single Event Transients in Filters

As seen previously in this document, RF receivers implement a filtering stage after the mixer in order to select the desired portion of the frequency spectrum. In the previous section, it has been observed that this filtering stage has an effect in the SET performance of the receiver. In this section, a more thorough study of this effect is carried out. Firstly, the study follows a theoretical approach. Once the behaviour of SETs in filters is understood, the theoretical concepts are reinforced by performing simulations with ideal filters.

6.2.1 Theoretical approach

In order to perform the theoretical study of the effect of SETs on filters, an ideal pulse with amplitude A and width τ is considered, as seen in Figure 6.27.

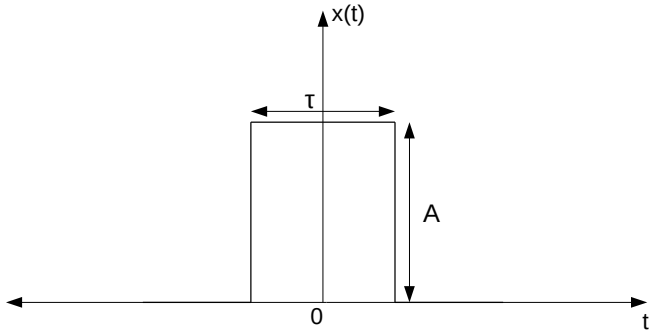


Figure 6.27. Ideal square pulse.

This ideal square pulse can be defined as [70]:

$$x\left(t\right)=\begin{cases}1,|t|<\frac{\tau}{2}\\0,|t|>\frac{\tau}{2}\end{cases}. \tag{6.5}$$

Applying the Fourier Transform

$$X(j\omega)=\int_{-\infty}^{\infty}x(t)e^{-j\omega t}dt, \tag{6.6}$$

the following frequency response is obtained:

$$X(j\omega)=\int_{-\frac{\tau}{2}}^{\frac{\tau}{2}}e^{-j\omega t}dt=2\frac{\sin\frac{\omega\tau}{2}}{\omega}. \tag{6.7}$$

This response can be expressed in terms of the *sinc* function:

$$X(j\omega) = \frac{2\tau}{2} sinc\left(\frac{\frac{\omega\tau}{2}}{\pi}\right). \tag{6.8}$$

Figure 6.28 shows a sketch of the frequency response of the ideal pulse ($X(j\omega)$). As it can be seen, this function has a crossing by 0 at $1/\tau$ and is centred at 0 Hz.

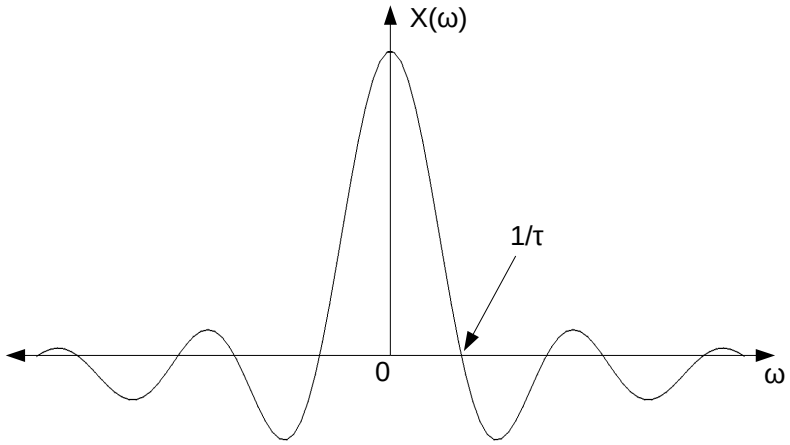


Figure 6.28. Frequency response of an ideal square pulse.

If only positive frequencies are considered, it can be stated that most of the information of the pulse can be found between 0 and $1/\tau$. This corresponds with the main lobe of the *sinc* function. Taking this into account, the filter must be able to capture the main lobe in order for the pulse to propagate to the output of the filter. This is represented in Figure 6.29, where an ideal low pass filter (LPF) with a cut-off frequency at $1/\tau$ is depicted.

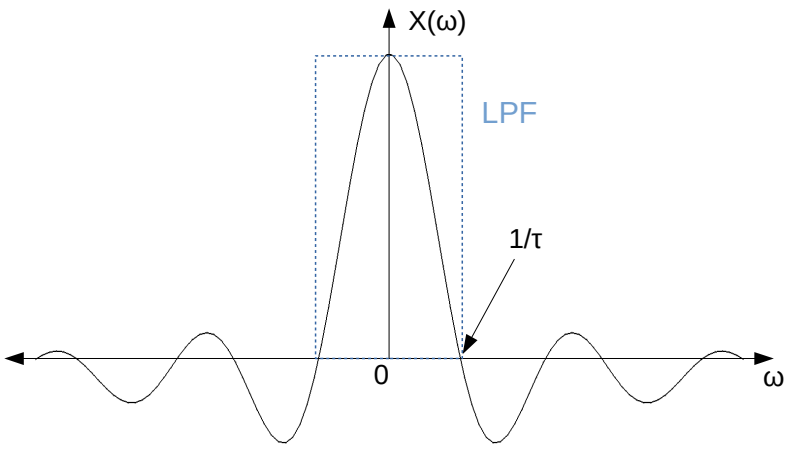


Figure 6.29. Frequency response of a square pulse and an ideal low pass filter.

In this particular case, a pulse with almost the same shape as the original pulse can be obtained at the output of the filter. In order to obtain the exact same shape, the cut-off frequency of the filter should be greater to capture more lobes of the *sinc* function. In any case, in this study it is considered that the pulse propagates to the output when the main lobe is captured and, therefore, the shape of the output pulse resembles the square pulse.

However, if a band pass filter (BPF) is used instead of a LPF, the information captured by the filter is different. The amount of spectral information captured by the BPF will depend on its centre frequency and its bandwidth. In this document, narrow-band receivers have been considered. Specifically, receivers for low power consumption wireless sensor networks have been studied (i.e. receivers for Bluetooth, ZigBee, etc.). In these standards, the bandwidth has a value of a few MHz. Therefore, for a square pulse with a width of a few nanoseconds, the BPF will only capture part of the main lobe, which results in a loss of spectral information and a minimised pulse at the output. This can be seen in Figure 6.30.

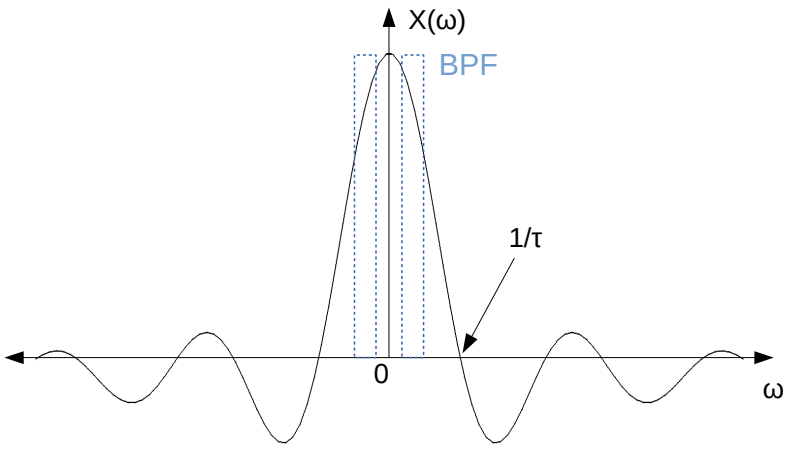


Figure 6.30. Frequency response of a square pulse and an ideal band pass filter.

6.2.2 Ideal Filters Simulations

In order to validate the concepts presented in the previous section, a setup with ideal Butterworth filters has been implemented. This setup is the same as the one used in the simulation of ideal mixers. Figure 6.31 shows the setup with ideal low pass filters.

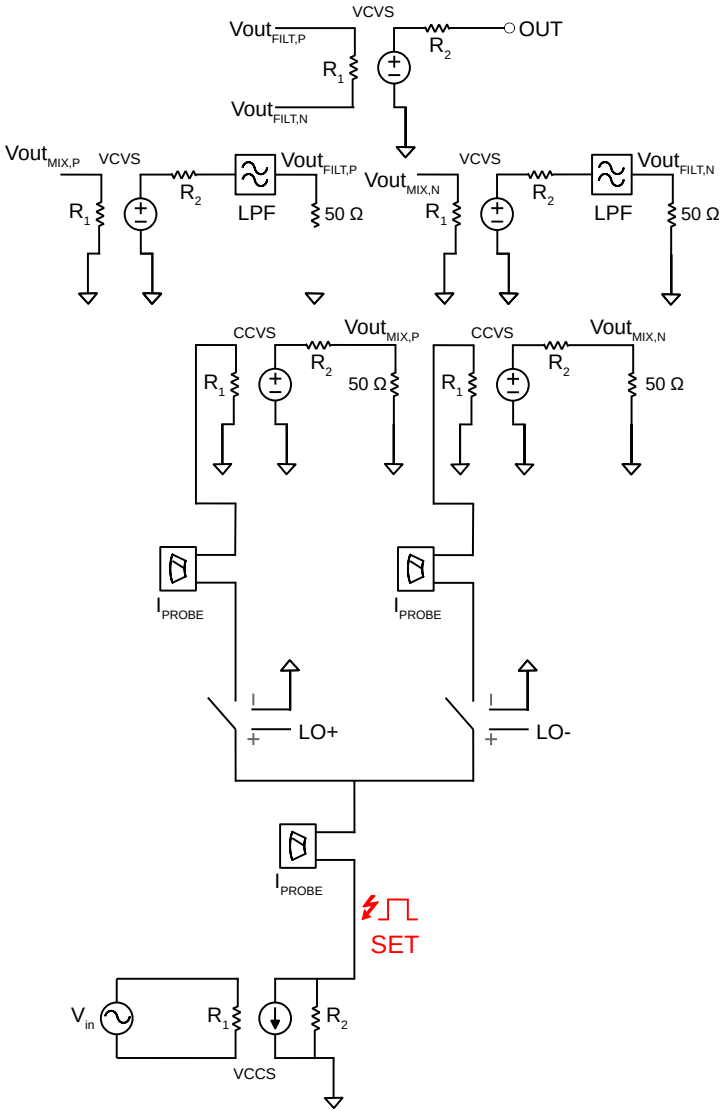


Figure 6.31. Setup of the ideal mixer with ideal low pass filters and a current pulse for SET analysis.

The passband edge frequency is set to 1 GHz (where there is a 3 dB attenuation) and the stopband edge frequency is set to 1.2 GHz (20 dB attenuation). Considering that the pulse introduced has a width of 2 ns, its frequency response will have its first zero-crossing at a frequency of 0.5 GHz ($\frac{1}{\tau} = \frac{1}{2ns}$). Therefore, the implemented filter will capture the main lobe of the pulse in the frequency domain. This results in the propagation of the pulse to the output of the filter, as seen in Figure 6.32.

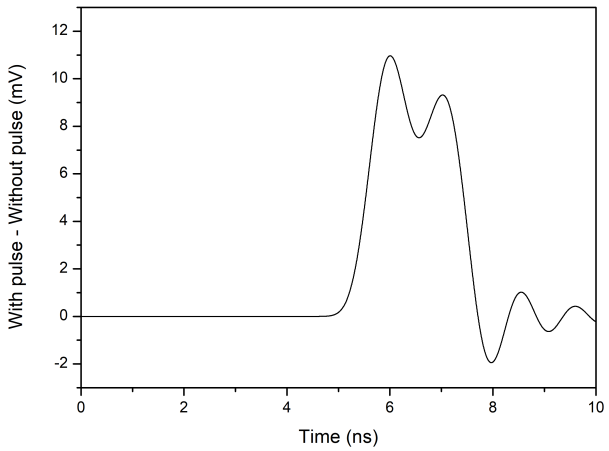


Figure 6.32. Signal observed at the output of one of the ideal low pass filters.

If the low pass filter is set to a passband edge frequency of 0.25 GHz and a stopband edge frequency of 0.5 GHz, this will result in a loss of information of part of the main lobe. Hence, the signal at the output of the filter will not have the shape of a square pulse, as seen in Figure 6.33. Additionally, the maximum voltage peak observed in this case has decreased due to the voltage loss during the filtering process.

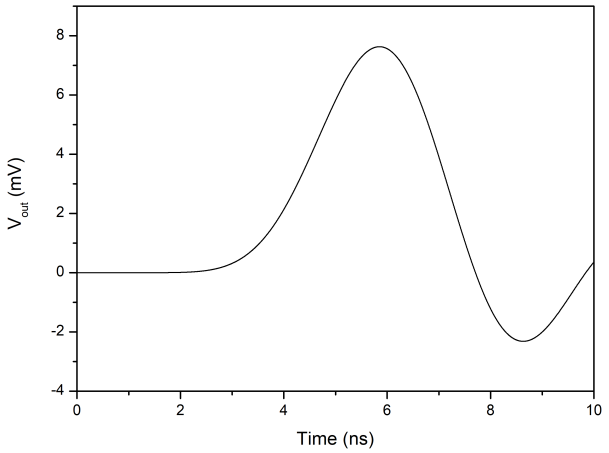


Figure 6.33. Signal observed at the output of one of the ideal low pass filters (passband edge frequency = 0.25 GHz).

If a band-pass filter is implemented, the information loss increases, as mentioned previously. In this case, a BPF with a centre frequency of 0.5 GHz, a passband edge-to-edge width of 0.5 GHz and a stopband edge-to-edge width of 1 GHz is implemented (see Figure 6.34).

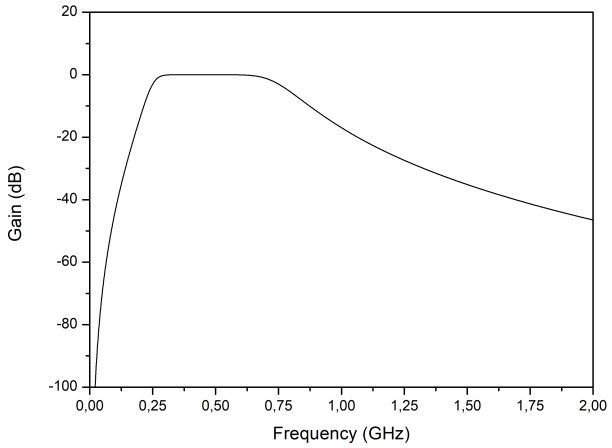


Figure 6.34. Ideal BPF centred at 0.5 GHz.

In this case, even more spectral information is lost, taking into account that a 2 ns-wide square pulse is implemented, so the main lobe ends at 0.5 GHz. This can be seen in Figure 6.35.

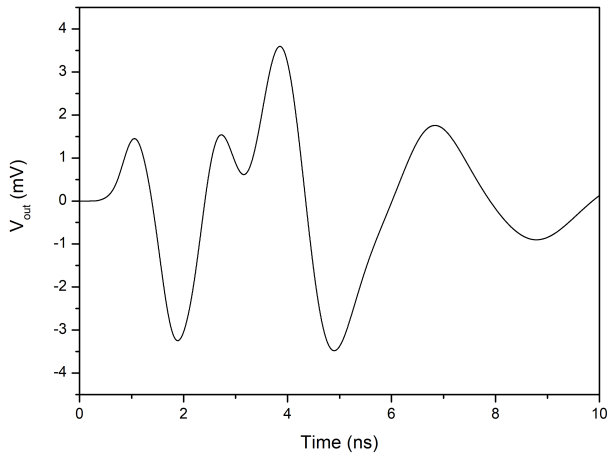


Figure 6.35. Signal observed at the output of one of the ideal band pass filters (centre frequency = 0.5 GHz).

As it was previously mentioned, in the case of low-IF receivers designed for low power consumption standards, the bandwidth of a channel is usually in the order of a few MHz. Therefore, this spectral information loss will be further increased in the case of pulses with a width of approximately a few nanoseconds, which is the typical width of SETs.

6.3 Single Event Transients in Receivers

Once individual circuits such as LNAs, mixers and filters have been analysed under the effects of radiation, a thorough study of the effect of SETs in the receiver architectures presented in *Chapter 5* is performed in this section. Firstly, a low-IF conventional architecture is studied. The main focus of this study is to understand

how a current pulse propagates through the different circuits that form the receiver. Secondly, the two current-reuse architectures are analysed in order to comprehend the difference in SET performance when compared to a conventional architecture.

6.3.1 Low-IF conventional architecture

In this section, the conventional low-IF architecture discussed in *Chapter 4* is studied. Figure 6.36 shows the block diagram of the receiver architecture. As mentioned previously, the first element of the receiver is a low noise amplifier, which is followed by a down-conversion mixer. The output current of the mixer is converted to voltage by the TIA and is finally filtered by a complex filter.

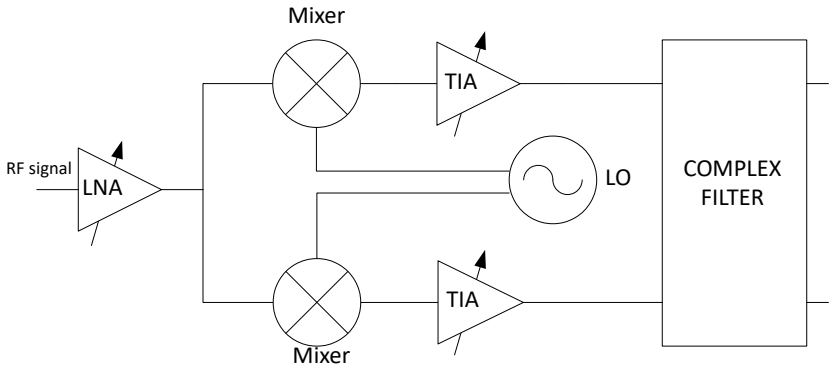


Figure 6.36. Architecture of the proposed low-IF conventional receiver.

In this study, an analysis of how current pulses generated in the LNA propagate through the receiver is carried out. To do so, the double exponential pulses generated with the *Sentaurus* tool, which have been presented in *Chapter 3*, are employed. Specifically, the pulse with the highest maximum current peak is introduced at the drain of the output transistor of the LNA, where the largest voltage peaks at the output were obtained (see Figure 6.37). Similarly, as in the case of the studies of the LNA and the mixer, the voltage signal is analysed. In the case of the receiver, the behaviour of the signal as it travels down the receiver chain is studied.

Figure 6.38 shows the observed signal at the output of the LNA. The depicted waveform shows a damped exponential due to the pulse response of the tank circuit of the LNA. This circuit is a parallel RLC circuit, whose response depends on the parameters α and ω_0 (see Equation 6.9 and Equation 6.10).

$$\alpha = \frac{1}{2RC} \tag{6.9}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{6.10}$$

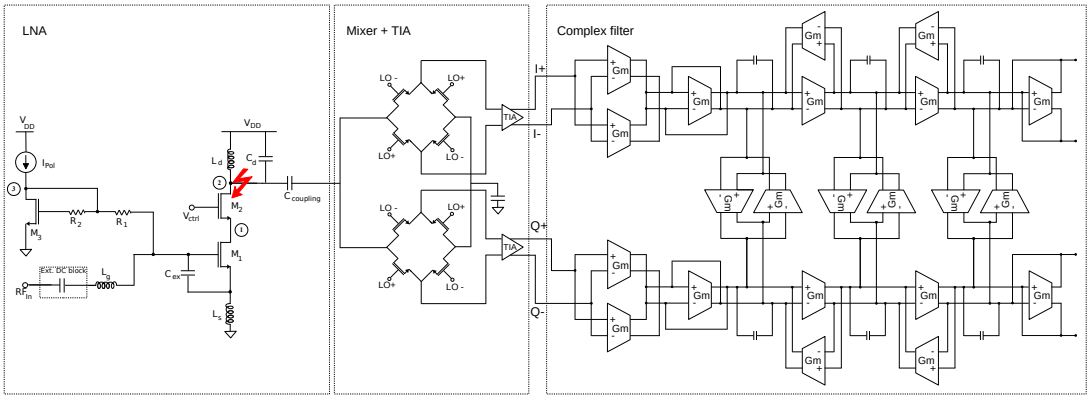


Figure 6.37. Schematic of the proposed conventional low-IF receiver with a strike at the drain of the output transistor of the LNA.

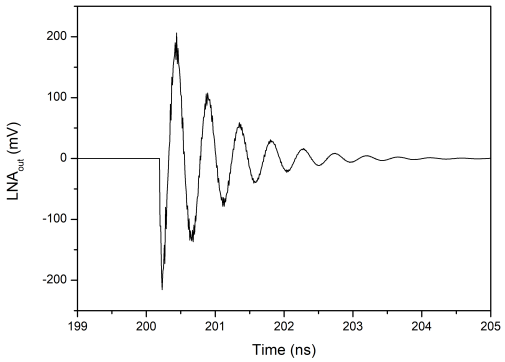


Figure 6.38. Effect of the pulse on the output of the LNA.

Depending on the values of α and ω_0, the response of a parallel RLC circuit can be classified into overdumped, critically dumped, underdamped and lossless. In this case, the values of L and C are 2.58 nH and 1.4 pF, respectively, while the quality factor (Q) of the tank is approximately 10.5, which results in a resistance of 464 Ω. Taking this into account, and substituting in Equation 6.9 and Equation 6.10, it can be seen that in this case an underdamped response is obtained. This explains the waveform seen in Figure 6.38.

In order to study the effect of the pulse in the mixer, the signal at the output of the TIA is observed, once the current signal is converted to voltage. Therefore, in this study the outputs of the TIAs are considered to be the outputs of the mixer. Figure 6.39 shows the difference between the case of a strike occurring and the case when there is no strike, for each of the four outputs.

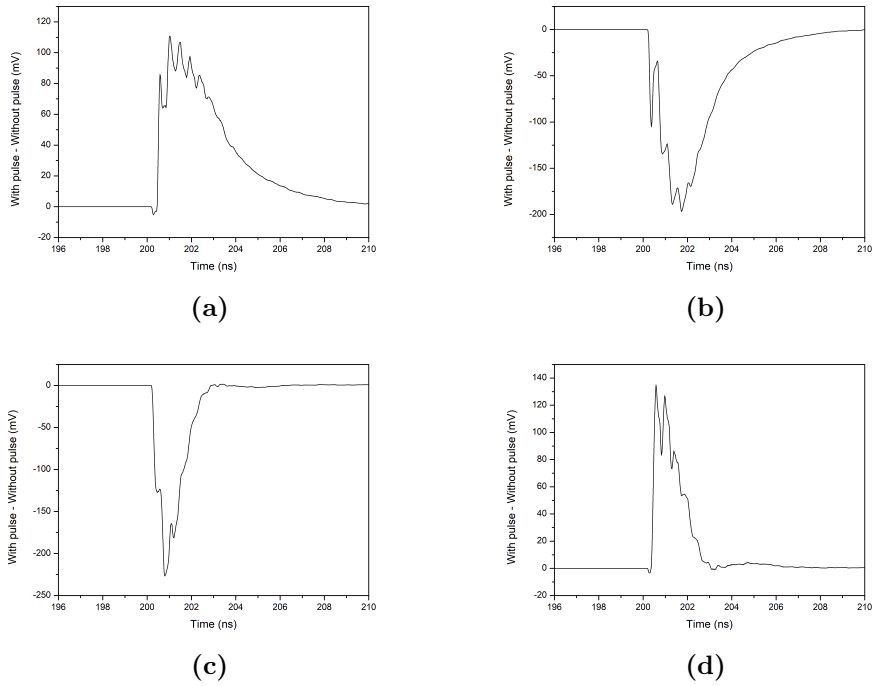


Figure 6.39. Effect of the pulse on the outputs of the mixer (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

As it can be seen, the shape of the pulse that appears at the outputs of the mixer resembles the shape of the input pulse. However, the obtained pulse does not have the exact same shape as its original counterpart. This can be explained by the fact that the input pulses are very narrow ($\tau \approx 0.1ns$). Hence, the condition presented in the previous section (Equation 6.2) is not met since the f_{LO}= 2.3975 GHz. Even though the pulse seen at the outputs of the mixer does not have the same shape as the input pulse, the obtained pulse has a width and amplitude that could be harmful for other circuits of the receiver chain.

The next element in the receiver chain is the complex filter. As it was explained in *Chapter 5*, the designed filter is a Butterworth third order gm-C complex filter. It was stated in the previous section that a filter effectively reduces the effect of pulses such as those implemented in this study. This is explained by the loss of spectral information during the filtering process since part of the signal is suppressed. In the case of a complex filter, this loss of information is further increased since the negative frequencies are filtered, thus suppressing the image frequency, as it can be seen in Figure 6.40.

Additionally, as it was mentioned previously, the bandwidth of a channel for low power consumption standards is usually in the order of a few MHz. Specifically, for the IEEE 802.15.4 standard the channel bandwidth is 3 MHz, as it can be seen in Figure 6.41. Taking into account that the frequency response of a double exponential pulse follows the shape sketched in Figure 6.42 [70], it can be stated that the complex filter is filtering most of the information of the double exponential pulse.

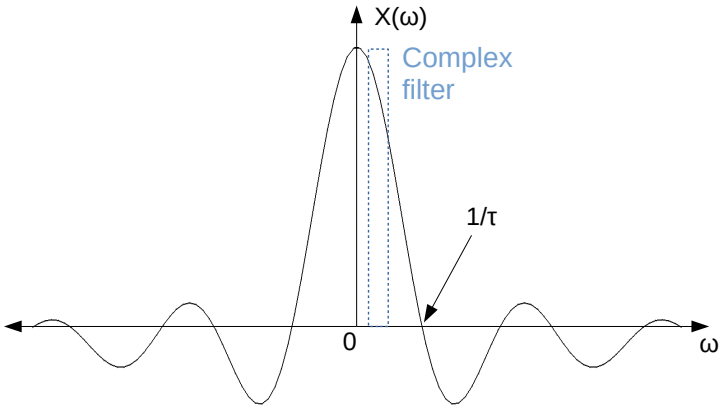


Figure 6.40. Frequency response of a square pulse with an ideal complex filter.

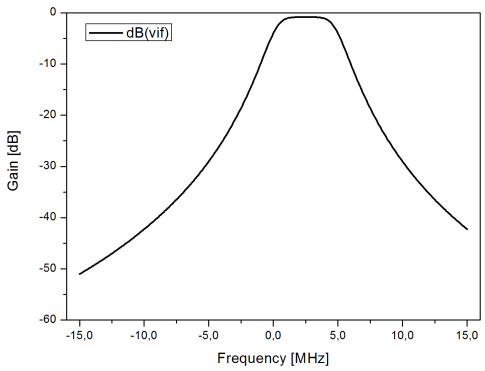


Figure 6.41. Frequency response of the designed complex filter.

This can be proven by observing the signal at the outputs of the complex filter. Figure 6.43 shows the difference between the case of a strike occurring and the case when there is no strike, for each of the four outputs.

It can be seen that the pulse has been considerably minimised. The maximum voltage peak has been reduced from the order of hundreds of mV to approximately

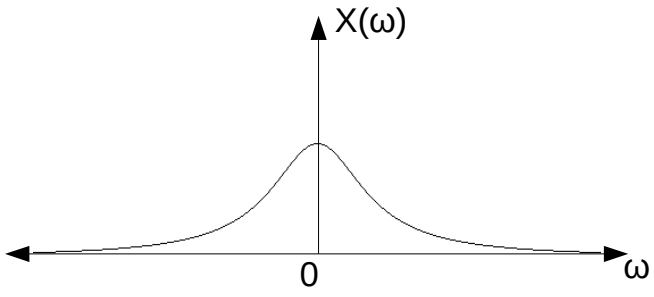


Figure 6.42. Double exponential pulse in the frequency domain.

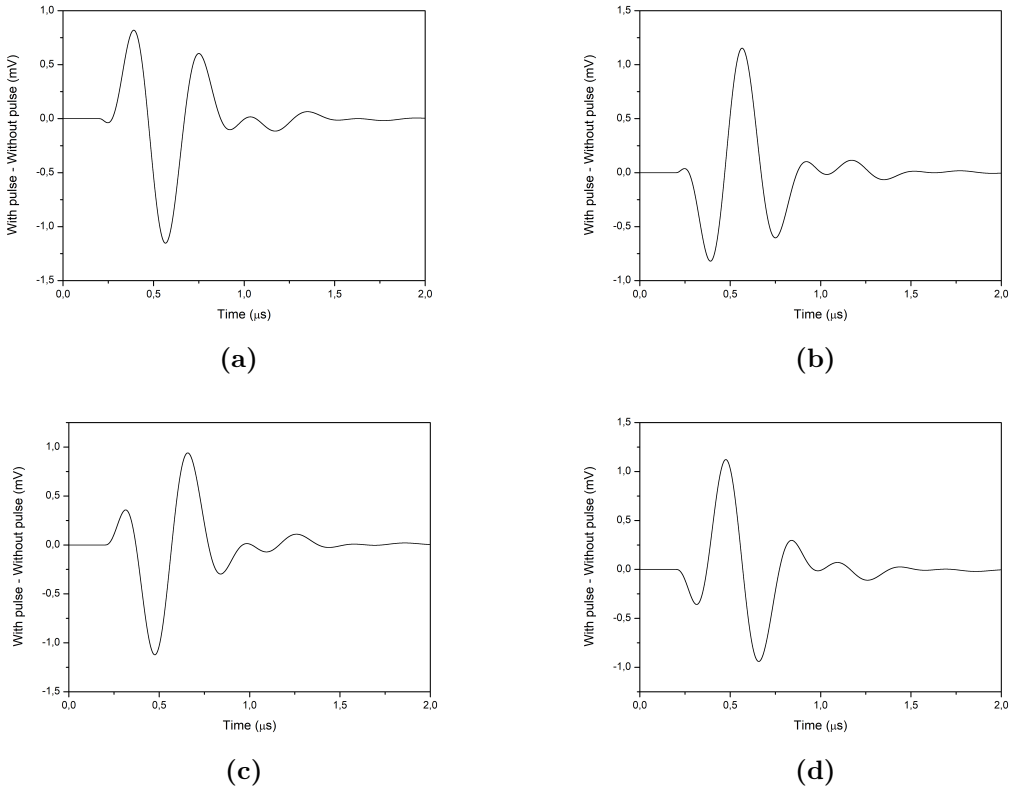


Figure 6.43. Effect of the pulse on the outputs of the complex filter (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

1 mV. Additionally, the shape of the double exponential pulse is no longer seen, due to the loss of information mentioned previously.

However, this minimised pulse can still cause harmful effects on the receiver, as it can be seen in Figure 6.44, which shows the voltage signal on the four outputs of the complex filter when there is a strike (blue) and when there is no strike (red).

It can be seen that there is a slight shift both in amplitude and phase of the output signals of the filter. This shift could result in a bit change in the digital circuits that follow the receiver front-end designed in this work, resulting in a slight increase of the bit error rate (BER) of the system. As mentioned in *Chapter 2*, the severity of the SET is only known once it propagates until the end of the signal processing chain. Therefore, it is difficult to quantify the impact on analog circuits before including them in a whole system.

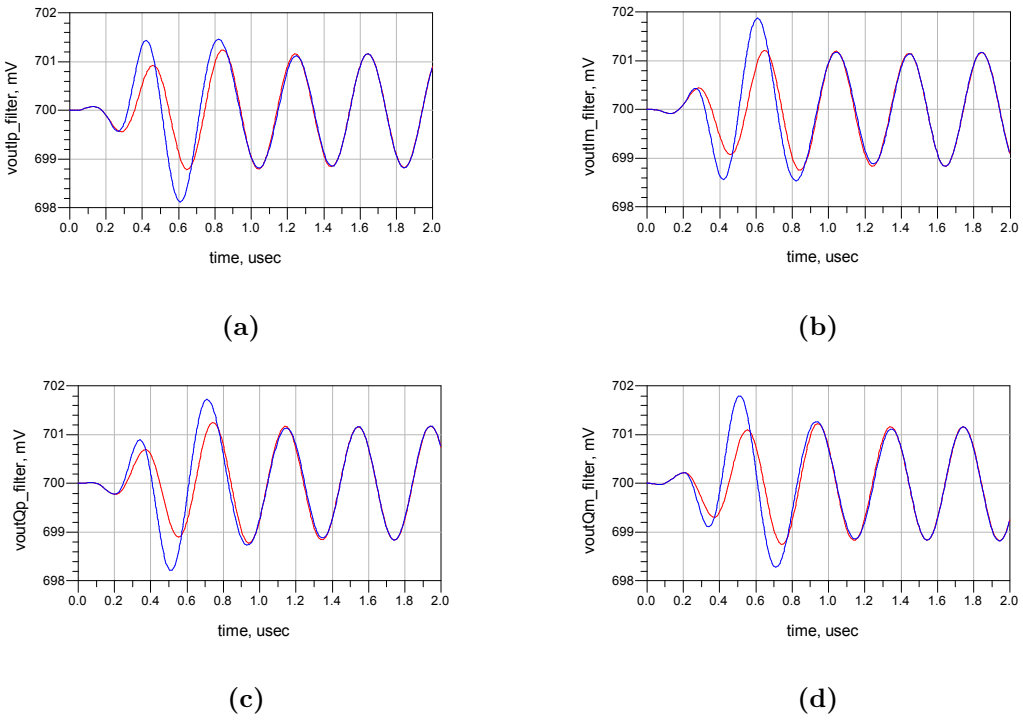


Figure 6.44. Output signals of the complex filter (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

6.3.2 Current-reuse architecture

In this section, the previously presented current-reuse receiver front-end is studied under the effect of current pulses that could cause SETs. As mentioned previously, this receiver follows a differential low-IF architecture. The differential RF input signal is amplified by an LNA and down-converted by an active I/Q mixer. Finally, the signal is filtered by a complex filter to improve the image rejection performance and sensitivity. The implemented complex filter follows the same topology as the one used previously in the conventional low-IF receiver. This is, a Butterworth third order gm-C complex filter. Figure 6.45 shows the system architecture of the current-reuse receiver.

In a similar way as in the case of the conventional low-IF receiver, the propagation of the pulses through the receiver chain is studied. The current pulses are introduced at the drain of one of the transistors that form the differential pair of the LNA and the voltage signal is analysed in different nodes of the receiver chain. In this case, the same double exponential pulses used in the case of the conventional receiver are introduced, in order to establish a fair comparison with the previous case. Figure 6.46 shows the difference between the case of a strike occurring and the case when there is no strike, for each of the four outputs of the mixer.

It can be seen that the pulse introduced at the LNA is propagated to the outputs of the mixer. However, the obtained pulse does not have the exact same shape as its

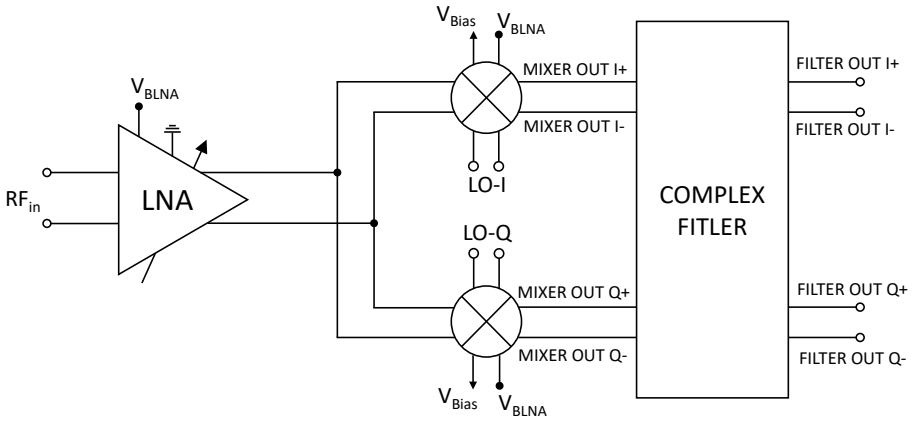


Figure 6.45. System architecture of the current-reuse receiver.

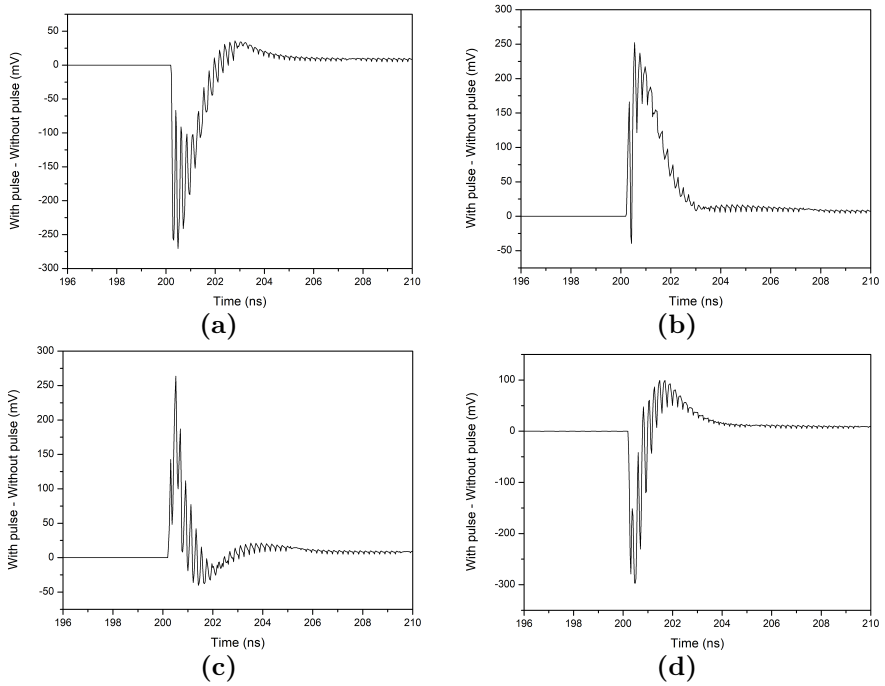


Figure 6.46. Effect of the pulse on the outputs of the mixer in the current-reuse architecture (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

original counterpart. As in the case of the conventional receiver, this is due to the pulse being very narrow ($\tau \approx 0.1ns$), so the expression presented in (Equation 6.2) is not met. Additionally, it can be seen that there is a slight feedthrough of the RF signal to the output of the mixer.

Figure 6.47 shows the difference between the case of a SET occurring and the case when there is no SET, for each of the four outputs of the complex filter. As it can be seen, the pulse has been considerably minimised. The maximum voltage peak has been reduced from the order of hundreds of mV to hundreds of μV. Additionally, the shape of the double exponential pulse is no longer seen due to the loss of information inherent to the filtering process.

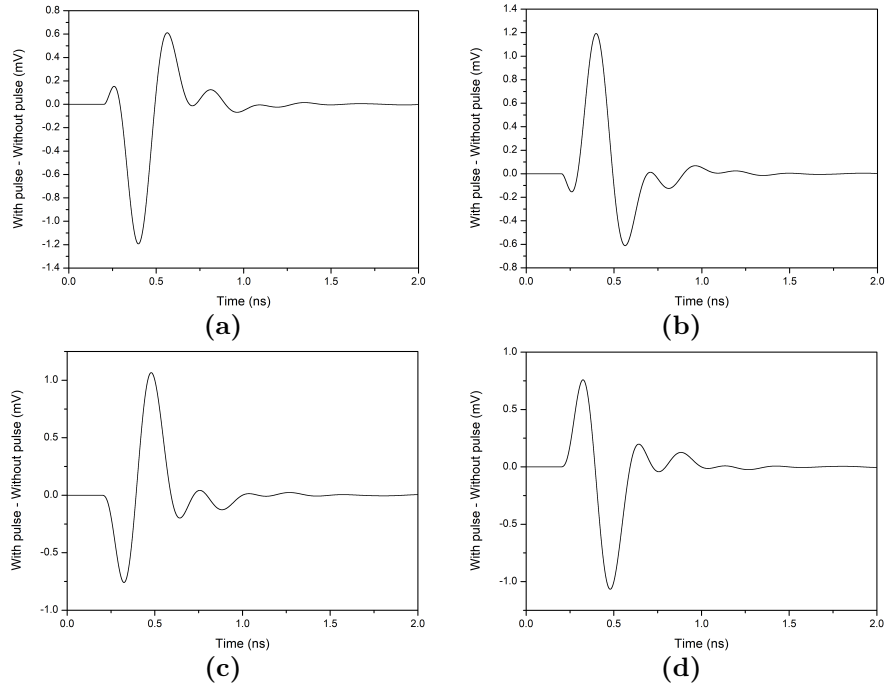


Figure 6.47. Effect of the pulse on the outputs of the filter in the current-reuse architecture (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

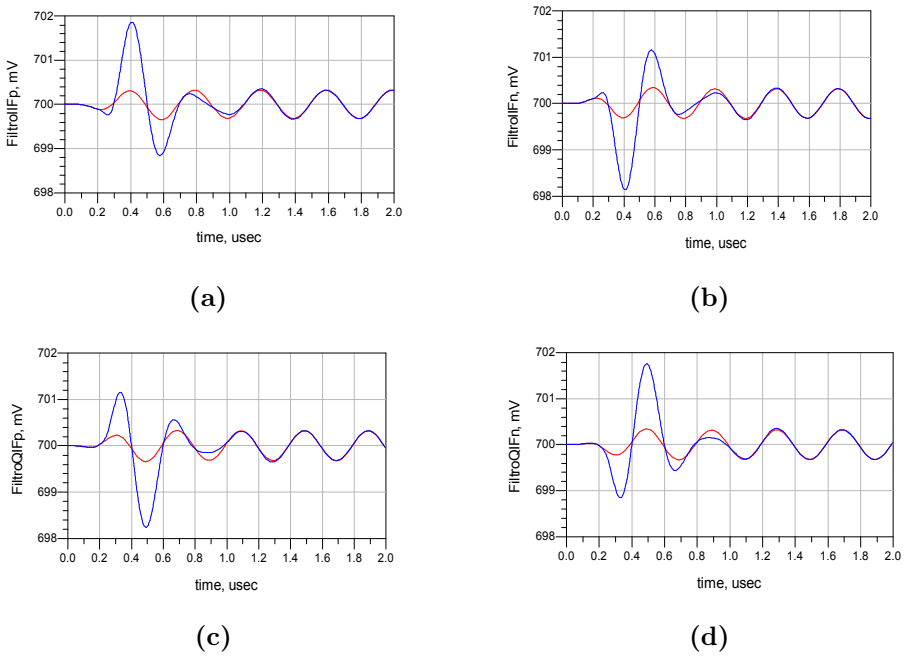


Figure 6.48. Output signals of the complex filter in the current-reuse architecture (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

As in the case of the conventional receiver, this minimised pulse causes a slight shift both in phase and amplitude on the output signals of the filter, as seen in Figure 6.48.

6.3.3 **Blixer architecture**

In this section, the previously presented narrowband receiver front-end based on a current-reuse Blixer topology is studied under the effect of radiation. As mentioned in *Chapter 5*, the front-end is formed by a noise-cancelling balun-LNA and a double-balanced I/Q mixer. The output current signals of the mixer are filtered by a current-mode Biquad which is stacked on top of the mixer. The filtered output currents are converted into voltage signals by the complex load, which performs both image rejection and channel selection [60]. The architecture of the proposed receiver front-end is shown in Figure 6.49, while the schematic of such receiver is shown in Figure 6.50.

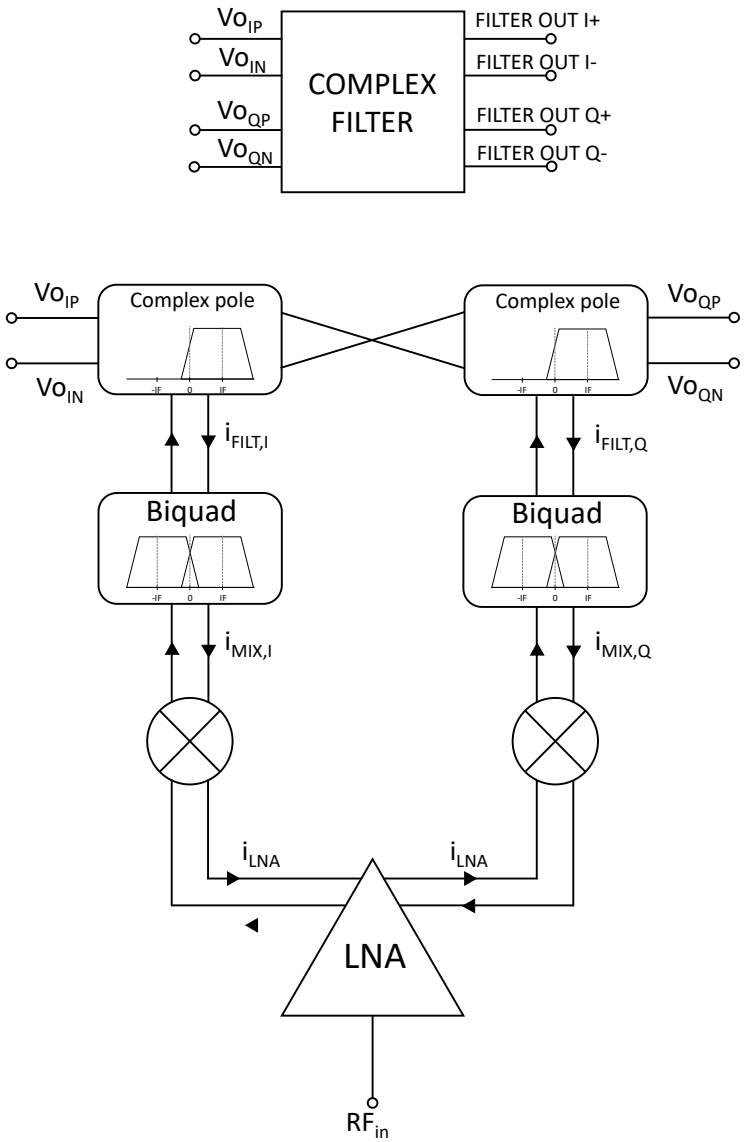


Figure 6.49. Receiver front-end current-reuse Blixer architecture.

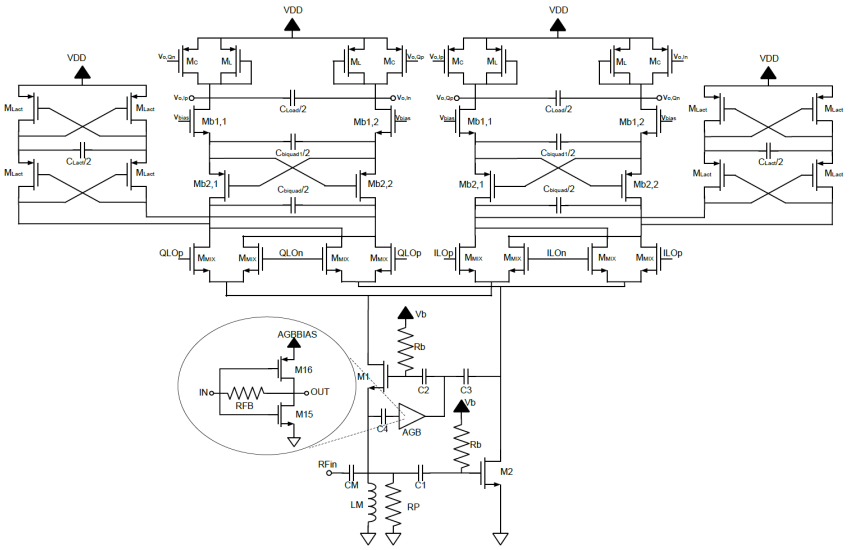


Figure 6.50. Schematic of the receiver-front end current-reuse Blixer topology.

Following the same procedure as in the previous receivers, the propagation of pulses through the receiver chain is studied. In this case, the current pulses are introduced at the drain of transistor M1, which corresponds to the common-gate transistor of the balun-LNA. In order to establish a fair comparison with the previous cases, the same double exponential pulses are applied. Figure 6.51 shows the difference between the case of a SET occurring and the case when there is no SET, for each of the four outputs of the mixer.

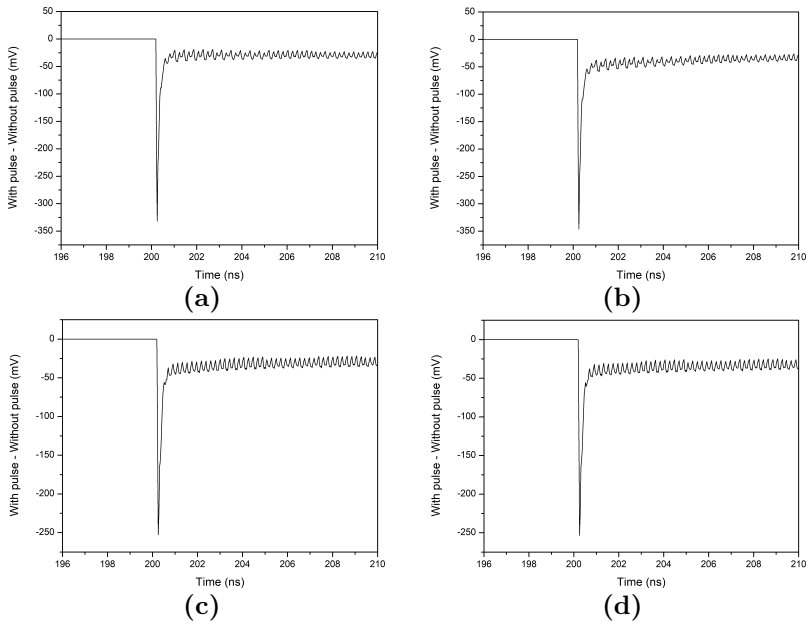


Figure 6.51. Effect of the pulse on the outputs of the mixer in the Blixer architecture (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

It can be seen that the pulse propagates to the output of the mixer, similarly as in the previously studied receivers. However, in this case, the pulse does not return

to zero, but it remains at an offset value of approximately 50 mV. This results in a considerable shift both in amplitude and phase of the signal at the output of the filtering stage, as it can be seen in Figure 6.52.

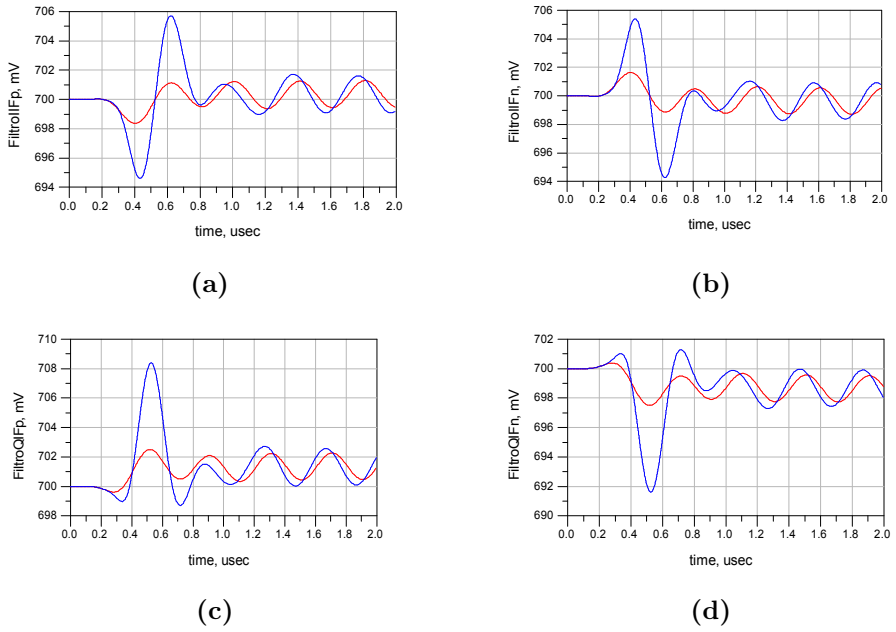


Figure 6.52. Output signals of the complex filter in the Blixer architecture (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

This can be explained by the fact that in this receiver there is a Biquad stacked on top of the receiver, while in the other current-reuse receiver there is an active load. More specifically, the responsible for this offset value is the capacitor $C_{biquad}/2$ (see Figure 6.50). The pulse will produce a voltage difference on the nodes of the capacitor. It is worth mentioning that in this receiver a 25% duty-cycle is employed, as it was previously mentioned. Therefore, only one of the transistors of the switching stage is active at an instant of time. Under these conditions, the pulse will travel through the receiver chain to one of the nodes of the capacitor, generating a voltage difference which produces the mentioned offset value. In order to prove this assumption, the previous simulations have been repeated for the front-end with an active load, like the one implemented in the previously studied current-reuse receiver, instead of the Biquad plus the complex load. Figure 6.53 shows the schematic of this front-end with the active load.

For these conditions, the difference between the case of a strike occurring and the case when there is no strike, for each of the four outputs of the mixer, is shown in Figure 6.54.

It can be seen that in this case there is no offset value, but there is also a feedthrough of the RF signal, as in the previously studied current-reuse receiver. However, in this case the feedthrough is slightly larger due to the p-transistors of the load being smaller.

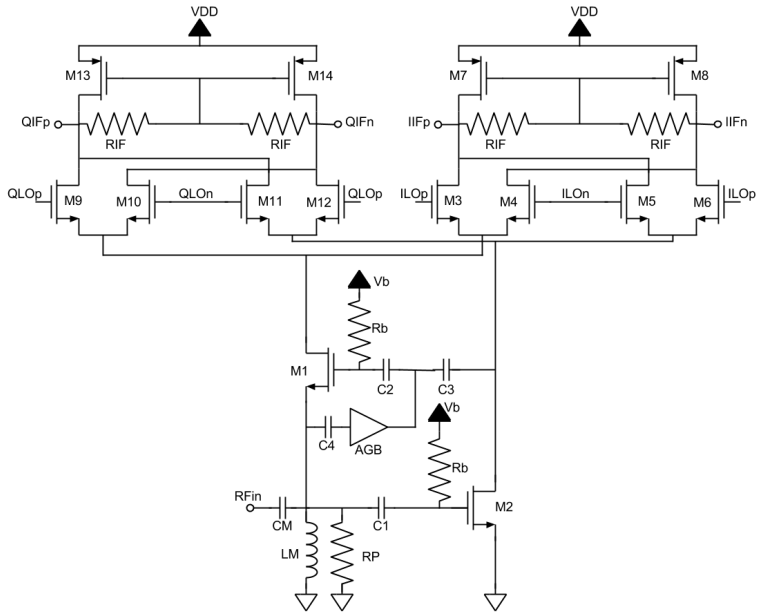


Figure 6.53. Schematic of the receiver-front end current-reuse Blixer topology with active load.

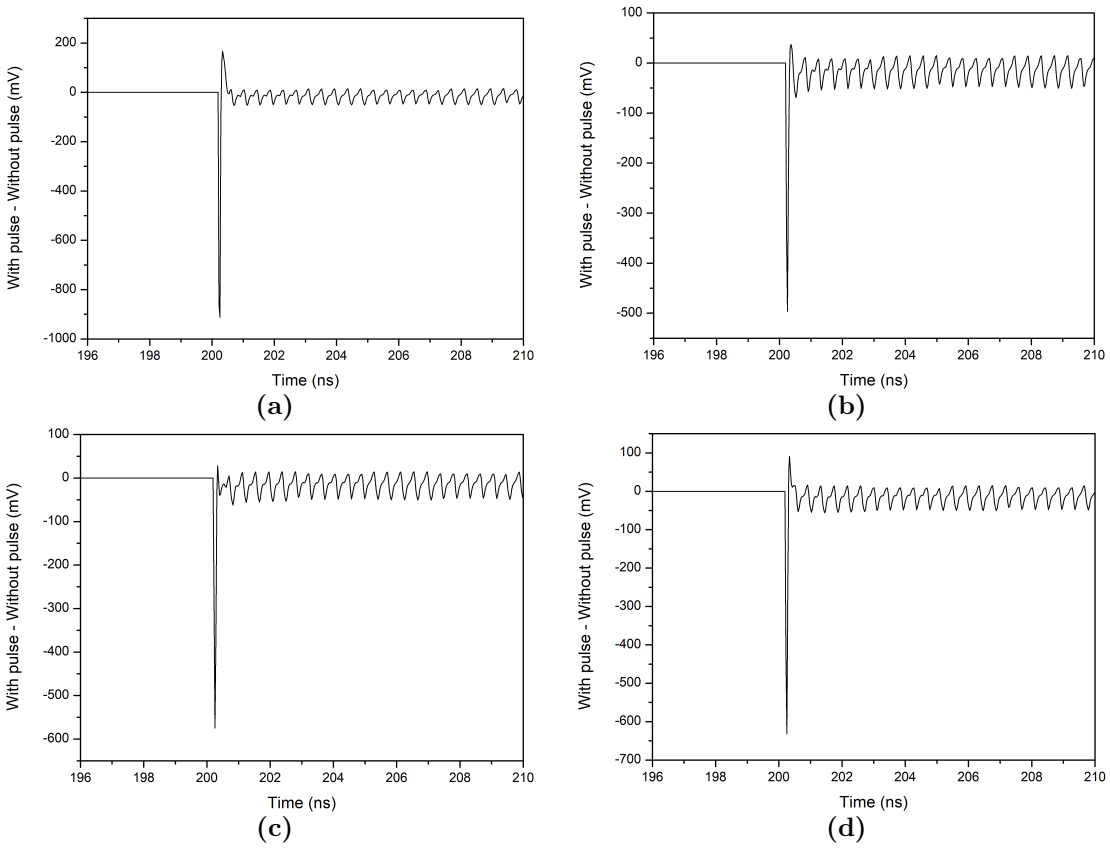


Figure 6.54. Effect of the pulse on the outputs of the mixer in the Blixer architecture with active load (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

Regarding the effect of the filtering stage, Figure 6.55 shows the four output signals of the complex filter both for the case of a strike and no strike occurring. It can be seen that the amplitude and phase shift has been considerably reduced, in a similar way as it did for the previously studied receivers.

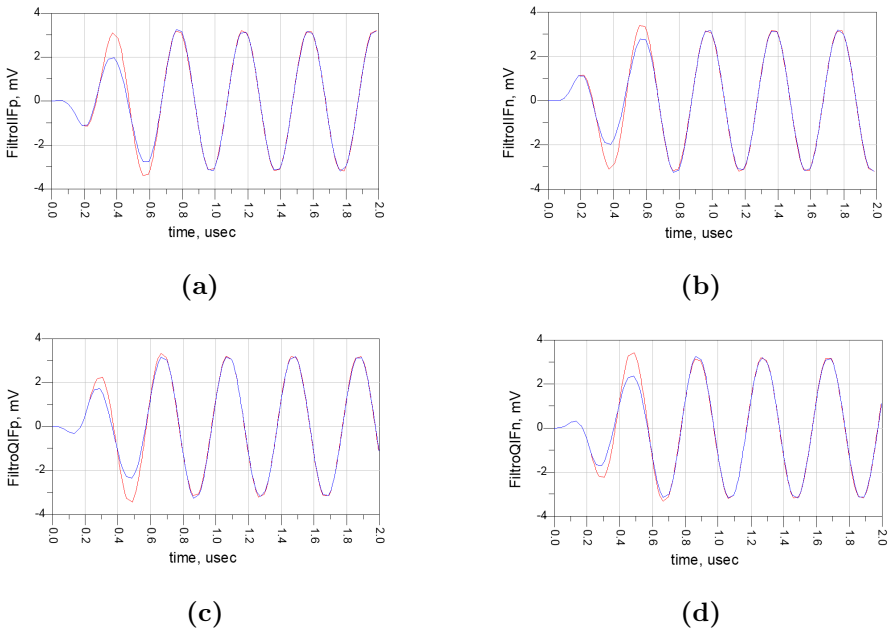


Figure 6.55. Output signals of the complex filter in the Blixer architecture with active load (a) positive I branch (b) negative I branch (c) positive Q branch (d) negative Q branch.

As a conclusion, it can be stated that stacking the Biquad and complex pole in the receiver implies the advantage of the reduction of power consumption since the current is reused by various circuits. However, the results obtained in this chapter show that this specific configuration leads to a worse behaviour under the effects of radiation in terms of amplitude and phase shift of the signals in the receiver.

6.4 Conclusion

In this chapter, the receivers presented in the previous chapter have been studied under the effects of radiation. In order to do so, it has been analysed how current pulses generated in the low noise amplifier propagate down the receiver chain.

First, the propagation of pulses through mixers was studied. Both single-balanced and double-balanced mixers were analysed, as well as the effect of the duty cycle in the propagation of said pulses. Simulation results show that, if certain conditions regarding the pulse width are met (see Equation 6.2), a pulse introduced at the input of the circuit will propagate to the output in all cases.

The effect of filters in the analysed current pulses has also been studied. The obtained results state that part of the information of the current pulses could be lost in the filtering process, thus minimising the effect of the pulse. In the case of low-IF receivers designed for low power consumption standards, the bandwidth of a channel is usually in the order of a few MHz. Therefore, this information loss will be further increased in the case of pulses with a width of approximately a few nanoseconds.

Finally, the analysis of SETs on different receiver architectures was performed. The conventional and the two current-reuse receivers explained in *Chapter 5* were analysed. The procedure that has been followed consists in analysing the voltage signal at different nodes of the receiver chain, checking for possible amplitude and phase variations in the signal. Taking this into account, the three receivers showed a similar behaviour since an amplitude and phase shift was observed in all of them. However, it should be noted that in the case of the Blixer, a worse behaviour is achieved under the effects of radiation in terms of amplitude and phase shift of the output signals when the Biquad and complex load are stacked on top of the receiver.

Chapter 7
CONCLUSIONS

7.1 Conclusions

The main objective of this research was to analyse how analog RF circuits behave in radiation environments.

In order to achieve this objective, first the different radiation sources and their effects on electronic devices were studied. Regarding the radiation sources, two major groups can be distinguished: radiation trapped in the magnetic field of planets and transient radiation environment. The ionizing particles trapped in the magnetic field of the Earth constitute a zone called the Van Allen belts. This area must be considered when launching satellites and other spacecrafts into space since they contain high energy particles that can affect the electronic systems on board. The South Atlantic Anomaly represents a specially troublesome region of the Van Allen belts since it can be found at smaller altitudes from the Earth's surface. As for the transient radiation, the two main contributors are galactic cosmic rays and particles emitted during solar events.

Regarding the radiation effects on electronic systems, there are three main categories: activation by nuclear reaction, displacement damage and ionizing effects. This last one is the focus of this research. These ionizing effects occur when an ionizing particle strikes a semiconductor device. As the particle traverses the device, electron-hole pairs are generated, which are the source to both single event effects (SEEs) and total ionizing dose effects (TID). The technology scaling in modern CMOS processes, where the gate lengths of the transistors have been considerably reduced, has made these processes more robust against TID. On the contrary, SEEs have become a greater problem in modern processes since particles with less energy are able to produce SEEs.

Once the different radiation sources and their effects on electronic devices were studied and understood, CMOS technologies were analysed under the effects of radiation. As mentioned previously, cost reduction can be achieved thanks to CMOS technologies by using cheap devices with minimum size and weight, besides operating at low power. However, CMOS technologies are vulnerable to radiation effects, specially to SEEs. In order to study these effects in CMOS technologies, a TCAD physics-based software tool was used to model CMOS semiconductor devices and perform ion strike simulations. The results obtained in these simulations were then

used to refine the circuit simulations performed in an electrical circuit domain simulator (ADS). This way the accuracy of the device solver is combined with the fast simulations performed in the circuit simulator.

In this work, the *Sentaurus* TCAD tool by *Synopsys* was used to model the transistors and perform heavy ion strikes simulations. In this case, a 0.18 μm CMOS process was modelled. Specifically, an NMOS transistor was modelled and once its adequate electrical performance was verified, it was studied under the effects of radiation using the heavy ion model included in *Sentaurus*. These heavy ion strike simulations showed that an increase in LET and penetration depth of the heavy ion in the semiconductor implies an increase in the drain current. Regarding the angle of incidence of the particle, higher currents are obtained for angles where the maximum number of electron-hole pairs is generated along the reverse-biased *n-p* junction. With this information, the TCAD-generated current pulses in the transistors were introduced in the critical nodes of analog RF circuits.

On another note, a high performance GaN technology was also studied under the effects of radiation. Although this was not in the original aim of this work, devices fabricated in an AlGaN/GaN on sapphire process became available to the research group during the process of this research. This presented a unique opportunity to complement the analysis performed on CMOS devices in this research. The methodology used was very similar as the one followed for the CMOS technology. First, the devices were modelled using the TCAD tool. Then, ion impacts were simulated for different locations, depth, LET and direction values. Simulation results show that the drain current density increases as the ion penetrates in the device, similarly as for the CMOS device. In the case of GaN transistors, this can be explained by the fact that a higher energy ion results in a deeper penetration and more ionization produced in the transistor. Additionally, angled strikes were also studied. In this case, the drain total current density decreases for bigger angles since as the angle of incidence increases, so does the recombination of electron-hole pairs.

In this dissertation, a model has been developed to match the response of the drain current density of the analysed GaN transistors. The model is composed of three exponential functions, each one of them modelling a different mechanism which leads to the obtained current density. The first mechanism is related to the collection of electrons at the drain after a generation of electron-hole pairs occurs when a heavy ion strikes the device. The second term of the equation is due to a diffusion-mechanism that takes place due to the excess of holes that is generated after the first mechanism occurs. Finally, the back-channel effect is the responsible for the third mechanism.

Once the effects of radiation were studied in the transistors of a CMOS process, the next step consisted of studying the effects of radiation in individual analog RF circuits. In this case, LNAs were studied. These circuits are generally the first elements of a receiver chain, which means that the current pulses generated in these circuits due to heavy ion strikes could propagate to subsequent circuits in the receiver chain and cause failures. In this work, two well-known LNA topologies, the

common-source and the common-gate cascode, were designed and analysed when heavy ions strike the most sensitive nodes of these circuits. Once an adequate performance of these amplifiers was achieved, the TCAD-generated curves for the CMOS process were introduced in the circuit domain simulator ADS to analyse the most vulnerable nodes of both LNAs. Simulation results show that the SET performance of both LNAs is considerably more sensitive to strikes on the biasing networks of the circuits. In light of these results, radiation hardening by design techniques were applied at these nodes in order to reduce the effect of SETs, without modifying the RF performance of the LNAs. The main approach was to reduce the voltage peaks by increasing the time constant of the sensitive nodes by including resistances and capacitances. These RHBD techniques considerably reduced the recovery time and maximum voltage peak of the output signal of both LNAs.

The common-gate LNA was fabricated and measured. Specifically, a CG LNA and its RHBD counterpart were integrated in one chip. A CSOIC-16 package was implemented and the chip was mounted on a custom PCB. The package was designed in a way that the lid can be removed for laser testing to assess the SET response of the circuit. Unfortunately, funding and time limitations made it impossible to test the circuits with laser equipment.

After radiation effects were studied in analog RF circuits, such as LNAs, the next step consisted in analysing their impact on an electronic system. In this case, the impact of the pulses generated in LNAs on RF receivers was studied. To do so, three different low-IF RF receivers were designed. All of these receivers were designed using CMOS process and designed for the IEEE 802.15.4 standard. The first receiver follows a conventional low-IF architecture, while the other two implement a current-reuse architecture. The conventional receiver was implemented using a 0.18 μm CMOS technology by UMC, while the other two were designed with a 65 nm CMOS process by UMC. All of the designed receivers meet the requirements of the IEEE 802.15.4 standard and perform favourably in terms of high level of integration and low power consumption.

These receivers were then analysed under the effects of radiation. The main focus was to understand how the current pulses generated in the LNA propagate through the different circuits that form the receiver. First, the propagation through mixers was studied. Simulation results show that a pulse introduced at the input of the circuit will propagate to the output if the following condition is met:

$$f_{LO} > \frac{2}{\tau} \tag{7.1}$$

where f_{LO} is the frequency of LO signal and τ is the width of introduce pulse.

The effect of filters on the analysed current pulses was also studied. The obtained results state that a portion of the information of the current pulses could be lost in the filtering process, thus minimising the effect of the pulse. In the case of

low-IF receivers designed for low power consumption standards, the bandwidth of the channel is generally in the order of a few MHz. Under these circumstances, the information loss will be further increased in the case of pulses with a width of approximately a few nanoseconds, such as the TCAD-generated ones achieved in this work.

Regarding the analysis of SETs on the designed RF receivers, the three of them showed a similar behaviour since in all of them an amplitude and phase shift was observed. This shift could result in a bit change in the digital circuits that follow the receiver front-end designed in this work, resulting in a slight increase of the bit error rate (BER) of the system. However, it is difficult to quantify the impact on analog circuits. The severity of the SET is only known once it propagates until the end of the signal processing chain.

In this dissertation, a procedure to analyse the effect of SETs in RF receivers has been proposed. The method consists in analysing the voltage signal at different nodes of the receiver chain, studying how this signal varies under the presence of SETs. As mentioned previously, all of the RF receivers that have been studied in this work behave in a similar way in terms of amplitude and phase shift. However, it should be noted that in the case of the Blixer, a worse behaviour is achieved under the effects of radiation in terms of amplitude and phase shift of the output signals when the Biquad and complex load are stacked on top of the receiver.

7.2 Areas for further research

The main objective of this work, which is analysing how analog RF circuits behave in radiation environments, has been achieved. However, there is still room for future explorations in this research line.

First of all, as mentioned previously, due to funding limitations it was impossible to perform laser testing on the designed circuits in order to experimentally assess the SET response of these circuits. Therefore, it can be seen clearly that the testing of the circuits under the effects of radiation needs further research.

Additionally, in order to quantify the impact of the amplitude and phase shifts observed in the RF receivers, the complete chain should be implemented. To do so, the circuits following the designed receivers should be designed, including the digital circuitry of the receiver.

Finally, it would be interesting to analyse the effects of radiation in a complete transmitter/receiver module. For this purpose, a RHBD transmitter should be designed and integrated together with the receiver. In this line, some studies have already been made in the research group regarding phase-locked loop (PLL) circuits [71].

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Part II

Appendices

Apéndice **A**

APPENDIX A: RESUMEN EN ESPAÑOL

A.1 Introducción

Las redes inalámbricas de sensores (WSNs, del inglés *Wireless Sensor Networks*) han permitido mejorar la interconexión y comunicación entre distintos dispositivos. Esto ha facilitado el desarrollo del internet de las cosas (IoT, del inglés *Internet of Things*). Sin embargo, existen aplicaciones en las que la presencia de alta radiación ambiental dificulta la implantación de este tipo de redes. Concretamente, aplicaciones en sectores como el aeroespacial, el aeronáutico, el nuclear o el de la salud. Teniendo esto en cuenta, se puede afirmar que es de especial interés para el sector del diseño de sistemas electrónicos el poder desarrollar dispositivos que permitan el despliegue de redes inalámbricas de sensores en entornos de alta radiación. Por ejemplo, en el sector aeroespacial, el uso de WSNs permite reducir el peso y tamaño de los satélites al minimizar el cableado utilizado en las comunicaciones intra-satélite. Esto, a su vez, permite reducir el coste de poner los satélites en órbita.

El principal problema de utilizar WSNs en entornos de alta radiación consiste en la interacción de los circuitos y sistemas electrónicos con las partículas ionizantes presentes en este tipo de entorno. Estas partículas pueden producir efectos negativos como son la dosis total de ionización (TID, del inglés *Total Ionizing Dose*) o los efectos de eventos singulares (SEEs, del inglés *Single Event Effects*). Los efectos TID pueden degradar de manera progresiva el funcionamiento de los sistemas electrónicos debido a un proceso acumulativo de generación de carga. Por otra parte, los SEEs provocan la corrupción de datos en circuitos digitales, perturbaciones transitorias en circuitos analógicos, así como picos de corriente que pueden llegar a ser destructivos. Estos efectos deben ser considerados durante el proceso de diseño, para prevenir fallos en el correcto funcionamiento de los circuitos. Este problema se agrava al aumentar la escala de integración de los circuitos, donde el número de componentes integrados aumenta y el tamaño de las puertas de los transistores disminuye. Esto se traduce en que partículas con menor energía pueden provocar SEEs.

Para mitigar los daños producidos por TID y SEEs en circuitos y sistemas electrónicos, se pueden utilizar materiales de blindaje. Sin embargo, para aplicaciones en sectores como la aeronáutica o el aeroespacial, en las que el peso adquiere

una gran importancia, este blindaje debe ser ligero. Esto significa que este blindaje no es capaz de detener todas las partículas de alta energía. Por tanto, es necesario estudiar cómo afectan las partículas ionizantes de alta energía a los circuitos electrónicos, así como desarrollar circuitos y sistemas robustos frente a la radiación. Es posible implementar técnicas de resistencia a la radiación a distintos niveles. Entre estas técnicas, las más populares son las conocidas como técnicas de diseño de circuitos resistentes a la radiación (RHBD, del inglés *Radiation Hardening By Design*). Las técnicas RHBD permiten desarrollar circuitos resistentes a la radiación sin modificar los procesos tecnológicos existentes, manteniendo así las prestaciones de los dispositivos a nivel electrónico.

Teniendo esto en cuenta, se puede afirmar que uno de los ámbitos de estudio de mayor interés en el campo del diseño de sistemas nanoelectrónicos es la tolerancia a la radiación de dichos sistemas. Los circuitos utilizados en aplicaciones espaciales tradicionalmente emplean tecnologías III-V, como el silicio germanio (SiGe) o silicio sobre aislante (SOI, del inglés *Silicon On Insulator*), que poseen una serie de características que las hacen tener cierta tolerancia a la radiación. Sin embargo, se pueden reducir considerablemente los costes al utilizar tecnologías CMOS, las cuales permiten desarrollar dispositivos de bajo coste, reducido tamaño y bajo consumo de potencia. Estas ventajas son precisamente las que han permitido el desarrollo de las WSNs. Sin embargo, los circuitos diseñados con este tipo de tecnologías son especialmente vulnerables a la radiación ambiental.

Tal y como se ha comentado anteriormente, los SEEs se han convertido en un problema cada vez mayor a medida que ha disminuido el tamaño de los dispositivos electrónicos, especialmente en tecnologías CMOS. Estos efectos se producen cuando una partícula energética impacta una región sensible de un circuito integrado, generando pares de electrón-hueco. Estos pares electrón-hueco pueden derivar en la generación de pulsos transitorios que pueden propagarse a otras áreas del circuito, produciendo lo que se conoce como *single event upsets* (SEUs). En general, los eventos transitorios que aparecen en los circuitos analógicos debido a la radiación se denominan eventos singulares transitorios (SETs, del inglés *Single Event Transients*). Estos efectos se definen como alteraciones transitorias de cierta amplitud y duración que pueden provocar errores o fallos en otros circuitos del sistema.

En el pasado, el estudio de este tipo de efectos ha sido analizado principalmente en circuitos digitales puesto que estos se suelen implementar utilizando el tamaño mínimo de los transistores, a diferencia de los circuitos analógicos. No obstante, el escalado de los dispositivos ha provocado que en los últimos años haya incrementado el número de estudios sobre los efectos de la radiación en circuitos analógicos. Sin embargo, las técnicas de diseño RHBD para sistemas analógicos completos y para circuitos de radiofrecuencia (RF) todavía son escasas y deben ser estudiadas con mayor tipo de detalle. Debido a esto, esta tesis se centra en estudiar los SETs en circuitos analógicos de RF, además de proponer técnicas que minimicen los efectos de la radiación en estos circuitos.

En cuanto a la metodología utilizada, en esta tesis se ha usado la herramienta TCAD *Sentaurus* de *Synopsys* para modelar dispositivos semiconductores y realizar

simulaciones de impactos de partículas ionizantes en los mismos. La información obtenida de estas simulaciones es utilizada posteriormente en una herramienta de simulación de circuitos. En este caso, se ha utilizado la herramienta *Advanced Design System* (ADS) de *Keysight*. De esta manera se combina la precisión del simulador de dispositivos con la rapidez de las simulaciones realizadas en el simulador de circuitos.

A.2 Objetivos

El objetivo principal de esta tesis doctoral es analizar cómo afecta la radiación espacial a circuitos analógicos de radiofrecuencia. Los resultados de esta tesis se encuentran integrados dentro del proyecto de investigación denominado Diseño de circuitos de comunicaciones para alta radiación ambiental (ComRad), financiado por el Ministerio de Economía y Competitividad (TEC2015-71072-C03-01). Además, este trabajo está cofinanciado por el Ministerio de Ciencia, Innovación y Universidades (RTI2018-099189-B-C22), por la Agencia Canaria de Investigación, Innovación y Sociedad de la Información (ACIISI) del Gobierno de Canarias (ProID2017010067) y el Programa Predoctoral de Formación del Personal Investigador de la Universidad de Las Palmas de Gran Canaria.

Con el fin de alcanzar el objetivo principal de esta tesis, se han planteado y alcanzado los siguientes objetivos parciales:

- **Comprender los efectos de la radiación en semiconductores**. Es de vital importancia analizar a fondo y comprender las diferentes fuentes de radiación y los efectos que tienen en los sistemas electrónicos basados en semiconductores antes de poder estudiar cómo afecta la radiación a los circuitos de RF.
- **Analizar los efectos de la radiación en tecnologías CMOS**. Tal y como se ha comentado anteriormente, los circuitos de RF analizados en esta tesis han sido diseñados utilizando tecnologías CMOS. Por lo tanto, se debe estudiar cómo se comportan los dispositivos CMOS bajo los efectos de la radiación.
- **Modelado de los transistores de la tecnología**. Para poder estudiar los efectos de la radiación en circuitos de RF primero se debe analizar el elemento básico de este tipo de circuitos, los transistores. Para ello, se han utilizado herramientas de diseño asistido por ordenador (TCAD) para modelar estos dispositivos y simular su comportamiento cuando les impacta una partícula ionizante.
- **Analizar los efectos de la radiación en circuitos de RF individuales**. En este caso, se han diseñado y analizado amplificadores de bajo ruido (LNA, del inglés *Low Noise Amplifier*). Generalmente, este tipo de amplificador es el primer elemento en una cadena de recepción. Por lo tanto, los pulsos de corriente que se generen en estos circuitos debido a los efectos de la radiación

podrían afectar a los siguientes elementos de la cadena de recepción. Además, se ha estudiado el comportamiento de mezcladores en entornos de alta radiación.

- **Analizar los efectos de la radiación en sistemas de RF**. Los distintos circuitos de RF se encuentran dentro de un sistema, como podría ser un receptor o un transmisor. En esta tesis, se ha estudiado cómo los efectos de la radiación que se producen en un circuito de RF pueden afectar al sistema. Una forma de realizar este tipo de estudio consiste en analizar en cómo varía la constelación del sistema bajo los efectos de la radiación. Sin embargo, para poder realizar este análisis, el período de símbolo del sistema debe ser del mismo orden de magnitud que la duración del efecto producido por la radiación. Esto no siempre se cumple, tal y como se demuestra en esta tesis. Teniendo esto en cuenta, en esta tesis se propone un procedimiento que consiste en analizar la señal en tensión en los nodos críticos del sistema, con el foco puesto en detectar las posibles variaciones de amplitud y fase de la señal.

A.3 Conceptos teóricos sobre los efectos de la radiación

A.3.1 Fuentes de radiación

Las fuentes de radiación que existen se pueden dividir en dos grupos: la radiación atrapada en los campos mágneticos de distintos planetas y las partículas libres que circulan por el espacio.

En cuanto al primer tipo de fuente de radiación, cabe destacar que una de las zonas cercanas al planeta Tierra donde existe una alta densidad de partículas ionizantes son los conocidos como cinturones de Van Allen. Estas zonas se encuentran en la magnetosfera debido a que el campo magnético de la Tierra atrapa partículas cargadas provenientes del Sol, formando una superficie toroidal de plasma, tal y como se puede ver en la Figura A.1. Estos cinturones están compuestos principalmente por electrones, protones e iones pesados de baja energía que se mueven en espiral a lo largo de las líneas del campo magnético terrestre.

Se pueden diferenciar dos zonas distintas en los cinturones de Van Allen: el cinturón interior y el exterior. El primero se encuentra entre 1000 y 15000 km por encima de la superficie terrestre, mientras que el segundo se sitúa entre 17000 y 60000 km.

Una región especial de los cinturones de Van Allen es lo que se conoce como la Anomalía del Atlántico Sur (SAA, del inglés *South Atlantic Anomaly*). Esta región se encuentra sobre la costa de Brasil y se forma debido a una depresión del campo magnético terrestre. Esto supone un problema para las aeronaves y satélites que

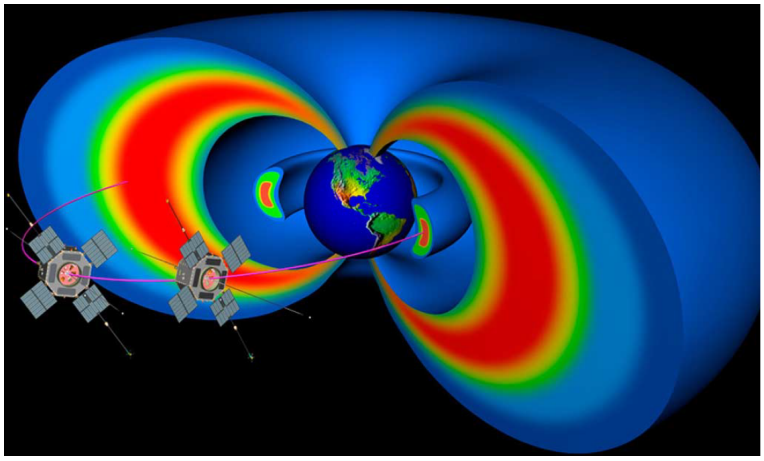


Figure A.1. Ilustración de los cinturones de Van Allen [3].

crucen esta zona ya que se pueden encontrar partículas ionizantes a unos 200 km por encima de la superficie terrestre.

En cuanto a las partículas libres que circulan por el espacio, existen diversas fuentes que producen estas partículas, pero los dos mayores contribuidores son: los rayos cósmicos galácticos (GCRs, del inglés *Galactic Cosmic Rays*) y las partículas emitidas durante eventos solares. Los GCRs se originan fuera de nuestro sistema solar y están principalmente compuestos de protones, aunque también hay presencia de electrones, partículas alfa e iones pesados. En cuanto a la radiación que se produce durante eventos solares, se pueden distinguir dos tipos: las eyecciones de masa corporal (CMEs, del inglés *Coronal Mass Ejections*) y las fulguraciones solares. Las CMEs se definen como radiación que se desprende del Sol en período de alta actividad solar. Este tipo de evento tiene una probabilidad alta de producir protones que alcancen a la Tierra. Por su parte, las fulguraciones solares se caracterizan por tener una alta densidad de iones pesados. Estos eventos ocurren periódicamente siguiendo los ciclos solares, que tienen picos de actividad aproximadamente cada 11 años.

A.3.2 **Efectos de la radiación**

Los efectos de la radiación se pueden diferenciar en tres categorías: activación por reacciones nucleares, daños por desplazamiento y los efectos ionizantes. El primero se produce cuando un núcleo estable se ve expuesto a un flujo de partículas energéticas, volviéndose inestable y radiactivo debido a las reacciones nucleares. Los daños por desplazamiento se producen cuando una partícula atraviesa un dispositivo semiconductor y genera colisiones elásticas con átomos de la estructura cristalina. En cuanto a los efectos ionizantes, se distinguen dos tipos de efectos: los efectos de dosis total de ionización (TID) o los efectos de eventos singulares (SEEs).

Cuando una partícula impacta un dispositivo semiconductor con suficiente energía, esta penetra el dispositivo. A medida que la partícula atraviesa el sustrato del semiconductor, la partícula pierde energía y crea pares electrón-hueco, tal y como se

muestra en la Figura A.2. Esta generación de pares electrón-hueco es la que origina tanto los efectos TID como los SEEs.

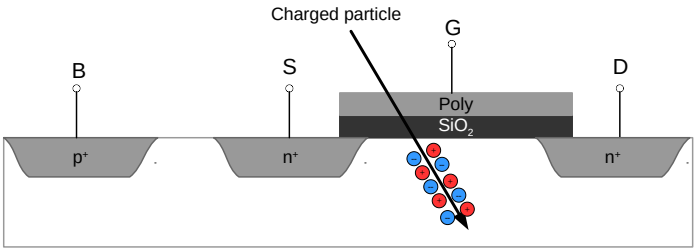


Figure A.2. Ilustración de cómo se generan pares electrón-hueco en un dispositivo semiconductor cuando una partícula ionizante lo atraviesa.

Los pares electrón-hueco generados se recombinan rápidamente a medida que son transportados mediante mecanismos de difusión. Sin embargo, la carga generada en capas dieléctricas y de interfaces puede permanecer atrapada durante largos períodos de tiempo. Esto se traduce en que los efectos TID aparecen cuando un dispositivo semiconductor se ve expuesto a la radiación durante largos períodos de tiempo.

En los dispositivos CMOS, la degradación de las prestaciones del dispositivo se produce principalmente por la carga generada en el óxido de la puerta. Las cargas acumuladas reducen la tensión umbral y aumentan las corrientes de fuga entre el surtidor y drenador de los transistores CMOS. Cabe destacar que en los procesos más modernos de tecnologías CMOS, donde las longitudes de puerta se han reducido considerablemente, el óxido de la puerta es lo suficientemente estrecho para evitar que se acumulen cargas atrapadas debido a efectos de túnel cuántico.

Los efectos de eventos singulares son otro efecto de la radiación generado por la ionización que se produce cuando una partícula atraviesa un dispositivo semiconductor. Existen dos tipos de mecanismos involucrados en la generación de SEEs: deposición de carga y recolección de carga.

El primero se produce cuando una partícula deposita carga en un dispositivo semiconductor. Esta deposición de carga se puede generar tanto por ionización directa como indirecta. La ionización directa ocurre cuando una partícula ionizante atraviesa un dispositivo semiconductor y pierde energía en el proceso, generando pares electrón-hueco. El número total de cargas es proporcional a la transferencia lineal de energía (LET, del inglés *Linear Energy Transfer*) de la partícula y la densidad del material atravesado. Por otra parte, la ionización indirecta la producen partículas ligeras como neutrones o protones. Cuando protones o neutrones con suficiente energía impactan un semiconductor, interactúan con su estructura cristalina a través de colisiones tanto elásticas como inelásticas. Esto puede generar reacciones nucleares cuyos productos pueden depositar energía mediante ionización directa.

El segundo mecanismo, la recolección de carga, ocurre cuando los pares electrón-hueco generados cuando una partícula atraviesa un dispositivo semiconductor impactan una unión polarizada de manera inversa. En transistores NMOS esta zona

se corresponde con la unión *n-p* entre el drenador y el sustrato. En este caso, los pares electrón-hueco son separados por el campo eléctrico generado desde la unión *n-p* polarizada en inversa antes de que se puedan recombinar. Esto se traduce en que los electrones fluyen hacia la región con difusión tipo *n* y los huecos hacia el contacto de sustrato en transistores NMOS.

La Figura A.3 muestra una ilustración de un transistor NMOS cuando lo impacta un ion pesado. En la Figura A.3 (a) se puede ver cómo la partícula genera pares electrón-hueco a medida que atraviesa el dispositivo. Las cargas generadas son atraídas por el potencial que existe en los contactos de drenador (D) y sustrato (B) del transistor NMOS, tal y como se ve en la Figura A.3 (b). Esto genera un pulso de corriente transitorio como el que se muestra en la Figura A.3 (c).

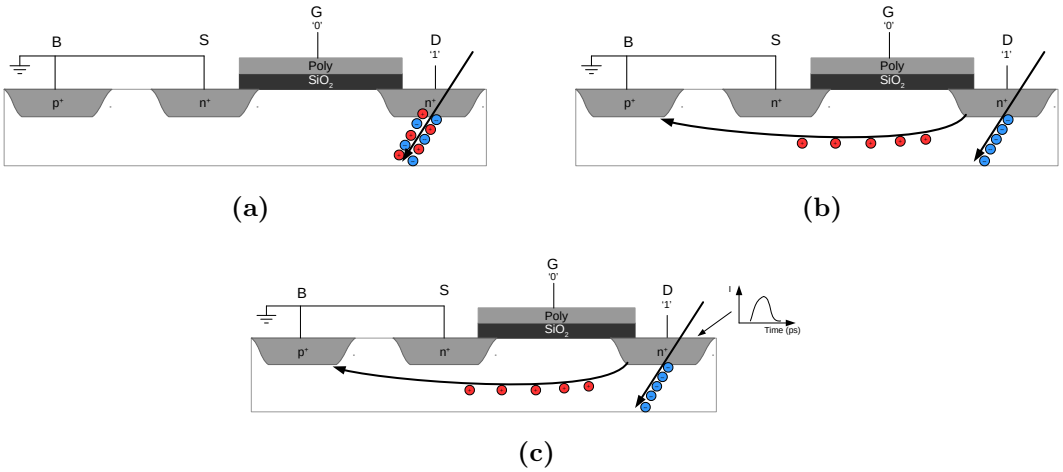


Figure A.3. Illustration of SEE generation process: (a) Charge generation (b) Charge collection (c) Circuit response.

A.4 Efectos de la radiación en dispositivos semiconductores

Tal y como se ha comentado anteriormente, el objetivo de esta tesis es analizar cómo se comportan los circuitos analógicos de RF en entornos de alta radiación. Para ello, el primer caso consiste en estudiar los efectos de la radiación en el elemento básico de este tipo de circuitos, los transistores. Una metodología bastante extendida consiste en utilizar herramientas TCAD para realizar este tipo de estudio. Esta herramienta permite modelar dispositivos semiconductores así como simular tanto la respuesta eléctrica como los efectos de la radiación en los mismos.

Los circuitos diseñados en esta tesis han sido implementados en tecnologías CMOS de la *foundry* UMC. Teniendo esto en cuenta, se ha modelado un transistor de un proceso de dicha tecnología. Por otra parte, durante el transcurso de la

investigación realizada para la elaboración de esta tesis se ha tenido acceso desde el grupo de trabajo a dispositivos de una tecnología de altas prestaciones en nitruro de galio (GaN). Esto supone una oportunidad única que permite complementar el estudio realizado sobre los efectos de la radiación en transistores CMOS. Es por esto por lo que también se ha incluido un estudio de los efectos de la radiación en transistores GaN.

A.4.1 Análisis de transistores CMOS

Se ha utilizado la herramienta *Sentaurus Structure Editor* (SDE) para modelar los transistores de la tecnología de 0,18 μm CMOS de UMC. La geometría del transistor ha sido modelada acorde a las dimensiones especificadas en la docmuentación de UMC. En cuanto a la concentración del dopaje en las distintas regiones del transistor, ha sido necesario averiguar los valores necesarios para el correcto funcionamiento del transistor. Para ello se han realizado simulaciones de manera iterativa hasta ajustar el comportamiento del modelo con las curvas del transistor proporcionado por la tecnología. En la Figura A.4 se muestra una vista 2D extrudida del modelo del transistor generado con la herramienta SDE.

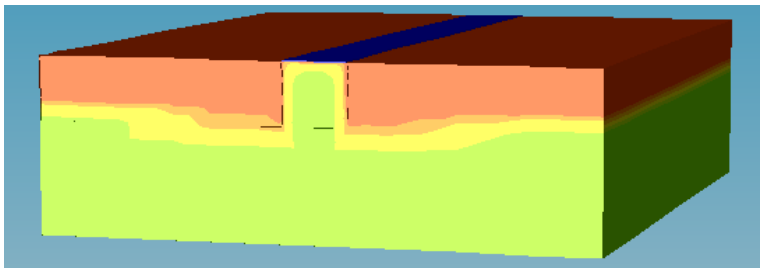


Figure A.4. Modelo 2D extrudido del transistor NMOS.

Con el fin de calibrar el modelo desarrollado, se han calculado las curvas *I-V* del mismo y se han comparado con las curvas obtenidas con el transistor proporcionado por el *kit* de diseño de UMC para ADS. En la Figura A.5 se muestra la corriente de drenador frente a la tensión de puerta para dos valores de tensión de drenador, tanto en escala lineal como logarítmica. Se puede observar que las curvas generadas con *Sentaurus* coinciden con las del transistor simulado en ADS. En la escala logarítmica se puede apreciar una diferencia en tensiones sub-umbrales. Sin embargo, esto no es un problema si los transistores de un circuito están polarizados con tensiones superiores para operar en la región inversa moderada o fuerte. Este es el caso de los circuitos diseñados en esta tesis.

Una vez comprobado el correcto funcionamiento del modelo del transistor NMOS, se ha analizado el efecto del impacto de un ion pesado en el dispositivo. Para ello se ha utilizado la herramienta SDEVICE dentro de *Sentaurus*. Concretamente, se han realizado estas simulaciones utilizando el modelo para iones pesados (*Heavy Ion*), el cual simula el efecto de una partícula ionizante atravesando el dispositivo semiconductor. Este modelo permite modificar distintos parámetros como son la

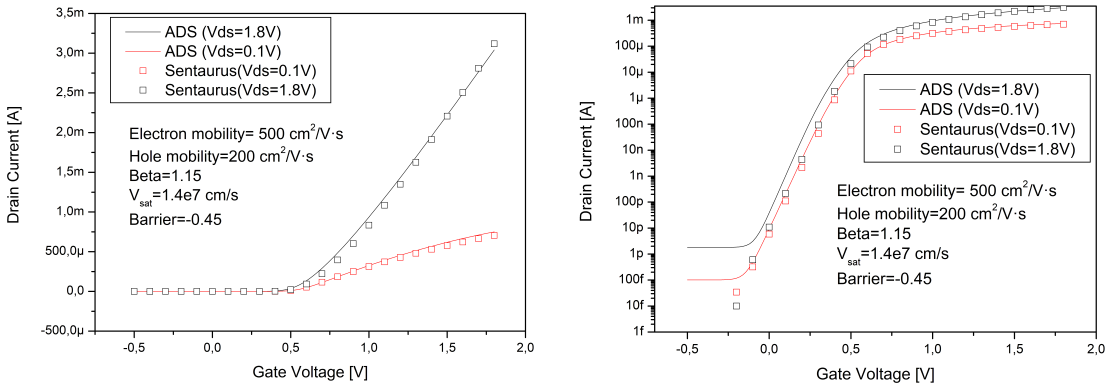


Figure A.5. Tensión de puerta frente a corriente de drenador obtenidas en Sentaurus comparadas con las obtenidas en ADS (a) escala lineal (b) escala logarítmica.

profundidad de penetración del ion pesado en el dispositivo, la transferencia lineal de energía (LET), el instante y lugar de impacto en el dispositivo o el ángulo con el que la partícula entra en el dispositivo.

En este caso, se han realizado simulaciones para distintos valores de profundidad de penetración, LET y ángulo. Todas las simulaciones se han realizado manteniendo la localización del impacto en el drenador del transistor NMOS ya que, tal y como se ha comentado anteriormente, corresponde con la región más sensible en este tipo de transistor. Las simulaciones se han realizado con valores de LET entre 1 y 30 MeV·cm^2/mg, mientras que la profundidad se ha variado entre 0,05 y 0,5 μm. En cuanto al ángulo de incidencia con respecto a la superficie del transistor (θ), se ha simulado para valores entre 15° y 90°.

En la Figura A.6 se pueden observar los pulsos de corriente generados en el drenador del transistor modelado debido al impacto del ion pesado para distintos valores de LET y profundidad, con $\theta = 90°$. Se puede observar que la corriente de drenador aumenta a medida que lo hace el valor de LET. Esto se debe a que un valor de LET se traduce en un mayor número de pares electrón-hueco generados y, por tanto, una mayor corriente. De manera similar, la corriente aumenta a la vez que lo hace la profundidad de penetración.

Con respecto al ángulo de incidencia, cabe destacar que los ángulos positivos representan una partícula con dirección hacia la puerta del transistor, mientras que los ángulos negativos hacen referencia a la partícula dirigida hacia el borde del dispositivo. Los mayores valores de corriente se producen cuando la partícula atraviesa una mayor zona de la unión entre el drenador y el sustrato. Esto se corresponde con ángulos de $\theta = 30°$, $\theta = 45°$ y $\theta = -60°$.

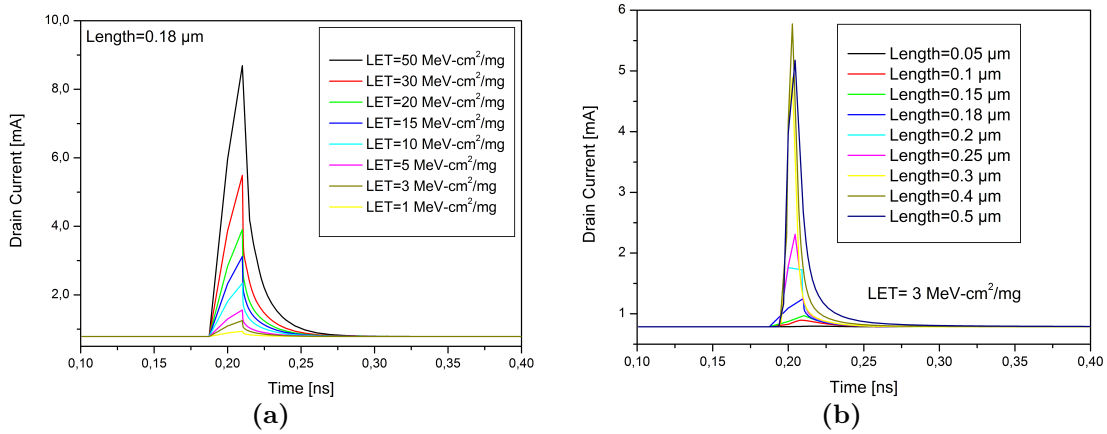


Figure A.6. Corriente de drenador para (a) distintos valores de LET con profundidad (*length*) constante (b) distintos valores de profundidad (*length*) con LET constante.

A.4.2 **Análisis de transistores GaN**

Los transistores GaN de alta movilidad de electrones (HEMT, del inglés *High Electron Mobility Transistor*) que han sido analizados bajo los efectos de la radiación están basados en un proceso AlGaN/GaN sobre zafiro. Estos transistores ya habían sido modelados por otro miembro del grupo de investigación.

La estructura del transistor AlGaN/GaN se muestra en la Figura A.7. De manera similar al caso del transistor CMOS, se utilizó la herramienta *Sentaurus* para modelar este dispositivo.

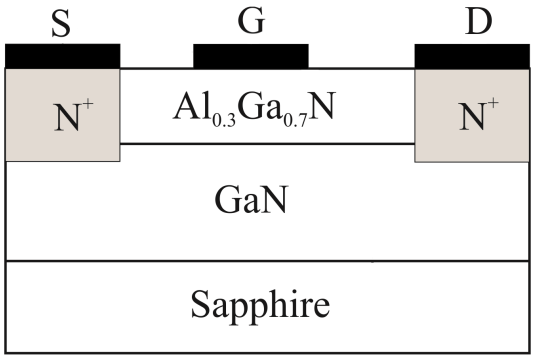


Figure A.7. Estructura de capas del dispositivo AlGaN/GaN HEMT.

Al igual que en el caso de los transistores CMOS, se ha utilizado el modelo *Heavy Ion* para simular el efecto de una partícula ionizante al impactar el dispositivo. La Figura A.8 muestra la densidad de corriente del drenador para impactos en distintos puntos del transistor. El efecto de la profundidad de penetración en el dispositivo y el ángulo de incidencia sobre la corriente de drenador también ha sido analizado.

La respuesta de la densidad de corriente de drenador en función del tiempo al impacto de un ion pesado se puede modelar con una ecuación basada en la suma de tres exponenciales:

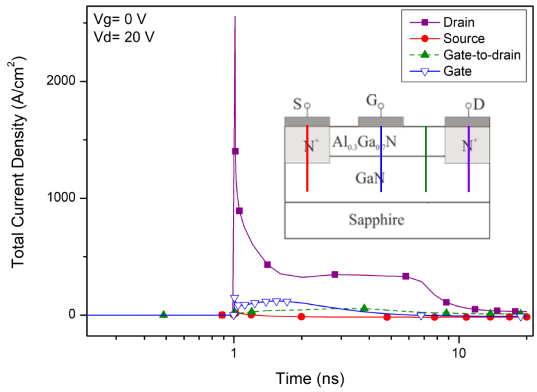


Figure A.8. Densidad de corriente de drenador en función del tiempo para distintas localizaciones de impacto de un ion pesado.

$$I_D = \sum_{n=1}^{3} \frac{Q_n}{t_{fn} - t_{rn}} \cdot \left(e^{-\left(\frac{t}{t_{fn}}\right)} - e^{-\left(\frac{t}{t_{rn}}\right)} \right), \tag{A.1}$$

donde Q_n hace referencia a la carga recolectada, t_{fn} el tiempo de bajada y t_{rn} el tiempo de subida. La primera exponencial simula el efecto del impacto del ion pesado en el dispostivo, lo cual genera pares electrón-hueco. Los electrones son atraídos rápidamente por el potencial en el drenador. Este efecto se modela con el primer término ($n = 1$). Esto produce un exceso de huecos en la capa *buffer* GaN. Cabe destacar que aparece un transistor bipolar parásito debido a la unión $n - p - n$ que se forma entre el surtidor, el exceso de huecos y el drenador. Estas cargas positivas reducen la barrera de potencial entre el surtidor y el canal, lo cual se traduce en una inyección adicional de electrones, que son recogidos en el drenador. Esto origina un mecanismo de difusión desde el surtidor (emisor del transistor bipolar parásito) al exceso de huecos (base del transistor bipolar parásito). La corriente derivada de este fenómeno se modela con el segundo término ($n = 2$). De manera adicional, un mecanismo de arrastre entre el surtidor y el canal, conocido como efecto *back-channel*, genera la corriente que se modela con el tercer término ($n = 3$).

La Figura A.9 muestra una comparación entre el modelo y la respuesta obtenida en *Sentaurus*, tras ajustar los parámetros del modelo.

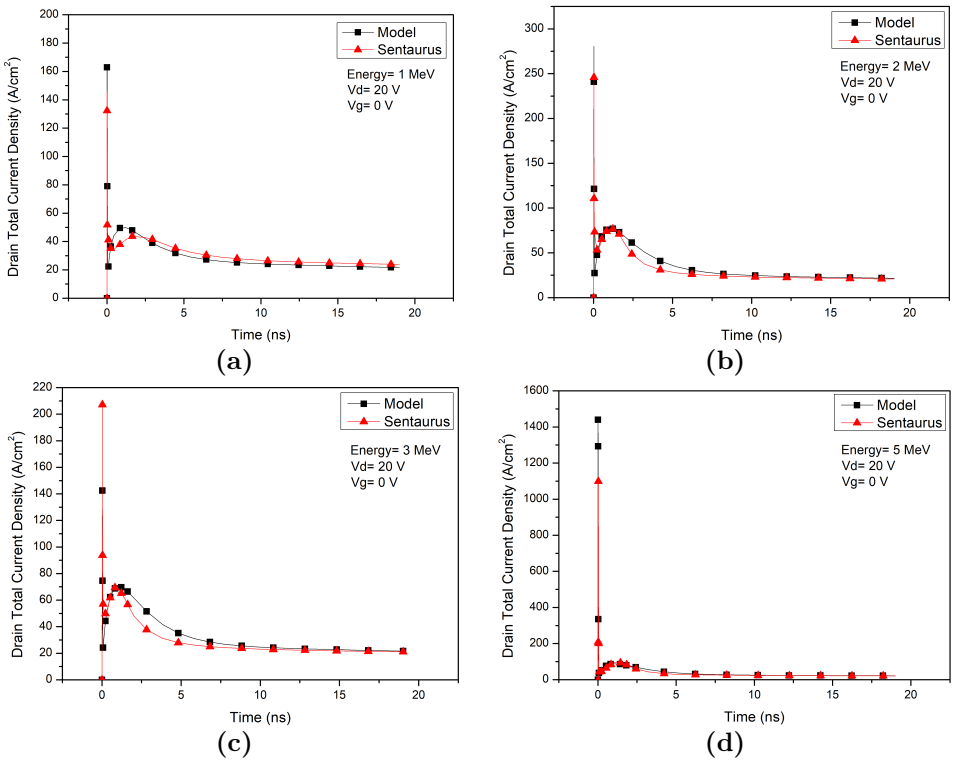


Figure A.9. Modelado de impacto de iones con distintas energías (a) 1 MeV (b) 2 MeV (c) 3 MeV (d) 5 MeV.

A.5 Efectos de la radiación en amplificadores de bajo ruido

A.5.1 Diseño de los amplificadores de bajo ruido

Los LNAs que se presentan en esta tesis han sido diseñados para el estándar IEEE 802.15.4 utilizando tecnologías CMOS. Este estándar está orientado a redes inalámbricas de sensores de bajo consumo. En esta tesis, se han diseñado dos LNAs basados en estructuras típicas de este tipo de circuito. En la Figura A.11 (a) se muestra el LNA diseñado en configuración de surtidor común (CS, del inglés *Common-Source*), mientras que en la Figura A.11 (b) se puede observar el segundo amplificador diseñado, basado en una estructura de puerta común (CG, del inglés *Common-Gate*).

A.5.2 Respuesta frente a SETs de los amplificadores de bajo ruido

Para estos LNAs, se ha estudiado el caso de impactos de iones pesados en los nodos más vulnerables de los circuitos. Para simular estos impactos, se han introducido los pulsos de corriente obtenidos en las simuaciones TCAD en los nodos críticos de los LNAs. Para ello, se ha utilizado la herramienta de diseño ADS.

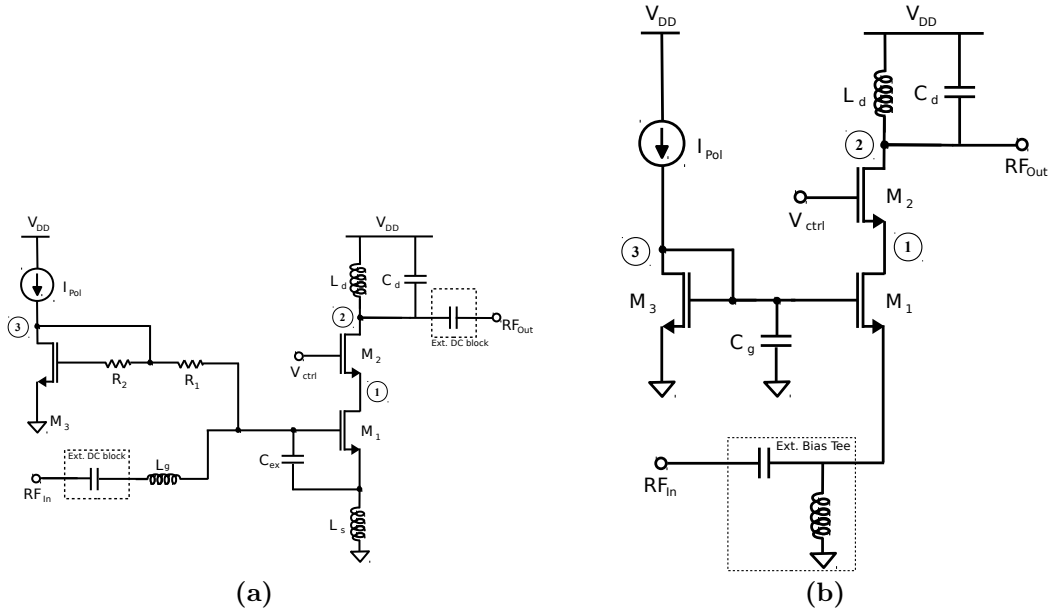


Figure A.10. (a) Esquemático del LNA con una estructura cascodo en configuración surtidor común (b) Esquemático del LNA con una estructura cascodo en configuración puerta común.

Tal y como se ha comentado anteriormente, las regiones más vulnerables frente a la radiación de los transistores NMOS se corresponden con el drenador de los mismos. Teniendo esto en cuenta, se han inyectado pulsos de corriente en los drenadores de los transistores de los circuitos (nodos 1, 2 y 3 en la A.10a y la A.10b).

Con el fin de estudiar la respuesta frente a SETs de ambos circuitos, se ha analizado el pico máximo de tensión y el tiempo de recuperación de la señal de salida de los LNAs para cada caso. En este estudio, se considera que la señal se ha recuperado cuando la diferencia entre la señal de salida en el caso de SETs y la señal de salida en el caso de que no haya un impacto sea menor que el 5 %.

Tras analizar los resultados de este estudio, se ha definido un área segura (SOA, del ingés *Safe Operating Area*) dentro de la cual se considera que los SETs tienen una amplitud y duración que no afectará al funcionamiento de los circuitos adyacentes. En la Tabla A.1 se muestra el porcentaje de SETs que se encuentra dentro del SOA para cada nodo de ambos circuitos. Tal y como se puede observar, el nodo 3 es el más vulnerable en ambos circuitos.

Table A.1: Porcentaje de SETs dentro del SOA para los LNAs CS y CG.

	LNA	
Nodo	CG	CS
1	80 %	80 %
2	65 %	60 %
3	50 %	40 %

A.5.3 **Técnicas de diseño robusto frente a la radiación**

En esta tesis, se han propuesto técnicas de mitigación de los efectos de la radiación a nivel de diseño (RHBD). Concretamente, se han implementado técnicas para minimizar los efectos de la radiación en el nodo 3 de los LNAS, al ser este el más vulnerable. En este caso, se han implementado técnicas basadas en el filtrado mediante resistencias y condensadores. Al incrementar la capacidad del nodo 3 se reduce la impedancia y se incrementa la constante de tiempo ($\tau = R \cdot C$), lo cual se traduce en un pico de tensión más pequeño debido a los SETs. Además, esto significa que el tiempo que la señal tardará en volver a estar por debajo del umbral es menor y, por tanto, el tiempo de recuperación se reduce. Teniendo esto en cuenta, se han modificado las redes de polarización de los dos LNAs de la manera que se muestra en la **??** y en la **??** para el CS y el CG, respectivamente.

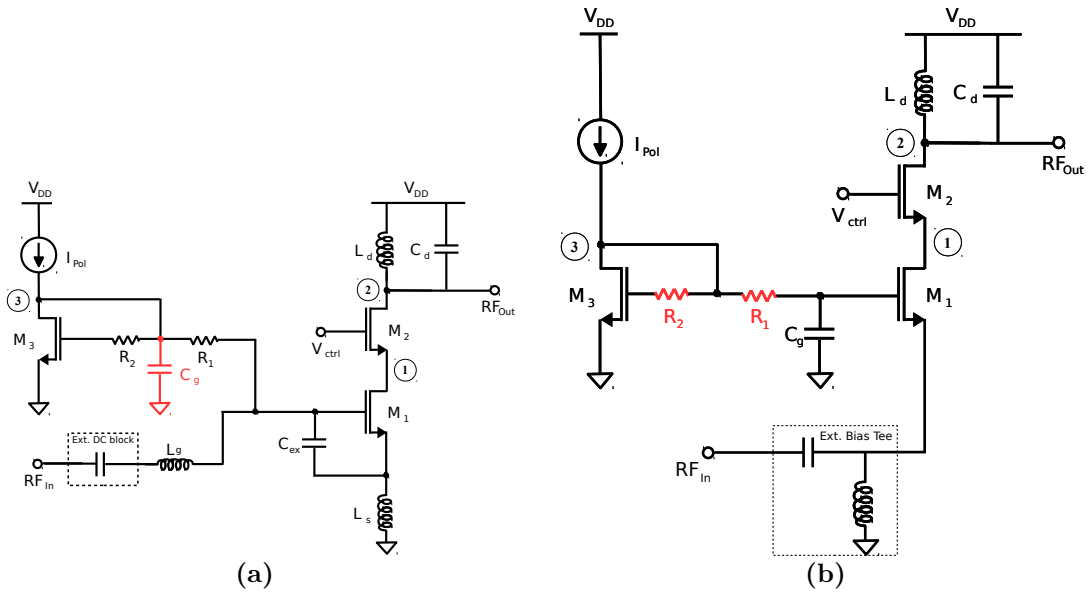


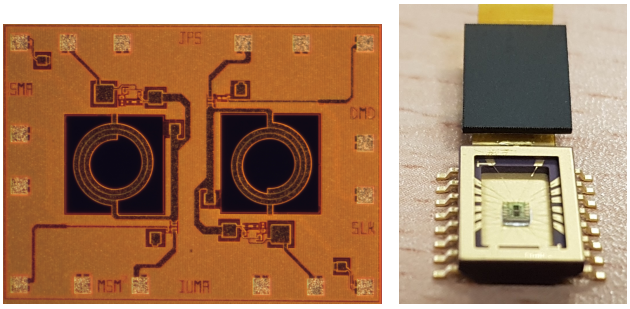
Figure A.11. (a) Esquemático del LNA CS con RHBD (b) Esquemático del LNA CG con RHBD.

Con estas técnicas se ha conseguido reducir tanto los tiempos de recuperación como los picos máximos de tensión de la señal de salida. De hecho, el 100 % de los SETs se encuentran dentro del SOA para los dos LNAs.

A.5.4 **Medidas de los amplificadores de bajo ruido**

Una vez se ha analizado el comportamiento frente a SETs de los dos LNAs, el siguiente paso consiste en fabricar y medir estos circuitos. Sin embargo, debido a limitaciones de financiación, solo ha sido posible fabricar uno de los LNAs. El LNA que se ha fabricado es el LNA CG debido a que tiene una respuesta frente a SETs ligeramente superior que la del LNA CS.

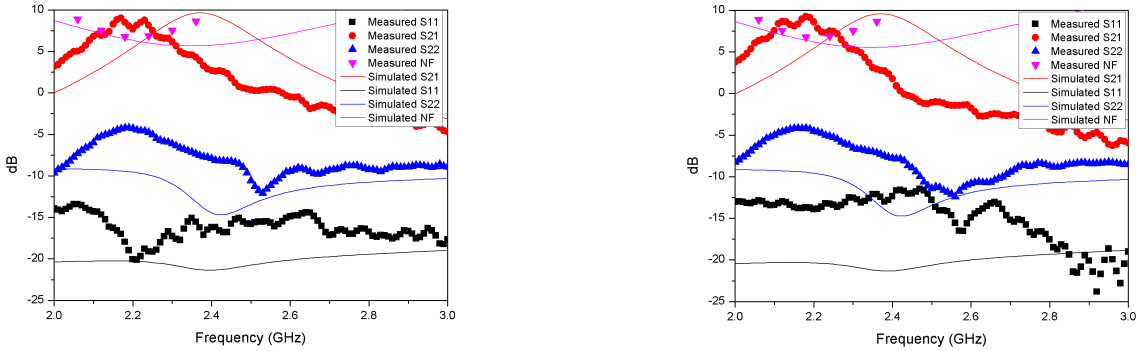
En la Figura A.12 (a) se muestra una microfotografía del circuito diseñado, tanto la versión convencional como la RHBD. En la Figura A.12 (b) se muestra el circuito encapsulado en un CSOIC-16.



(a) **(b)**

Figure A.12. (a) Microfotografía de los LNAs fabricados (b) Encapsulado CSOIC-16 de los LNAs fabricados.

El chip encapsulado ha sido soldado en una placa PCB con conectores SMA para las señales de alta frecuencia y BNC para las alimentaciones. La Figura A.13 muestra los resultados de medida del LNA, tanto convencional como RHBD, una vez han sido calibradas las pérdidas del encapsulado y los parásitos del circuito.



(a) **(b)**

Figure A.13. Resultados de medida (a) LNA CG (b) LNA CG RHBD.

A.6 Diseño de receptores de RF

En esta tesis se han diseñado tres receptores de RF, todos ellos para el estándar IEEE 802.15.4 y utilizando procesos CMOS. El primero de los receptores está basado en una arquitectura *low-IF* convencional, mientras que los otros dos emplean una topología con reutilización de corriente. El segundo de estos receptores con reutilización de corriente está basado en la topología *Blixer* en la cual un *balun*-LNA, que convierte la señal de entrada asímetrica en diferencial, y el mezclador se encuentran apilados.

A.6.1 Receptor low-IF convencional

La arquitectura del receptor *low-IF* convencional se muestra en la Figura A.14. Se puede observar que el LNA es el encargado de amplificar la señal de RF de entrada y el mezclador I/Q se encarga de trasladar la frecuencia de trabajo a una frecuencia inferior (IF, del inglés *Intermediate Frequency*). La señal de corriente a la salida del mezclador se convierte en una señal en tensión a través del amplificador de transimpedancia (TIA, del inglés *Transimpedance Amplifier*). Por último, se incluye una etapa de filtrado compuesta por un filtro polifásico.

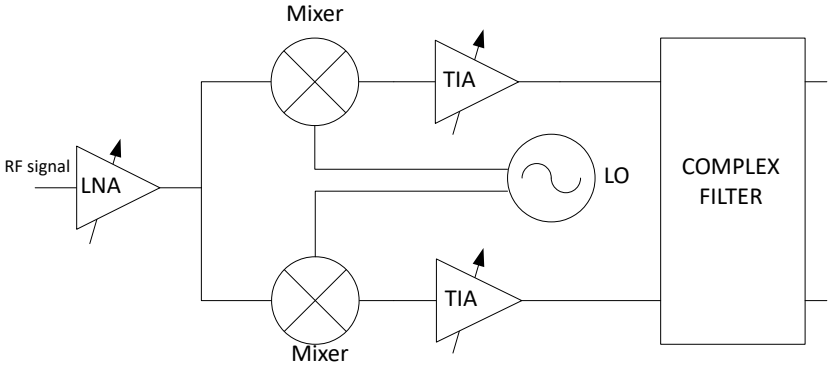


Figure A.14. Arquitectura del receptor *Low-IF* convencional.

A.6.2 Receptor con reutilización de corriente

El receptor con reutilización de corriente que se propone sigue una arquitectura *low-IF* diferencial. De la misma manera que en el caso del receptor *low-IF* convencional, el LNA amplifica la señal diferencial de entrada y el el mezclador I/Q se encarga de trasladar la frecuencia de trabajo a la frecuencia de IF. En este caso, el mezclador se encuentra apilado encima del LNA con el fin de reutilizar la corriente de polarización, reduciendo así el consumo del receptor de manera considerable. En la Figura A.15 se muestra el diagram de bloques de esta arquitectura.

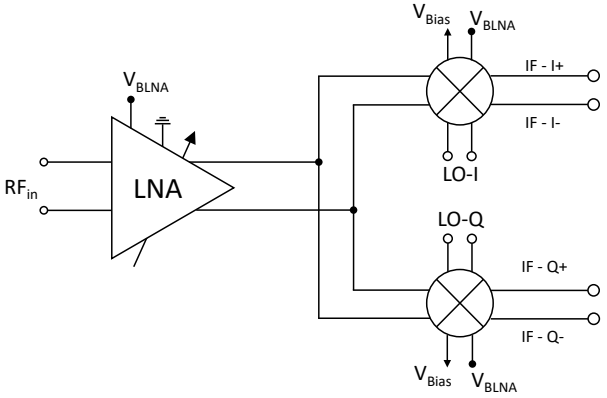


Figure A.15. Arquitectura del receptor con reutilización de corriente.

A.6.3 **Receptor con estructura Blixer**

El tercer receptor que ha sido diseñado se basa en la estructura *Blixer*, que está formada por un *balun-LNA* con cancelación de ruido y un mezclador I/Q doblemente balanceado apilado. Además, se ha apilado tanto una primera etapa de filtrado compuesta por un filtro bicuadrático como una carga compleja, encargada de rechazar la imagen y seleccionar el canal. El diagrama de bloques del receptor con estructura Blixer se muestra en la Figura A.16.

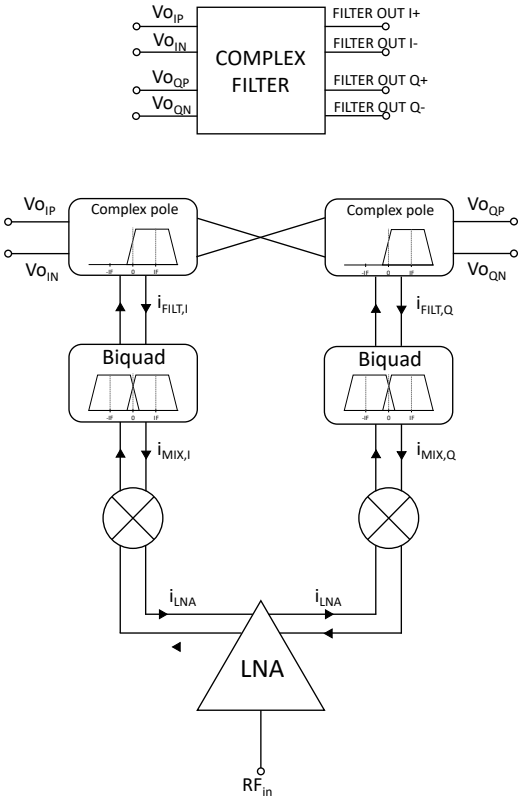


Figure A.16. Arquitectura del receptor con estructura Blixer.

A.7 **Efectos de la radiación en receptores de RF**

Una vez han sido diseñados los receptores de RF, se han analizado los mismos bajo los efectos de la radiación. En esta tesis se presenta un procedimiento para analizar cómo se comportan los receptores de RF cuando se producen SETs. Para ello se analizan los pulsos que se generan en los LNA y cómo se propagan por la cadena de recepción. En este caso, se ha estudiado la propagación de estos pulsos por los mezcladores, seguido del análisis de cómo se propagan por etapas de filtrado.

En cuanto al procedimiento que se presenta en esta tesis para estudiar el comportamiento de receptores de RF bajo los efectos de SETs, este consiste en analizar

la señal en tensión en los nodos críticos de la cadena de recepción buscando posibles variaciones de la señal.

Se ha analizado la propagación de pulsos de corriente en mezcladores tanto simplemente como doblemente balanceados. Además, se ha estudiado cómo afecta el ciclo de trabajo de los mezcladores en la respuesta frente a SETs de los mismos. Los resultados de simulación demuestran que si se cumple la Ecuación A.2, un pulso introducido en la entrada del mezclador se propagará a la salida.

$$f_{LO} > \frac{2}{\tau} \tag{A.2}$$

donde f_LO es la frecuencia del oscilador local y τ es el ancho del pulso introducido.

El efecto de los filtros en los pulsos de corriente mencionados también ha sido analizado. Los resultados indican que parte de la información espectral de los pulsos de corriente se descarta en el proceso de filtrado. Esto supone una minimización del efecto de los pulsos en los circuitos adyacentes. En el caso de los receptores *low-IF* diseñados para estándares de bajo consumo, el ancho de banda suele ser del orden de unos pocos MHz. Por tanto, esta pérdida de información espectral se ve agravada en el caso de pulsos de corriente de aproximadamente unos pocos nanosegundos, como es el caso de los pulsos estudiados en esta tesis.

En cuanto al análisis de los efectos de los SETs en distintos receptores, se han analizado los tres receptores diseñados (el *low-IF* convencional y los dos con reutilización de corriente). Tal y como se ha comentado anteriormente, se propone un procedimiento que consiste en analizar la señal en tensión en distintos nodos de la cadena de recepción. En este caso, los tres receptores muestran un comportamiento similar en términos de variación de amplitud y fase. A modo de ejemplo, en la Figura A.17 se muestra la señal en las cuatro salidas del filtro polifásico del receptor *low-IF* convencional.

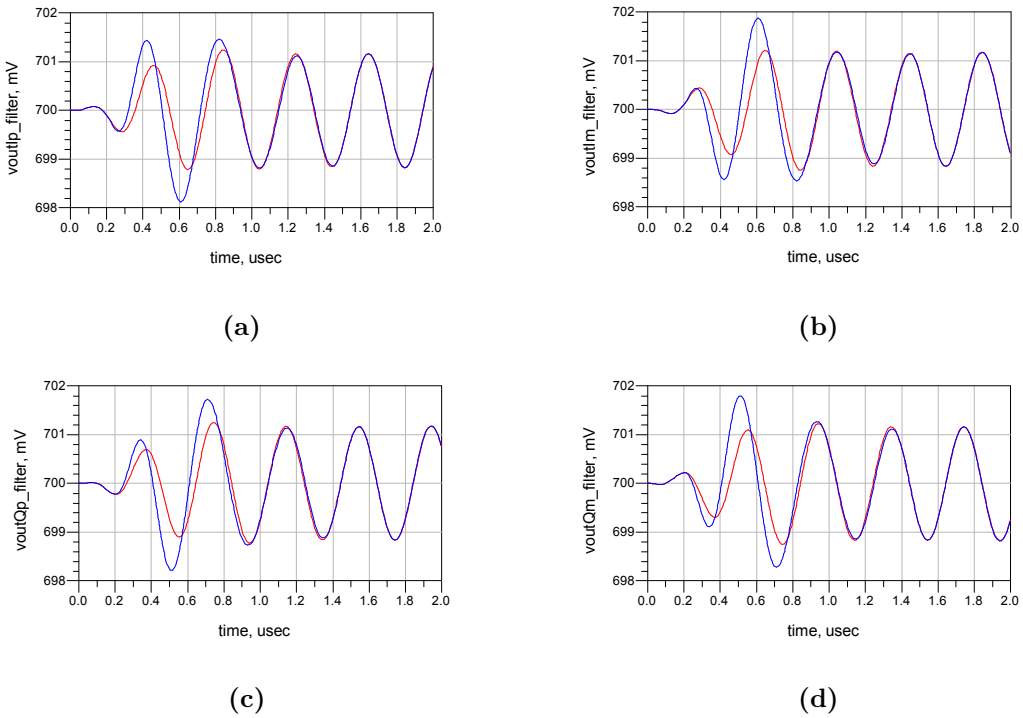


Figure A.17. Señales de salida del filtro polifásico (a) Rama I positiva (b) Rama I negativa (c) Rama Q positiva (d) Rama Q negativa.

A.8 Conclusiones

El objetivo de esta tesis es analizar cómo se comportan los circuitos analógicos de RF en entornos de alta radiación ambiental. Con el fin de alcanzar este objetivo, el primer paso consiste en estudiar estos entornos, las fuentes de radiación y los efectos que tienen en dispositivos electrónicos. En esta tesis se han estudiado las distintas fuentes de radiación existentes, destacando entre ellas los cinturones de Van Allen, los cuales representan zonas en la magnetosfera de la Tierra en las que han quedado atrapadas partículas ionizantes.

En cuanto a los efectos de la radiación en sistemas electrónicos, existen tres tipos principales: activación por reacciones nucleares, daños por desplazamiento y los efectos ionizantes. En esta tesis, se ha puesto el foco en estos últimos. Los efectos ionizantes ocurren cuando una partícula ionizante impacta en un dispositivo semiconductor y genera pares electrón-hueco. Este evento es el origen tanto de los efectos de dosis total de ionización (TID) como de los efectos de eventos singulares (SEEs).

Una vez han sido estudiados los efectos y las fuentes de radiación, se han analizado los efectos de la radiación en dispositivos CMOS. Tal y como se ha comentado, es posible reducir considerablemente el coste de desarrollar sistemas electrónicos al utilizar procesos CMOS. En esta tesis se ha utilizado la herramienta TCAD *Sentaurus* para modelar los transistores CMOS y realizar simulaciones de impactos de

iones pesados. Los resultados obtenidos en estas simulaciones se han incluido posteriormente en simulaciones con la herramienta ADS para la simulación de circuitos electrónicos. De esta manera se combina la precisión del simulador de dispositivos con la rapidez de las simulaciones realizadas en el simulador de circuitos.

En esta tesis se ha modelado un transistor NMOS de un proceso CMOS de 0,18 μm. Los resultados de simular el efecto del impacto de un ion pesado en este transistor muestran que la corriente de drenador aumenta a medida que lo hace el LET y la profundidad de penetración en el dispositivo, ya que la cantidad de pares electón-hueco generados es mayor. En cuanto al ángulo de incidencia, se obtienen mayores corrientes de drenador cuando se genera el máximo número de pares electrón-hueco en las uniones $n-p$ polarizadas en inversa.

Tal y como se ha mencionado, también se ha estudiado el efecto de la radiación en transistores AlGaN/GaN sobre zafiro. De manera similar al caso del transistor CMOS, la corriente en el drenador aumenta a medida que lo hace la profundidad de penetración de la partícula ionizante en el dispositivo. Cabe destacar que en esta tesis se ha modelado la respuesta de la densidad de corriente del drenador de un transistor GaN. Para ello se ha desarrollado una ecuación basada en tres funciones exponenciales. Cada una de estas exponenciales representa un mecanismo que contribuye a la densidad de corriente obtenida.

Tras analizar la respuesta frente a la radiación de los transistores CMOS, se ha estudiado el comportamiento de LNAs con la presencia de SETs. Concretamente, se ha diseñado un LNA en configuración surtidor-común y otro con una estructura puerta-común. Se han introducido los pulsos de corriente obtenidos en la herramienta TCAD en los nodos críticos de los circuitos. Los resultados obtenidos indican que las redes de polarización son los nodos más vulnerables de estos circuitos. Con el fin de mitigar los efectos de los SETs, se han implementado técnicas RHBD en estos nodos. En este caso, las técnicas implementadas se basan en la reducción de los picos de tensión al incrementar la constante de tiempo en estos nodos incluyendo resistencias y condensadores.

Por último, se ha analizado el comportamiento de distintos receptores de RF bajo los efectos de la radiación. Concretamente, se ha estudiado el impacto de los pulsos generados en los LNAs en el resto de circuitos del receptor. Para ello, se han diseñado tres receptores para estándares de bajo consumo, uno basado en una arquitectura *low-IF* convencional y dos en arquitecturas basadas en la reutilización de corriente. Con el fin de comprender cómo pueden afectar los pulsos generados en el LNA al resto de circuitos, primero se ha realizado un análisis de cómo afectan estos pulsos en mezcladores y filtros. Tras esto, se han analizado los tres receptores diseñados. En esta tesis se propone un procedimiento para realizar este análisis en el cual se observa la señal de tensión en distintos nodos de la cadena de recepción. En este caso, los tres receptores muestran un comportamiento similar en términos de variación de amplitud y fase.

Appendix **B**

APPENDIX B: PUBLICATIONS

In this appendix, a list of journal and conference publications directly related to this research work is presented. Additionally, contributions related to other research works are listed in this appendix.

B.1 Publications directly related with this dissertation

B.1.1 Journal Publications

J.1 **S. Mateos-Angulo**, D. Mayor-Duarte, M. San-Miguel-Montesdeoca, S.L. Khemchandani and J. del Pino, "Single Event Transients in an IEEE 802.15.4 Receiver for Wireless Sensor Networks", *IEEE Sens. J.*, **Submitted** & **under reviewing process**.

J.2 **S. Mateos-Angulo**, R. Rodríguez, J. del Pino, B. González and S.L. Khemchandani, "Single event effects analysis and charge collection mechanisms on AlGaN/GaN HEMTs", *Semicond. Sci. Technol.*, vol. 34, 035029, Feb. 2019.

J.3 **S. Mateos-Angulo**, M. San-Miguel-Montesdeoca, D. Mayor-Duarte, S.L. Khemchandani and J. del Pino, "SET analysis and radiation hardening techniques for CMOS LNA topologies", *Semicond. Sci. Technol.*, vol. 33, 085010, Jul. 2018.

B.1.2 Conference Contributions

C.1 G. Ojeda-Rodríguez, M. San-Miguel-Montesdeoca, D. Mayor-Duarte, **S. Mateos-Angulo**, S.L. Khemchandani and J. del Pino, "An Enhanced Current Reuse RF Receiver Front-End for the IEEE 802.15.4 Standard", emphConference on Design of Circuits and Integrated Systems, DCIS 2017, Barcelona, Spain, Nov. 22-24, 2017.

C.2 **S. Mateos-Angulo**, M. San-Miguel-Montesdeoca, D. Mayor-Duarte, S.L. Khemchandani and J. del Pino, "SET Analysis and Radiation Hardening Approaches for Different LNA Topologies", *41st WOCSDICE- Workshop on Compound Semiconductor Devices and Integrated Circuits held in Europe*, Las Palmas de Gran Canaria, Spain, May 22-24, 2017.

C.3 **S. Mateos-Angulo**, M. San-Miguel-Montesdeoca, S.L. Khemchandani and J. del Pino, "Single-Event Effects Analysis Using TCAD and Circuit-Domain Combined Simulations", *Biannual European-Latin American Summer School on Design, Test and Reliability (BELAS)*, Rotterdam, Netherlands, May 08-10, 2017.

C.4 **S. Mateos-Angulo**, D. Mayor-Duarte, M. San-Miguel-Montesdeoca, S.L. Khemchandani and J. del Pino, "Single-Event Effects Sensitivity Analysis of a 0.18 μm CMOS Low-Noise Amplifier", emphConference on Design of Circuits and Integrated Systems, DCIS 2016, Granada, Spain, Nov. 23-25, 2016.

C.5 **S. Mateos-Angulo**, D. Mayor-Duarte, S.L. Khemchandani and J. del Pino, "A Low-Power Fully Integrated CMOS RF Receiver for 2.4-GHz-band IEEE 802.15.4 Standard", emphConference on Design of Circuits and Integrated Systems, DCIS 2015, Estoril, Portugal, Nov. 25-27, 2015.

B.2 Other Publications

B.2.1 Journal Publications

J.1 V. Díez-Acereda, S.L. Khemchandani, J. del Pino and **S. Mateos-Angulo**, "RHBD Techniques to Mitigate SEU and SET in CMOS Frequency Synthesizers", *Electronics*, 8, 690, Jun. 2019.

J.2 J. del Pino, S.L. Khemchandani, **S. Mateos-Angulo**, D. Mayor-Duarte and M. San-Miguel-Montesdeoca, "Area Efficient Dual-Fed CMOS Distributed Power Amplifier", *Electronics*, vol. 7, 139, Aug. 2018.

J.3 D. González, S.L. Khemchandani, J. del Pino, D. Mayor-Duarte, M. San-Miguel-Montesdeoca, **S. Mateos-Angulo**, "Single event transients mitigation techniques for CMOS integrated VCOs", *Microelectronics Journal*, vol. 73, pp. 37-42, Mar. 2018.

B.2.2 Conference Publications

C.1 M. San-Miguel-Montesdeoca, D. Mayor-Duarte, **S. Mateos-Angulo**, S.L. Khemchandani and J. del Pino, "A Ku-Band SSB Subharmonically Pumped

Mixer designed using a 100nm GaN-on-Si process", emphConference on Design of Circuits and Integrated Systems, DCIS 2018, Lyon, France, Nov. 14-16, 2018.

C.2 D. Mayor-Duarte, A. Cruz-Ramón, M. San-Miguel-Montesdeoca, **S. Mateos-Angulo**, S.L. Khemchandani and J. del Pino, "A CMOS Programmable Gain Amplifier for 2.4-GHz-band IEEE 802.15.4 Standard", *Conference on Design of Circuits and Integrated Systems, DCIS 2016*, Granada, Spain, Nov. 23-25, 2016.

C.3 M. San-Miguel-Montesdeoca, **S. Mateos-Angulo**, D. Mayor-Duarte, S.L. Khemchandani and J. del Pino, "A Low-Power Fully Integrated CMOS RF Transmitter for 2.4-GHz-band IEEE 802.15.4 Standard", *Conference on Design of Circuits and Integrated Systems, DCIS 2016*, Granada, Spain, Nov. 23-25, 2016.

In the following pages, the two already published journal papers directly related to the research presented in this dissertation are attached.

IOP Publishing Semiconductor Science and Technology
Semicond. Sci. Technol. **34** (2019) 035029 (8pp) https://doi.org/10.1088/1361-6641/ab058a

Single event effects analysis and charge collection mechanisms on AlGaN/GaN HEMTs

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Abstract

This paper focuses on the effect of single event transients on AlGaN/GaN on sapphire high-electron-mobility-transistors (HEMTs). This results in a novel study in high performance transistors using sapphire substrate. Technology computer aided design tools are used in order to perform the radiation simulations, once the DC response of the transistors have been reproduced. Results show the relationship of the drain current density with ion energy and angle of incidence. The current increases as the ion penetrates deeper in the device due to higher energies, while it decreases as the angle increases. To our knowledge, angle strikes have never been studied before in AlGaN/GaN HEMTs. Several charge collection mechanisms are discussed and their relationships with ion energy and angle of incidence are established.

Keywords: AlGaN/GaN, SET, TCAD, heavy-ion, electron-hole pair, charge collection

(Some figures may appear in colour only in the online journal)

1. Introduction

Gallium nitride (GaN) technology has been identified as a promising one for space applications due to its inherently radiation hard nature [1, 2]. However, it is important that the reliability limits of the technology are understood before using GaN in this environment. Several studies have focused on the accumulative dose effects on GaN transistors, concluding on the high tolerance of the technology to these effects [3–5].

Nevertheless, other studies have shown the vulnerability of GaN transistors to single-event effects (SEE), which represent one of the biggest issues in space electronics. SEEs are caused when a charged particle impacts a vulnerable node of an integrated circuit. Bazzoli *et al* provides results that commercial GaN transistors are not sensitive to single-event burnout (SEB). However, a phenomenon similar to single-event gate rupture (SEGR) was observed [6]. Rostewitz *et al* studies both SEB and single-event transients (SET) on DC and RF operated AlGaN/GaN high-electron-mobility-transistors (HEMTs), concluding on the vulnerability of this technology to the mentioned effects [7]. Kuboyama *et al* indicates that different damage modes occur in AlGaN/GaN HEMTs when irradiated with heavy ions [8]. Zerarka *et al* analyses SEEs in commercial normally-off GaN power transistors, using a technology computer aided design (TCAD) simulator [9]. This kind of simulator is extensively used in the study and modeling of SEEs in different technologies [10–12]. A thorough study is performed where the case of ions vertically generated in the volume of the transistors at different positions is analyzed. The cases of different track lengths and different linear energy transfers (LET) are also analyzed.

In this work, a detailed of the effect of SETs on RF AlGaN/GaN HEMTs on sapphire HEMTs is performed. To our knowledge, this type of study has never been performed before on transistors using a sapphire substrate. AlGaN/GaN HEMTs are commonly used in the design of RF integrated circuits, such as low noise amplifiers and power amplifiers. In these circuits, the transistor is biased by setting both the gate

and drain voltages. This differs from the biasing done in [9], where only the drain voltage is fixed since power switching transistors are used. Additionally, in this type of transistor it is important to study effects such as SEB or SEGR, while in RF circuits it is paramount to study the propagation of the disturbances caused by ion strikes. The electron-hole pairs generated by these strikes can result in transient pulses that could propagate to other circuits in the RF chain. This temporary voltage or current disturbance at a circuit node is a SET [13].

A model for SETs that is extensively used in the literature consists in transient double exponential current pulses at sensitive nodes [14]:

$$I_{\text{rad}} = \frac{Q}{t_f - t_r}(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}}), \quad (1)$$

where Q represents the collected charge, t_f the fall time and t_r the rise time.

In this paper, the Sentaurus TCAD tool by Synopsys has been used to perform single-event simulations under different conditions (different strike locations, energy and angle), once the DC response of the transistors has been reproduced. With the results obtained from these simulations, a more accurate model is proposed.

Additionally, the effect of angled heavy ion strikes has been analyzed. To our knowledge, this effect has never been studied before in AlGaN/GaN HEMTs.

The device structure of the transistor, as well as the DC characterization, is presented in section 2. Section 3 describes the single-event simulations performed using both the stopping and range of ion in matter (SRIM) tool, which is used to study the behavior of ions as they traverse through matter, and the TCAD simulator. Charge collection mechanisms are discussed in section 4. Finally, some conclusions are given in section 5.

2. AlGaN/GaN on sapphire HEMTs

In this section we characterize, experimentally and numerically, the DC performance of AlGaN/GaN on sapphire HEMTs.

2.1. Structure

The AlGaN/GaN HEMTs structure used in this study was grown through the [0001] direction (wurtzite) on 330 μm thick sapphire. The layout (typical for microwave design, also valid for DC performance) and layer stack are shown in figures 1(a) and (b), respectively. It consists of a 3 μm thick GaN buffer and a 19 nm thick $Al_{0.3}Ga_{0.7}N$ barrier, unintentionally doped. The 2DEG concentration in the channel is modulated by a Schottky gate, which is 2 μm long and 300 μm wide.

Source and drain terminals are 4 and 10 μm distanced, respectively, from the gate borders, with a donor concentration of 10^{20} cm^3 extended down to the GaN channel.

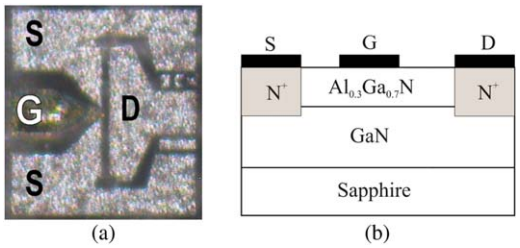

Figure 1. AlGaN/GaN HEMT (a) layout and (b) device structure.

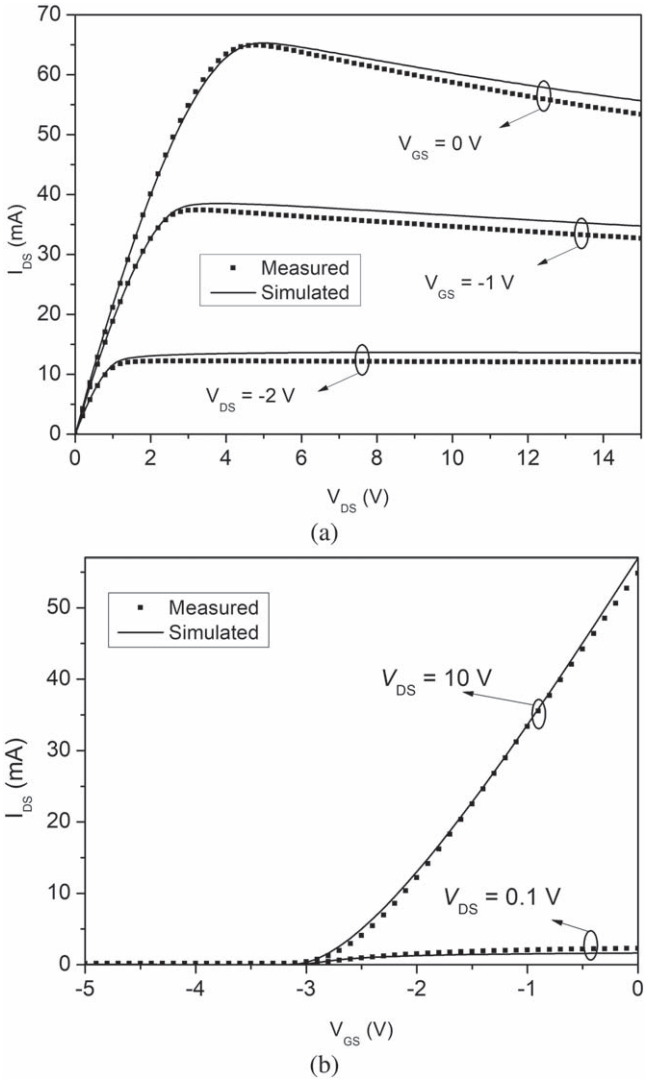

Figure 2. Measured (a) output characteristics and (b) transfer characteristics.

Corresponding measured output and transfer characteristics are shown in figures 2(a) and (b), with symbols, respectively.

2.2. Numerical simulations

Numerical simulations have been developed with Sentaurus Device TCAD tool [15]. The impact of SHEs on the transistor DC response has been in-depth analyzed by auto consistently solving the heat flow equation together with the Poisson and

drift-diffusion equations, as in [16], polarization charges [17], and the rest of physical parameters from [18]. Thermionic-emission is considered for all interfaces [19], and for the particular case of the gate contact, a Schottky diode with Poole–Frenkel emission is considered [20].

To be able to take into account effects such as gate-lag and modulation of the ON resistance of the transistor, due to the presence of traps in different locations, two main trapping centers have been considered. Firstly, traps on the top of the AlGaN barrier with a donor sheet concentration of $2.3 \times 10^{13}\,\mathrm{cm}^{-2}$ and an activation energy from the center of the band gap of 0.4 eV. Secondly, acceptor traps in the GaN buffer, with a concentration of $5 \times 10^{16}\,\mathrm{cm}^{-3}$ and an activation energy from the valence band maximum of 0.368 eV [21]. These effects are neglected in DC characteristics, but they can be considerable in transient operation mode, which is the aim of this work [22].

In addition, to set the threshold voltage, no fitting for the polarization charge is needed when traps under the gate are determined [23], as they (in volume) can modify the Fermi level position in the energy band diagram, or (when superficial) produce a straight on threshold voltage displacement [24]. For the HEMT under consideration, a layer 2 nm deep of donor traps just below the gate terminal, with an activation energy from the conduction band minimum of 0.2 eV, and capture cross-section of $10^{-15}\,\mathrm{cm}^{-2}$, is assumed. All of these considerations result in the simulated curves depicted in figure 2.

3. Single-event simulations

In order to perform the single event simulations, it is important to know how the ion behaves as it penetrates the device. To do so, the SRIM code was used [25]. This way, the track created by the ion is obtained. This information is later imported into the TCAD tool.

3.1. SRIM simulations

The impact of an oxygen ion with different energies on a AlGaN/GaN device was simulated. It should be noted that, in this case, a target device composed of three layers (Si_3N_4, AlGaN and GaN) was generated, following the dimensions of the transistor presented in section 2.

The LET can be calculated with the SRIM tool considering the energy loss in the device due to ionization and the density of the target material. This tool allows us to simulate the impact of different elements on a target device. Thus, a study of how different elements impact an AlGaN/GaN device was performed. Their LET versus depth curves are shown in figure 3.

Considering that all strikes were simulated with the same ion energy (2 MeV), it can be seen that the penetration depth is inversely proportional to the atomic number. This is explained by the fact that a smaller ion results in less collisions with the lattice structure of the device, which slow down the ion.

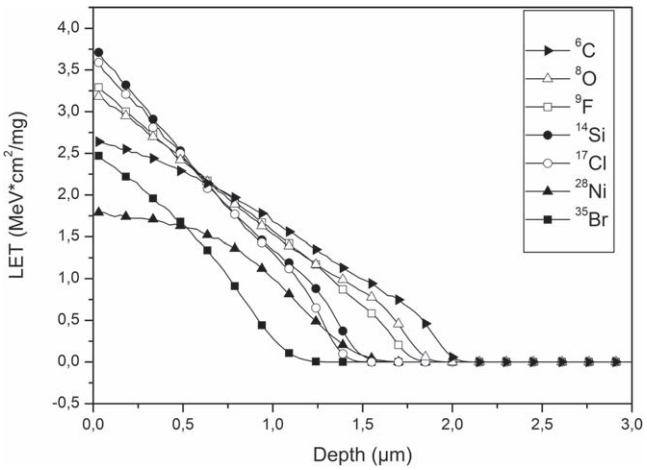

Figure 3. LET versus depth for different elements in GaN.

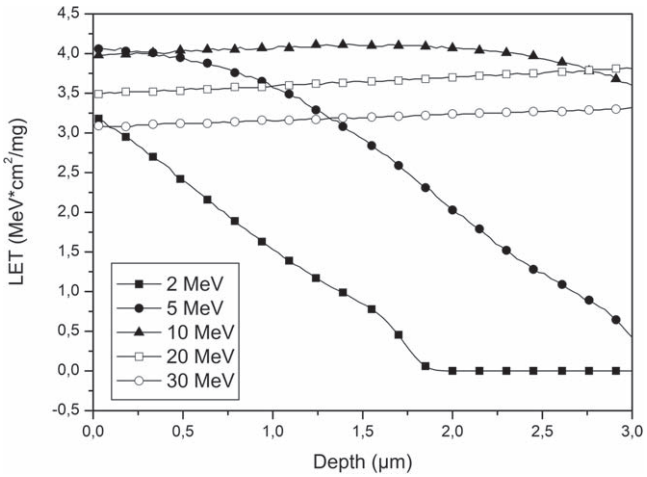

Figure 4. LET versus depth for different energies of oxygen ions in GaN.

Regarding the effect of the ion energy, the LET versus depth curves for different energies of oxygen ions are shown in figure 4.

It is known that a high-energy heavy-ion track can be modeled with constant LET, while the LET of low-energy ions varies significantly along their track and their track lengths are shorter [26]. This is confirmed by the curves displayed in figure 4, where it can be seen that for low energies (2 and 5MeV) the LET varies with the depth, while for higher energies (10, 20 and 30 MeV) the LET remains almost constant. Additionally, it can be observed that the maximum LET value is achieved for an energy of 10 MeV, when a Bragg peak appears if LET is represented against the energy the ion has before the impact, as shown in figure 5.

Additionally, the effect of the angle of incidence was studied using the SRIM tool. The angle θ corresponds to the angle of incidence from the normal. As seen in figure 6, the penetration depth is deeper for smaller angles of incidence. Regarding the LET, the area under each curve should be the same since the same ion energy is used for each case. Therefore, for bigger angles the ionization occurs in the first

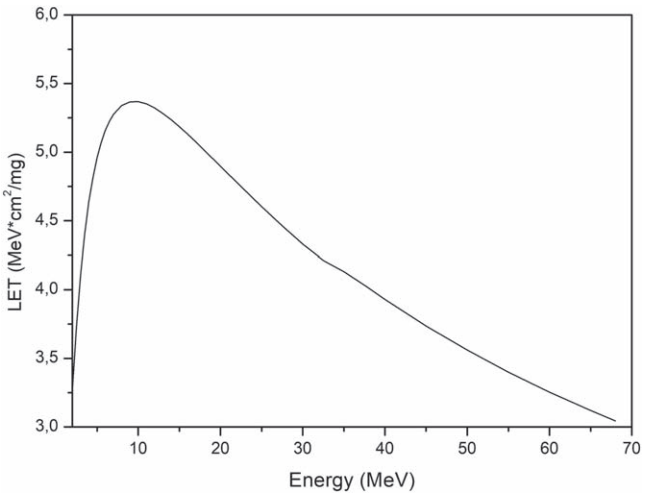

Figure 5. LET versus energy for oxygen ions in GaN.

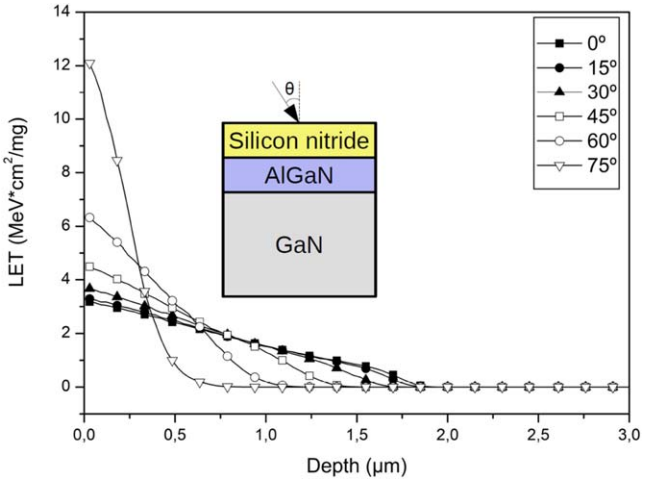

Figure 6. LET versus depth for different angles of incidence of oxygen ions in GaN.

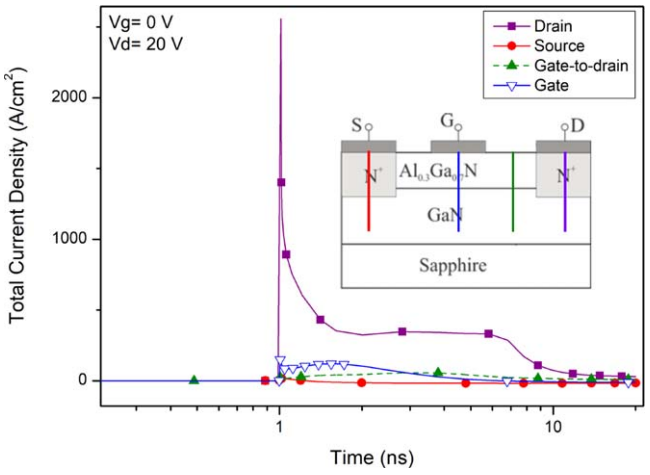

Figure 7. Drain current density over time of heavy ion strikes at different positions.

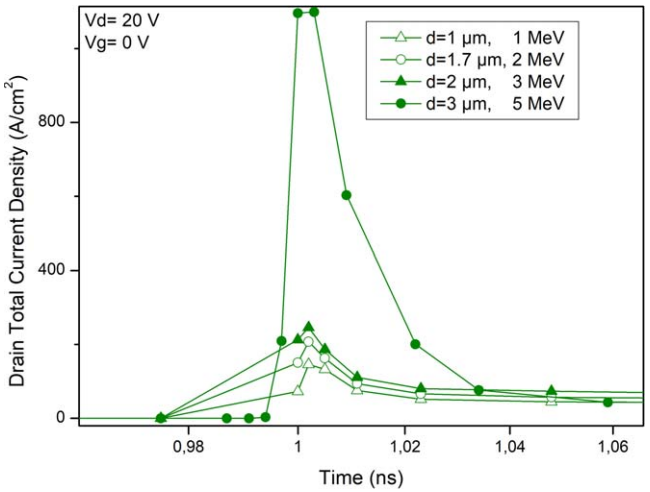

Figure 8. Drain current density over time for ion strikes on the depletion region with different penetration depth.

micrometers of the device while for smaller angles the same ionization is distributed along the depth of the device.

3.2. TCAD simulations

The Sentaurus TCAD tool presents various radiation models which simulate the effect of a high-energy particle impinging on a semiconductor device [15]. A commonly used model to perform SET simulations is the heavy ion model [27, 28]. When a heavy ion passes through a device, it loses energy and creates electron-hole pairs. These pairs could generate large enough currents which can translate into SETs.

In this paper, transient simulations were performed for different locations, depths, LET and direction values, keeping the characteristic distance and time constant, with the transistor operating in saturation region (with $V_g = 0$ V and $V_d = 20$ V, which are typical bias values for RF circuits). In this section, all simulations were performed using the track information obtained in the SRIM simulations when the target device is impacted with an oxygen ion. Specifically, the LET function, penetration depth of the heavy ion in the device and characteristic distance parameters are obtained from the SRIM simulations.

Figure 7 shows the drain current density for ion strikes at different points of the transistor. It can be seen that the highest drain current density is obtained when there is a strike at the drain, as expected. The lowest current is achieved when there is a strike at the source of the transistor. This can be explained by the fact that this is the contact further away from the drain and, therefore, the generated electron-hole pairs due to the strike recombine before reaching the drain. Taking this into account, it would be expected for the drain current density to be larger when there is a strike in the gate-to-drain region compared to a strike in the gate. However, the opposite occurs since the generated current due to the strike at the Schottky gate reaches the drain through the transistor's channel.

Regarding the penetration depth of the particle in the device, the energy of the ion before impacting the device must be considered. The bigger the energy, the deeper the ion will penetrate in the device. Figure 8 shows the drain current density for ion strikes on the gate-to-drain region with different penetration depth (d).

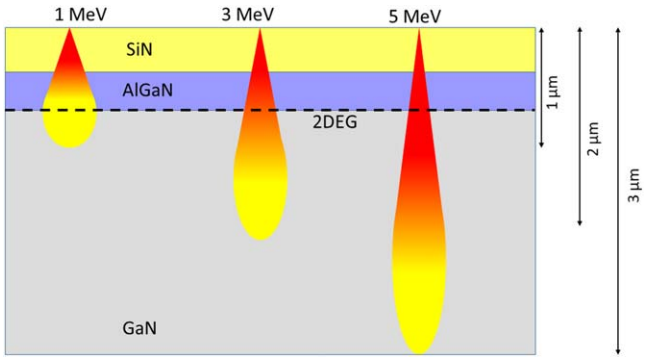

Figure 9. Illustration of different energy ions impacting on a GaN device.

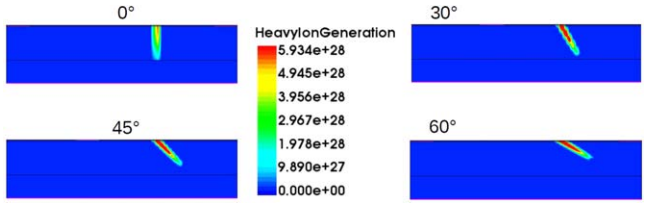

Figure 10. Electron-hole pair generation rate for different angle values.

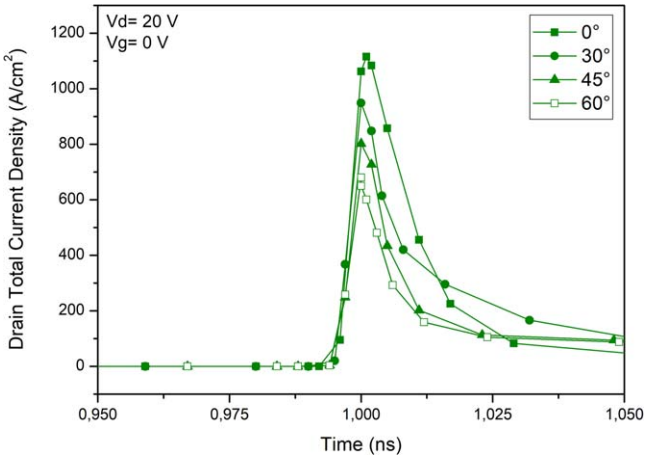

Figure 11. Drain current density over time for ion strikes with different angles of incidence.

It can be seen that the drain current density increases as the ion penetrates further in the device. This is explained by the fact that a higher energy ion results in more ionization produced in the transistor, including in the 2DEG zone, as seen in figure 9.

Similarly, as in the SRIM simulations, the effect of the angle of incidence was studied with the TCAD tool. To do so, the direction of the heavy ion model was modified. The angle of incidence from the normal (θ) ranges from 0° to 60°. Figure 10 shows the electron-hole pair generation rate for different θ values, at the strike instant of a 5 MeV oxygen ion on the gate-to-drain region.

The curves in figure 11 depict an inversely proportional relationship between drain current density and angle of incidence. Hence, the drain total current density decreases for bigger angles, when the recombination of electron-hole pairs enhances. In the case of a vertical strike ($\theta = 0°$) the longitudinal electric field produces carrier trajectories non coincident. However, as the angle of incidence increases, the carrier trajectories coincidence grows and recombination is augmented.

4. Discussion

The SET response of the AlGaN/GaN HEMT transistor can be modeled following equation (2) for the drain current:

$$I_D = \sum_{n=1}^{3} \frac{Q_n}{t_{fn} - t_{rn}} \cdot \left(e^{-\left(\frac{t}{t_{fn}}\right)} - e^{-\left(\frac{t}{t_{rn}}\right)}\right), \qquad (2)$$

where Q_n represents the collected charge, t_{fn} the fall time and t_{rn} the rise time. The model is composed of three exponential functions. The first of them simulates the effect of a heavy ion striking the device, which results in the generation of electron-hole pairs. The electrons are collected quickly at the drain (due to a drain voltage of 20 V) and is modeled by the first term ($n = 1$). This leads to an excess of holes in the GaN buffer layer. It should be noted that a parasitic biploar transistor appears due to the *n–p–n* junction formed by the source, the excess of holes and drain. These positive charges lower the potential barrier between the source and the channel, leading to additional injections of electrons, which are collected at the drain. Thus, a diffusion-mechanism from the source (the emitter of the parasitic bipolar transistor) to the excess of holes (the base of the parasitic bipolar transistor) is originated. The derived current is modeled by the second term ($n = 2$). Additionally, a long-term drift-mechanism from the source to the channel (back-channel effect) produces the current modeled by the third term ($n = 3$) [29]. Figure 12 shows the model compared to the curves generated with Sentaurus, presented in figure 8.

The effect of the energy of the ion on the collected charge can be studied using this model. The curves shown in figure 8 have been replicated and the resulting values of the model parameters are shown in table 1:

In order to correctly study the effect of the energy on the collected charge, all rise and fall times, t_{f1}, t_{r1}, t_{f2}, t_{r2}, t_{f3} and t_{r3}, are kept constant and equal to 0.0115, 0.005, 0.65, 2, 0.1 and 90 ns, respectively. Taking this into account, it can be seen that both Q_1 and Q_2 increase as the energy increases, as expected. If the ion impacts the device with higher energy, more electron-hole pairs are generated, which results in higher collected charges Q_1 and Q_2. However, regarding Q_3, as it is related to the back-channel effect, which is a long-term charge enhancement, it can be assumed constant and small [29]. Figure 13 shows how Q_1 and Q_2 increase linearly with the energy. The obtained Q_1 and Q_2 values are transistor dependant, since the doping and dimensions of the transistor affect the collected charge and current generated by a heavy ion strike.

Regarding the effect of angled strikes on the collected charge, for an energy of 5 MeV, table 2 shows the resulting

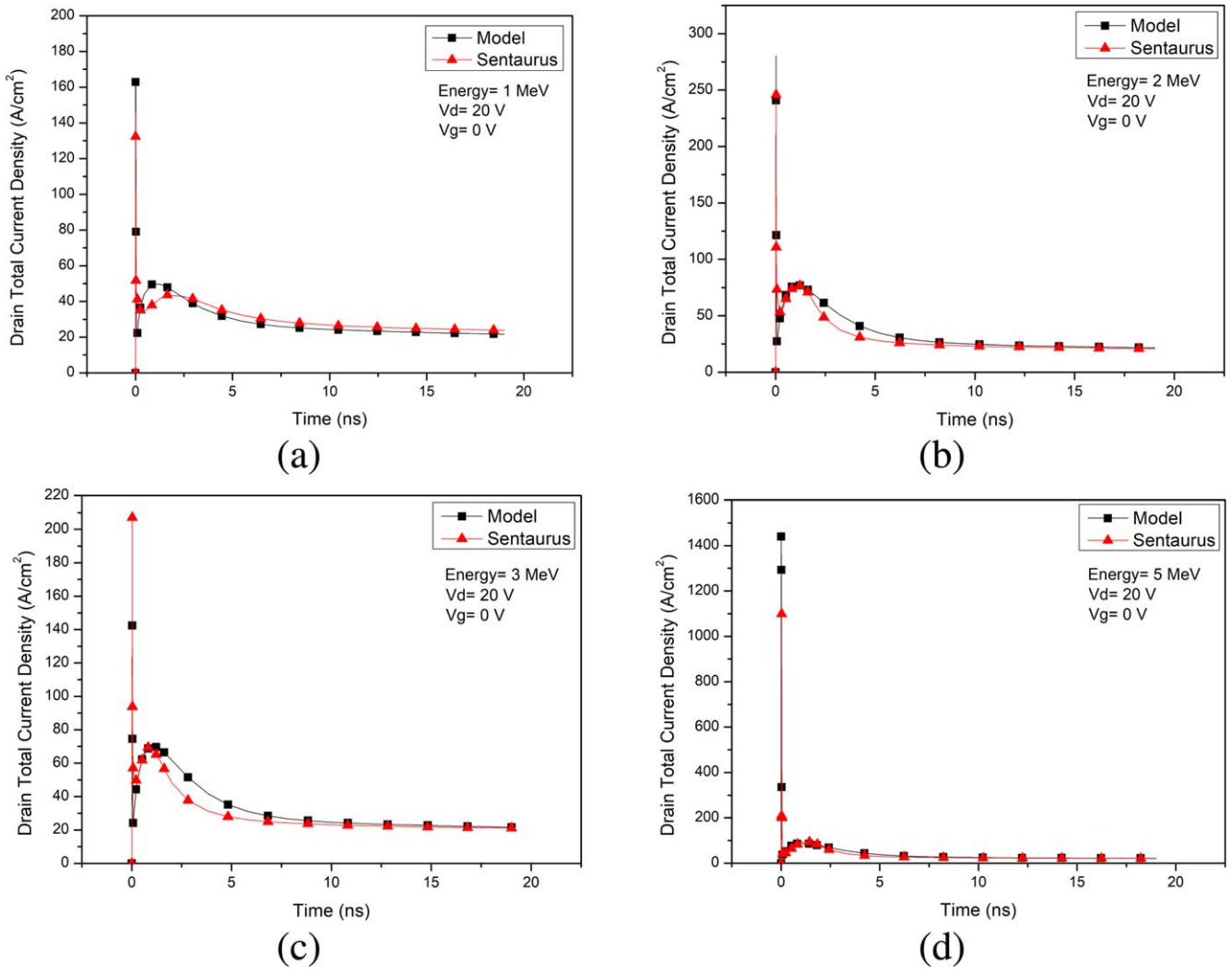

Figure 12. Modelling of different energy ion strikes on the gate-to-drain region (a) 1 MeV (b) 2 MeV (c) 3 MeV (d) 5 MeV.

Table 1. Model parameter values for different energies.

Energy (MeV)	1	2	3	5
Q_1 (nC)	3.75	9.5	16.5	28
Q_2 (nC)	130	150	175	220
Q_3 (nC)	120	120	120	120

model parameter values for different angles once the curves in figure 11 have been replicated. As in the previous case, all rise and fall times are kept constant and with the same values. Figure 14 shows how Q_1 and Q_2 behave for different angles of incidence.

As it can be seen, Q_1 decreases as the angle of incidence increases. This is in agreement with the results shown in the previous section (figure 11). However, Q_2 follows the opposite behavior, since the base of the parasitic bipolar transistor (the excess of holes) is deeper located as the angle of incidence decreases, thus reducing the diffusion-mechanism transport. Therefore, the second charge collection mechanism is larger in the case of larger angles of incidence.

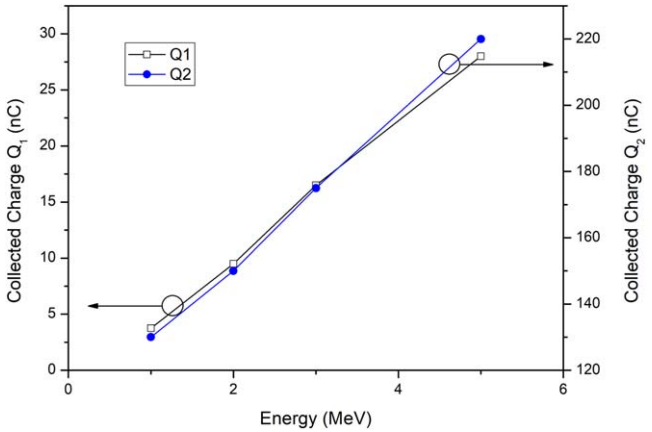

Figure 13. Q_1 and Q_2 versus energy ion strike.

5. Conclusions

The effect of SETs on AlGaN/GaN on sapphire HEMTs has been studied. To do so, the Sentaurus TCAD tool has been used. Oxygen ion impacts were simulated for different locations, depths, LET and direction values. Simulation results

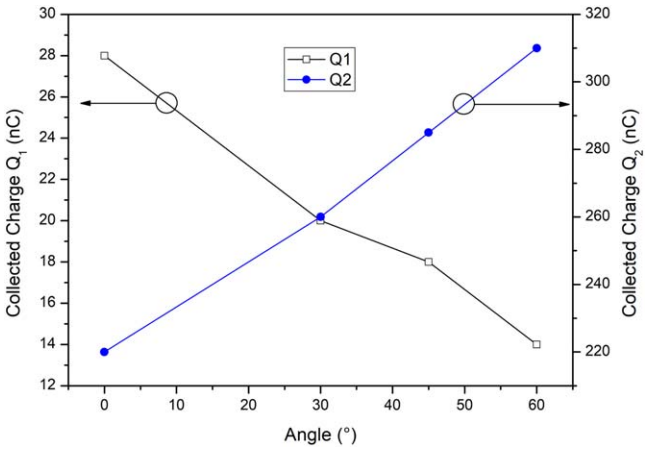

Figure 14. Q_1 and Q_2 versus angle of incidence.

Table 2. Model parameter values for different angles.

Angle (°)	0	30	45	60
Q_1 (nC)	28	20	18	14
Q_2 (nC)	220	260	285	310
Q_3 (nC)	120	120	120	120

show that the drain current density increases as the ion penetrates further in the device. This can be explained by the fact that a higher energy ion results in a deeper penetration and more ionization produced in the transistor, including in the 2DEG zone. Additionally, the drain total current density decreases for bigger angles since as the angle of incidence increases, so does the recombination of electron-hole pairs. The single event response of AlGaN/GaN HEMTs has been modeled using a combination of three exponential functions, each simulating a charge collection mechanism. The first of them simulates the electrons collected quickly at the drain when electron-hole pairs are generated after an ion strike. This leaves an excess of holes in the GaN buffer layer which leads to the other two charge collection mechanisms. Firstly, electrons are injected from the source of the transistor and travel by diffusion to the excess of holes and are collected by the drain. The last mechanism refers to the back-channel effect which is a long-term drift mechanism. Simulation results show that the collected charge increases as the ion energy increases, since more electron-hole pairs are generated. As for the effect of angled strikes in the collected charge, the second mechanism is lower in the case of lower angles of incidence due to the fact that the excess of holes is deeper located, therefore reducing diffusion-mechanism transport.

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SET analysis and radiation hardening techniques for CMOS LNA topologies

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Abstract

This paper analyses the effects of single-event transients (SETs) on CMOS low noise amplifiers (LNA) designed for a 0.18 μm technology. Two well-known topologies, the common-source and common-gate cascodes, have been analysed when heavy ions strike the most sensitive nodes of these structures. In order to simulate these strikes both a physics-based technology computer aided design (TCAD) tool and an electrical circuit domain simulator have been used. This way the physics information given by the TCAD tool is combined with the fast transient simulations performed in circuit simulators. To study their SET performance, the maximum voltage peak and the recovery time of the output signal were calculated for both LNAs. Additionally, a safe operating area can be defined, setting the boundaries for acceptable SETs. Radiation hardening by design techniques have been applied at the most vulnerable nodes of both LNAs. The proposed mitigation approaches make both LNAs hardened against radiation, considerably improving their SET performance.

Keywords: SET, TCAD, low noise amplifier (LNA), radiation hardened by design, heavy ion, recovery time, CMOS

(Some figures may appear in colour only in the online journal)

1. Introduction

Recently, radiation tolerance in circuits has become a relevant topic in the field of nanoelectronic systems design. Circuits used in space applications have conventionally been implemented in radiation hardened technologies such as III–V technologies, silicon-germanium (SiGe) or silicon-on-insulator (SOI). However, thanks to CMOS technologies, cost reduction can be achieved by using cheap devices with minimum size and weight, besides operating at low power [1]. Indeed, a special hot topic nowadays is using commercial-off-the-shelf (COTS) parts to enable low-cost missions [2]. Despite these advantages, CMOS technologies are vulnerable to radiation effects even at terrestrial level, thus affecting circuits that are used in many applications apart from space-intended devices, such as medical and military equipment, nuclear plant control systems, etc. Furthermore, the technology scaling has increased the probability of faults when the circuits are exposed to ion radiation [3].

Single-event effects (SEEs) are one of the greatest liabilities in CMOS devices [4]. These effects are generated when an energetically charged particle strikes a sensitive region in an integrated circuit. The resulting electron–hole pair generation caused by these strikes can produce transient pulses that could propagate to other areas of the circuit generating single-event upsets. This temporary voltage or current disturbance at a circuit node is called a single-event transient or SET [5].

This effect has been mainly studied in digital circuits [3–10], while analogue and mixed-signal circuits are yet to be thoroughly analysed under high-radiation environments. This paper focuses on the study of SETs in analogue radio frequency (RF) circuits, as well as proposing radiation hardening by design solutions. These circuits were implemented in a UMC 0.18 μm CMOS technology.

Usually, in order to carry out SET analyses, experimental measurements are performed in laboratories equipped with laser beam testing and other ion-inducing devices [1, 11].

However, this equipment will mean high costs both financially and time-wise. As an alternative, simulation tools allow researchers to predict the behaviour of analogue circuits in harsh environments. A practical way to analyse the effect of SETs in circuits is to perform transient simulations. Despite the time required for this kind of studies [1], these simulations give an approximation of how the circuit's parameters are affected without needing to carry out expensive experimental measurements using heavy ion or laser strikes.

In CMOS circuits, the effects of SETs are usually simulated with a current source connected at the drain of the transistors [12]. Typically, the current pulse generated by this source follows a double-exponential function:

$$I_{\text{rad}} = \frac{Q}{t_f - t_r}(e^{-\frac{t}{t_f}} - e^{-\frac{t}{t_r}}), \quad (1)$$

where Q is the collected charge, while t_f and t_r are the fall and rise time, respectively. This current pulse is introduced in an electrical circuit domain simulation tool, where transient simulations are performed.

However, in order to obtain a more accurate model of this double-exponential function, a technology computer aided design (TCAD) physics-based software can be used [13]. It is known that these tools provide the means to simulate the effects of radiation on physics parameters of semiconductor devices and are widely used to predict the response of these devices to incident radiation.

In [14] a review of techniques for physics-based device-level simulation of SEEs in silicon based microelectronic devices and integrated circuits is given. It is known that the simulation of radiation effects can be approached at different levels: (1) interaction of ionising particles with matter, (2) physical device simulators that estimate the response of devices to incident radiation, (3) circuit simulators that model circuit response to a single-event and (4) codes that predict the error rate that will be observed. The physics-based device simulators typically follow the drift-diffusion models, where the Poisson and the current continuity equations are discretized and solved on a mesh using finite-element techniques. Due to the computational efficiency of these models, the physics-based device simulators have become a very popular simulation tool, even for deep submicron devices.

In [15] TCAD simulations are performed to investigate the effects of SETs in SOI RF CMOS technologies. In this case, the *Synopsys Sentaurus* TCAD tool is used to calibrate the device models and verify the results obtained in laser inducing experiments.

Studies on silicon–germanium (SiGe) heterojuntction bipolar transistors (HBTs) have proliferated in recent years [16, 17]. Similarly as in Si CMOS transistors, both bulk and silicon-on insulator (SOI), TCAD tools are also used to simulate the effects of radiation in SiGe HBT devices. These same studies can be replicated in non-silicon-based devices, like the one performed in [18], where the electrical behaviour of COTS gallium-nitride (GaN) transistors under heavy ion irradiation is studied using the *Synopsys Sentaurus* TCAD tool.

In this paper, the *Synopsys Sentaurus* TCAD tool is used to model 0.18 μm CMOS semiconductor devices and perform ion strikes simulations. The results obtained in these simulations will then be used to refine the circuit simulations performed in an electrical circuit domain simulator like *Advanced Design System* (ADS) software by *Keysight Technologies*. This way the accuracy of the device solver is combined with the fast simulations performed in the circuit simulator. This methodology has been proven by [17], where a close agreement between the simulation and experimental results is obtained. Therefore, it can be stated that the methodology presented in this reference can be applied for any other RF circuits.

Following this methodology, the effect of SETs on low noise amplifiers (LNA) is studied in this paper. Two well-known topologies, the common-source (CS) and common-gate (CG) cascodes, are analysed when a current pulse is injected in the most sensitive nodes of the circuits. Both circuits were designed for the 2.4 GHz band of the IEEE 802.15.4 standard in UMC 0.18 μm technology. Once this analysis is performed, radiation hardening by design (RHBD) techniques are presented with the goal of obtaining robust circuits against single events.

Conventionally, there are three hardening techniques which can be applied to develop extreme environment electronics: hardening by-process, hardening by-reconfiguration and hardening by design. A combination of these three techniques can be implemented in order to design robust against radiation circuits [19]. RHBD techniques have been thoroughly studied in digital circuits as a cheaper alternative compared to the other approaches. However, in analogue RF circuits these techniques are less covered in the literature.

The process followed to obtain the transistor's models in the *Synopsys Sentaurus* TCAD is explained in section 2. The two LNA topologies where the SET simulations were performed are described in section 3. Section 4 focuses on the analysis of the recovery time and maximum output voltage peak when an energetic particle strikes the most critical nodes of both circuits. Section 5 proposes radiation hardening techniques that could be applied to the LNAs in order to reduce the effect of SETs. Finally, some conclusions are given in section 6.

2. TCAD simulations

The *Synopsys Sentaurus* TCAD software is a physics-based package used for modelling semiconductor fabrication process and device electrical operation [20]. As it was stated in section 1, this type of simulation tool is widely used in order to carry out SET analyses.

2.1. Transistor modelling

The *Sentaurus Structure Editor* (SDE) tool was used to model the 0.18 μm CMOS technology transistors. This tool provides a graphical user interface which aids the design of 2D and 3D devices. The geometric shape and device parameters, such as

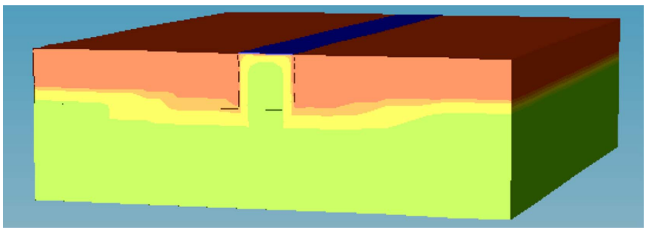

Figure 1. NMOS transistor model generated with *Sentaurus Structure Editor*.

doping concentration, can be defined with this tool [20]. The transistor sizes were obtained from the UMC technology documentation and the layout masks. Once the geometry of the transistor is defined, the doping concentration of the different regions and the mesh were specified. Figure 1 shows the electron density in the 2D extruded model of the transistor generated with SDE tool.

In order to calibrate the designed model, the characteristic *I–V* curves were calculated and compared to those given by the technology, which were obtained from the UMC design kit for ADS. To perform these electrical simulations at device-level, the *Sentaurus Device* (SDEVICE) tool was used. Figure 2 shows the drain current against the gate voltage for two different drain voltages, both in a linear and a logarithmic scale. As it can be seen, the curves generated with *Sentaurus* match with those provided by the technology. In the logarithmic scale, it can be seen that the curves slightly differ at subthreshold voltages. However, this difference is minimal and, in both LNAs presented in this paper, moderate or strong inversion regions are used.

To achieve these results, parameters like the doping concentration, electron mobility and hole mobility had to be modified. First, the threshold voltage is fixed by modifying the work function of the gate and the doping concentrations of the substrate. In this case, the substrate had a boron doping concentration of 5×10^{15} cm^{-3}, while the source and drain of the transistors were doped with a phosphorus concentration of 1×10^{20} cm^{-3}. In order to modify the work function of the gate, the parameter *Barrier* is used. Once the threshold voltage has been set, the transconductance must be modified to adjust the gradient of the curve. To do so, the Lombardi and Canali model were used to define carrier mobilities at low and high fields, respectively. After several simulations, an electron mobility of 500 cm^2 V^{-1} s^{-1} and a hole mobility of 200 cm^2 V^{-1} s^{-1} were obtained. Regarding the Canali model, the parameters β_0 and v_{sat} are used to model the transition from linear to saturation regions and the saturation velocity, respectively. In this case, a β_0 of 1.15 and a v_{sat} of 1.4×10^7 cm s^{-1} were obtained.

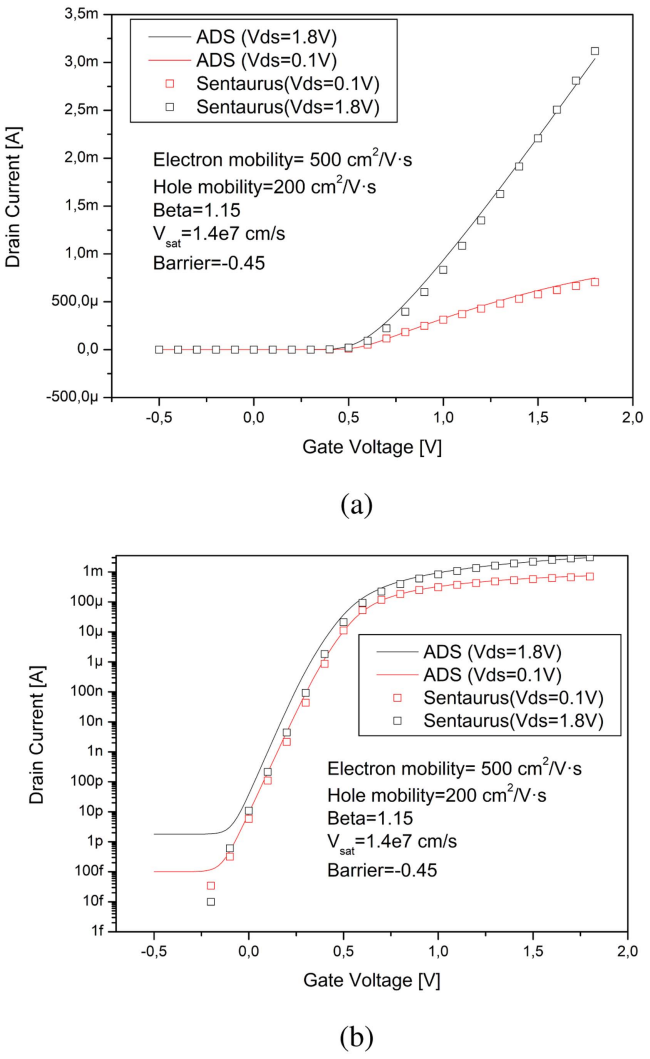

Figure 2. Gate voltage versus drain current in Sentaurus compared to the ADS model (a) linear scale (b) logarithmic scale.

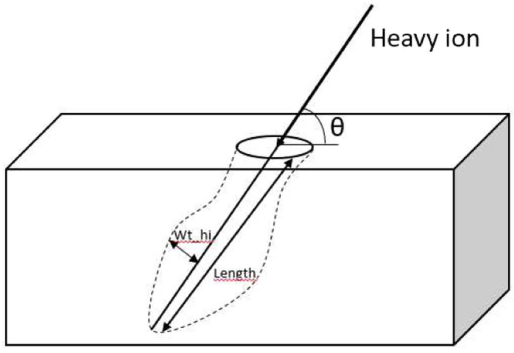

Figure 3. Heavy ion penetrating in a semiconductor device.

2.2. Heavy ion model

The SDEVICE tool presents many different radiation models which simulate the effect of a high-energy particle penetrating a semiconductor device. A commonly used model to perform SET simulations is the heavy ion model [15, 21, 22]. When a heavy ion passes through a device, it loses energy and creates electron–hole pairs. These pairs could generate large enough currents which can translate into SETs.

Some important factors that should be considered in this model are the energy of the ion, the angle of penetration or the relation between the linear energy transfer (LET) and the number of pairs created.

Figure 3 shows a simple model for the heavy ion penetration process. The generation rate caused by the pass of the ion through the device follows equation:

$$G(l, w, t) = G_{\mathrm{LET}}(l)R(w, l)T(t), \tag{2}$$

where $R(w, l)$ and $T(t)$ describe the spatial and temporal variations of the generation rate. $G_{\mathrm{LET}}(l)$ is the LET generation rate density, which represents the energy loss of a charged particle due to ionisation and excitation. $T(t)$ is defined as a Gaussian function:

$$T(t) = \frac{2 \cdot \mathrm{e}^{-\left(\frac{t-t_0}{\sqrt{2}\cdot s_{\mathrm{hi}}}\right)^2}}{\sqrt{2} \cdot s_{\mathrm{hi}}\sqrt{\pi}\left(1 + \mathrm{erf}\left(\frac{t_0}{\sqrt{2}\cdot s_{\mathrm{hi}}}\right)\right)}, \tag{3}$$

where t_0 is the instant of the heavy ion impact, s_{hi} is the characteristic value of the Gaussian and erf is the Gauss error function.

The spatial distribution $R(w, l)$ can be defined as an exponential function (4) or a Gaussian function (5):

$$R(w, l) = \mathrm{e}^{-\frac{w}{w_t(l)}}, \tag{4}$$

$$R(w, l) = \mathrm{e}^{-\left(\frac{w}{w_t(l)}\right)^2}, \tag{5}$$

where w is the perpendicular distance from the track and w_t is the characteristic distance which can be a function of the length. In this paper, the Gaussian function is used.

The parameters from the heavy ion model that can be modified in the SDEVICE tool are shown in table 1.

In this paper, transient simulations were performed for different length, LET and direction values, keeping the characteristic distance and the location constant. Regarding the location of the impact of the heavy ion, it is known that the drain of a CMOS transistor is the most sensitive area of the device [12]. In this case, the LET ranges from 1 to 30 MeV cm^2 mg^{-1}, since LETs as low as 3 MeV cm^2 mg^{-1} are capable of generating significant transients in a 0.18 μm technology [3]. Regarding the length, simulations were run for values ranging from 0.05 to 0.5 μm. Finally, the angle of incidence from the surface of the device (θ) ranges from 15° to 90°, for the cases of an ion angled towards the gate and away from the gate.

Figure 4 shows the current pulse generated at the drain of the modelled transistor due to the impact of a heavy ion. Specifically, the pulse shown corresponds to a LET of 3 MeV cm^2 mg^{-1}, a length of 0.18 μm and an angle of incidence θ of 90°.

As it can be seen, the generated pulse has the shape of a double-exponential and, in this case, has a maximum peak over the DC offset of less than 1 mA. It should be noted that the current has a DC offset of approximately 0.8 mA because the transistor has been biased with a gate voltage of 1 V and a drain voltage of 1.8 V.

Figure 5 shows how the current pulse changes for different values of length and LET, with $\theta = 90°$. It can be seen that as the LET value increases so does the current at the drain. This can be explained by the fact that an increase in LET means that the number of generated electron–hole pair

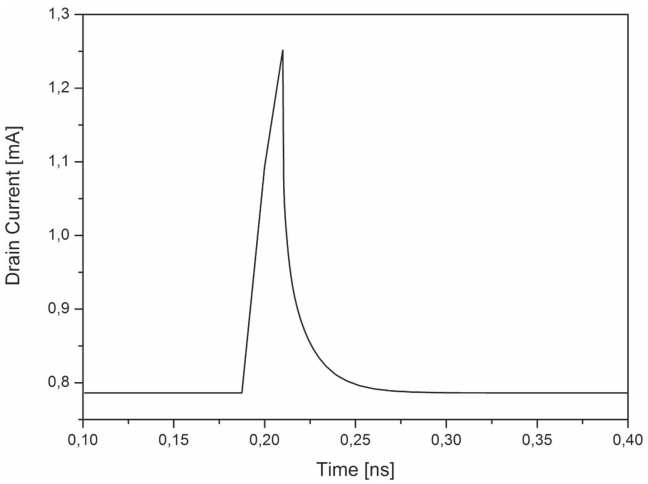

Figure 4. Current pulse in the drain of the transistor due to a heavy ion impact.

Table 1. Heavy ion model parameters.

Parameter	Description
Length	Penetration depth of the heavy ion on the device
LET$_f$	Linear energy transfer function
Wt_{hi}	Characteristic distance
Location	Point where the heavy ion enters the device
Direction	Direction of motion of the ion
Time	Time at which the ion penetrates the device

increases, translating into a higher current. Similarly, the drain current increases as the length increases.

Regarding the angle of incidence, figure 6 shows the electron–hole pair generation when θ ranges from 15° to 90°, while the length and the LET are kept constant to 0.18 μm and 3 MeV cm^2 mg^{-1}, respectively. It should be noted that a positive value of θ corresponds to a heavy ion angled towards the gate of the transistor, while a negative value represents an angle towards the edge of the device.

The drain current of the device depends on the penetration depth and the angle of incidence of the impact of the heavy ion. A higher current will be obtained when the track of the heavy ion, as it passes through the device, lands on a p–n junction. These regions are typically the most sensitive due to the presence of high fields. The electric field causes the holes to drift into the p-region and the electrons into the n-region. This phenomenon can be observed in figure 7, where the maximum drain current is obtained for smaller positive angles ($\theta = 30°$ or 45°) and for $\theta = -60°$. In the case of positive angles, the track of the heavy ion enters the region under the gate of the transistor, where the channel is formed. Regarding the case of negative angles, it must be taken into account that at smaller angles the ions exit through the side of the transistor, leading to reduced electron–hole pair generation. Therefore, for $\theta = -60°$ the maximum number of electron–hole pairs is generated along the reversed biased p–n junction between drain and substrate.

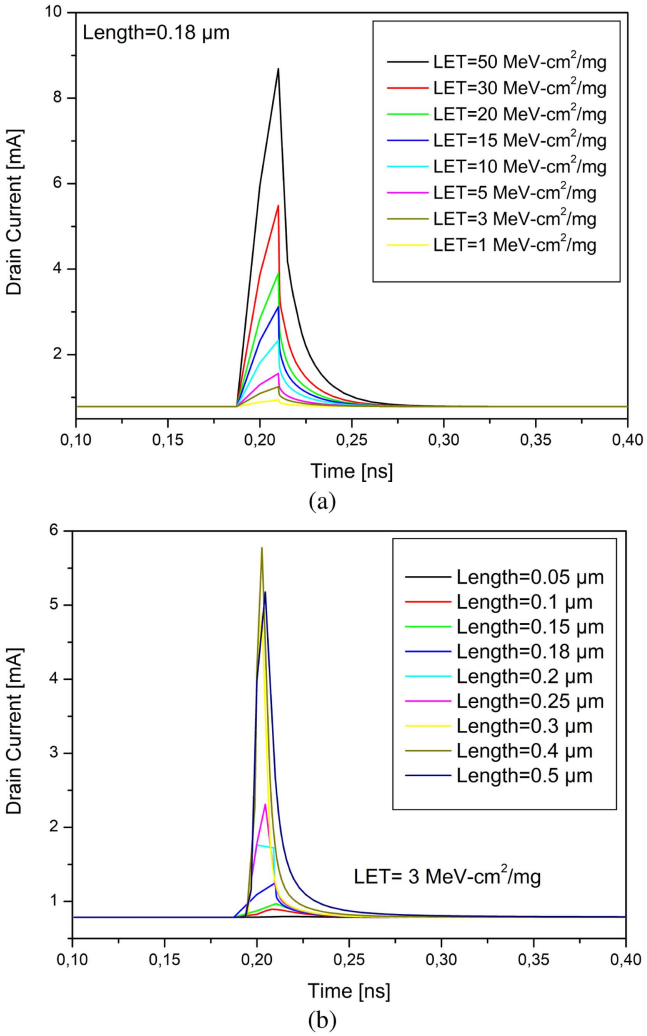

Figure 5. Drain current. (a) Different values of LET for a constant length. (b) Different values of length for a constant LET.

3. LNA structures

In this paper, two well-known LNA topologies are studied: the CS cascode and the CG cascode. Both structures should provide a low noise figure (NF), high gain to sufficiently reduce the NF contribution of the subsequent stages, a high linearity to accommodate high input signals and strong interferences and a 50 Ohm input impedance to match the output impedance of any off-chip component.

3.1. CS cascode LNA

A conventional CS cascode LNA topology with inductive degeneration is shown in figure 8. This topology is known to provide a high gain, low noise and high input/output isolation. In order to simultaneously achieve low noise and high input matching, the degeneration technique is used.

The inclusion of the degeneration inductor L_S adds a real part to the input impedance which reduces the discrepancy between the optimum noise impedance and the LNA input impedance. However, under low power consumption conditions, the required inductance value to obtain adequate noise

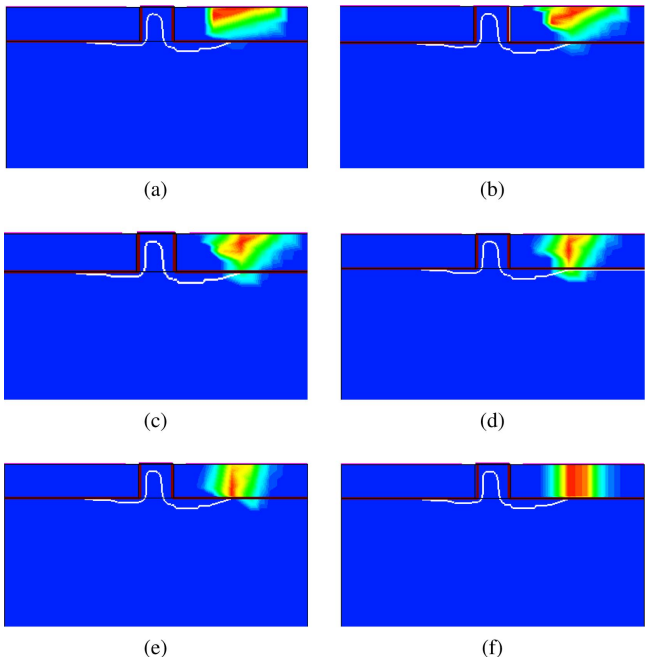

Figure 6. Electron–hole pair generation rate for different angles of incidence (a) $\theta = 15°$ (b) $\theta = 30°$ (c) $\theta = 45°$ (d) $\theta = 60°$ (e) $\theta = 75°$ (f) $\theta = 90°$.

and input matching is very large. This results in a minimum achievable NF of the LNA significantly higher than its NF_{min} [23]. This can be solved by adding the C_{ex} capacitor shown in figure 8 [24]. By adding this capacitor, lower L_S inductance values can be used to achieve better noise and input matching. As seen in (6), the effect of the inductance of L_g on the input impedance can also be reduced by including C_{ex}. In addition, the parasitic resistances are reduced, thus improving the NF of the LNA

$$Z_{in} = s \cdot (L_s + L_g) + \frac{1}{s \cdot C_t} + \frac{g_m \cdot L_s}{C_t}, \tag{6}$$

where C_t is the total capacitance between the gate and the source of M_1, while g_m is the transconductance of the transistor.

3.2. CG cascode LNA

The low input impedance of the CG stage makes it an attractive topology for LNA design. This input impedance is even lower when a cascode structure is used. Figure 9 shows the the schematic of a CG cascode LNA. In this case, the input impedance is approximately $1/g_{m1}$.

As it can be seen in figure 9, the implemented CG LNA has an inductorless topology except for the required L_d inductor, which is part of the load tank of the circuit. This results in a considerably smaller area size in comparison to the CS LNA previously presented. Additionally, it is known that the CS LNA's input matching network is series resonant while the CG LNA's is parallel resonant. Because of this, the input matching network of the CG has a lower quality factor and, as a consequence, it provides a better input matching and

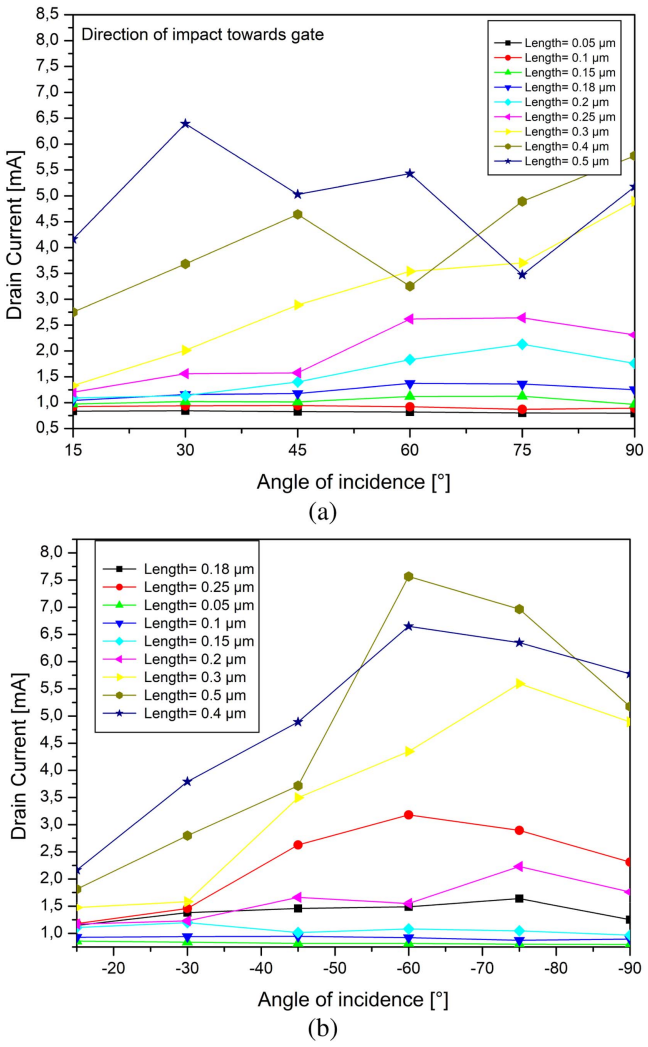

Figure 7. Maximum drain current for different angles. (a) Angles towards gate. (b) Angles away from gate.

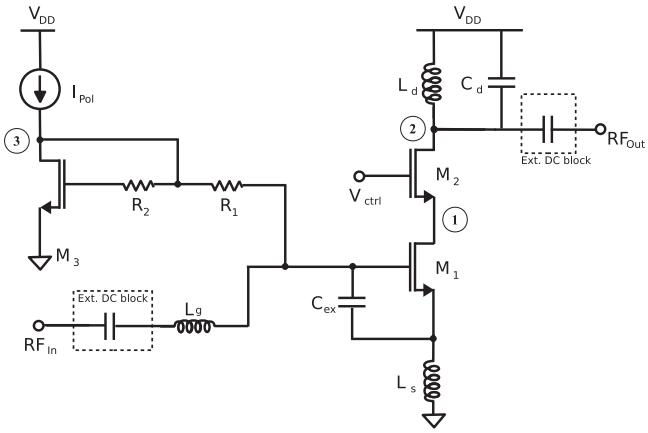

Figure 8. Schematic of the common-source cascode LNA.

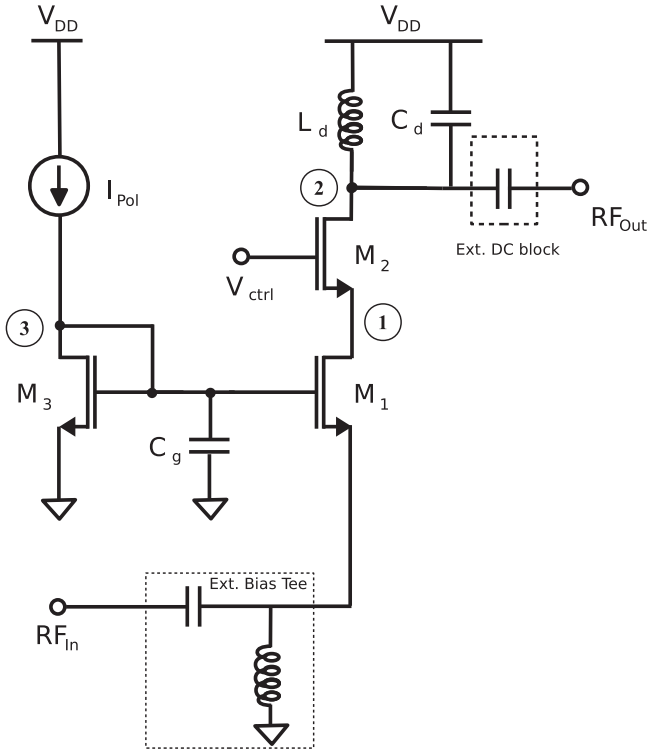

Figure 9. Schematic of the common-gate cascode LNA.

it is more robust against typical production process, voltage and temperature variations.

3.3. RF performance comparison

Both LNA structures were designed in UMC 0.18 μm CMOS technology for the 2.4 GHz band specified by the IEEE 802.15.4 standard. The design of the circuits was performed looking for good trade-offs between low power consumption, high gain and low noise.

Figure 10 shows the performance of both LNA topologies. As it can be observed, the CS has a gain of approximately 18.2 dB while the CG achieves 10.4 dB. Regarding the noise figure (NF), figure 10 shows that the CS offers a better performance (3.2 dB against 5 dB). However, the CG provides a superior input matching than the CS at the desired 2.4 GHz frequency, as expected (−28.7 dB against −11.3 dB). Considering the achieved results, it can be stated that both LNAs meet the IEEE 802.15.4 standard specifications.

4. Experimental results

In the previous section, the two LNA structures were studied regarding their RF and electrical performance. Despite the fact that both LNAs perform favourably according to the standard specifications, it is yet to be analysed how these amplifiers operate in harsh radiation environments. To do so, an investigation on the effect of SETs was performed.

The current pulses generated with the *Sentaurus* TCAD software were introduced in a circuit domain simulator and placed in current sources that were applied at the most

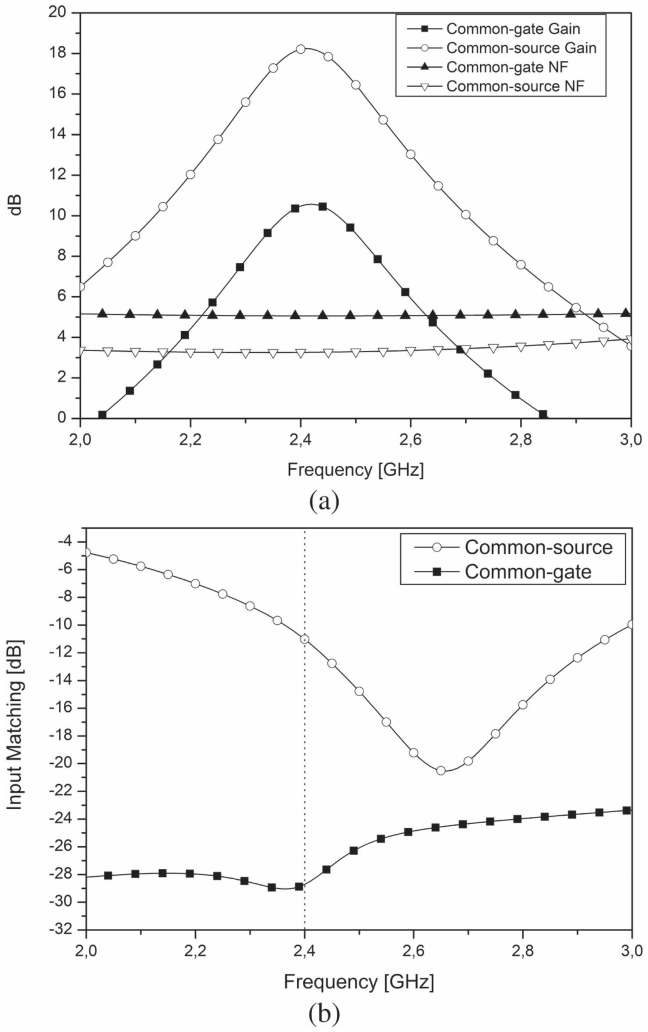

Figure 10. RF performance comparison between the CS and CG. (a) Gain and noise figure. (b) Input matching.

vulnerable nodes of both LNAs (nodes 1, 2 and 3 as seen in figures 8 and 9). This way, the semiconductor physics information obtained from the TCAD tool is combined with the fast electrical simulations performed in a circuit domain simulator. As stated previously, the ADS simulator was used, where transient simulations were performed with the current sources connected at the drain of each transistor of both LNAs.

In order to assess the SET behaviour of both circuits, the maximum voltage peak and the recovery time of the output signal were calculated for each case. The output signal is considered to be recovered when the difference between the output voltage signal when the SET strikes and the voltage signal when there is no strike is below 5%. In this section, the results shown correspond to current pulses with different LET and length value, while the angle of incidence remains with a constant value of $\theta = 90°$. This corresponds to a heavy ion impacting the transistor perpendicularly, which is a widely used approach in this kind of studies [15, 16].

Figure 11 shows the obtained maximum voltage peak against the recovery time of the output signal for both LNAs. A safe operating area (SOA) can be defined, setting the boundaries for acceptable SETs. The events that occur inside this area have amplitudes and durations that do not affect the functionality of adjacent circuits. This SOA is specified by the designer and is application-dependent [25]. In this case, a maximum voltage peak of 20 mV and a recovery time of 7 ns have been defined as the boundaries of the SOA. Table 2 shows the percentage of SETs that are inside the SOA for each node of both circuits. From these results it can be stated that node 3 is the most critical node in both circuits.

Additionally, it can be seen that the largest voltage peaks at the output are obtained when a strike occurs at node 2 in both LNAs. This is because this node is directly connected to the output of the LNAs. Regarding the recovery time, it can be observed that both circuits take longer to recover when there is a strike in node 3 compared to the other nodes. This can be explained since bias circuits, which are responsible for setting the operating voltage for the transistors are known to be very sensitive to SETs. Therefore, any voltage variation induced by an ion strike in the bias circuit will result in a deviation of the circuit response [26].

5. Radiation hardening techniques

Once the effects of SETs have been analysed for both LNAs, several mitigation techniques can be applied to reduce the effect of these events.

As seen in section 4, node 3 is the most critical node in both LNAs. Therefore, the mitigation techniques proposed in this paper are focused on this node. These RHBD techniques should improve the SET performance of the LNAs without affecting their RF performance.

In this paper, resistor-capacitor (RC) filtering is implemented to achieve RHBD LNAs. Increasing the capacitance of node 3 lowers the impedance and increases the time constant ($\tau = R \cdot C$), hence the resulting voltage deviation due to the SET is much lower. Therefore, since the peak is now smaller, the time it takes for the signal to get back within the threshold is shorter, resulting in a smaller recovery time. Taking this into account, the biasing networks of both LNAs have been modified. As seen in figure 12, the capacitor C_g was included at node 3 of the CS. This way the amplitude and duration of the peaks caused by the strikes is reduced by the capacitor, since more charge is required to overcome the stored charge in the capacitor to initiate the transient [27]. Therefore, a large capacitor results in a bigger reduction of the voltage peaks. However, area constraints must also be considered. In this case, the capacitor has a value of 1.45 pF, which is the same value as the C_g present in the CG LNA.

Regarding the CG, resistances R_1 and R_2 were included to reduce the voltage peak by increasing the time constant at node 3. These resistances should be large enough that its equivalent noise current is small enough to be ignored. Taking this into account, it can be assumed that a high resistance value should be chosen for these resistors. However, it should be noted that increasing the resistance will result in a larger area consumption. Therefore, two 2 kΩ resistors were chosen. Figure 13 shows the RHBD CG LNA schematic.

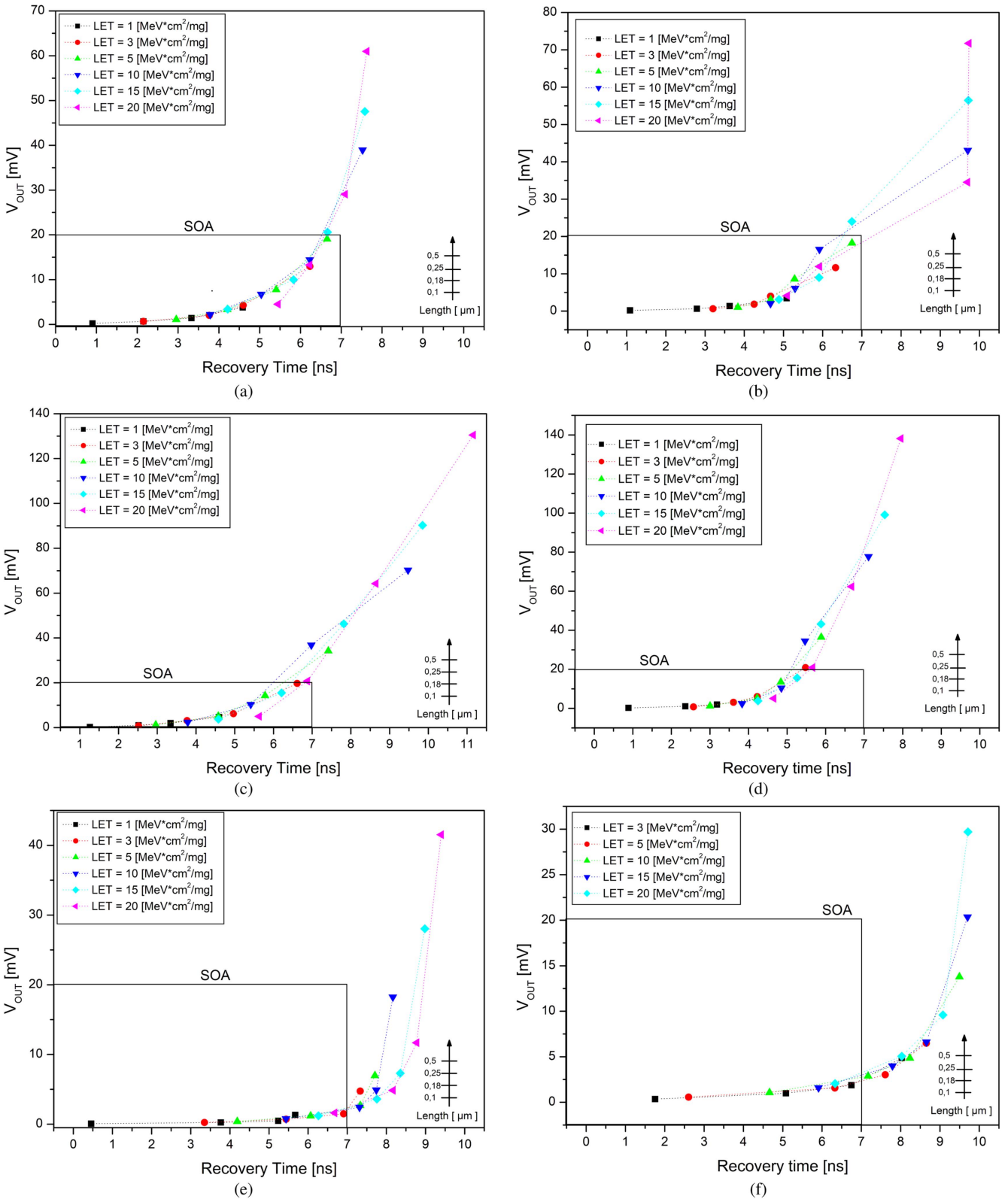

Figure 11. Maximum voltage peak against recovery time of the output signal. (a) Strike at node 1 of the CG. (b) Strike at node 1 of the CS. (c) Strike at node 2 of the CG. (d) Strike at node 2 of the CS. (e) Strike at node 3 of the CG. (f) Strike at node 3 of the CS.

Figure 14 shows the maximum voltage peak against the recovery time of the output signal for the two RHBD LNAs when there is a strike at node 3. It can be observed that both the recovery time and the maximum voltage peak of the output signal have been considerably reduced. In fact, now 100% of the SETs are inside the SOA for both LNAs.

As seen in the previous section, nodes 1 and 2 are less vulnerable to SETs compared to node 3 in both LNAs. Still,

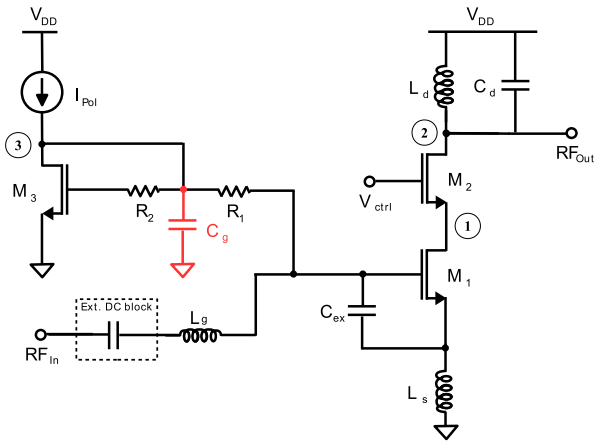

Figure 12. Modified common-source LNA.

Table 2. Percentage of SETs inside the SOA for the CG and CS LNAs.

	LNA	
Node	CG	CS
1	80%	80%
2	65%	60%
3	50%	40%

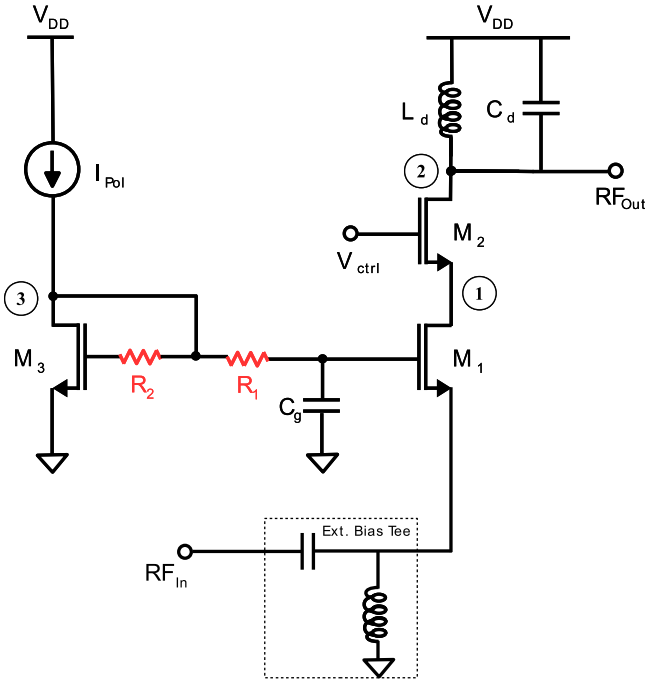

Figure 13. Modified common-gate LNA.

the SET performance of the circuits when there is a strike at these nodes could be further improved by increasing the time constant including resistances and capacitances, similarly as for node 3. However, this approach is not advisable since the RF performance of the LNAs will be worsened by introducing noise and shifting the frequency response of the circuit.

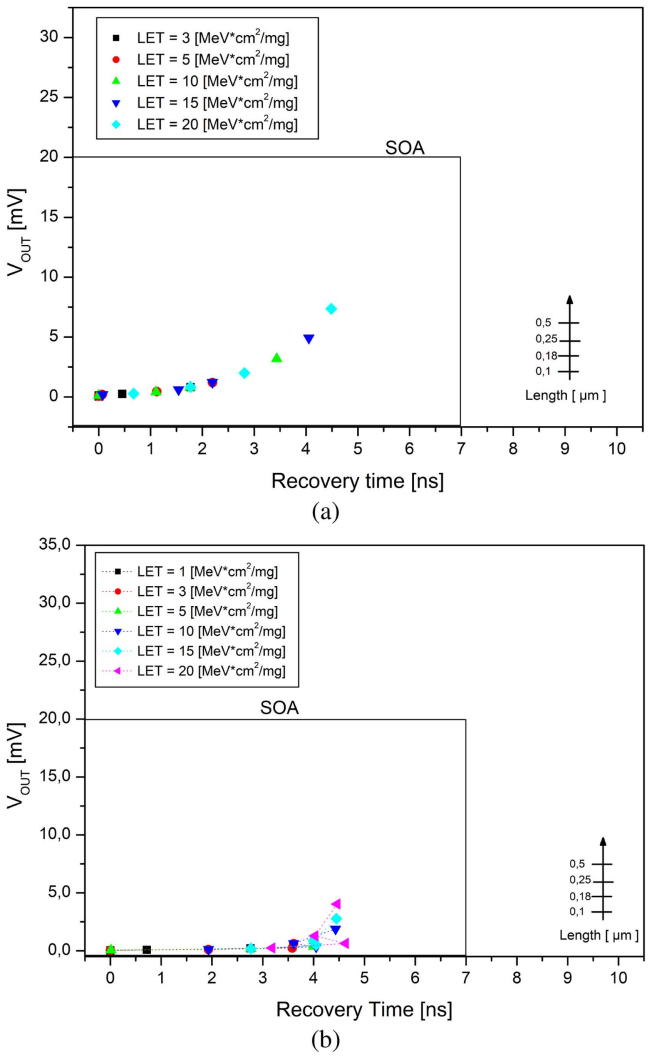

Figure 14. Maximum voltage peak against recovery time of the output signal. (a) Strike at node 3 of the RHBD CS. (b) Strike at node 3 of the RHBD CG.

6. Conclusions

The effect of SETs in low noise amplifiers has been analysed in this paper and radiation hardened by design techniques have been applied without modifying the RF performance of the LNAs. To do so, a proven simulation methodology has been applied. The physics-based *Sentaurus* TCAD simulator was used to model an NMOS transistor of the UMC 0.18 μm technology and to perform heavy ion simulations. The heavy ion model was used to simulate the effect of a charged particle striking the modelled transistor. These simulations showed that an increase in LET and penetration depth of the heavy ion in the semiconductor implies an increase in the drain current. Regarding the angle of incidence, higher currents are obtained for angles where the maximum number of electron–hole pairs is generated along the reversed biased p–n junction. The TCAD-generated current pulses were then introduced in the circuit domain simulator ADS to analyse the most vulnerable nodes of a CS and a CG cascode LNA. Simulation results show that the SET performance of both LNAs is considerably

more sensitive to strikes at the biasing networks of the circuits. In light of these results, mitigation techniques were applied at these nodes in order to reduce the effect of SETs. The main approach was to reduce the voltage peaks by increasing the time constant of the sensitive nodes by including resistances and capacitances. These RHBD techniques considerably reduce the recovery time and the maximum voltage peak of the output signal of both LNAs. The proposed modifications make both LNAs more robust against SETs since 100% of the generated SETs are inside a defined SOA for both the CS and CG.

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