Geometric Modeling of Thermal Resistance in GaN HEMTs on Silicon

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***Abstract*—In this paper, pulsed measurements of thermal resistance in GaN-based high electron mobility transistors (HEMTs) on silicon, with different gate geometries and gate-to-drain extensions, are analyzed and modeled. Simple expressions for the thermal resistance of SOI-MOSFETs, which take into account the gate width and channel length, can be adapted to model the thermal resistance of these GaN-based HEMTs. Narrow width effects and the increase in the heat flow through the gate as the channel length increases were correctly reproduced. In addition, numerical simulations were performed to explain the reduction obtained in thermal resistance as the gate-to-drain extension increases. Our approach can also be applied easily to other well-established models using circuit simulators.**

***Index Terms*—Channel temperature, electro-thermal characterization, gallium nitride, high-electron mobility transistors (HEMTs), pulsed measurement, thermal resistance.**

I. Introduction

Due to their high breakdown voltage and power density operation, GaN-based high electron mobility transistors (HEMTs) have become the most important devices for RF power applications, particularly following the emergence of advanced device pilot lines with silicon substrates and the consequent reductions in cost [1], [2]. When predicting the power performance of HEMTs, self-heating effects cannot be neglected [3], and this is a problem that has yet to be overcome.

Several methods have been used to measure the thermal resistance (temperature rise per Watt) of GaN-based HEMTs. In a study by Kuzmík [4], a value was obtained by making use of the DC output characteristics at room temperature (subsequent current traces required the device charge to be restored) and the temperature dependences of the saturation drain current, threshold voltage and source resistance (where the assumption of no temperature dependence for the electron saturation velocity was made). Measurements of the drain current time-domain dynamic response to positive drain bias pulses (i.e. pulsed thermal dynamic behavior) were used in [5]. Detailed temperature profiles can be created using IR thermography, and in particular by high-spatial-resolution Raman thermography [6]. However, these thermography techniques are not always practical, since specific device samples and equipment are usually required in the laboratory. Finally, pulsed measurement is a feasible methodology for obtaining the thermal resistance at different ambient temperatures [3], [7]–[9], and this is the approach used in the present work.

Various studies have been carried out of the dependence on gate geometry of the measured thermal resistance of GaN-based HEMTs [4], [7], [10]. However, unlike for silicon-on-insulator (SOI) metal–oxide–semiconductor field-effect transistors (MOSFETs) [11]–[15], modeling of this dependence has not been extensively conducted. Most recent works are based on numerical simulations [16], [17], and have given rise to elaborated analytical closed-form expressions for thermal resistance, including device geometric parameters, different layer thicknesses, and the corresponding thermal conductivities [18], [19]. However, they do not account for implanted buffer composition, which is usually unknown and can significantly influence the self-heating of the device [20].

The use of thermal circuits that include several thermal resistances and capacitances is another option for the modeling of self-heating effects [21]. However, although detailed thermal models are desirable in order to achieve a complete physical representation, simplification is necessary when dealing with compact models, which is the main topic of this work.

The transistors under study and the experimental setup are described in Sections II and III, respectively. Section IV explains the methodology used, and the thermal resistances resulting from varying the gate geometry and gate-to-drain extension are discussed and modeled in Section V. Finally, our conclusions are presented in Section VI.

II. Device Structure

The AlGaN/GaN layer stack of the HEMTs investigated here (provided by CEA-Leti) consisted of Ga(Al)N epitaxial layers grown on a Si substrate of thickness 1 mm in the

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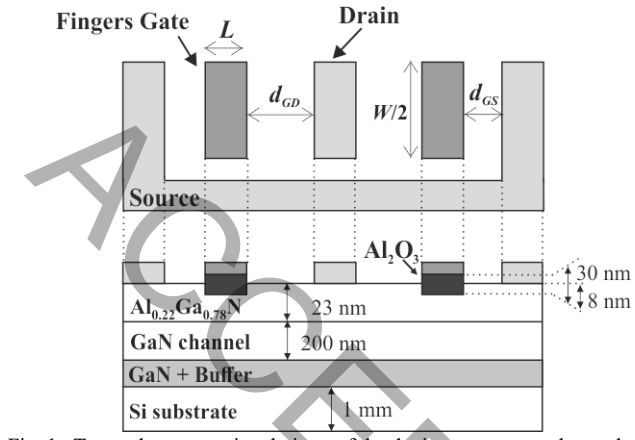

Fig. 1. Top and cross-sectional views of the device structure under study.

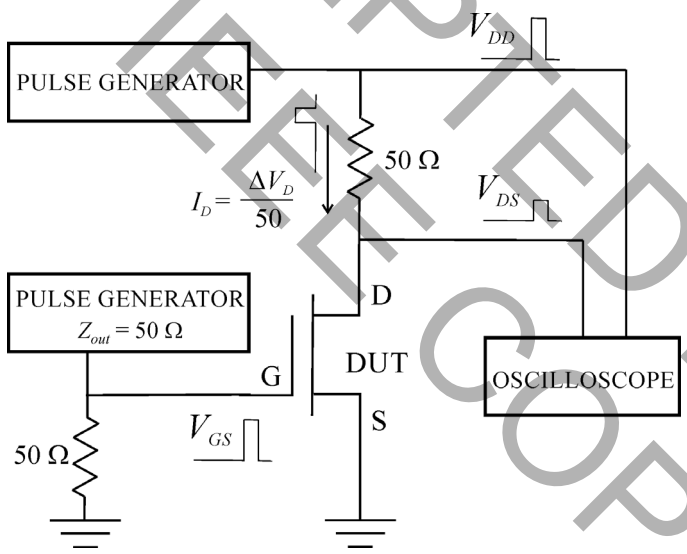

Fig. 2. Experimental setup for the double-pulsed method.

(1-1-1) direction [2], with a non-intentionally doped GaN channel and $Al_{0.22}Ga_{0.78}N$ barrier that were 200 and 23 nm thick, respectively. The depletion-mode transistors were based on a partial $Al_{0.22}Ga_{0.78}N$ etching, with a gate recess of 8 nm, to give a negative threshold voltage of –4 V, using TiN/W (double finger) gate metal and Al_2O_3 gate oxide of thickness 30 nm.

A reference device with a gate length, L, of 2 μm, a gate width, W, of 100 (2 × 50) μm, and a gate-to-drain extension, d_{GD}, of 15 μm, was used. Other gate lengths of 1, 3, and 4 μm, total widths of 20, 40, and 200 μm, and gate-to-drain extensions of 15, 20, 25, and 30 μm were also used. In all cases, the gate-to-source separation, d_{GS}, was 2 μm. Top and cross-sectional views of the device structure under study, with various dimensions labeled, are shown in Fig. 1.

III. Experimental Setup

The measurement setup was performed using Agilent HP8110A and HP8114A pulse generators for gate and drain pulsing, respectively, with a pulse rise time of 10 ns, and a Tektronix TDS680 oscilloscope [22]. The transistors were placed on a hotplate to give a temperature range of 25–150°C for the reverse of the substrate, which was applied in steps of 25°C. The system was remotely controlled by a personal computer using LabVIEW [3].

A diagram of the experimental setup is shown in Fig. 2. Note that in order to avoid signal reflections, a 50 Ω feed-through terminator was used to ensure efficient impedance matching between the 50 Ω output pulse generator and the high-impedance gate terminal of the device under test (DUT). The drain current was determined based on Ohm's law, with the drain terminal being pulsed through a 50 Ω sensing resistor, where the voltage drop was evaluated with an oscilloscope ($\Delta V_D = V_{DD} - V_{DS}$ in Fig. 2).

IV. Methodology

The thermal resistance of the device, R_{th}, was measured as the ratio between the channel temperature rise, $\Delta T_{ch} = T_{ch} - T_a$, with T_{ch} and T_a as the channel and base-plate (ambient) temperatures, respectively, and the corresponding quiescent power dissipation, $P_D = I_D V_{DS}$, where I_D and V_{DS} represent the quiescent drain current and drain-to-source voltage, respectively (i.e. $R_{th} = \Delta T_{ch}/P_D$), and the channel temperature rise was obtained as follows.

External heating and self-heating can modify the channel temperature of a device. First, per the methodology reported in [7], the temperature dependence of a temperature-sensitive electrical parameter (TSEP) was calibrated through external heating. In this case, the channel and base-plate (ambient) temperatures can be assumed to be equal, i.e. $T_{ch} \approx T_a$. Following this, the channel temperature under operation was obtained by measuring the same TSEP, pulsing from various bias conditions that dissipate different amounts of power, which lead to self-heating effects for a given ambient temperature.

The TSEP used as a thermometer was the maximum-pulsed drain current, $I_{D,max}$, extracted from pulsed output characteristics. In addition, to avoid disturbing the channel temperature, the pulsed voltages used should avoid any additional dynamic self-heating effects.

Thus, the output characteristics (see Fig. 3 for the reference device, with drain current per 1 mm device width) were measured using short pulsed voltages, 200 ns wide, with a duty cycle of 0.02%, from quiescent gate-to-source bias voltages without pinch-off of the channel. The current collapse was therefore minimal, since the drain-to-source voltage was pulsed in the ON state [7], [22].

As previously indicated, $I_{D,max}$, for gate-to-source and drain-to-source pulsed voltages of V_{GS} = 0 V and V_{DS} = 5 V, respectively, was obtained by heating the device in two ways. First, to calibrate its temperature dependence, the ambient temperature was varied using the hotplate, with a zero power dissipation quiescent bias point, P_D = 0 W/mm, with V_{GS} = –3 V and V_{DD} = 0 V, as shown in Fig. 3(a). In this case, $T_{ch} \approx T_a$ = 25–150°C. Following this, as shown in Fig. 3(b), for a given ambient temperature, T_a, various quiescent bias points were set with V_{GS} = 0 V (the gate was not pulsed in this

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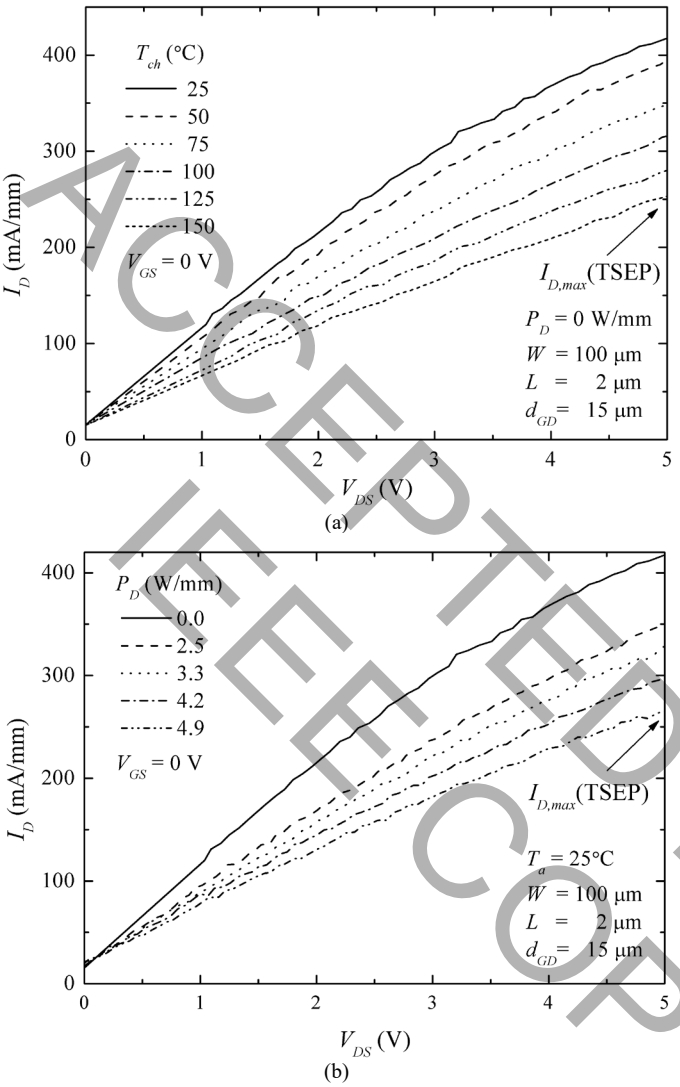

Fig. 3. Pulsed output characteristics for the reference device: (a) at different channel temperatures from zero power dissipation quiescent bias point (P_D = 0 W/mm); and (b) from various quiescent bias points with nonzero power dissipation (P_D = 0–4.9 W/mm) at room temperature. V_{GS} = 0 V.

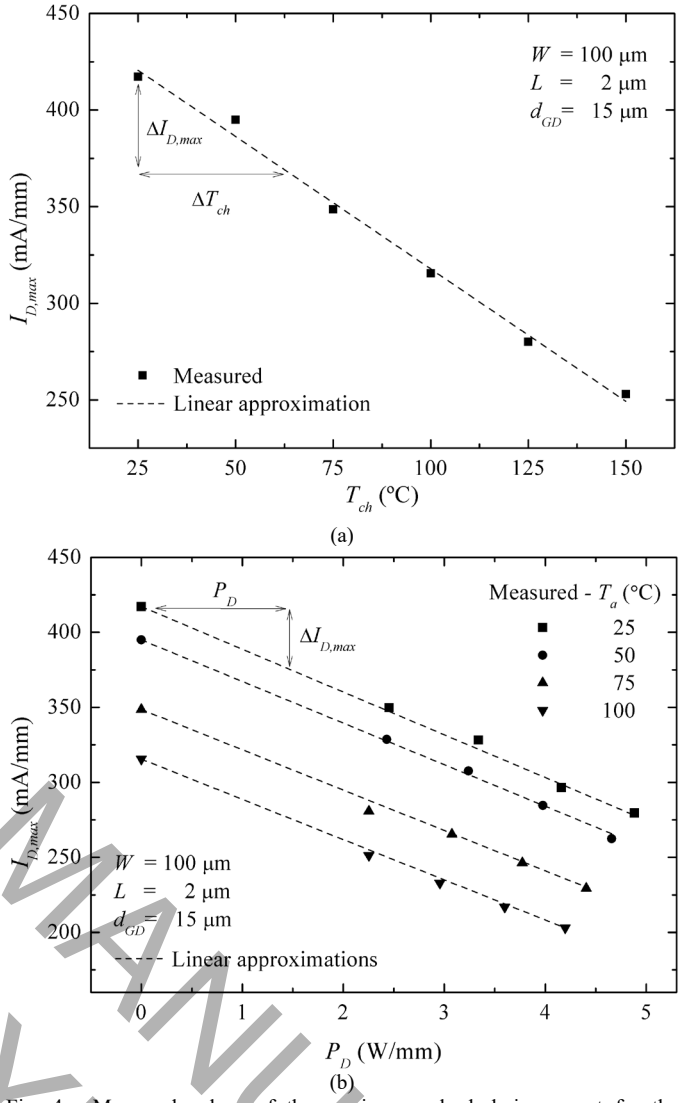

Fig. 4. Measured values of the maximum-pulsed drain current for the reference device (closed symbols) with (a) channel temperature; and (b) power dissipation at different ambient temperatures. The corresponding linear approximations are represented by dashed lines. V_{DS} = 5 V, V_{GS} = 0 V.

case) and different power dissipations, $P_D = I_D V_{DS}$ = 0–4.9 W/mm, for which V_{DD} was varied from 0 to 16 V.

The maximum-pulsed drain current varied linearly with the channel temperature, as shown in Fig. 4(a) for the reference device with drain current per 1 mm device width. The measured data are represented with symbols and the corresponding linear fittings with dashed lines. At different ambient temperatures of between 25−100°C, $I_{D,max}$ also varied linearly with the power dissipation, as shown in Fig. 4(b). Analogous results were obtained for the remainder of the HEMTs.

Since $I_{D,max}$ ($T_{ch} = T_a$) and $I_{D,max}$ ($P_D = 0$)$|_{T_a}$ coincide, the thermal resistance of the device can be evaluated as the relation between the linear deviations in the maximum-pulsed drain current with power dissipation and ambient temperature (see Fig. 4(a) and (b)), i.e.:

$$R_{th}(T_a) = \frac{\Delta I_{D,max}/P_D\big|_{T_a}}{\Delta I_{D,max}/\Delta T_{ch}} \quad (1)$$

In this case, the thermal resistance does not depend on the power dissipation (giving linear ΔT_{ch}–P_D characteristics as a result). For the reference device, the measured thermal resistance per unit width is 19.8°C mm/W, with a maximum deviation of 0.3°C mm/W for the ambient temperature range used here. Similar results were obtained in [6] (15.8°C mm/W) and [7] (23.1°C mm/W) for double-finger GaN-based HEMTs on silicon at room temperature.

It should be pointed out that the thermal resistance of GaN-based HEMTs can increase with both power dissipation (3.9% per Watt in [23]) and ambient temperature (0.44% per degree Celsius in [5]). This is the case for multi-finger devices if hot spot phenomena arise [6], [18], due to progressive thermal coupling as the number of fingers increases, or for HEMTs with low thermal conductivity substrates such as sapphire [24], at high power dissipation and/or ambient temperature levels. This is attributed to a nonlinear decrease in the thermal conductivity of the semiconductors with an increase in the lattice temperature, which predominates over

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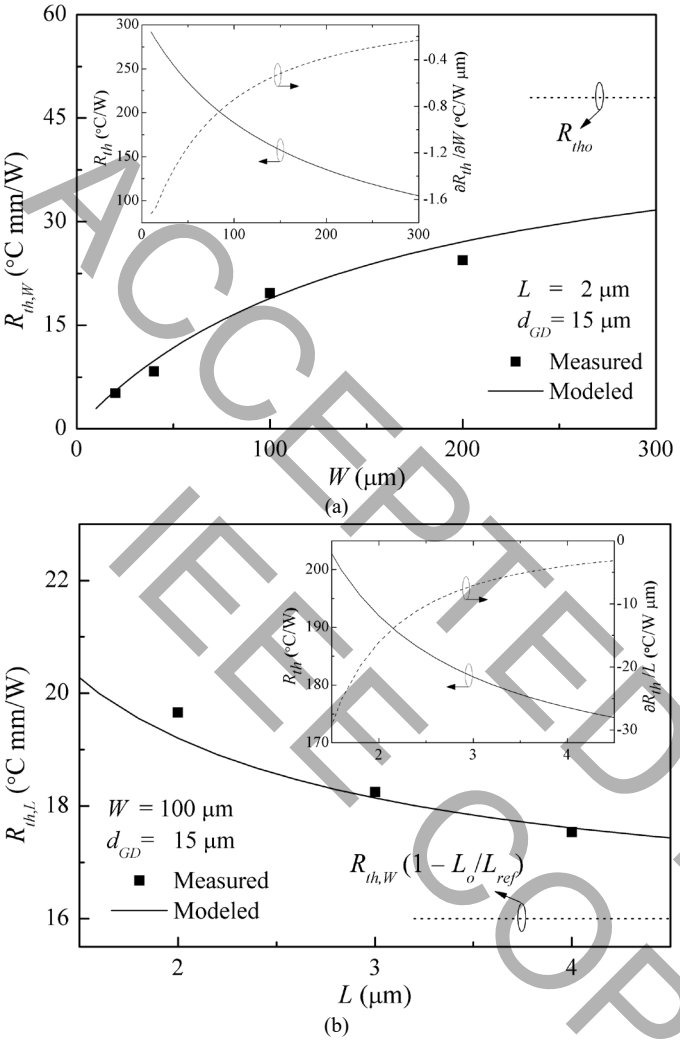

Fig. 5. Thermal resistance per unit width with (a) gate width; and (b) channel length. The measured and modeled data are shown by symbols and lines, respectively. The insets show the corresponding dependence of the modeled thermal resistance (left axis, with solid line) and its derivative function (right axis, with dashed line).

TABLE I
PARAMETERS TO MODEL THE DEPENDENCY OF THERMAL RESISTANCE ON DEVICE GEOMETRY

R_{tho} (°C mm/W)	48.0
a (mm)	0.15
L_o (μm)	0.33
L_{ref} (μm)	2.00
$R_{th,\infty}$ (°C mm/W)	4.90
d_o (μm)	43.9

the global self-heating response of the device [25], [26]. Nonlinear $I_{D,max}$–P_D and $I_{D,max}$–T_{ch} characteristics can then be found to convert $I_{D,max}$ to the channel temperature [7], giving nonlinear ΔT_{ch}–P_D characteristics as a result.

V. MEASUREMENT RESULTS AND MODELING

In this section, we model the geometry dependence of the measured thermal resistances in the GaN-based HEMTs.

A. Dependency on Gate Width

Regarding the gate width, the thermal conductance, $G_{th} = 1/R_{th}$, obeys the linear dependency observed for SOI-MOSFETs [13], [14]. That is, $G_{th} = (W + a)/R_{tho}$, where a/R_{tho} represents a positive thermal conductance at a hypothetical zero device width, and R_{tho} represents the thermal resistance per unit width for sufficiently wide HEMTs (i.e., when $W >> a$ and periphery effects can be neglected). The parameters R_{tho} and a can be determined from the slope and W-axis intercept, respectively [13]. Their values are shown in Table I for HEMTs with the same gate length as the reference device, $L = L_{ref} = 2$ μm.

Thus, the dependence on gate width of the thermal resistance per unit width in GaN-based HEMTs is given by

$$R_{th,W} = R_{tho}\frac{W}{W+a}. \tag{2}$$

Hence, the wider the gate, the higher the thermal resistance per unit width, and this tends to R_{tho} for a sufficiently high gate width. In this case, the thermal resistance can be expressed as the ratio between R_{tho} and the gate width (i.e. $R_{th} \approx R_{tho}/W$), which is a common approximation. However, as mentioned above, a considers the relevance of narrow width effects. For a sufficiently low gate width ($W << a$), a remnant thermal resistance due to periphery effects is still present, which is given by $R_{th} \approx R_{tho}/a$.

Fig. 5(a) shows the measured and modeled data as symbols and a line, respectively, and good agreement between these results can be observed (with an average relative error of 10%). R_{tho} is indicated with a dotted line. The observed narrow width effects (no constant thermal resistance per unit width) are similar to those found in [7] for SiC-based HEMTs.

B. Dependency on Channel Length

The variation in the thermal resistance per unit width with gate length was similar to that obtained in [7] and modeled as that for SOI-MOSFETs in [15]:

$$R_{th,L} = R_{th,W}\left[1+L_o\left(\frac{1}{L}-\frac{1}{L_{ref}}\right)\right] \tag{3}$$

where L_o is a technology-dependent fitting parameter, which is shown in Table I, and determines the relevance of the dependence on gate length of the thermal resistance (for a null value no dependence on gate length results). Fig. 5(b) shows the measured and modeled results, represented with symbols and a line, respectively, with a relative error between them lower than 2.3%.

The dependence on gate length indicates that there was a non-negligible heat flow from channel through the gate, in contrast to the assumption, typically made for simulation purposes, that all heat flows towards the substrate [3], [17]. Further evidence of this was found in [27], where the thermal performance of a GaN HEMT on sapphire could be improved by a factor of 2.6 using a flip-chip integration approach, where bumps were placed directly onto the ohmic contacts of the source, drain, and gate. In addition, the Raman thermography temperature profiles reported in [6] demonstrated that the temperature at all of the terminals of a GaN-based HEMT on SiC (with lower thermal conductivity than Si) may be

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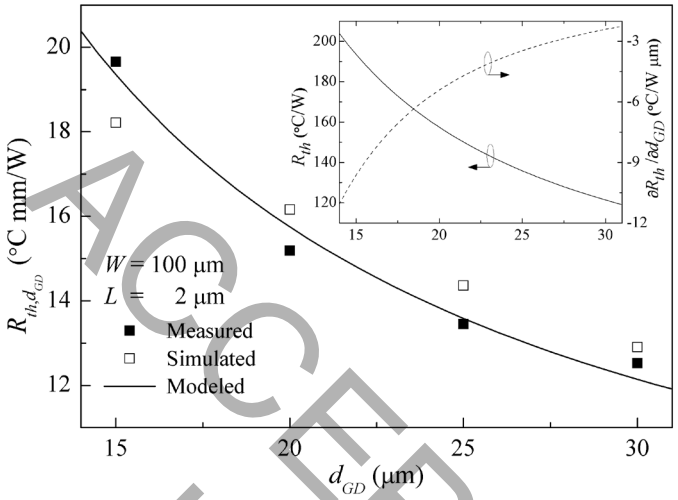

Fig. 6. Thermal resistance per unit width vs. gate-to-drain extension. The measured, simulated, and modeled data are shown by the closed symbols, open symbols, and line, respectively. The inset shows the corresponding dependence of the modeled thermal resistance (left axis, with solid line) and its derivative function (right axis, with dashed line).

significantly above the ambient temperature, indicating heat dissipation via all terminals.

In our case, the thermal resistance is reduced as the length of the channel increases, which evidences that the heat flow through the gate contact becomes more significant. However, this tendency, that increases with L_o, vanishes for very long channels (i.e., when $L >> L_{ref}$ and $R_{th,L} \approx R_{th,W}(1-L_o/L_{\text{ref}}) =$ 15.5°C mm/W, as indicated by the dotted line in Fig. 5(b)) when no additional heat flow is dissipated via the gate. Thus, L_{ref} establishes the maximum reduction in thermal resistance for very long channels.

In case a thinner Al_2O_3 gate oxide was used (note that in our case, the 30 nm thickness is greater than that of conventional HEMTs [28]), the gate length dependence of the (reduced) thermal resistance would be enhanced.

Finally, by substituting (2) into (3), a general expression for the thermal resistance can be found, as follows:

$$R_{th} = \frac{R_{tho}}{W+a}\left[1+L_o\left(\frac{1}{L}-\frac{1}{L_{ref}}\right)\right], \tag{4}$$

which is simple enough to be easily applied to other well-established models in circuit simulators.

It should be noted that in the case of nanometric channels, where the heat flow through the gate is negligible, the thermal resistance must tend to a constant value (the source and drain contacts do not shrink) [15]. Then, in order to avoid variation in R_{th}, $L + \Delta L$ should be substituted for L in (3) and (4), where ΔL is a technology-dependent fitting parameter (and has a value of zero in our case).

In addition, in the case of multi-finger devices, we suggest that self-heating coupling can be modeled by replacing W in (2) and (4) by an effective channel width, W_{eff} ($W_{eff} < W$), which may depend on the number of fingers, as in [14], for SOI-MOSFETs. For a physical explanation, not just for circuit simulation purposes, a more detailed model is needed.

C. Dependency on Gate-to-Drain Extension

Fig. 6 shows the resulting dependence on gate-to-drain extension of the measured thermal resistance per unit width (shown as closed symbols), which is similar to that obtained with the variation in gate length and is empirically modeled (shown as a line) by

$$R_{th,d_{GD}} = R_{th,\infty}\left(1+\frac{d_o}{d_{GD}}\right) \tag{5}$$

where d_{GD} is the gate-to-drain extension and d_o is a technology-dependent fitting parameter that models the impact of gate-to-drain spacing on the thermal resistance, with the heat flowing from the channel, between the gate and drain, towards the gate metal, substrate and drain terminal (as indicated below). This heat flow does not vary for very long gate-to-drain spacings, when $d_{GD} >> d_o$, and $R_{th,\infty}$ represents the thermal resistance per unit width in this case. The values of these parameters are shown in Table I.

Note that the longer the gate-to-drain access region, the lower the thermal resistance results, and these tend to $R_{th,\infty}$ only after several millimeters (an impracticable size). The reduction in heat flow through the drain contact, as the gate-to-drain extension increases, would lead to an increase in the thermal resistance (in our case, metallization of the source/drain contacts extended down to the channel, acting as an efficient heat sink). The opposite behavior of the thermal resistance observed in this experiment must therefore be due to a larger increase in the dissipation of internal heat to other parts of the device. In order to clarify this point, 2D numerical simulations were performed with Sentaurus Device [29] by solving the heat flow equation with the Poisson and drift-diffusion equations. Due to symmetry, only half of the device needed to be simulated. The polarization charges and saturation velocity effects were included. Dirichlet boundary conditions for the lattice temperature (25°C) and proper surface thermal resistances (0.009°C cm^2/W) were used at all terminals, and the substrate was replaced by an additional equivalent surface thermal resistance (0.006°C cm^2/W). Thus, the obtained gate-to-drain extension dependence of the thermal resistance was numerically reproduced, as shown by the open symbols in Fig. 6, with a relative error between the measured and simulated data of less than 7.5% in all cases.

Fig. 7 shows the resulting temperature profile for the reference device (half of the device is shown with relevant geometric dimensions). The inset shows a magnified view of the gate area with field plates G-FP1 and G-FP2, located above the thin film of silicon nitride (thickness 150 nm) grown on the AlGaN barrier and the SiO_2 field oxide (thickness 400 nm), respectively. Similar results were obtained for the remainder of the devices. The results indicate that a significant heat flow is not only dissipated from the device via the substrate and the reverse of the contacts, but also the field plates, and particularly the gate field plates, via the passivation layer/barrier interface. It is known that the hottest region in the channel extends outwards into the drain extension below G-FP1 [6], and this could be increased by the velocity

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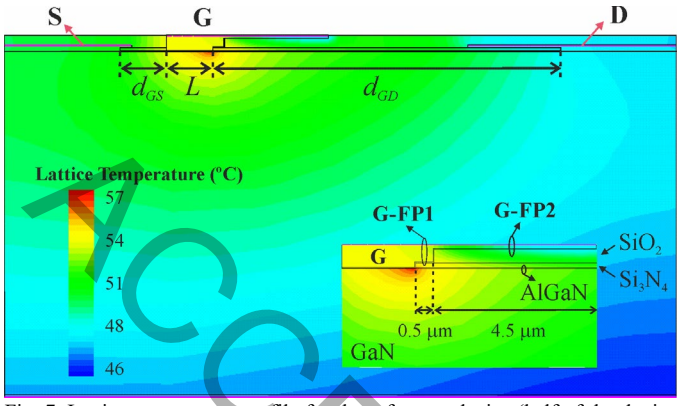

Fig. 7. Lattice temperature profile for the reference device (half of the device is shown here). The inset shows a magnified view of the gate area with the gate field plates (G-FP1 and G-FP2). V_{DS} = 5 V, V_{GS} = 0 V, T_a = 25°C.

overshoot effect [30]. The increase in the simulated heat flow through the gate metal and substrate as the gate-to-drain extension is increased predominates over the heat flow reduction towards the drain, giving rise to the gate-to-drain dependence of the thermal resistance as shown in Fig. 6.

The gate-to-drain extension is a technology-dependent parameter that cannot be controlled by circuit designers. High values of this parameter are desirable in order to reduce the thermal resistance of the device. However, this may negatively affect other necessary device performance characteristics, such as a high current supply and/or low on-resistance, R_{on}. A suitable value for d_{GD} is required in a given application.

For the suitable gate-to-drain extension, the thermal resistance can be determined by following the procedure described in Sections V-A and B.

Finally, for a better comprehension of the dependence on gate width, gate length, and gate-to-drain extension of the thermal resistance, the insets in Fig. 5(a) and (b) and Fig. 6 show the corresponding dependence of the modeled thermal resistance (left axis, with solid line) and its derivative function (right axis, with dashed line). Notice that, as expected in all cases, the thermal resistance significantly reduces as the device geometry expands since more heat flow can be spread out of the device through the terminals (including field-plates) and substrate. For the same variation in gate width, gate length, and gate-to-drain extension, the dependence on gate length and gate width turns out to be the most and least relevant, respectively. Nevertheless, compared with the changes in gate length and gate-to-drain extension, the change in gate width is much greater (it could be up to several millimeters). Therefore, in practice, the channel width has a more significant impact on device self-heating.

VI. Conclusion

The pulsed methodology described here is a well-established approach that was successfully applied to determine the thermal resistance of GaN-based HEMTs for different gate geometries and gate-to-drain access regions. The expected dependencies of the thermal resistance on channel width and gate length were observed and successfully modeled using simple expressions previously applied to SOI-MOSFETs. In this way, narrow width effects were correctly reproduced, and the increase in the heat flow through the gate as the channel length increases was derived by a reduction of the thermal resistance, which vanishes with a channel length of greater than a few microns. Additional numerical simulations demonstrated that the increase in the thermal flow through the gate metal and substrate as the gate-to-drain extension increases predominates over the reduction towards the drain contact, giving rise to reduction in the thermal resistance, which was also modeled. Finally, the modeling approach developed here to take into account the self-heating effects can be easily applied to circuit simulators as an add-on to other well-established models.

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