Geometric Modeling of Thermal Resistance in GaN HEMTs on Silicon

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***Abstract*—In this paper, pulsed measurements of thermal resistance in GaN-based high electron mobility transistors (HEMTs) on silicon, with different gate geometries and gate-to-drain extensions, are analyzed and modeled. Simple expressions for the thermal resistance of SOI-MOSFETs, which take into account the gate width and channel length, can be adapted to model the thermal resistance of these GaN-based HEMTs. Narrow width effects and the increase in the heat flow through the gate as the channel length increases were correctly reproduced. In addition, numerical simulations were performed to explain the reduction obtained in thermal resistance as the gate-to-drain extension increases. Our approach can also be applied easily to other well-established models using circuit simulators.**

***Index Terms*—Channel temperature, electro-thermal characterization, gallium nitride, high-electron mobility transistors (HEMTs), pulsed measurement, thermal resistance.**

I. Introduction

Due to their high breakdown voltage and power density operation, GaN-based high electron mobility transistors (HEMTs) have become the most important devices for RF power applications, particularly following the emergence of advanced device pilot lines with silicon substrates and the consequent reductions in cost [1], [2]. When predicting the power performance of HEMTs, self-heating effects cannot be neglected [3], and this is a problem that has yet to be overcome.

Several methods have been used to measure the thermal resistance (temperature rise per Watt) of GaN-based HEMTs. In a study by Kuzmík [4], a value was obtained by making use of the DC output characteristics at room temperature (subsequent current traces required the device charge to be restored) and the temperature dependences of the saturation drain current, threshold voltage and source resistance (where the assumption of no temperature dependence for the electron saturation velocity was made). Measurements of the drain current time-domain dynamic response to positive drain bias pulses (i.e. pulsed thermal dynamic behavior) were used in [5]. Detailed temperature profiles can be created using IR thermography, and in particular by high-spatial-resolution Raman thermography [6]. However, these thermography techniques are not always practical, since specific device samples and equipment are usually required in the laboratory. Finally, pulsed measurement is a feasible methodology for obtaining the thermal resistance at different ambient temperatures [3], [7]–[9], and this is the approach used in the present work.

Various studies have been carried out of the dependence on the geometry of the measured thermal resistance of GaN-based HEMTs [4], [7], [10]. However, unlike for silicon-on-insulator (SOI) metal–oxide–semiconductor field-effect transistors (MOSFETs) [11]–[15], modeling of this dependence has not been extensively conducted. Most recent works are based on numerical simulations [16], [17], and have given rise to elaborated analytical closed-form expressions for thermal resistance, including device geometric parameters, different layer thicknesses, and the corresponding thermal conductivities [18], [19]. However, they do not account for implanted layer composition, which is usually unknown and can significantly influence the self-heating of the device [20].

The use of thermal circuits that include several thermal resistances and capacitances is another option for the modeling of self-heating effects [21]. However, although detailed thermal models are desirable in order to achieve a complete physical representation, simplification is necessary when dealing with compact models, which is the main topic of this work.

The transistors under study and the experimental setup are described in Sections II and III, respectively. Section IV explains the methodology used, and the thermal resistances resulting from varying the gate geometry and gate-to-drain extension are discussed and modeled in Section V. Finally, our conclusions are presented in Section VI.

II. Device Structure

The AlGaN/GaN layer stack of the HEMTs investigated here (provided by CEA-Leti) consisted of Ga(Al)N epitaxial layers grown on a Si substrate of thickness 1 mm in the

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