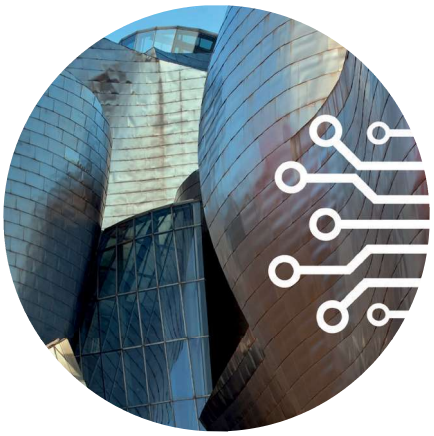
Proceedings

XXXIV Conference on Design of Circuits and Integrated Systems

2019
February 20^{th}-22^{nd}
Bilbao, Spain



DCIS 2019

XXXIV Conference on Design of Circuits and Integrated Systems

20-22 November. Bilbao (Spain)

Organizer

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14:00-16:00 **5A POWER ELECTRONICS** — **BAROJA ROOM**

Chairman: **Nicola Delmonte.** University of Parma.

14:00 ***Super Class AB OTA Based on Current-Starved Nonlinear Mirrors and Dynamic Biasing.***
Antonio López-Martin, Jose M. Algueta, M. Pilar Garde, Ramon G. Carvajal, Jaime Ramírez-Angulo.

14:25 ***A 1.2-V GaAs MMIC Ultra-Low-Noise Amplifier for K-band Applications.***
David Galante Sempere, Daniel Mayor Duarte, Mario San Miguel Montesdeoca, Sunil Lalchand Khemchandani, Javier del Pino.

14:50 ***Power Amplifiers Load Modulation Techniques for 5G in GaN-on-Si Techonology.***
Victoria Díez Acereda, Ayoze Diaz Carballo, Roberto Rodríguez Hernández, Javier del Pino, Sunil Lalchand Khemchandani.

15:15 ***FPGA and CPU based real-time simulation platform for EV propulsion system analysis under driving cycles.***
Markel Fernández, Edorta Ibarra, Endika Robles, Oihane Cuñado, Maite Aranguren, Iñigo Kortabarria, Yahia Bouzid.

15:40 ***Fast and efficient prototype system for embedded control algorithms in electric traction.***
Carlos Cuadrado Viana.

5B INDUSTRIAL AND MEDICAL APPLICATIONS — **ARRIAGA ROOM**

Chairman: **José Machado da Silva.** University of Porto.

14:00 ***Accelerating Host-Compiled Simulation by Modifying IR code: Industrial application in the spatial domain.***
Hector Posadas, Eugenio Villar.

14:25 ***A plethysmographic sensor for monitoring volumen changes in cardiovascular pathologies.***
Enrique Rando, Gloria Huertas, Alberto Yufera.

14:50 ***Resolution enhancement of VCO-based ADCs by passive interpolation and phase injection.***
Leidy Mabel Alvero González, Eric Gutiérrez Fernandez, Luis Hernández Corporales.

15:15 ***Dermatologic Hyperspectral Imaging System for Skin Cancer Diagnosis Assistance.***
Himar Fabelo, Verónica Melian, Beatriz Martínez, Patricia Beltrán, Samuel Ortega, Margarita Marrero, Gustavo M. Callicó, Roberto Sarmiento.

15:45-16:30 ***2019 meeting of IEEE CAS Spain Chapter.*** — **BARANDIARAN ROOM**

16:00-16:30 Coffee break.

16:30-18:30 ***Best paper award of the IEEE CEDA Spain Chapter.*** — **BAROJA ROOM**

PANEL: Women and Engineering.
"Where are we? Where should we be? How to get there?"

Co-sponsored by the Spain Chapter of IEEE CEDA.
Organizers: Francisco Fernández (CEDA, Univ. Sevilla), Carlos López Barrio (UPM), Marisa López Vallejo (UPM).
Participants: Teresa Riesgo (UPM and Dirección General de Investigación, Desarrollo e Innovación Spanish Government), Celia López Ongil (Univ. Carlos III), Julia Merino Fernández (Tecnalia), Linda Milor (Georgia Tech), Eduard Alarcon (UPC).

How to promote STEM degrees between female students.
Women in male-dominated professions. Is it a problem?
Promotion of women to leadership positions. Which are the obstacles?
Is society taking the correct measures? Is our community taking the correct measures? Should we take measures?".

20:00-24:00 Conference Dinner at Yandiola - Azkuna Zentroa.

A 1.2-V GaAs MMIC Ultra-Low-Noise Amplifier for K-band Applications

D. Galante-Sempere, D. Mayor-Duarte, M. San-Miguel-Montesdeoca, S.L. Khemchandani and J. del Pino
Institute for Applied Microelectronics (IUMA), Departamento de Ingeniería Electrónica y Automática
Universidad de Las Palmas de Gran Canaria
Las Palmas de Gran Canaria, Spain

***A*bstract— A four-stage K-band MMIC Low-Noise Amplifier (LNA) is designed using a 70 nm GaAs mHEMT OMMIC process (D007IH). Based on Momentum EM simulation results, the four-stage LNA achieves a gain of 29.5 dB ±1 dB, a Noise Figure (NF) as low as 1 dB and an Input Return Loss better than -10 dB across the band. The LNA chip size is 2500µmx1750µm. The design work flow allows the improvement of the NF and the Input Return Loss of the LNA since the source impedance is selected to minimize the number of elements required to implement the input matching network. The input matching network of the proposed circuit consists of a single tapered octagonal inductor in series with the gate of the active device, resulting in a low impact for the NF achieved by the first stage and a remarkable improvement of the Input Return Loss of the LNA.**

Index terms: Low Noise Amplifier (LNA), Monolithic Microwave Integrated Circuit (MMIC), Noise Figure (NF), Input Return Loss, Electromagnetic Simulation, Gallium Arsenide (GaAs), K-band.

I. Introduction

III-V semiconductor compounds have attracted the attention of integrated circuit designers in the latest years. For instance, gallium nitride (GaN) devices exhibit numerous advantages in terms of power management and efficiency, and they possess the ability to withstand high input signal levels [1]. On the other hand, gallium arsenide (GaAs) technologies provide a very low noise figure (NF) at higher frequencies. Thus, GaAs devices are suitable for systems with very restrictive noise requirements and high frequency scenarios such as mmWave applications, radio satellites, TV broadcast and 5G networks. The K-band, operating from 18 to 27 GHz, is of particular interest since it is typically utilised for satellite communications and high-resolution radar, as well as short range military aircraft radios and astronomical observations. In addition, Monolithic Microwave Integrated Circuit (MMIC) processes offer a compact solution to implement discrete components as well as complete radio interfaces [2]. One of the main components of wireless transceivers is the Low-Noise Amplifier (LNA). The NF contributed by this element directly adds to that of the receiver, affecting its overall sensitivity and linearity [2], [3]. Few works have been reported demonstrating LNAs with a NF below 2 dB while achieving a high gain and reduced Input Return Loss [4]–[6]. In this work, a four-stage GaAs MMIC Low-Noise Amplifier with a NF below 1 dB and a DC Supply of 1.2 V is presented. The LNA operates in the upper end of the K-band (25.5 GHz up to 27 GHz), achieving a total gain of 29.5 dB with 1 dB ripple and an Input Return Loss as low as -12 dB at a centre frequency of 26 GHz. In Section II, the design approach for this circuit is explained, while Section III provides key details regarding the proposed design. Section IV shows the simulation results of the final LNA design and some conclusions are drawn in Section V.

II. Design Approach

The implementation of the first stage of the LNA is vital for the overall performance of the amplifier. The most common approach to design this stage is to select a source impedance that leads to the minimum NF possible. This solution requires a large number of elements to implement the input matching network, which yields a poor NF. In order to avoid this situation, the first stage of the LNA can be designed for minimum Input Return Loss and the active device can be selected so that its optimum source impedance (S_{opt}) presents a real part of approximately 50 Ω. To achieve maximum power transfer, the conjugate match must be achieved at the input. Since the real part of the S_{opt} is 50 Ω, the matching network must only cancel the imaginary part of this impedance. By following this approach, the number of elements needed in the input signal's path is minimized.

To prove the validity of the above statement, two single stage amplifiers were simulated. The first amplifier was designed for minimum NF (NF_{min}) while the second one was designed following the approach described above. Since the contribution of the first stage to the overall NF is critical, once it is successfully implemented the requirements for subsequent stages can be relaxed.

The value of V_G and V_D for both amplifiers is fixed to -0.1 V and 1.2 V, respectively. The device size selected for minimum NF is 8x28 µm, obtaining an ideal NF_{min} of 0.432 dB and a maximum gain of 6.8 dB. To approximate the real part of the S_{opt} to 50 Ω, a device size of 6x25.5µm is selected, obtaining a slightly higher NF_{min} (0.436 dB) and a maximum gain of 8.1 dB. The selected source impedance for the minimum NF amplifier is given by equation (1) and the load impedance is given by equation (2). The selected source and load impedances for the second amplifier are given by expressions (3) and (4), respectively. Note that source and load impedances are very close to each other for the latter case.

$$Z_{S1} = 38.6 + j \cdot 8.6\ (\Omega) \quad (1)$$

$$Z_{L1} = 47.75 + j \cdot 17.65\ (\Omega) \quad (2)$$

$$Z_{S2} = 49.95 + j \cdot 19.7\ (\Omega) \quad (3)$$

$$Z_{L2} = 52.2 + j \cdot 21.7\ (\Omega) \quad (4)$$

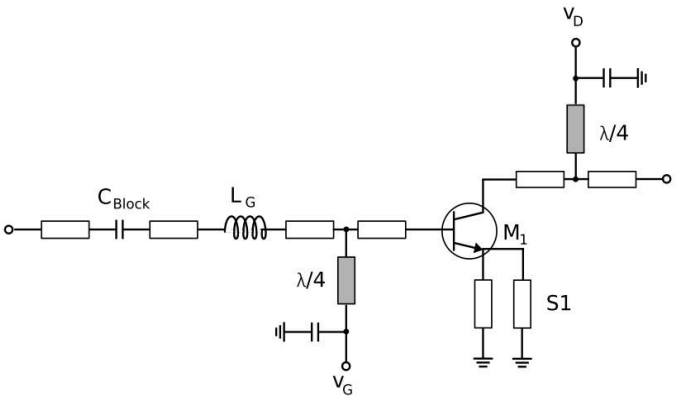


Fig. 1. Simplified schematic of the single stage Low-Noise Amplifier.

Simulations were performed using the Advanced Design System (ADS) software and OMMIC's D007IH process models. Simulation results reveal that the NF_{min} amplifier requires a shunt inductor of 0.557 nH and a series capacitor of 0.39 pF, yielding a noise figure of 0.61 dB and a gain of 6.621 dB. On the other hand, the second approach needs a single series inductor with a value of 0.184 nH, resulting in a NF of 0.554 dB and a gain of 7.98 dB. These results show that our proposal provides better results than the traditional approach. However, the noise performance of the input matching network can be further improved by minimizing the series resistance (loss) of the inductor, which results in a higher quality factor at the frequency of interest [3].

III. Proposed Design

The OMMIC D007IH GaAs process is selected for the proposed design. The technology is characterized by a 70 nm gate length, a f_T of 300 GHz and a NF of 0.5 dB @ 30 GHz. Each stage of the LNA is implemented with the topology shown in Fig. 1. Each stage is designed with 6x25.5 µm, 6x23.5 µm, 6x23.5 µm and 6x23.5 µm transistors, respectively. A V_G of -0.1 V and a V_D of 1.2 V are applied to all the transistors in order to obtain a DC drain current of 30.2 mA for M1 and 28.7 mA for M2-M4. A simplified schematic of the four-stage LNA is shown in Fig. 2 and the layout of the circuit is depicted in Fig. 3. The die size of the full amplifier is 2500µmx1750µm.

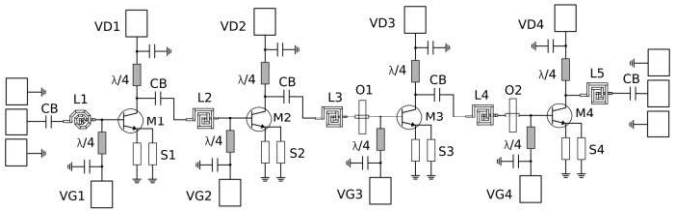


Fig. 2. Schematic of the proposed four-stage Low-Noise Amplifier.

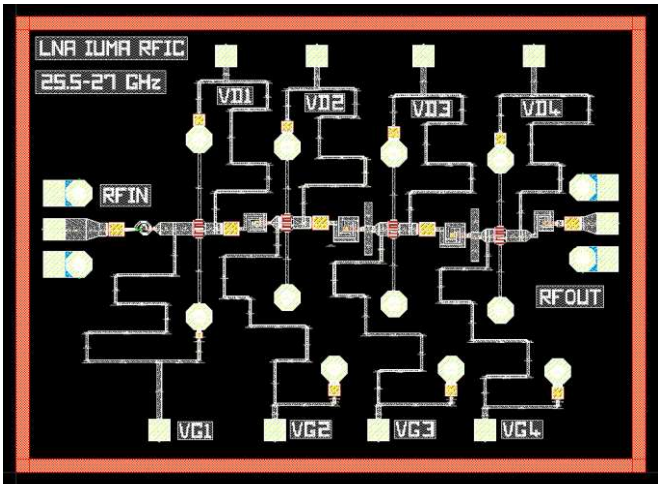
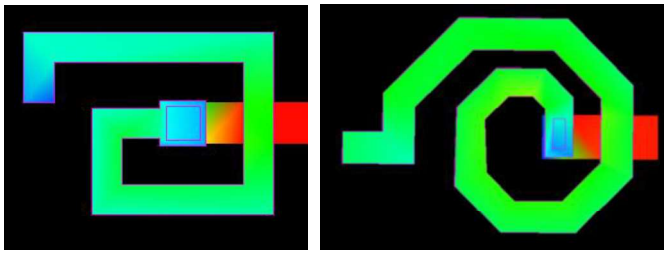


Fig. 3. Layout of the Low-Noise Amplifier.

Source feedback is applied to all the transistors due to the multiple advantages it provides [6]. Namely, it prevents instability and improves the Process-Voltage-Temperature (PVT) variations of the circuit. The inductance arising from the two source transmission lines (S1 in Fig. 1 and 2) allows the input impedance of the transistor to approximate to the optimum source impedance (S_{opt}). Thus, source feedback can improve the Input Return Loss of the LNA. The size of S1 is 250µmx10µm in order to achieve stability and a reduced NF for the first stage. Transmission lines S2, S3 and S4 have a size of 200µmx10µm, which is enough to stabilize the transistors and obtain a slightly higher gain than that of the first stage. Quarter wavelength transmission lines (λ/4) with a length of approximately 1 mm and a shunt capacitor (0.74 pF) are used as RF Chokes to bias the active devices [7]. The main advantage of this approach is that it barely affects the matching networks and it has a low impact on the overall NF of the LNA. Finally, a DC Block capacitor (CB in Fig. 2) of 1.18 pF is placed between stages to provide DC isolation.

As previously mentioned, the quality factor (Q) of the input matching network has a great impact in the NF of the first stage of the LNA. Therefore, the implementation of the inductor included in the input matching network is a key parameter. For the proposed design, a square inductor provided by the PDK was tested using EM simulations (Fig. 4(a)). Fig. 5 shows that the inductance and quality factor of this inductor are adequate. However, to minimize the series resistance of the inductor, a custom octagonal tapered inductor [8], [9] with a tapering of 1µm per turn, shown in Fig. 4 (b), was tested. Its EM simulation results are also presented in Fig. 5.



(a) (b)

Fig. 4. Simulated current density of the (a) square and (b) octagonal tapered inductor at 26 GHz.

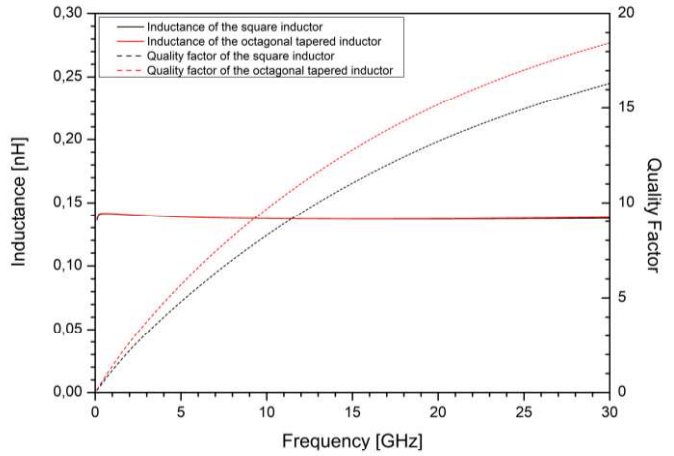


Fig. 5. Inductance and quality factor of the implemented inductor.

As shown in Fig. 5, the inductance of both elements is similar (the goal was to provide an inductance of 0.138 nH at 26 GHz), although the quality factor of the octagonal inductor is larger (17.34 @ 26 GHz for the octagonal inductor vs 15.2 @ 26 GHz for the square one). These results can be explained in terms of two mechanisms. Firstly, it is widely known that the quality factor of a rectangular inductor can be increased by approximating its geometry to that of an ideal spiral inductor. This approach improves the current circulation and, therefore, reduces the losses across the inductor's geometry. The quality factor can be further improved if the number of sides or the number of turns is increased while the inductance value is maintained [3]. Secondly, the skin and proximity effects may produce severe current crowding at the inner turns of the inductor, limiting its quality factor [8], [10]. As presented in [8], a higher Q can be obtained if the strip widths of the inner turns are reduced. Therefore, a tapered inductor can achieve a higher Q than a regular inductor. For this reason, the octagonal tapered inductor was selected to implement the input matching network of the LNA, as depicted in Fig. 2.

Once the first stage is successfully designed with a NF of 0.9 dB and a gain of 7.2 dB, the requirements for the next stages can be relaxed so they can be designed to provide a higher gain. As depicted in Figs. 2 and 3, the impedance matching network between stages 1-2 is achieved by means of a single square inductor (L2) with a value of approximately 0.37 nH. To implement the matching networks between stages 2-3 and 3-4, inductors L3, L4 (0.36 nH each) and two double open stubs (O1, O2) were used. The double open stubs O1 and O2 have a size of 30µmx90µm and 30µmx100µm, respectively. Finally, the output matching network is implemented with a single series inductor L5 of 0.24 nH.

IV. Simulation Results

Scattering and noise parameters were simulated at room temperature with ADS software and Momentum EM simulator. The resulting Input and Output Return Losses are depicted in Fig. 6, and the gain and NF are presented in Fig. 7. The simulated LNA presents an Input Return Loss of -12 dB at 26.25 GHz and an Output Return Loss of -23 dB at the same frequency. A gain of 29.5 dB ± 1 dB across the band of interest, and a NF of 1 dB are obtained. The device isolation coefficient (S_{12} parameter) is lower than -47 dB in the band of 25.5 GHz to 27 GHz. As shown in Fig. 8, the value of the stability factor *k* is above unity for all frequencies, and presents a minimum value of 2.760 at a frequency of 13.2 GHz. Individual stability was ensured as well, concluding that the amplifier is unconditionally stable.

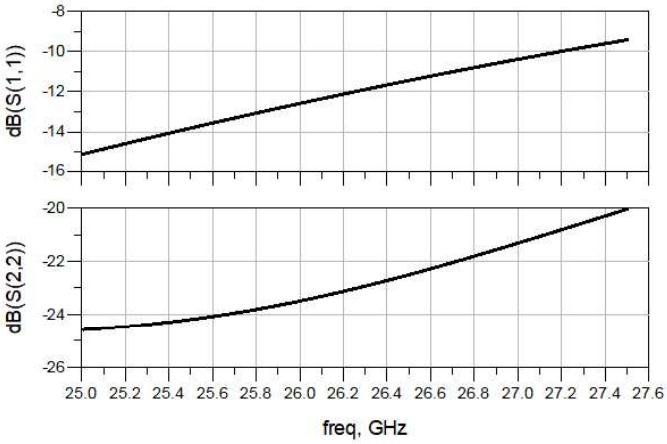


Fig. 6. Input and Output Return Loss of the proposed LNA.

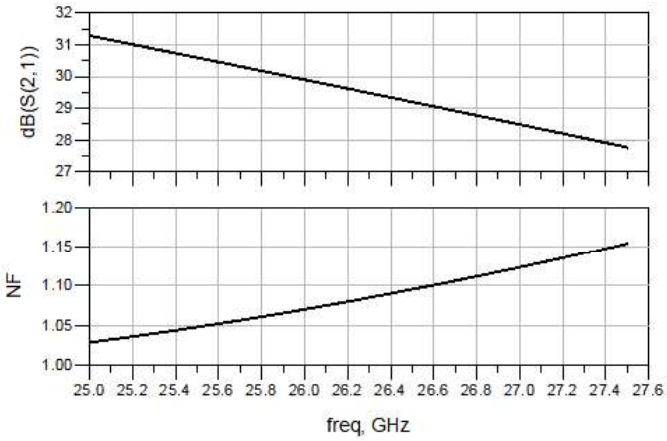


Fig. 7. Gain and Noise Figure of the proposed LNA.

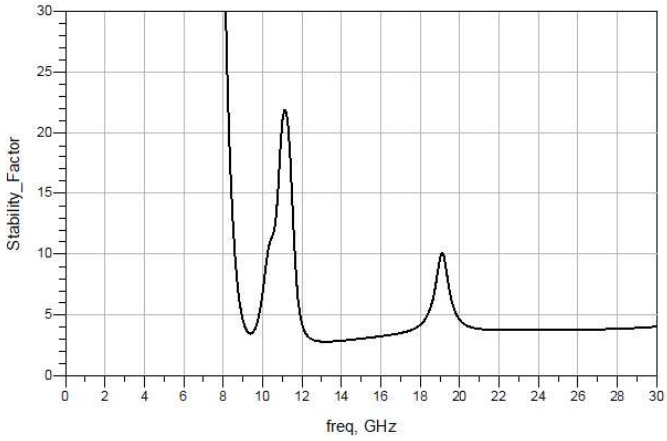


Fig. 8. Stability factor of the proposed LNA.

The main results of the proposed design and a brief overview of similar works are given in Table 1. To the authors' knowledge, the results presented in this work are expected to deviate from the simulations to some extent. However, the

overall performance of the circuit is expected to stay within the requisites. The performance of the proposed LNA is similar to other GaAs LNAs so far reported in the same frequency band at room temperature.

Table 1. Results summary and overview of similar works.

	[4]	[5]	[6]	*This Work*
Freq. Range (GHz)	*26-36*	*25-31*	*18-31*	*25.5-27*
Gain (dB)	*33 ±0.7*	*22*	*22*	*29.5 ±1*
Noise Figure (dB)	*1.5*	*1.7*	*1.7*	*1*
Input Return Loss (dB)	*-12*	*-12*	*<-30*	*-12*
Output Return Loss (dB)	*-12*	*-20*	*<-20*	*-20*
Supply (V)	-	*3.5*	*3.5*	*1.2*
Process	*GaAs 100 nm*	*GaAs 90 nm*	*GaN 100 nm*	*GaAs 70 nm*
Area (μm^2)	*2800x1300*	*2400x1000*	*2300x1000*	*2500x1750*

V. Conclusions

An approach to enhance the NF and Input Return Losses of MMIC LNAs is presented in this paper. The design work flow allows the improvement of the NF and the Input Return Loss of the LNA since the source impedance is selected to minimize the number of elements required to implement the input matching network. Two single stage amplifiers are designed and simulated at room temperature to compare the performance with the traditional approach, showing remarkable improvements in the Noise Figure and Input Return Loss of the amplifier.

A four-stage K-band MMIC Low-Noise Amplifier based on the previous approach is also presented. The LNA is designed using the models of the 70 nm GaAs mHEMT OMMIC process. The input matching network of the first stage consists of a single tapered octagonal inductor in series with the gate of the active device. The LNA is DC-biased with 1.2 V and the chip size is 2500µmx1750µm. Electro-magnetic simulation results at room temperature prove that the four-stage LNA achieves a total gain of 29.5 dB with 1 dB ripple, a Noise Figure as low as 1 dB, an Input Return Loss better than -10 dB and an Output Return Loss better than -20 dB across the band of interest.

VI. Acknowlegments

This work is partially supported by the Spanish Ministry of Economy and Competitiveness (TEC2015-71072-C03-01), the Canary Agency for Research, Innovation and Information Society (ACIISI) of the Canary Islands Government (ProID2017010067) and by the Spanish Ministry of Science, Innovation and Universities (RTI2018-099189-B-C22).

VII. References

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