Power Amplifiers Load Modulation Techniques for 5G in GaN-on-Si Technology

V. Díez-Acereda, A. Diaz-Carballo, R. Rodríguez-Hernández, J. del Pino and Sunil L. Khemchandani

Institute for Applied Microelectronics (IUMA), Departamento de Ingeniería Electrónica y Automática
Universidad de Las Palmas de Gran Canaria
Las Palmas de Gran Canaria, Spain

Abstract— **A Doherty power amplifier (DPA) and a Chireix power amplifier for 5th Generation (5G) wireless applications are presented in this paper. The power amplifiers are integrated in OMMIC 100 nm GaN-on-Si process. In both amplifiers, the λ/4 T-Line are replaced with lumped-elements to reduce its area. The DPA presents a P_{sat} of 34 dBm (>2.5 W), a peak PAE of 41% and a 9.4 dB gain at 3.6 GHz. At 7 dB output back-off (OBO) it exhibits a 34.2% PAE. On the other hand, the Chireix outphasing PA provides a P_{sat} of 32 dBm (>1.5 W), a peak PAE of 54.9%, a gain of 10.4 dB and a 25 % PAE at 7 dB OBO. The occupied area of the DPA and Chireix amplifiers are 3.26 mm^2 and 3.2 mm^2, respectively, including pads.**

Keywords—Doherty PA, Chireix Outphasing PA, Power Added Efficiency (PAE), Output power Back-Off (OBO), GaN, 5G

I. INTRODUCTION

Modern wireless communications such as 5th Generation (5G) are coming with many challenges [1], [2]. Due to presence of large number of independently modulated subcarriers in an orthogonal frequency-division multiplexing (OFDM) system, the peak value of the system can be very high as compared to the average of the whole system. Peak-to-average power ratio (PAPR) is the relation between the maximum power of a sample in a given OFDM transmit symbol divided by the average power of that symbol expressed in dB. In order to provide high data rates, 5G technology is characterized for having a very high PAPR. As a result, the efficiency at output power back-off (OBO) of the power amplifiers (PA) needs to be improved as well as maintaining a high linearity.

5G has three frequency bands divided in low frequency band, high frequency band and millimeter wave band. The frequency range of the first band is from 600 to 700 MHz and it is normally used for traditional local coverage applications such as Internet of Things (IoT), transport infrastructure and vehicle-to-everything (V2X). The high frequency band covers from 2.5 to 7 GHz and it can be used for higher throughput data transfer and finally, the mm-wave band, whose frequency is above 24 GHz and it will allow for wireless hotspots to emerge [3].

For many years, several PA architectures have been reported to solve this challenge by using two back-off efficiency enhancement techniques: bias modulation and load modulation. The most common bias modulation techniques are the envelope elimination and restoration (EER) [4] and the envelope tracking (ET) [5]. While the Doherty power amplifier (DPA) [6] and the Chireix outphasing PA [7] are the most popular solution of load modulation techniques. Currently, the DPA and the ET techniques are becoming more relevant for 5G [8].

In this paper, load modulation techniques area used to design a Doherty and a Chireix outphasing PAs for 3.4−3.8 GHz meeting 5G requirements [9]. To cater the specifications of high efficiency and linearity, the PAs were designed using the OMMIC 100 nm GaN-on-Si process with depletion mode transistors. This technology uses a high resistivity silicon starting material below the active layer epitaxy. The DPA and the Chireix outphasing PA are described in Sections II and III, respectively. Simulation results of both PAs are shown in Section IV. Finally, some conclusions are drawn in Section V.

II. DOHERTY PA

The architecture of the DPA was presented in 1936 by W. H. Doherty [6]. The block diagram of the DPA is shown in Figure 1 which is composed of a power splitter, a Main (or Carrier) amplifier and an Auxiliary (or Peaking) amplifier. As seen in the figure, the Main PA is followed by a λ/4 transmission line (T-Line), which is added for the proper load modulation. To match the delay through this line, another λ/4 T-Line is inserted in the input of the Auxiliary amplifier.
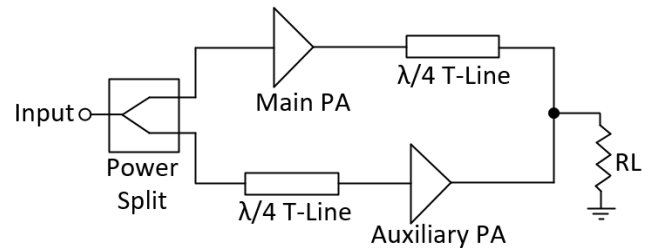

Figure 1. DPA block diagram.

The DPA behavior is depicted in Figure 2 and it is divided into two operating regions: the low-power region and the Doherty region. In the low-power region, only the main PA (Class-B or AB) is turned on while the auxiliary PA is off due to its Class-C polarization, which needs a higher input signal to produce a current flow. When the main amplifier reaches its saturation and it achieves the first efficiency peak, the Auxiliary amplifier is turned on, entering in the Doherty

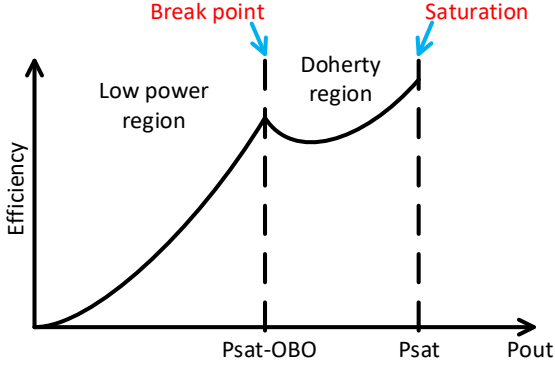region. At maximum output power, the second efficiency peak is achieved.

Figure 2. DPA behavior.

A. Design of the DPA

The main amplifier was biased in Class-AB and the auxiliary was polarized in Class-C. The schematic of DPA is depicted in Figure 3 where an asymmetric configuration was adopted and the peaking amplifier is larger than the main amplifier. To avoid instabilities, an RC network was added in the main amplifier (R1 and C1) [10]. In order to reduce the number of components, and minimize the circuit area, a 90-degree hybrid coupler was used [11]. This coupler divides the input power and provides the 90-degree phase difference of the λ/4 T-line, so this line can be eliminated.

At 3.6 GHz, the transmission lines take a large area (7700 μm long and 81 μm wide) and as a result, they cannot be integrated into a chip. For this reason, the output λ/4 T-line was designed with lumped-elements (π-network) composed by C10, L10 and C11 [12]. Lck are choke inductors and capacitors C2−C5 are used for impedance matching and as a coupling capacitors.

As seen in Figure 3, there are inductors in parallel with capacitors which can be eliminated at the expense of resizing other PA passive components. All changes on the circuit were applied carefully and one at a time. For each change, the PAE performance was degraded and then an optimization was done to recover the previous performance. The final schematic of the DPA is shown in Figure 4.
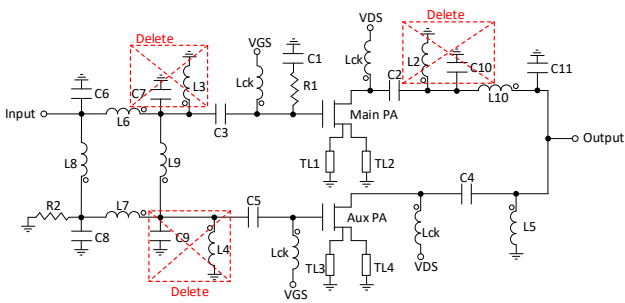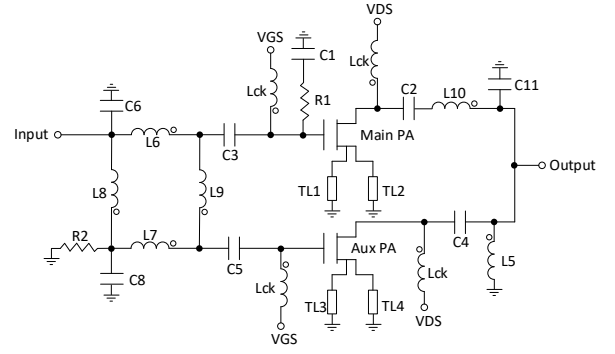

Figure 3. DPA schematic.

Figure 4. Final DPA schematic.

B. Layout implementation of the DPA

The DPA was fully integrated in D01GH process. The scheme takes up an area of 2517.1 μm x 1293.5 μm. It was not possible to integrate the Lck inductors due to their high value. As seen in Figure 5, RF PADs were positioned on the left and right border of the chip and bias PADs on the top and bottom.
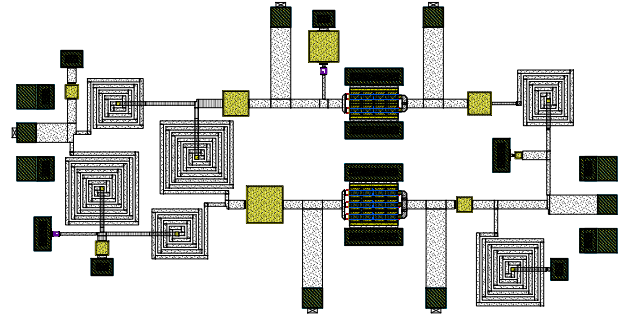

Figure 5. Layout implementation of the DPA.

III. CHIREIX OUTPHASING PA

A year before Doherty presented his amplifier, the outphasing power amplifier was developed by Chireix in 1935 [7]. A few years later, its application was extended to microwave frequencies under the name of linear amplification using non-linear components (LINC).

The block diagram of the outphasing PA is illustrated in Figure 6: the input signal component separator (SCS) network translates the amplitude-modulated (AM) signal into two constant-envelope phase-modulated (PM) signals with opposite phase. These two signals are amplified by high efficiency nonlinear amplifiers and added together to produce the output AM signal, improving the efficiency in back-off.
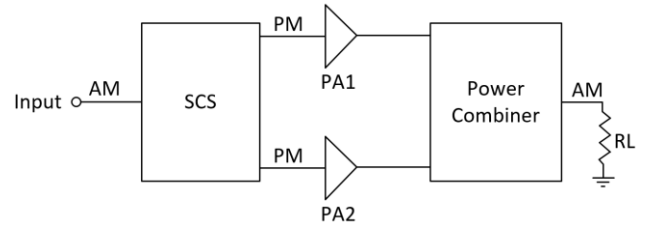

Figure 6. Block diagram of the Outphasing PA.

A. Design of the Chireix Outphasing PA

The schematic of the Chireix PA is shown in Figure 7 where a symmetrical configuration was chosen. The PAs were

biased in Class-B which provides a good trade-off between efficiency and linearity. To avoid instabilities, an RC network was added at the input of the amplifiers (R1 and C1) [10]. Passive components (L4, C4, L5 and C5) are used as polarization network and also to avoid unwanted oscillations of the power supply that can affect the circuit. Inductors and capacitors (L2, C2, L3 and C3) are used to match the input and the output.

The amplified AM signal at the output can be combined with a λ/4 T-Line. However, due to the large area of this line, the quarter-wavelength combiner was replaced by an LC balun (C6, L6, C7 and L7).

As seen in Figure 7, there are components that can be eliminated or merged because they are in parallel with inductors or capacitors. Therefore, L2 and C6 from PA1 are eliminated because they are in parallel and inductors L2 and L7 from PA2 are merged. The resulting schematic of the Chireix outphasing PA is shown in Figure 8.
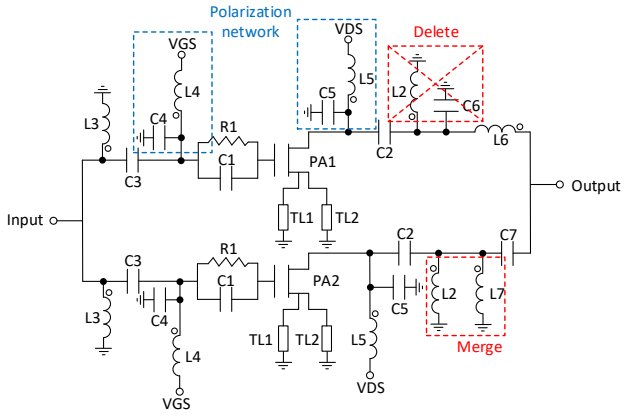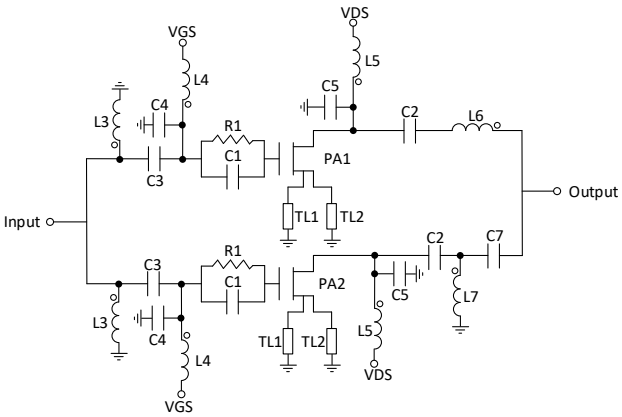

Figure 7. Chireix outphasing PA schematic.

Figure 8. Final Chireix outphasing PA schematic.

B. Layout implementation of the Chireix Outphasing PA

The layout implementation of the Chireix outphasing PA is shown in Figure 9. The layout of this PA takes up an area of 1755 μm x 1824 μm and it was fully integrated in D01GH process. The input and output PADs are on the right and left of the circuit, and the bias PADs are on top and the bottom.
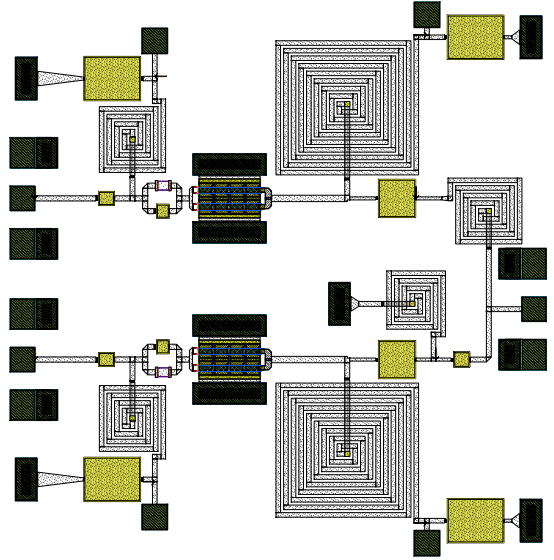

Figure 9. Layout implementation of the Chireix outphasing PA.

IV. COMPARATIVE SIMULATION RESULTS

The PAE performance of each DPA amplifier is depicted in Figure 10. As seen in the figure, the main PA (blue signal) was designed to enter on the compression region in a lower output power than the auxiliary PA (red signal). The distance in dB between the compression points of both PAs can guess the back-off of the final DPA. The gain of each DPA amplifier is shown in Figure 11, a similar behavior is shown as in PAE performance.
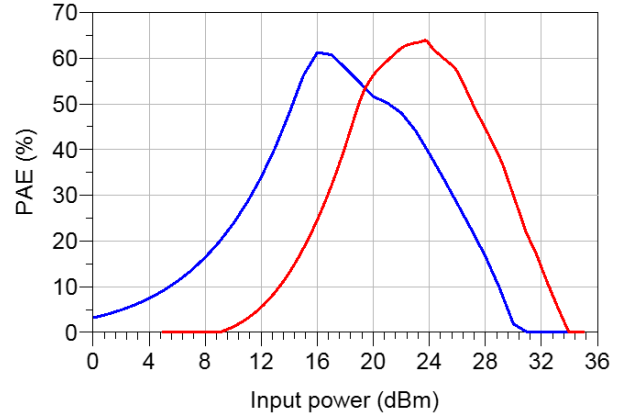

Figure 10. PAE vs input power of the DPA, the main amplifier (blue) and the auxiliary amplifier (red).
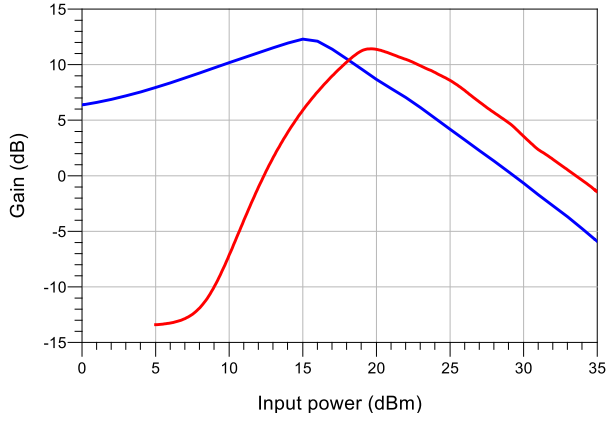
Figure 11. Gain vs input power of the DPA, the main amplifier (blue) and the auxiliary amplifier (red).

Figure 12 shows the large signal simulation results of the DPA and Chireix PAs. The DPA exhibits a saturated output power of 34 dBm. For that point, the gain value is 8.1 dB and the PAE is 41%. On the other hand, the Chireix outphasing PA provides a saturated output power of 32 dBm, the gain is 9.8 dB and the PAE is 54.9% at this point. The saturated output power was calculated at 1 dB output compression. Focusing on the OBO performance, the DPA provides a PAE of 34.2% and a gain of 9.9 dB, while the Chireix outphasing PA exhibits a PAE of 25% and a gain of 10.8 dB at 7 dB OBO.
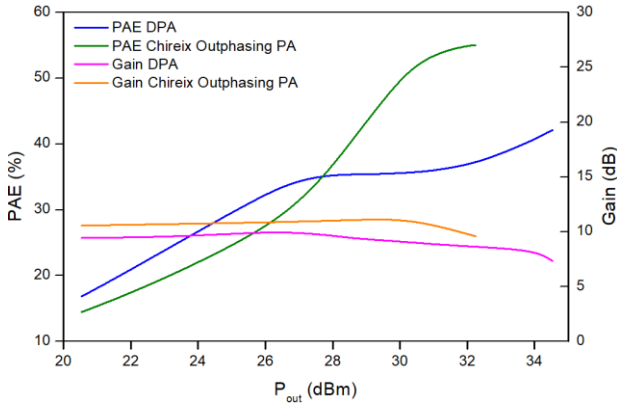

Figure 12. Large signal post-layout simulation results at 3.6 GHz.

Figure 13 shows the small signal post-layout simulation results of both PAs. At 3.6 GHz the gain in the DPA is 9.4 dB and in the Chireix outphasing PA is 10.4 dB. The S11 in the DPA and in the Chireix outphasing PA is -8 dB and -20.3 dB, respectively. The Chireix PA provides a better input matching than the DPA.
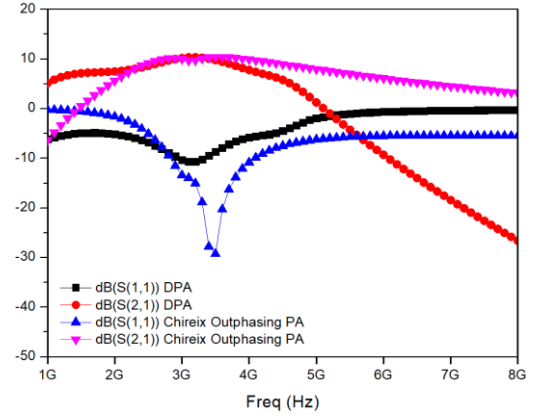

Figure 13. Small signal post-layout simulation results at 3.6 GHz.

V. CONCLUSIONS

This paper describes the design and layout implementation of a Doherty power amplifier and a Chireix outphasing power amplifier using OMMIC 100 nm GaN-on-Si process (D01GH) for 5G wireless applications. In both amplifiers, the $\lambda/4$ T-Line were replaced with lumped-elements to reduce their area. A comparison to the state-of-art GaN Doherty and Chireix outphasing PAs is presented in Table I. For the same frequency band, the Chireix outphasing PA provides a higher value of gain and PAE than the DPA with less P_{sat}. However, at OBO region, the DPA structure exhibits better results of PAE.

Table I. Comparison performance with recently reported PAs.

	[13]	[14]	[15]	[16]	**This work**	**This work**
Freq (GHz)	3.3-3.6	3.3-3.75	9.7	3.1-3.7	3.4-3.8	3.4-3.8
P_{sat} (dBm)	44.3	48-48.8	36.8	42.9	34	32
PAE_{max} (%)	52	58-71[a]	57.4	>42	41	54.9
PAE @OBO (%)	44	44-55[a]	44.1	>21	34.2	25
Gain (dB)	28-29	14	-	-	9.4	10.4
Architecture	Chireix PA	DPA	Chireix PA	Chireix PA	DPA	Chireix Outphasing PA
PA Class	Class-E	Class-J	Class-F	Class-B	Class-AB and Class-C	Class-B
Technology	GaN	GaN	GaN	GaN	GaN	GaN

a. *Drain efficiency*

REFERENCES

[1] M. Jaber, M. A. Imran, R. Tafazolli, and A. Tukmanov, '5G Backhaul Challenges and Emerging Research Directions: A Survey', *IEEE Access*, vol. 4, pp. 1743–1766, 2016.

[2] J. G. Andrews *et al.*, 'What Will 5G Be?', *IEEE J. Sel. Areas Commun.*, vol. 32, no. 6, pp. 1065–1082, Jun. 2014.

[3] '5G Spectrum GSMA Public Policy Position', 2018.

[4] F. Wang *et al.*, 'An Improved Power-Added Efficiency 19-dBm Hybrid Envelope Elimination and Restoration Power Amplifier for 802.11g WLAN Applications', *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 12, pp. 4086–4099, Dec. 2006.

[5] Feipeng Wang, A. H. Yang, D. F. Kimball, L. E. Larson, and P. M. Asbeck, 'Design of wide-bandwidth envelope-tracking power amplifiers for OFDM applications', *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 4, pp. 1244–1255, Apr. 2005.

[6] W. H. Doherty, 'A New High Efficiency Power Amplifier for Modulated Waves', *Proc. IRE*, vol. 24, no. 9, pp. 1163–1182, Sep. 1936.

[7] H. Chireix, 'High Power Outphasing Modulation', *Proc. IRE*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.

[8] Qian-Fu Cheng, Shou-Kui Zhu, and H.-F. Wu, 'Investigating the global trend of RF power amplifiers with the arrival of 5G', in *2015 IEEE International Wireless Symposium (IWS 2015)*, 2015, pp. 1–4.

[9] P. M. Asbeck, N. Rostomyan, M. Ozen, B. Rabet, and J. A. Jayamon, 'Power Amplifiers for mm-Wave 5G Applications: Technology Comparisons and CMOS-SOI Demonstration Circuits', *IEEE Trans. Microw. Theory Tech.*, vol. 67, no. 7, pp. 3099–3109, Jul. 2019.

[10] I. J. Bahl, 'Stability Analysis', in *Fundamentals of RF and Microwave Transistor Amplifiers*, Hoboken, NJ, USA: John Wiley & Sons, Inc., 2018, pp. 479–505.

[11] A. Grebennikov and S. Bulja, 'High-Efficiency Doherty Power Amplifiers: Historical Aspect and Modern Trends', *Proc. IEEE*, vol. 100, no. 12, pp. 3190–3219, Dec. 2012.

[12] R. W. Vogel, 'Analysis and design of lumped- and lumped-distributed-element directional couplers for MIC and MMIC applications', *IEEE Trans. Microw. Theory Tech.*, vol. 40, no. 2, pp. 253–262, 1992.

[13] M. Ozen, M. van der Heijden, M. Acar, R. Jos, and C. Fager, 'A Generalized Combiner Synthesis Technique for Class-E Outphasing Transmitters', *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 64, no. 5, pp. 1126–1139, May 2017.

[14] C. Huang, S. He, and F. You, 'Design of Broadband Modified Class-J Doherty Power Amplifier With Specific Second Harmonic Terminations', *IEEE Access*, vol. 6, pp. 2531–2540, 2018.

[15] M. Litchfield, T. Cappello, C. Florian, and Z. Popovic, 'X-Band GaN Multi-Level Chireix Outphasing PA with a Discrete Supply Modulator MMIC', in *2016 IEEE Compound Semiconductor Integrated Circuit Symposium (CSICS)*, 2016, pp. 1–4.

[16] A. Piacibello, R. Quaglia, M. Pirolaf, and S. Cripps, 'Design of an S-Band Chireix Outphasing Power Amplifier Based on a Systematic Bandwidth Limitation Analysis', in *2018 13th European Microwave Integrated Circuits Conference (EuMIC)*, 2018, pp. 186–189.