High Performance CMOS Level up Conversion for Systems with Low-Voltage Power Supply

José-Carlos García and Juan A. Montiel-Nelson
Institute for Applied Microelectronics. University of Las Palmas de Gran Canaria, Spain
{jcgarcia, montiel}@iuma.ulpgc.es

S. Nooshabadi
Department of Electrical and Computer Engineering, Michigan Technological UniversityMichigan, USA
saeid@mtu.edu

Abstract— **A single supply CMOS non-inverting level shifter circuit, *ccm-ls*, for converting input signals from 0.3V up to 0.7V is presented. The circuit is optimized and pre-layout simulated in a 65nm CMOS process technology. At the target design voltage of 0.3V, the level shifter has a propagation delay of 1.06ns, an energy consumption of only 0.79pJ, and energy-delay product of 0.84pJns for capacitive load of 1pf. Simulation results are compared to other similar published works at a frequency of 500 MHz, and it shown that the proposed circuit outperforms them.**

Keywords: Up converter; voltage domain; low-energy; low-voltage; single supply; level shifting; bootstrap; CMOS design

I. INTRODUCTION

In recent years, there has been considerable research effort in the development of low-energy consumption level shifters, with very small supply voltage and improved subthreshold range due mainly to their low-power application in portable systems. Several level converters topologies have been proposed to achieve voltages in the order of a few mV with a low-voltage power supply. Multi-threshold voltage CMOS processes are used in the design of voltage level shifter in order to reduce delay (with low-threshold transistor) and power (with high threshold transistor). The design presented in [1] uses a level shifter to connect the output of a 2:1 multiplexer operating at supply voltage of 0.2V to a static random access memory (SRAM) operating at 1V supply voltage; the circuit was implemented in a 90nm CMOS technology. The work in [2], reported a level shifter using a diode-connected transistor and dynamic current switching. Requiring a control circuit, only during the high-to-low transitions of the output, a current is forced into the diode-connected device. The proposed circuit was fabricated in both 40nm and 180nm standard CMOS technologies. The level converter in [3] achieves low power by employing a new topology based on a reduced-swing buffer while a pass transistor enhances the speed of the fall transition so that the conversion delay can be significantly improved. Measurement results from a test chip fabricated in 65nm CMOS technology show low leakage and high speed. The reported level shifter can convert deep sub-threshold voltage as low as 100mV to the super-threshold voltage of 1.2V.

This paper deals with a high performance level up shifter, *ccm-ls*, designed to convert near-threshold voltages to power supply voltage level. The remainder of this work is organized as follows. Section II presents the proposed voltage level up shifter. In Section III, pre-layout simulation results are discussed and evaluated. Section IV is dedicated to compare the proposed design with other reported circuit, *ss-ls*, modified [4]. Section V describes the comparison between *ccm-ls* and other CMOS level converters of the state-of-the-art. Post-layout simulation details are presented in Section VI. Finally, Section VII concludes the work.

II. CIRCUIT TOPOLOGIES AND OPERATION

Fig. 1 shows a level shifter termed *ss-ls* based on a bootstrap capacitor (MPC) which is charged to supply voltage (Vddh), this enables to increase the output level of node 3 during low to high transitions at node 1. The drain of MP6 charges MPC in conjunction with MP2 up to Vddh-Vddl. The current source (MP5 and MP6) is only turned on during a low to high transition at the input node (in). When MN2 is turned on, MPC provides a negative voltage that turns MN3 off quickly and reduces the static leakage current.

In this work we propose a 6-stage circuit shown in Fig. 2, termed *ccm-ls*. The first inverter has a diode-connected transistor (MN7) for reducing the voltage at node 6 to Vddh-0.3V, and for minimizing the static power consumption when node in is in high logic level, where MN1 is on.

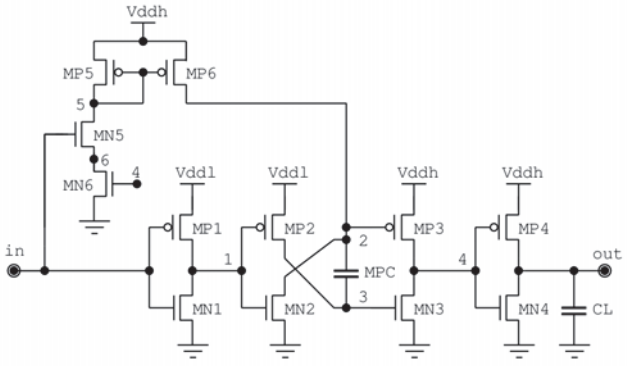

Figure 1. The circuit diagram for *ss-ls*, modified [4].

978-1-7281-0397-6/19/$31.00 ©2019 IEEE

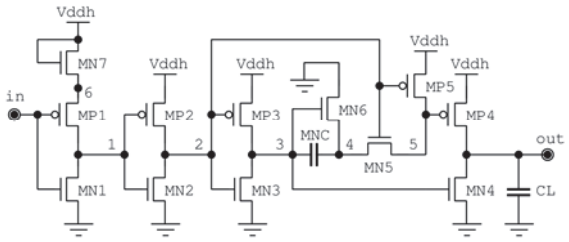

Figure 2. Schematic for *ccm-ls* level up shifter.

The principal stage is the fourth, which consists of MN6 and MNC. If node in is low, node 3 is high, and MNC is charged through MN6, MN4 is also turned on and the output, node out, is set to low. In addition, in that case, node 2 is low, MP3, and MP5 conduct, whereas MN5 and MP4 are turned off. If a high logic level is applied at node in, node 1 and 3 are low, MN5 conducts, and MP4 quickly turns on, so that output is pulled up. Table I shows channel widths for transistors in both circuits (length = 65nm). Note that active area for *ss-ls* is three times higher than that for *ccm-ls*. Sizing for both circuits is obtained for the best figure-of-merit criterion of energy-delay-product (EDP). In contrast to *ss-ls*, *ccm-ls* is capable of operating correctly with an input signal of 0.3V for a supply voltage of 0.7V, and a capacitive load of 1pF, with a propagation time delay of 1.06ns, the energy consumption of 0.79pJ, and EDP of 0.84pJns.

III. SIMULATION RESULTS

Fig. 3 illustrates simulation waveforms of both designs when the input signal has a voltage level of 0.38V, Vddl is 0.38V, and Vddh is 0.7V. Operating frequency is 500MHz, and the load capacitance is 600fF. Fig.3 shows that propagation time delay for *ss-ls* is 1.35ns and for *ccm-ls* is 0.89ns. Each circuit is simulated adding a parasitic capacitor of 25fF and an inverter with 80µm/20µm PMOS/NMOS channel widths ratio connected to node out. It is observed that they both exhibit a rail-to-rail switching characteristic.

Fig. 4 presents optimized EDP when the input signal is 0.38V and the capacitive load ranges from 60 to 600fF for both

TABLE I. SIZING FOR PMOS AND NMOS TRANSISTORS

Ss-ls (Active area = 103.35µm^2)			***Ccm-ls*** (Active area = 30.43µm^2)		
Transistor(s)	***Type***	***Width (µm)***	***Transistor(s)***	***Type***	***Width (µm)***
MP1	P	28 x 10	MP1	P	6 x 10
MP2	P	4 x 10	MP2	P	0.4 x 10
MP3	P	15 x 10	MP3, MP4	P	2 x 10
MP4	P	6 x 10	MP5	P	1 x 10
MP5, MP6	P	2 x 10	MNC	N	0.025 x 10
MPC	P	50 x 10	MN1, MN7	N	10 x 10
MN1	N	5 x 10	MN2	N	2 x 10
MN2	N	12 x 10	MN3, MN5	N	0.2 x 10
MN3	N	4 x 10	MN4	N	8 x 10
MN4	N	1 x 10	MN6	N	5 x 10
MN5, MN6	N	15 x 10	—	—	—

VThn = 0.28V and VThp =- 0.2V. The channel length for all transistors is 65nm.

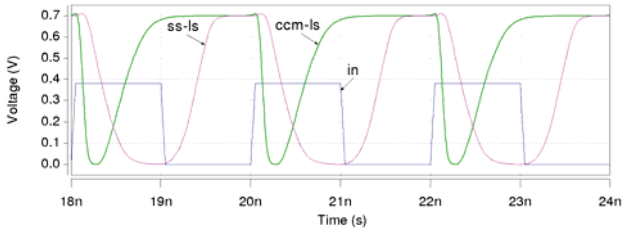

Figure 3. Waveforms using a capacitive load of 600fF.

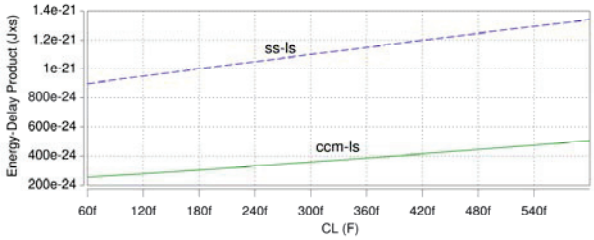

Figure 4. Energy-delay-product versus capacitive load for *ss-ls* and *ccm-ls* circuits.

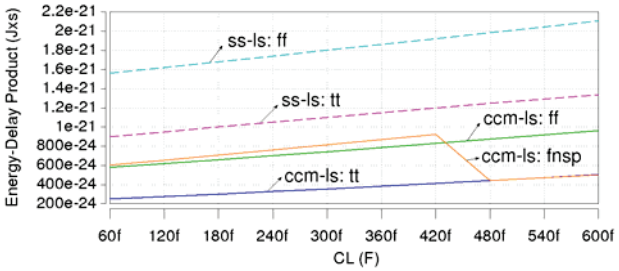

Figure 5. Energy-delay-product for *ss-ls* and *ccm-ls* circuits at different process corners.

ss-ls and *ccm-ls* circuits. Variation in load capacitance effects on the *ss-ls* is far more than on *ccm-ls*.

Fig. 5 compares EDP results for typical-typical and fast-fast process corners considering a working frequency of 500MHz. For fast NMOS-slow PMOS case, *ss-ls* fails to operate correctly, unless the input frequency is reduced to 320MHz. For the slow-slow process corner the, frequency of operation needs to reduce to below 160MHz for the correct operation of both *ss-ls* and *ccm-ls*. For the process corner of slow NMOS-fast PMOS, *ccm-ls* works correctly at 400MHz. In contrast *ss-ls* can only achieve that a maximum frequency of 250MHz.

A decrease of a 10% in Vddh reduces the operational frequency to 200MHz for the case of *ccm-ls*. For *ss-ls* the corresponding reduction in frequency is 400MHz. However, both crcuits perform correctly when Vddh is increased by 10%. In this case *ccm-ls* presents a 60% lower EDP than *ss-ls* at 500MHz. EDP comparisons at 200MHz, across a range of capacitive loading, are shown in Fig. 6 for the Vddh variation of ±10% at 0.7V. *Ccm-ls* exhibits a much better EDP.

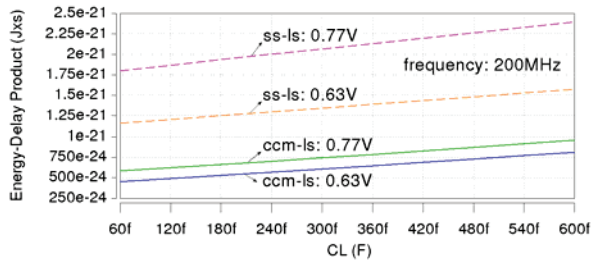

Figure 6. EDP for *ss-ls* and *ccm-ls* circuits evaluated for different voltage corners at 200Mhz when the input signal level is 0.38V.

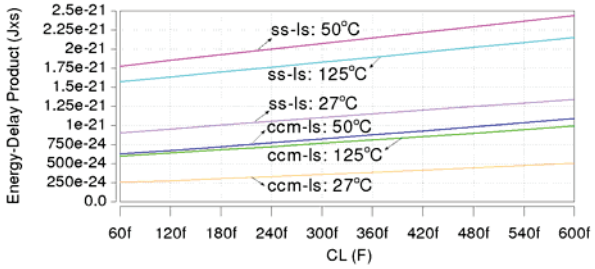

Figure 7. EDP for *ss-ls* and *ccm-ls* circuits evaluated for different positive temperatures at 500MHz when the input signal level is 0.38V.

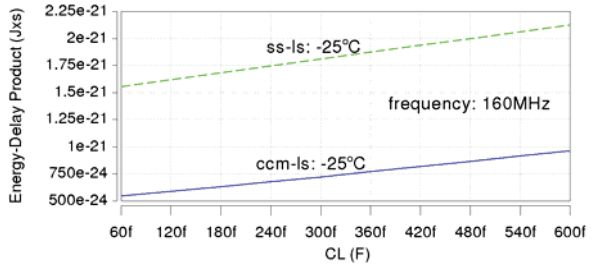

Figure 8. EDP for *ss-ls* and *ccm-ls* circuits evaluated for a negative temperatures at 160MHz when the input signal level is 0.38V.

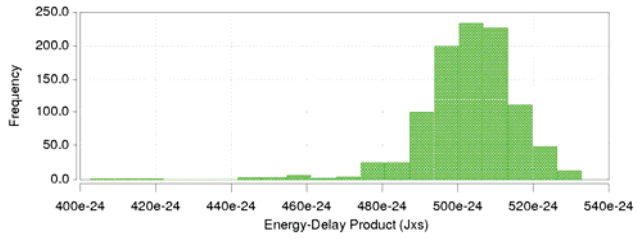

Figure 9. Histogram for EDP of *ccm-ls* at 500MHz when the input signal level is 0.38V

Simulations results for three different positive workig temperatures are shown in Fig. 7. *Ccm-ls* exhibits the best EDP at 27°C. For the negative working temperature of -25°C,

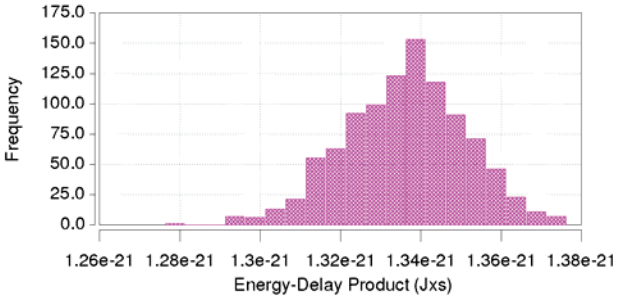

Figure 10. Histogram for EDP of *ss-ls* at 500Mhz when the input signal level is 0.38V.

the input signal frequency must be decreased to 160MHz for both *ccm-ls* and *ss-ls*. Fig. 8 shows the EDP comparison for the case in which the temperature is -25 °C. At 600fF output loading condition EDP for *ccm-ls* is 54.7% lower than the required for *ss-ls*. To analyze how mismatch in the device paramters affects the performance of *ccm-ls*, a 1000-point Monte Carlo simulation is shown in Fig. 9. The mean for EDP, μ, is 502.89pJps and standard deviation, σ, is 13.01pJps, and normalized variance value of σ/μ of 0.02. The EDP shows a very small sensitivity toward device parameters mismatch. More than a 70% of all simulated results for *ccm-ls* fall between 490 and 520pJps. Fig. 10 exposes the similar histogram for *ss-ls*. The spread for *ss-ls* has a mean of 1336pJps and a standard deviation of 14.97pJps. The normalized variance value, σ/μ, is 0.01, lower than that required for *ccm-ls*.

IV. Pre-layout comparison results

The two circuits are simulated in 65nm CMOS technology process with input supply voltage of 0.38V. From the results, it is observed that propagation time delay and EDP for *ccm-ls* are 34% and 62.4% lower than those for *ss-ls*, respectively. Considering only the power supply of Vddh, with the load of CL=600fF, the static currents for *ccm-ls* for the cases of low and a high input levels are 0.13μA and 0.28μ, respectively. In other words, *ccm-ls* has got 72% and 54% lower static current than *ss-ls*, respectively. Note that *ss-ls* uses a second power supply, Vddl that introduces an additional static power consumption.

V. Comparison with other published level shifters

Table II presents the differences between *ccm-ls* and references [1]-[4]. Our converter denotes pre-layout results as [1] but *ccm-ls* uses a higher capacitive load. Delay for [1] is roughly ten times higher than obtained for *ccm-ls*. However, [1] has lower active area and power consumption than *ccm-ls* apart from a wider input voltage range of conversion. In [2] is used a CMOS technology with the lowest gate length than the rest of designs in Table II. In addition, [2] improves the area, power consumption and conversion range in comparison with *ccm-ls* but requires a higher EDP. Circuit in [3] uses the same

technology node as *ccm-ls*, and both has similar EDP using different operational frequency. Design in [3] improves area, power consumption and the input voltage range but its output capacitive load is unknown. Delay for [3] is 7 times higher than *ccm-ls*. On the other hand, design in [4] presents a chip area, delay, EDP, and conversion range greater than required for *ccm-ls* using a capacitive load that is 100 times smaller.

TABLE II. COMPARISON TO THE STATE-OF-THE-ART

Design	**[1]**	**[2]**	**[3]**	**[4]**	***ccm-ls***
Year	2016	2018	2018	2017	2018
Technology	90nm CMOS	40nm CMOS	65nm CMOS	180nm CMOS	65nm CMOS
Results	Pre-layout	Measure	Measure	Measure	Pre-layout
Area	1.12µm^2	12µm^2	7.45µm^2	229.5µm^2	30.43µm^2
Delay	10.99ns @ 0.2V	80ns @ 0.3V	7.5ns @ 0.3V	29ns @ 0.4V	1.06ns
Power	1.52nW	0.18nW@ 0.35V	123.8nW	61.5nW	395µW
Frequency	Not available	10KHz	1MHz	500KHz	500MHz
EDP (FoM)	Not available	1.44pJns	0.92pJns	3.56pJns	0.84pJns
Load	1fF	4 inverters	Not available	10fF	1pF
Voltages (V)	0.1 to 1	0.05 to 1.1	0.1 to 1.2	0.33 to 1.8	0.3 to 0.7

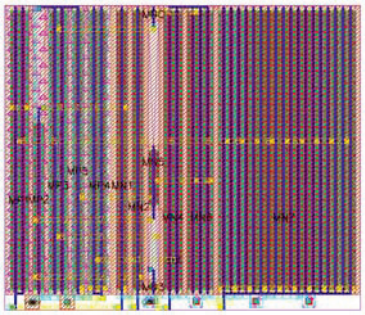

Figure 11. Layout for *ccm-ls* with the core area of W×H is 12.63µm × 10.85µm.

VI. POST-LAYOUT SIMULATION RESULTS

It is necessary to reduce the operating frequency from 500MHz to 400MHz when the input signal reaches the limit of 0.7V and the output is set to 0.7V with a CL of 50fF. We use layout shown in Fig. 11 to evaluate the effective input conversion range of *ccm-ls* at 400MHz operating frequency. It is demostrated that it is feasible to work with the input signal range of 0.38 to 0.7V, with the output voltaje of 0.7V while achieving a low EDP. Table III prsenents the the transistor sizing for the layout in Fig. 11 using optimized EDP strategy and output full swing at 50fF load capacitance. In this case, EDP is 0.46pJns, and delay is 1.24ns at 400MHz.

We can maintain an input voltage in the range of 0.3V to 0.7V at an increased operating frequency up to 500MHz at CL to 525fF with a design resizing. For this purpose is necessary to modify the width for MN1 (10×10µm), MN2 (2×10µm), MN3 (0.1×10µm), and MP1 (6×10µm). Active area for the resized design is 30.50µm^2. The core area for *ccm–ls* is 16.35µm×10.85µm (WxH). The EDP for this layout is 0.65pJns and the delay is 1.47ns.

TABLE III. POST-LAYOUT SIZING FOR *CCM-LS* OPERATING AT 400MHZ

Ccm-ls (Active area = 21.35µm^2)		
Transistor(s)	***Type***	***Width (µm)***
MP1, MP3 and MP4	P	2 x 10
MP2	P	0.6 x 10
MP5	P	1 x 10
MNC and MN3	N	0.025 x 10
MN1 and MN2	N	1 x 10
MN4	N	2 x 10
MN5	N	0.2 x 10
MN6	N	3 x 10
MN7	N	18 x 10

VII. CONCLUSIONS

A low power bootstrapped CMOS level shifter is designed in order to reduce power consumption and enhance the speed of switch for up shifting and driving a large load. According to the HSPICE simulation results, the proposed level converter reduces the EDP figure-of-merit by 62.4% compared to a similar reported design at 500MHz and with a capacitive load of 600fF.

ACKNOWLEDGMENT

This work was funded by project SURF (TEC201460527C21R) of the Spanish Ministry of Economy and Competitiveness.

REFERENCES

[1] P. Gosatwar and U. Ghodeswar, "Design of voltage level shifter for multi-supply voltage design," in Proc. ICCSP, Apr. 2016, pp. 853–857.

[2] R. Lotfi, M. Saberi, S. R. Hossini, A. R. Ahmadi-Mehr, and R. B. Staszewski, "Energy-efficient wide-range voltage level shifters reaching 4.2fJ/transition," IEEE Solid-State Circuits Letters, vol. 1, no. 2, pp. 34–37, Feb. 2018.

[3] V. L. Le and T. T.-H. Kim, "An area and energy efficient ultra-low voltage level shifter with pass transistor and reduced-swing output

buffer in 65-nm CMOS," IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 65, no. 5, pp. 607–611, May 2018.

[4] E. Maghsoudloo, M. Rezaei, M. Sawan, and B. Gosselin, "A high-speed and ultra low-power subthreshold signal level shifter," IEEE Trans. Circuits Syst. I, vol. 64, no. 5, pp. 1164–1172, May 2017.