Temperature Dependent Thermal Capacitance Characterization for SOI-MOSFETs

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***Abstract*—Thermal capacitances are required to describe fast dynamic thermal behavior in SOI devices. This paper presents a physical model based on the AC technique, together with the characteristic thermal frequency determination through the frequency response of the output conductance, for calculating the thermal capacitance of single-finger and multi-finger SOI-MOSFETs. The model accounts for total gate width and substrate temperature, making evident the augmented thermal coupling when multi-fingers are used. Thermal capacitances and corresponding time constants, extracted from a variety of gate widths and number of fingers, are correctly predicted up to a substrate temperature of 150°C.**

Index Terms—**electrothermal characterization, model, SOI-MOSFET, substrate temperature, thermal capacitance.**

I. Introduction

Silicon-on-insulator (SOI) MOSFETs, having a buried oxide layer thicker than 100 nm, suffer from a reduction of the heat flow towards the substrate [1], [2]. This, together with the ultra-thin internal layers used at nanometer length scales, with a reduced thermal conductivity [3], [4], results in a remarkable self-heating effect, particularly in DC operation/biasing with relevant electrical power levels involved (as from dozens of mW [5]). This makes the design and configuration of terminals, acting as heat sinks, critical in SOI-MOSFET performance [1], [6].

The typical thermal model for the temperature rise in devices, induced by self-heating effects, consists of the equivalent circuit shown in Fig. 1, with the thermal resistance, R_{th}, and capacitance, C_{th}, being connected in parallel. This model is based on the following analogy between electrical

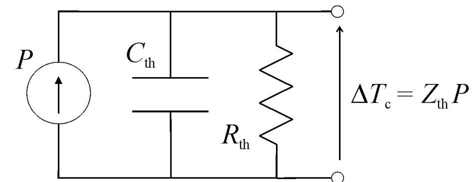

Fig. 1. Equivalent circuit for self-heating effects in devices.

and thermal magnitudes: The temperature rise in the device channel, ΔT_c, above the substrate temperature, T_{sub}, is actually the "voltage drop" when the "current" flowing through the circuit is the electrical power dissipated, P, in the device (i.e. $\Delta T_c = Z_{th}P$, with $1/Z_{th} = 1/R_{th} + j\omega C_{th}$). By making use of more sophisticated thermal networks [7], hot spots could even be localized (i.e. not only the average device temperature can be determined). Nevertheless, our thermal model maintains a higher degree of simplicity, to be useful in the context of compact model development for circuit simulators.

For DC response, the SOI-MOSFET thermal resistance has been extensively investigated in the literature [8–11]. Regarding characterization, several well-established techniques have been used for obtaining the thermal resistance, such as the AC/RF conductance method [8], pulsed characteristics [9], [10], or with impedance analyzers [11]. Regarding modeling, precise and simple enough compact models for circuit simulation purposes have been developed, including thermal coupling in case of multi-finger devices [12–17].

With respect to the thermal capacitance, it is necessary to describe the fast dynamic thermal behavior in SOI devices subjected to abrupt changes in power generation [7], which was also demonstrated in [9], with the decrease of drain current as SOI-MOSFETs heat up after being turned on. Despite this, too few studies concerning this thermal capacitance issue have been published, and more advancement in both measurement techniques and modeling is required.

Small-signal equivalent circuit analysis has been used for investigating heat flow paths in SOI-MOSFETs [18]. Nevertheless, empirical approaches are needed, such as fitting of the elements of the electrical/thermal circuit or the use of multiple-pole RC networks for the thermal part [6], [15].

Other studies are based on the transient response to pulsed measurements and the determination of the thermal time constant, τ_{th} ($\tau_{th} = R_{th}C_{th}$) [19]. This method has been applied to high-voltage MOSFETs, when a resistance connected to

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