GENERADOR Y VOBULADOR

DE

AUDIOFRECUENCIAS

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INDICE

Pagina

Página

INTRODUCCION

El sonido es una vibración o una perturbación rítmica que actúa dentro de un campo de frecuencias audibles. La menor es de unos 20 Hz (periodos por segundo) y la mayor, también audible, de unos 20.000 Hz.

Este trabajo está basado en el estudio de la respuesta de un determinado equipo a las señales comprendidas en el margen de audio. Este espectro de señales pueden ser analizadas de muy diversas formas, dependiendo del problema que queramos resolver en cada momento.

La principal división que podemos hacer en lo que se refiere al análisis de las señales, es representarlas en el dominio del tiempo, o por el contrario estudiarlas en el dominio de las frecuencias. Si expresamos la señal como una función del tiempo,

f(t), estaremos trabajando en el dominio del tiempo. Si por el contrario la señal es representada como una función de la frecuencia, estaremos especificando su espectro, es decir, las amplitudes de las diferentes componentes de frecuencia.

De forma general, podríamos decir que el método a seguir para estudiar el comportamiento de un equipo, es generar una señal patrón. Esta señal patrón debe cumplir unas exigencias mínimas de distorsión y estabilidad. Introduciendo esta señal patrón en el equipo a analizar, nos sirve de referencia para su estudio posterior.

Son muchas las formas de generar esta señal patrón, y muchas las formas de medirla. Por ejemplo, con un generador de funciones podremos producir una señal de una frecuencia y amplitud fijas. Esta onda introducida en el equipo bajo test, podría ser medida y estudiada con un osciloscopio, con el que obtendríamos, la relación de la amplitud de entrada/salida, el desfase, la distorsión aparente, etc. Este sería un estudio en el dominio del tiempo, porque estaríamos visualizando la evolución de la onda

en cada instante. De la misma manera esta señal podría ser estudiada con un analizador de onda, con lo cual estaríamos viendo las amplitudes de su frecuencia fundamental y de sus distintos armónicos. Nos encontramos en este caso en el dominio de la frecuencia.

Entre las muchas formas de generar una onda patrón podríamos mencionar:

Generandor de funciones. Nos produce una onda de frecuencia fija, de la cual podremos seleccionar su forma (onda sinusoidal, cuadrada y triangular, entre las más comunes), su frecuencia, y su amplitud. A parte de esto algunos introducen la posibilidad de variar la simetría de la onda, la modulación, tanto en frecuencia como en amplitud, etc.

Vobuladores o generadores de barrido. Nos producen una onda de amplitud fija, pero cuya frecuencia variará en el tiempo. Esta variación o barrido, hará que la señal vaya pasando de forma progresiva por todas las frecuencias comprendidas dentro de unos márgenes. De esta manera podremos

estudiar la variación en el tiempo de la respuesta del equipo bajo test. Los vobuladores nos dan también la posibilidad de seleccionar la amplitud de la señal, la forma de la onda, los márgenes entre los que se realiza el barrido, y otra serie de parámetros según las características del fabricante. Algunos generadores de funciones también están preparados para realizar este tipo de barridos.

Generadores de ruido. Nos dan una señal compuesta que produce todas las frecuencias del margen de estudio a la misma vez. Así podremos estudiar de una manera global el comportamiento del equipo dentro de todo el margen. Estos ruidos están clasificados según su espectro. Por ejemplo: el ruido blanco, tiene un espectro de potencia igual para cada octava de frecuencia; el ruido rosa, aumenta progresivamente tres Db por octava, etc.

La mayoría de estos equipos están constituídos esencialmente por un oscilador de audio.

Los osciladores de audio están diseñados para generar señales senoidales o casi senoidales en el

margen de frecuencias de 20 a 20.000 Hz. No obstante muchos osciladores de audio cubren el margen de 10 a 40.000 Hz y algunos alcanzan casi los MHz.

Los osciladores de audio se pueden diseñar para que cubran el espectro de audio en un barrido del dial o en varias décadas. Estos osciladores deben tener muy baja distorsión armónica total y una impedancia de salida esencialmente constante para una tensión de salida constante. La distorsión armónica total no debe ser superior a 1% y preferiblemente a 0,25% o menos.

Los osciladores de audio se emplean en las medidas de diferentes dispositivos tales como amplificadores, filtros, ecualizadores y sistemas de registro. Como la mayoría de estos elementos son sensibles a la distorsión armónica, el oscilador de audio debe tener una distorsión armónica interna muy baja. Como ejemplo los sistemas modernos de amplificadores de alta fidelidad presentan distorsiones armónicas del orden de 0,25% e incluso menores.

Si el oscilador de prueba tiene una

distorsión mayor que la del dispositivo a medir, no se pueden realizar medidas exactas de las características de distorsión del mismo. La contribución a la distorsión producida por el oscilador no se puede sustraer directamente de la distorsión medida.

La distorsión del oscilador, a menos que sea extremadamente grande, por regla general no afecta a las medidas de frecuencia.

El generador de barrido de audiofrecuencia es un oscilador de audio el cual recoge automáticamente toda la banda de frecuencias de audio.

En un principio el generador consistía en un disco rotativo en el cual se fotografiaba una onda senoidal comenzando en las frecuencias bajas y aumentando hasta las altas. El disco se hacía girar por un motor síncrono 20 veces por segundo, y la imagen de la onda senoidal se proyectaba en el blanco o diana de células fotoeléctricas, se amplificaba y se aplicaba al dispositivo que se deseaba medir.

La respuesta de frecuencia era observada

visualmente por medio de un osciloscopio conectado a la salida del dispositivo a medir.

En la actualidad esta función se realiza, de un modo más simple, electrónicamente empleando un oscilador de audio controlado por tensión.

El análisis en el campo de las frecuencias, resulta fundamental para el estudio de las señales de audio. Este se apoya sobre una estructura matemática denominada Teorema de Fourier. Este teorema desarrolla cualquier función periódica en el tiempo en una serie de sumas y restas de senos y cosenos.

La onda seno es extrordinaria; agregando este tipo de señales con amplitudes y fase adecuadas, se produce una onda triangular. Respondiendo a una combinación diferente de ondas seno, se puede producir la señal Dientes de Sierra, y así cualquier otro tipo de señal. En otras palabras, cualquier onda periódica es una superposiciòn de ondas senoidales.

Las ondas senoidales están relacionadas armónicamente, lo que quiere decir que sus frecuencias

son armónicas, o múltiplos de una fundamental, la frecuencia mínima. Según el teorema de Fourier, la señal periódica va a ser igual a una componente continua, más la primera armónica, más la segunda, y así indefinidamente hasta infinito.

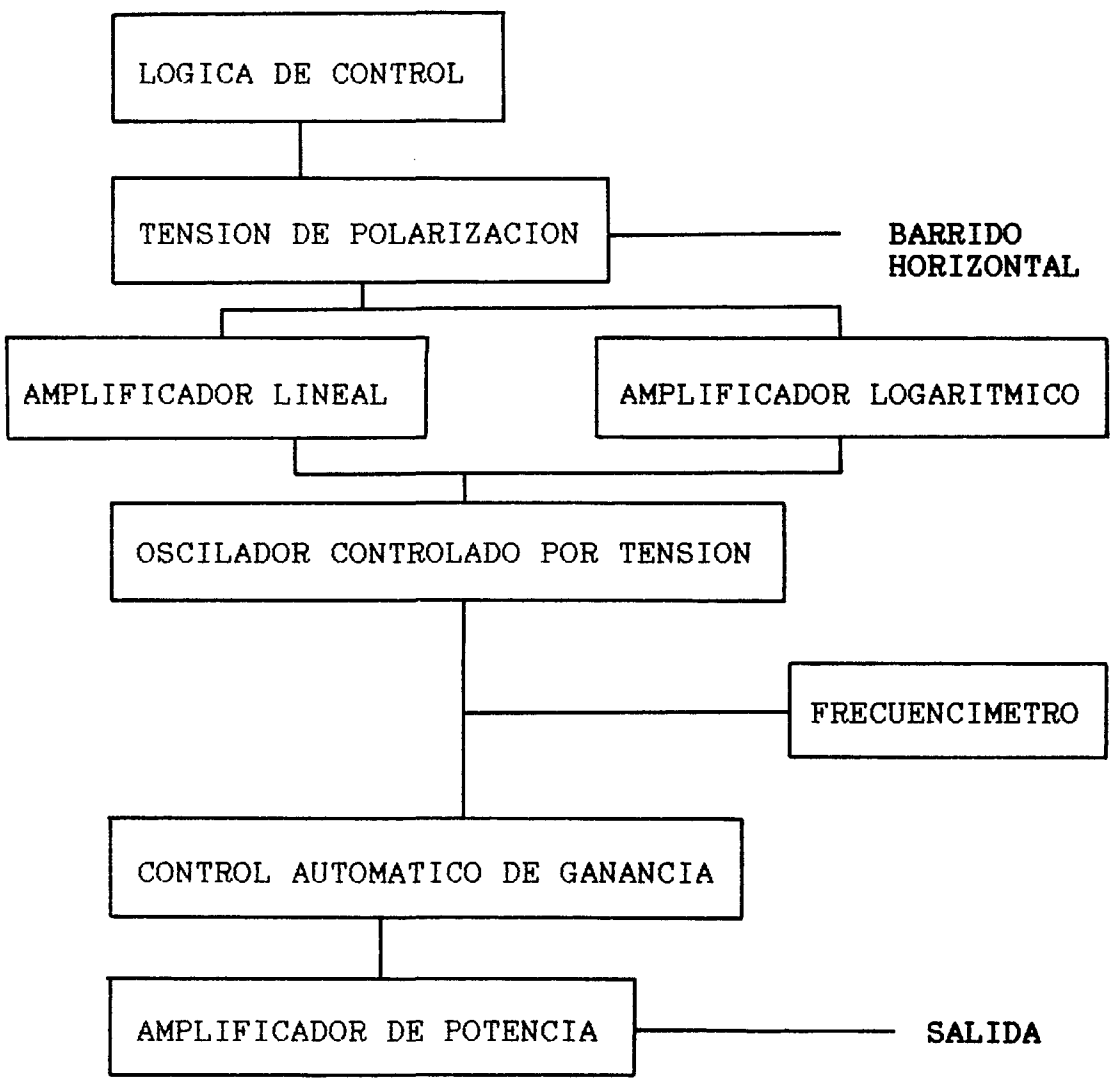
Teóricamente las armónicas continúan hasta infinito, sin embargo, entre cinco y diez términos son con frecuencia suficientes para sintetizar una señal periódica dentro del 5 %. Con una combinación correcta de amplitudes a distintas frecuencias y de angulos de fase, es posible producir cualquier forma de onda periódica.

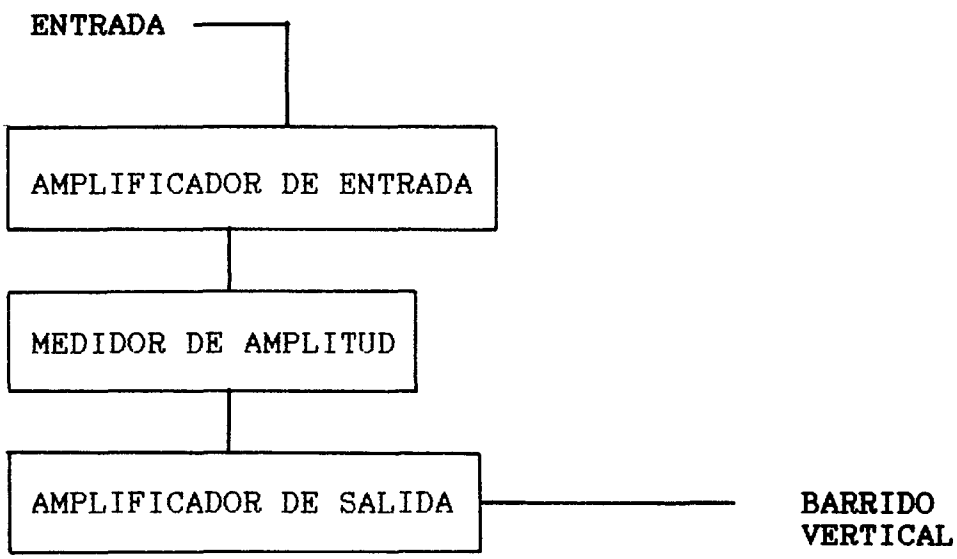
El Teorema de Fourier es clave para el análisis en el dominio de la frecuencia. Como ya se conoce bastante bien el comportamiento de las ondas senoidales, se puede reducir la onda periódica a sus componentes senos y analizarse en seguida en forma indirecta a través de estos componentes; en otras palabras, existen dos formas de efectuar el análisis de circuitos no senoidales. Primero, se puede encontrar lo que sucede con la onda periódica en cada instante de tiempo o determinarse lo que pasa con cada una de sus

componentes armónicas.

DESARROLLO

DIAGRAMA DE BLOQUES





OSCILADOR CONTROLADO POR VOLTAJE

Un oscilador es un circuito capaz de generar a su salida una señal periódica, en ausencia de excitación externa. Consiste en un amplificador de error cuya salida se realimenta a la entrada.

El voltaje de arranque del que parte el oscilador está contenido dentro de cada resistor incluido en éste. Este voltaje se debe al ruido producido por el movimiento de los electrones que existen en el resistor. El resistor se comporta como una pequeña fuente de voltaje que produce esencialmente todas las frecuencias hasta varias decenas de GHz.

Cuando se enciende el oscilador, las únicas señales presentes a la entrada son las producidas por el voltaje de ruido. La frecuencia a la cual funcionará un oscilador senoidal, es aquella en que el desfase total introducido, al transmitirse la

señal desde los terminales de entrada por el amplificador y la red de realimentación, hasta volver de nuevo a la entrada, es precisamente cero, o múltiplo entero de 360 grados.

La ganancia de lazo abierto del circuito realimentado tiene que ser mayor que uno para que empieze a oscilar. La señal, en un principio muy pequeña, irá ganando amplitud hasta que la salida se recorte. En este momento la ganancia del lazo abierto empieza a disminuir hasta llegar a ser la unidad, de esta manera se mantendrá constante la amplitud de la oscilación a la salida. La condición de que la ganancia de lazo sea la unidad se denomina criterio de Barkhausen.

En la práctica, en todo oscilador la ganancia de lazo es ligeramente mayor que la unidad, y la amplitud de las oscilaciones está limitada por la falta de linealidad. En la mayoría de los casos, el trabajo dentro de los límites de la no linealidad es pequeño, por lo cual se podrán despreciar todas estas faltas de linealidad.

En el equipo se ha utilizado un oscilador por corrimiento de fase. El oscilador por corrimiento de fase tiene condiciones particularmente útiles para una gama de frecuencias que va desde algunos hertz a varios cientos de kilohertz, incluyendo por tanto la gama de audiofrecuencias. En cuanto a la banda de los megahertz, presentan mejores ventajas otros circuitos que emplean redes sintonizadas LC.

El oscilador por corrimiento de fase está basado en la realimentación a través de tres redes de adelanto en la entrada de un amplificador con configuración inversora. Cada red de adelanto produce en corrimiento de fase entre 0 y 90 grados, dependiendo de la frecuencia. Por lo tanto, el desfasamiento total de las tres redes de adelanto es igual a 180 grados a una frecuencia en particular. Como las tres redes se realimentan en la entrada inversora, la fase real del lazo es de 360 grados, que equivalen a cero.

El oscilador descrito es en principio el utilizado en nuestro equipo. La única diferencia es que el vobulador no precisa una frecuencia determinada, sino que necesita una consecución de frecuencias

progresiva a lo largo del tiempo. Conmutando resistencias o condensadores podríamos conseguir distintos valores de frecuencia, pero a parte de ser costoso y engorroso, sólo conseguiríamos valores discretos y no progresivos.

El OTA es un dispositivo monolítico de ganancia programable, con entrada diferencial y circuitería de conversión a salida única.

Recibe la denominación de OTA el término Operacional Transconductance Amplifier o Amplificador Operacional de Transconductancia variable. A su vez la transconductancia es una simple abreviación del término Transferencia de Conductancia, y esta última es la recíproca de la resistencia. Dado pues que R = V / I, la transferencia de conductancia es la relación existente entre una corriente de salida y una entrada de tensión.

En efecto el OTA suministra una salida en corriente, en lugar de tensión, que es proporcional a la transconductancia (Gm) y a la tensión diferencial de entrada.

El circuito utilizado para la realización del VCO (Oscilador Controlado por Tensión) es el LM 13600. La serie LM 13600 consiste en dos amplificadores de transconductancia controlados por corriente, cada uno con entradas diferenciales y salidas del tipo Push-Pull. Estos amplificadores tienen una fuente de alimentación común, pero operan independientemente.

El LM 13600 está dotado también de dos diodos de linealización que están colocados en las entradas para reducir la dirtorsión y permitir mayores niveles de entrada. El resultado es una mejora de la relación señal-ruido de 10 dB referido a 0.5 % de THD, (Total Harmonic Distorsion).

Las redes de adelanto que conforman el circuito de realimentación están formadas por filtros RC. Cada una de las redes de adelanto tienen que ser iguales entre sí, siendo el valor de las impedancias el que va a determinar la frecuencia de corte del filtro, y por tanto la frecuencia de la oscilación.

Para obtener anchos de banda superiores a

los obtenidos con redes pasivas, se utilizan los amplificadores operacionales como elementos activos. Existen amplificadores operacionales con productos de ganancia por ancho de banda del orden de 100 MHz. Con estos amplificadores operacionales cabe diseñar filtros activos de frecuencias hasta varios megahertz. El factor que limita la respuesta a plena potencia a estas altas frecuencias es la relación de variación del amplificador operacional.

La relación de variación del amplificador operacional es la evaluación de tiempo de cambio de la tensíon de salida del amplificador en cadena cerrada con señales grandes. Se pueden conseguir comercialmente integrados con relación de variación de hasta 100 V/microseg.

Aprovechando las características del OTA podemos controlar la frecuencia de corte del filtro, y con un ancho de banda lo suficientemente grande como para cubrir todo el margen de audio, sin tener que variar los elementos pasivos del filtro.

Las redes de adelanto utilizadas en la

red de realimentación del oscilador empleado en este equipo estan formadas por tres filtros activos paso-bajo montados con el circuito integrado LM 13600.

El VCO completo utiliza dos encapsulados del LM 13600. De los cuatro amplificadores que conforman los dos encapsulados, tres de ellos están montados con la configuración tipo filtro paso-bajo de la que ya hemos hablado, y el cuarto como amplificador limitador-inversor. Este VCO es teóricamente capaz de operar desde 5 Hz hasta los 50 KHz, con un THD menor que el 1%. La corriente de control del OTA para cubrir este margen va a estar comprendida entre 0 y 1 mA.

En la práctica es difícil conseguir este margen de trabajo. A frecuencias muy bajas la señal sufre serias distorsiones y su amplitud disminuye considerablemente. La frecuencia mínima conseguida con una calidad de señal aceptable está sobre los 10 HZ, pero la amplitud es inferior a la amplitud del resto de las frecuencias. Esta es la razón por la que se ha tenido que introducir en el circuito un control automático de ganancia. De esta manera podremos conseguir una amplitud constante dentro de todo el

margen.

CONTROL AUTOMATICO DE GANANCIA

La señal obtenida a partir del oscilador controlado por tensión cumple las condiciones de estabilidad en cuanto a amplitud y frecuencia, pero la amplitud a lo largo de todo el espectro no es constante.

En los límites más bajos de corriente de polarización, cercana a los 0 miliamperios, no existe señal alguna en la salida del oscilador. Aumentando progresivamente esta corriente, empezamos a obtener una señal aceptable a partir de los 7 o 10 Hz. A partir de este punto la señal va aumentando en frecuencia pero también en amplitud, hasta llegar a los 100 Hz aproximadamente donde la amplitud se mantiene prácticamente constante hasta pasados los 25 kHz.

Habrá que conseguir que la curva de amplitud en función de la frecuencia sea constante en

todo el espectro. Para esto, tenemos que introducir un circuito que amplifique todas la señales que estén por debajo de un determinado nivel, y que atenúe todas las que lo sobrepasen.

Esta es la función que realiza el control automático de ganancia. Este circuito se encarga de mantener una salida constante aunque existan variaciones a la entrada.

La idea básica del control automático de ganancia es la de un circuito realimentado que para un incremento de la señal de entrada produce que el amplificador de error disminuya de ganancia, mientras que para una disminución de la amplitud de entrada, el detector de error amplifique más hasta estabilizarse en el nivel adecuado.

La forma más práctica de construir un control automático de ganancia, es la que utiliza un FET como resistencia controlada por tensión en su circuito de realimentación. La tensión que va a atacar a esta resistencia variable constituída por el FET podría ser la obtenida en un lazo de control de

detección de pico.

El transistor de efecto de campo y de canal N, conectado a la entrada no inversora del amplificador operacional detector de error y a masa, determina la ganancia en lazo cerrado del conjunto. Los picos negativos de la señal a la salida del amplificador de error aplicados a la base de un transistor harán que este conduzca cuando sobrepasen la tensión Vbe. La tensión en el colector del transistor, una vez filtrada para evitar oscilaciones nos van a determinar la resistencia del canal de transistor de efecto de campo.

Teóricamente se pueden obtener un control automático de ganancia con un margen de entrada de 60 dB, teniendo en cuenta las variaciones de la resistencia del canal del FET (entre 120 ohmios a más de varios millones de megaohmios). El único problema que hay que tener en cuenta es que a variaciones muy grandes de la tension de entrada el FET empieza a trabajar en una zona no lineal, produciéndose distorsiones en la señal a la salida.

AMPLIFICADOR DE POTENCIA

Una vez conseguido una señal de amplitud constante, a lo largo de todo el espectro de las frecuencias, el único detalle que queda por introducir es adecuarla para que pueda servir de entrada a cualquier equipo que queramos analizar. Por esto no hace falta un amplificador de potencia como última etapa de salida.

En general hay que entregar una determinada potencia a una cierta impedancia de carga. La potencia requerida puede ser desde miliwatios hasta kilowatios y la carga puede ser unos auriculares, un altavoz, un amplificador, ecualizador filtro, etc. En el diseño, además hay que tener en cuenta el efecto de esta etapa de salida sobre el ancho de banda global del amplificador, como mantener la linealidad y minimizar la distorsión, estar seguros de que los dispositivos están trabajando por debajo de sus

límites máximos de tensión, corriente, disipación de potencia y todo ello aún dentro de las condiciones ambientales y de funcionamiento más extremas. El hecho de que la relación de transferencia de entrada a salida del amplificador de potencia sea no lineal, causa que la forma de onda de salida no sea idéntica a la entrada, sino una versión distorsionada.

Gran parte de la distorsión armónica causada por la falta de linealidad de la característica de transferencia, puede eliminarse en contrafase o push-pull. En este circuito la excitación se produce por medio de un transformador con toma intermedia o a través de un amplificador operacional que suministre tensiones iguales con diferencias de fase de 180 grados.

La corriente total de salida en la carga será proporcional a la diferencia entre las corrientes de colector en los dos transistores en contrafase.

El circuito en contra fase tiene la ventaja de que va a compensar todos los armónicos de orden par de la salida, y dejará el tercer armónico como fuente principal de distorsión, todo esto

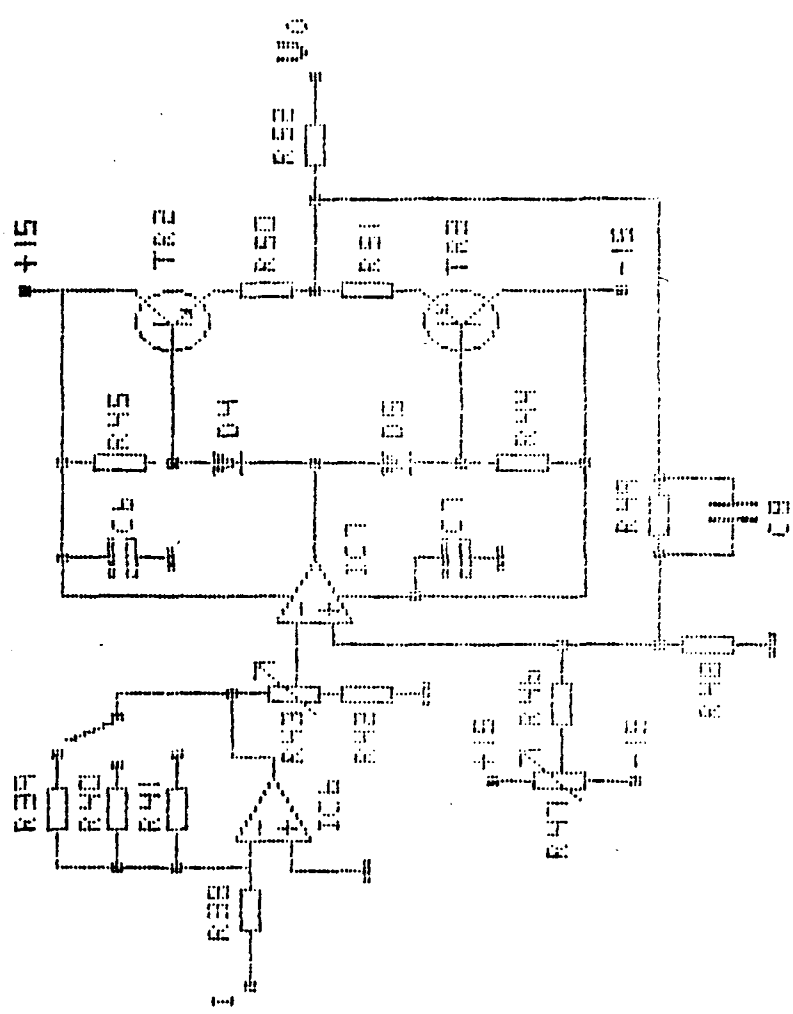
suponiendo que los transistores en contrafase sean idénticos.

La ventaja que este sistema aporta es que por una distorsión determinada da más salida por elemento activo.

La dificultad de este circuito estriba en la obtención de transistores perfectamente complementarios.

Si hay desequilibrio en las características de los dos transistores, los armónicos pares no quedan eliminados completamente.

En la región de corrientes pequeñas en las que trabajan los transistores, la salida es mucho menor de lo que sería si la respuesta fuese real; este efecto se denomina distorsión de cruce, el cual se puede eliminar empleando realimentación negativa de la salida a la entrada.



SEÑAL DE POLARIZACION

Como ya hemos visto para que el oscilador controlado por tensión pueda barrer frecuencias que vayan desde las bajas frecuencias del margen de audio, 20 Hz, a las más altas, 20 KHz necesitamos una corriente que polarice a los circuitos de transconductancia variable.

Aplicando la ley de Ohm podemos conseguir que la variable que controle la frecuencia, en vez de ser una corriente, sea una tensión proporcional a ésta, que denominaremos Tensión de Polarización. La corriente de polarización resultante será igual al producto de la tensión de polarización por la inversa de la impedancia a través de la cual se suministra.

Esta tensión de polarización podría obtenerse a partir de un divisor de tensión

controlándose manualmente por medio de un potenciometro. Pero el fin de este equipo de medida es otro. Se pretende barrer frecuencias que cubran todo el margen de audio de una manera automática.

La tensión que controle los Amplificadores Operacionales de Transconductancia variable debe pasar, pues, desde un valor determinado a otro, de manera automática y continua, sin que influya en ésto la subjetividad del usuario.

Las tensiones que debemos aplicar, según las características del oscilador controlado por tensión que hemos construido, van desde unos 14 voltios negativos, para las frecuencias más bajas, hasta unos 15 voltios positivos, para que supere el límite de las frecuencias más altas.

Si el paso de las frecuencias más bajas a las más altas se produce de una manera lineal, la función que represente la tensión de polarización respecto del tiempo deberá ser una rampa. Si el paso de una frecuencia a otra se produce en intervalos de tiempo iguales por octava, la función de la señal de

polarización respecto del tiempo será logarítmica.

El método más común para construir una rampa de tensión de automática lo constituye el integrador analógico. Está construido básicamente por un amplificador operacional constituido en modo inversor, con la única diferencia que la impedancia que que se realimenta de la salida a la entrada inversora, en vez de ser resistiva es capacitiva.

Se llama integrador porque se puede demostrar matemáticamente que realiza la operación matemática de la integración. El amplificador suministra, por tanto, una tensión de salida proporcional a la integral de la tensión de entrada.

Si la tensión de entrada es constante, la salida será igual a una rampa de valor:

$$Vo = - v * t / R * C$$

donde Vo es la señal de salida, v la tensión de entrada, t es el tiempo, R la resistencia de entrada al amplificador operacianal, y C la impedancia de realimentación.

El problema de este tipo de circuitos reside en la respuesta de la carga del condensador. Cuando se trata de periodos de tiempo cortos, el condensador no llegará a alcanzar nunca su carga máxima, por tanto su curva de carga, es decir, la integral de la tensión continua presentada a la entrada, será una rampa ascendente y completamente lineal. Una aplicación de este circuito particularmente útil, es el barrido para un tubo de rayos catódicos de un osciloscopio.

Por el contrario, cuando integramos periodos de tiempo más largos, el condensador alcanza valores elevados de carga, llegando a su zona no lineal. Para conseguir aumentar el tiempo de integración tendríamos que ir aumentando el valor de impedancia del condensador y del la resistencia de entrada.

Analicemos por un momento la señal que vamos a obtener como resultado final. La frecuencia más baja que necesitamos generar tiene que ser de unos 20 Hz o inferior. A esta frecuencia el periodo de la señal es de 0.05 segundos. Si vamos a barrer desde los

20 Hz hasta los 20 KHz en varios segundos, la fracción de tiempo que corresponda a las frecuencias bajas será tan pequeña que no dará tiempo a que se produzca un solo ciclo completo de éstas.

A parte de esto, consideremos que el barrido de frecuencias que queremos producir va a ser representado en un Plotter o trazador gráfico. Esto va a suponer que la velocidad a la que se va a generar el barrido tiene que ser muy baja, para que la pluma del trazador gráfico pueda dibujar el máximo detalle de las irregularidades de un espectro.

Cuanto más tiempo dure el ciclo de un barrido, mayor definición tendrá la curva. Estamos hablando de períodos de tiempo que van a superar al minuto incluso a varias decenas de minutos.

Con períodos de tiempo tan largos, se precisan condensadores con valores de capacidad muy elevados que aparte de ser de muy alto costo y volumen presentan tantas pérdidas que las ventajas que ofrece este circuito serían prácticamente nulas.

Para poner solución a todas estas exigencias se ha optado por conseguir una rampa por otros medios que no sea el de la integración.

Utilizando un convertidor digital analógico podremos conseguir cualquier función de tensión con respecto al tiempo a partir de una serie de valores digitales en su entrada.

Si estos valores de entrada son los producidos por un contador de impulsos a la salida obtendremos una rampa de tensión formada por un determinado número de escalones, igual a 2 elevado al número de bits del contador.

El tiempo de duración de la rampa será igual al producto del tiempo de duración de un ciclo de reloj por el número de escalones que forman dicha rampa, pudiéndose variar la duración de ésta sin que quede modificada.

El número de escalones que formen la rampa, tendrá que ser tal que el salto de uno a otro sea tan pequeño que se pueda despreciar.

En un principio se utilizó un contador de 8 bits, seguido de un convertidor digital-analógico, para comprobar el efecto que la rampa producía sobre el oscilador controlado por tensión. Los saltos entre escalones eran tan grandes que las variaciones de frecuencia producidas en el oscilador no se podían aceptar.

Es por esto por lo que se aumentó el número de bits de 8 a 16. De esta manera los escalones pasarían de ser 256 para un contador de 8 bits a 65.536 escalones para el de 16. El salto producido ahora de un escalón a otro será tan pequeño, y la variación de frecuencia producida por el oscilador tan baja, que se podrán despreciar.

Para la conversión digital analógica se ha utilizado el circuito integrado denominado DAC-08. La serie DAC-08 consiste en un convertidor digital-analógico monolítico de 8 bits, que provee una elevada velocidad e infinitas aplicaciones a un bajo costo. Es directamente compatible con todas las populares familias lógicas con una completa inmunidad al ruido, provee de salidas de corriente complementaria,

aumentando la versatilidad y posibilitando la operación diferencial para salidas de pico a pico.

El contador de 16 bits que proporciona la entrada a los convertidores digital-analógicos está formado por 4 circuitos integrados de la serie 74191. Este dispositivo es un contador reversible síncrono con facilidad de prefijación del control de habilitación, con control reversible en una sola línea, posibilidad de conexión en cascada para funcionamiento multidécada y entradas con bufferes. El elemento es un contador binario de 4 bits. El funcionamiento síncrono está conseguido activando simultáneamente con el reloj todos los flips-flops, de manera que las salidas cambian de modo coincidente entre sí cuando se cumplen las condiciones de entrada. Este modo de funcionamiento elimina los picos de cómputo de salida que suelen ir asociados a los contadores síncronos.

Dado que los convertidores digitales-analógicos utilizados están provistos de entradas de tan solo 8 bits, el problema consistirá en asociar a cada uno el peso que le corresponde en la cuenta para que la salida final sea la deseada.

El modo del funcionamiento será el siguiente: en el tiempo que el convertidor de menor peso produce un escalón, el otro convertidor debe producir los 256 escalones correspondientes a sus 8 bits de entrada, es decir debe de producir una rampa en un tiempo 256 veces menor al de la rampa producida por el otro convertidor, y con una amplitud total igual a la de un escalón de dicha rampa.

Debido a que la salida de los convertidores digital-analógicos es en corriente, se efectúa primero una conversión corriente-tensión, por medio de un amplificador operacional para a continuación realizar la suma de las dos partes.

Los impulsos de reloj se han generado utilizando el circuito integrado 555, en modo aestable. El condensador conectado a la patilla de umbral y descarga del integrado, junto con las resistencias que componen este circuito, nos van a determinar la frecuencia del tren de impulsos que este produce. La duración de un ciclo de reloj multiplicada por 65.536 nos va a dar la duración total de la rampa.

AMPLIFICADOR LINEAL Y LOGARITMICO

A la hora del diseño de este equipo se ha pensado en la posibilidad de que pueda realizar barridos no sólo lineales, sino también logarítmicos para así poder estudiar una curva de frecuencias con intervalos iguales por octavas de frecuencia. Esta es la forma más usada en el estudio de señales de audio puesto que la respuesta del oido humano a las variaciones de frecuencia se ajusta más a una curva de este tipo que a cualquier otra función.

La misión del amplificador logarítmico y del amplificador lineal es ajustar la rampa, obtenida a base de escalones de los convertidores digital analógicos, a unas condiciones determinadas para que pueda servir como entrada al resto de los circuitos que vayan a continuación.

La señal obtenida del sumador de

tensiones a partir de los convertidores digital analógicos, es una rampa descendente con su origen en cero. Para poder atacar directamente al oscilador controlado por tensión necesitamos convertir esta rampa y variar los límites de tensiones.

Utilizando un inversor a base de un amplificador operacional podemos conseguir variar la polaridad de la rampa. Ahora tendremos una rampa que en vez de ser descendente será ascendente a partir de cero voltios. La cuestión es simplemente calcular la mitad del valor que alcanza la rampa, y este será el valor de nivel de offset que debemos restar para que la onda sea simétrica respecto al origen. Una vez conseguido esto sólo queda amplificarla hasta obtener los valores deseados por encima y por debajo del nivel cero.

Los valores finales que precisamos son de unos 14 voltios por debajo del nivel de cero y de unos 15 voltios o más por encima del nivel cero. Esto quiere decir que no será exactamente simétrica para esto se provee de un parámetro de ajuste con el que poder variar con mayor precisión el nivel de las tensiones de trabajo. La rampa obtenida en este punto

ya esta en condiciones para atacar directamente al oscilador controlado por tensión y producir un barrido lineal.

Es posible obtener una tensión proporcional al logaritmo o al antilogaritmo de la tensión de entrada mediante el empleo de los módulos convertidores logarítmicos, cuyo principio de funcionamiento está basado en la característica de la unión p-n del semiconductor.

Un circuito básico podría ser el formado por un operacional con una resistencia en la entrada inversora y un diodo como realimentación de la salida a la entrada inversa. La salida será proporcional al logaritmo de la entrada.

Esta tensión de salida contiene un término adicional constante que interesa minimizar seleccionando un diodo cuya corriente inversa sea lo menor posible. Otras fuentes de error proceden de la caida de tensión óhmica en la resistencia serie del diodo.

Para obtener mejores resultados se puede sustituir el diodo por la unión base-emisor de un transistor. En este caso se denominaría configuración transdiodo.

Puesto que las características de los diodos que intervienen en las expresiones obtenidas son muy dependientes de la temperatura, es preciso introducir circuitos adecuados de compensación.

El circuito utilizado como amplificador logarítmico para el generador de barrido de audio se corresponde con el esquema básico descrito.

Como realimentación utiliza un diodo rectificador 1N 4148 y a la salida un amplificador no inversor. Como red de compensación utiliza un segundo diodo igual al primero, de manera que las derivas producidas en uno se compensen con las producidas en el otro. Además se incluye una fuente de corriente compuesta por un transistor con la base a una tensión fija de referencia, cuya misión es la de polarizar la salida del amplificador logarítmico.

Para que este circuito trabaje a pleno rendimiento necesitamos tensiones no inferiores a los cero voltios, ya que a valores cercanos a este el logaritmo tiende a infinito.

Por tanto para producir una curva logarítmica ascendente, necesitaremos una señal de entrada que sea una rampa lineal descendente, con límite inferior superior a los cero voltios. Los límites entre los cuales va a estar esta curva deberán ser ajustados para que el oscilador de frecuencia variable alcance los márgenes deseados.

El ajuste de offset y amplitud se hará de forma idéntica al utilizado en el amplificador lineal.

Con estos dos amplificadores ya hemos completado los modos de funcionamiento del equipo. Tan sólo necesitamos una tensión que nos controle el movimiento en el eje X, al tiempo que se produce el barrido de frecuencias. Esta se consigue a partir del sumador de tensiones de los convertidores digital-analógicos, utilizando un simple amplificador

operacional montado en modo inversor.

El barrido en el eje X, que nos va a dar la escala de tiempo de la curva, debe partir desde 0 con una amplitud total que no supere los 12 voltios.

LOGICA DE CONTROL

El sistema de contadores, que van a dar los valores digitales de los escalones que a su vez construirán los convertidores digital-analógico, están constituídos por los circuitos integrados del tipo 74191. Como ya hemos descrito se trata de un contador binario, ascendente y descendente, con carga paralela y posibilidad de conexión en cascada.

Para conseguir una rampa ascendente como resultado final, tendremos que prefijar una serie de valores que nos determinen la forma de conteo de estos circuitos.

Las condiciones de cuenta serán: cuenta ascendente, para la cual necesitaremos un "0" en la patilla número 5, que determina que la cuenta sea ascendente. La entrada de carga paralela deberá estar a "1" para que esté desabilitada y se permita el conteo

sin tener en cuenta los valores de inicialización paralelos.

La salida de conexión en cascada de cada contador, deberá ir conectada a la entrada de habilitación de cuenta del siguiente. La habilitación del primer contador deberá estar a nivel bajo para que permita contar a todo el sistema. El reloj debe estar presente en todos los contadores al mismo tiempo.

Tal como hemos descrito conseguiremos que todo el sistema entre en funcionamiento y se mantenga activo indefinidamente. La salida será una rampa repetitiva con un período igual a 64.000 veces el período de reloj.

La primera función de control será conseguir que cada vez que se produzca una rampa el sistema se detenga. Además pretendemos conseguir poder inicializar el circuito de manera externa, tanto al final de un ciclo como durante el mismo.

Para detener la cuenta una vez que se llegue al final de un ciclo, se aprovecha la salida de

conexión en cascada del último contador. Esta nos dará un impulso a nivel bajo cuando llegue a su máximo estado de cuentas y por tanto al máximo valor de la cuenta de todos los contadores.

Utilizando un flip-flop J-K, conseguiremos un cambio de estado a la salida, cada vez que se produzca un pulso de fin de cuenta.

El estado del flip-flop podrá permitir por medio de una puerta AND, que el reloj llegue hasta los contadores, o por el contrario que quede cortado en este punto. Esto quiere decir que si el estado del flip-flop es "1", la puerta AND reflejará a la salida lo que posea en la otra entrada, es decir los impulsos del reloj. Sin embargo si el estado del flip-flop es "0", lo cual ocurre cuando se llega al final de la cuenta, la salida de la puerta AND será siempre "0", y el reloj no llegará a los contadores.

Para poder conseguir que la cuenta una vez detenida se inicialice, se ha dispuesto de un pulsador, que produzca el mismo nivel bajo que produce la salida de conexión en cascada del último contador.

De esta manera cambiará el estado del flip-flop y el reloj estará presente de nuevo en los contadores.

Para lograr que se produzca una detención de la cuenta y se comience desde el principio, se han puesto todas las entradas de carga paralela a "0", y la entrada de habilitación de la carga conectada al pulsador de inicialización. Así cada vez que se produzca una detención manual, la inicialización partirá de "0".

Tal y como tenemos el circuito hasta ahora hemos conseguido un generador de rampas automático, con detención automática y manual. Además de esta función se le ha querido dar a este equipo la posibilidad de seleccionar una frecuencia determinada manualmente. De esta forma podremos generar un barrido, con la posibilidad de detenernos en los puntos de mayor interés, pasar de una frecuencia a otra, hacia adelante y hacia atrás, de una manera rápida o con un ajuste más fino.

Utilizando otra puerta AND activada por un pulsador, podremos conseguir controlar el paso del

reloj a los contadores, sin que esta vez se inicialice el sistema. La utilidad de ésto es poder variar la frecuencia del oscilador manualmente para poder colocarlo en el punto deseado, avanzando paso a paso.

Para la localización de frecuencias se ha dotado al circuito de la posibilidad de avanzar con dos velocidades, para permitir una búsqueda más rápida, y una vez situado sobre la zona deseada, hacer un ajuste fino de la frecuencia.

La velocidad de ajuste fino es la normal del barrido, y la otra es 256 veces superior, para permitir el salto de las frecuencias bajas a las altas sin que tenga que transcurrir todo el período de tiempo de un barrido.

El modo de conseguir esta función es cortar la cadena de conexión en cascada de los contadores segundo y tercero. Lo que permite esto es controlar que se tenga en cuenta a los dos primeros contadores o no. Por medio de un commutador se introduce un nivel alto en la entrada de habilitación de cuenta del primer contador para que este no pueda

contar, y un nivel bajo en la entrada de habilitación del tercero, para que su funcionamiento no dependa del acarreo del anterior.

De esta manera el primer y segundo contador estarán en activo y el tercero y cuarto no. Este mismo commutador hará que el pulso a nivel bajo, de conexión en cascada del segundo contador llegue o no al tercero.

La cuarta y última de las funciones externas, es la de permitir la búsqueda o avance hacia arriba o hacia abajo, para permitir centrarse en un valor de frecuencia sin el problema que plantea el hecho de que al buscarla, nos pasemos del valor deseado y tengamos que retornar al principio para volverlo a intertar.

Sólo queda un pequeño detalle por analizar, y es el de la commutación del modo automático al modo manual.

Todas estas funciones anteriormente descritas, tendrán un valor determinado y fijo para el

funcionamiento automático y sin embargo deberán ser variables y controlar desde el exterior para el modo manual.

Para solucionar esto se ha provisto de una serie de interruptores electrónicos o buffers. Estos interruptores están dotados de una entrada de control, que según el valor de ésta, la entrada estará presente a la salida o por el contrario tendrá un estado de alta impedancia.

Con un juego de interruptores para cada modo de funcionamiento, permitiremos que las funciones de control sean las prefijadas en el caso de estar en modo automático, o las variables para el caso de estar en modo manual.

Un commutador externo activará un juego de commutadores, y através de un inversor desactivará el otro, y al contrario.

ENTRADA Y MEDIDA DE AMPLITUD

La señal de barrido en frecuencia producida por el vobulador debe ser introducida en el equipo que se desea medir. La salida del equipo que estamos analizando debe ser recogida por nuestro equipo, el cual va a transformar la señal alterna a un valor continuo, proporcional al valor de pico de la señal en alterna, y lo va a acondicionar para poder ser representado por el trazador gráfico.

A la entrada del equipo necesitamos un amplificador que nos sitúe la señal en un nivel adecuado para poder ser medido. Este amplificador está provisto de un conmutador de selección, para amplificar en caso de tener niveles bajos de entrada, y atenuar en el caso contrario, como sería en el caso de estar analizando la respuesta de un amplificador de potencia.

Las condiciones que debe cumplir este

amplificador de entrada son que la impedancia de entrada sea alta y que el ancho de banda sea grande.

El hecho de que la impedancia de entrada sea grande es primordial, porque de lo contrario nuestro equipo estaría cargando al equipo medido y no estaríamos obteniendo la verdadera respuesta.

Para conseguir una impedancia de entrada lo más alta posible se ha escogido un amplificador operacional con entrada J FET. El circuito pertenece a la serie de integrados TL 080. El modo de conexión es el de un inversor utilizando valores de resistencia altos, para que disminuya lo menos posible la impedancia intrínseca del operacional.

A partir de esta señal acondicionada tenemos que conseguir el valor de tensión RMS para ser representado. Los convertidores de alterna a valor RMS a parte de ser costosos, son complicados de implementar, por lo que se ha optado por conseguir una solución más sencilla que nos de un resultado aceptable.

Esta solución es la de pasar la señal alterna a través de un rectificador de onda completa. A la salida obtendremos una señal que será igual a la función valor absoluto de la señal de entrada. Los semiciclos positivos de la señal se mantendrán invariables, mientras que los negativos experimentarán un cambio de signo.

Son diversas las formas de implementar un rectificador de onda completa. Estos consisten en dejar pasar el semiciclo de la onda que es positivo por un camino, y el semiciclo negativo por otro. Este último se invierte, y al final se suma con el positivo.

El principio del circuito utilizado como rectificador de onda completa en nuestro equipo, se corresponde con esta estructura básica.

La señal presente a la entrada, por un lado pasa a través de un diodo rectificador, el cual suprimirá los semiciclos negativos de la onda. La salida de este diodo será la señal de entrada con la diferencia que en el tiempo del semiciclo negativo tendrá un valor de señal de 0 voltios. Por otro lado

se hace pasar la señal de entrada por un inversor. Situando un diodo rectificador a la salida produciremos el mismo efecto que antes con un desfase de 180 grados. Estas dos señales sumadas nos darán a la salida la forma de onda perseguida.

Lo que hemos conseguido hasta ahora es que la onda sea completamente positiva, en vez de simétrica, con los semiciclos negativos invertidos. Ahora sólo nos resta transformar esta forma de onda en un nivel de continua, el cual debe ser proporcional a la tensión de pico de la tensión de entrada.

A la salida del rectificador de onda completa se ha colocado un filtro compesador paso bajo. Este consiste simplemente en una resistencia en serie, con un condensador en paralelo puesto a masa.

El funcionamiento de este filtro es el siguiente. El condensador almacena energía durante el tiempo de conducción, entregándola a la carga durante el tiempo de no conducción. De este modo, aumenta el tiempo durante el cual la corriente circula por la carga, reduciéndose el rizado.

Durante el tiempo en el que la tensión de la entrada al filtro es superior a la del condensador, éste se va cargando, hasta el momento en que la onda de entrada disminuye de tensión.

Para conseguir un bajo rizado a la salida, debe utilizarse un condensador de gran capacidad, del orden de decenas de microfaradios. El máximo rizado se producirá cuando las frecuencias sean bajas, puesto que los periodos de descarga son más grandes que a frecuencias superior.

Habrá que tener en cuenta que estamos midiendo niveles de tensión variables. Cuanto mayor sea la capacidad del condensador mayor será tambien el tiempo de carga. Si colocamos un condensador con capacidad muy alta, para una variación brusca de la onda de entrada, la respuesta del condensador será muy lenta, por lo que estaremos falseando la medida.

Por esta razón hay que buscar un valor de capacidad tal que el rizado sea aceptable, y que la velocidad de respuesta sea alta, teniendo en cuenta la duración del barrido.

Para barridos en tiempos muy cortos, nos afecta más la velocidad de respuesta que el factor de rizado. Como el barrido que queremos realizar es muy lento, debemos atender más la cuestión del rizado, siempre que la velocidad de respuesta sea admisible.

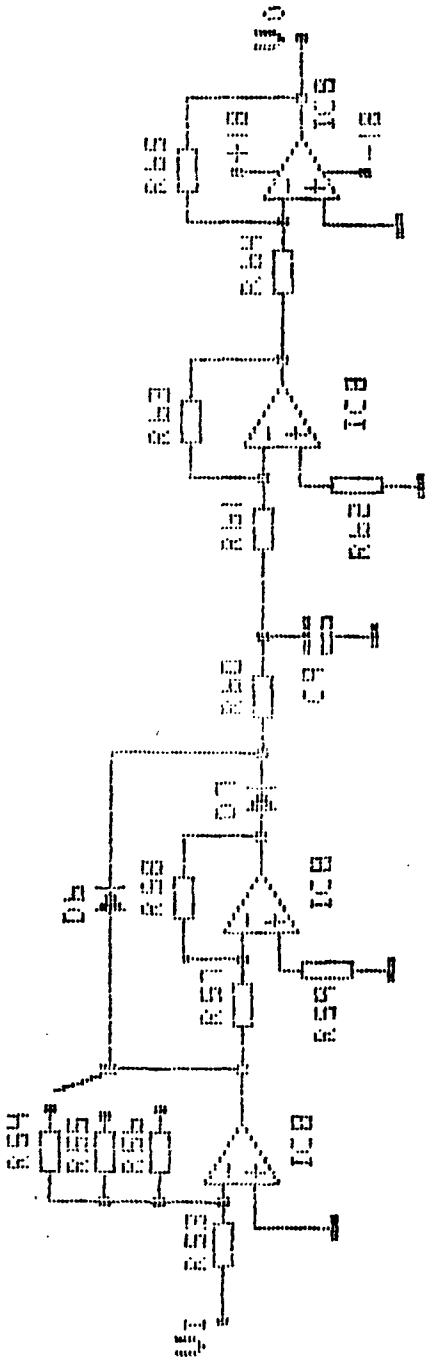
Para atacar directamente a la salida que nos gobierne el eje Y del trazador gráfico, solo necesitamos una etapa separadora, para que la entrada al registrador no carge a la salida del filtro.

Esta etapa separadora consta de dos amplificadores operacionales inversores. Hay que cuidar que el primero tenga muy alta impedancia de entrada, para no modificar la salida del filtro. Del segundo hay que tener en cuenta que su impedancia de salida sea baja, además de servirnos para devolver la polaridad positiva a la tensión de salida.

Si la señal que se va a medir viene sumada a un nivel de continua, al representarla no va a dar un resultado real, y menos aún cuando este nivel de offset varíe con el tiempo o con la frecuencia.

La razón de que el resultado final no sea real es que al venir la onda con un semiciclo mayor que el otro, con respecto a los cero voltios, al ser rectificada y pasada por el filtro, las cargas y descargas no serán iguales. El nivel de continua resultante será prácticamente proporcional al nivel del semiciclo de mayor amplitud. Esto quiere decir, que para una entrada de igual amplitud, pero con distintos niveles de continua la salida del rectificador será distinta.

Para poder reducir lo maximo posible este defecto se introduce a la entrada del rectificador un filtro paso alto, consistente en un condensador en serie con la etapa anterior y el propio rectificador. Este cortará el paso a los niveles de continua, pero nos limitará tambien en velocidad. Habrá que escogerlo de un valor tan grande como sea posible siempre que el compromiso con la velocidad no se vea excesivamente afectado.



FRECUENCIMETRO DIGITAL

El frecuencímetro del que se ha dotado el vobulador de audio cumple una función muy importante a la hora de utilizarlo como simple generador, y para la búsqueda de frecuencias. En el caso de no haberlo introducido se habría hecho imprescindible la conexión exterior de un aparato de estas características.

La filosofía del frecuencímetro es simplemente medir el número de ciclos de señal por segundo. Con un generador de pulsos cuya duración sea exactamente un segundo se puede habilitar la entrada a un contador. El resultado de la cuenta será el número de pulsos que entren dentro de ese segundo, y por tanto el valor de la frecuencia de la señal de entrada.

El frecuencímetro utilizado consta de un contador de seis décadas formado por dos circuitos integrados de tecnología CMOS del tipo 4553, cada uno

de los cuales posee en su interior tres décadas contadoras en código BCD, con salida multiplexada. Estos circuitos integrados contadores poseen en su interior el multiplexor propiamente dicho, e incluso el oscilador que produce el desplazamiento de los encendidos, a excepción solamente de la capacidad de la constante de tiempo, la cual va situada en el exterior del núcleo, permitiendo elegir la frecuencia básica del multiplexor.

En este caso, y por tratarse de dos circuitos integrados idénticos, se ha utilizado únicamente uno de los dos osciladores, usando esta frecuencia para el pilotaje de los dos. Esta circunstancia permite la utilización de un único juego de transistores de encendido, produciéndose éste de dos en dos displays y ahorrando tres transistores de commutación.

Toda la información que poseen las tres décadas contadoras estarán presentes a la salida de cada circuito, aunque troceada por la acción del circuito multiplexor. Esta información, junto con las órdenes de encendido proporcionadas por el mismo

integrado, permiten reconstruir, a través de los decodificadores de siete segmentos, la información de los contadores pero ya en los displays.

El circuito integrado posee en su interior un circuito completo de memoria de doce bits, el cual permite tener memorizada una lectura de tres cifras todo el tiempo que sea necesaria, independientemente de que a partir del instante de memorización, los contadores sigan contando, se paren, o sean sustituídas por otras nuevas, resultado de un nuevo cómputo.

El terminal número doce de los contadores es la entrada de reloj al contador de la cifra menos significativa, produciéndose internamente el acarreo de los contadores de las siguientes cifras. El terminal número catorce proporciona un impulso cada vez que los contadores completan un ciclo de conteo, es decir cada vez que, del número máximo contado retornan automáticamente a cero. Esta salida puede ser utilizada como acarreo para hacer contar al siguiente grupo de décadas, de cifras de órdenes más significativas que las tres anteriores.

En definitiva, estos dos circuitos integrados van a constituir el contador de seis décadas, multiplexado y con memoria.

La información en código BCD multiplexado, da salida a cada uno de los cómputos de tres décadas, es codificada por medio de un decodificador de siete segmentos del tipo 4543, de baja corriente de salida, y montado con lógica negativa, el cual se encuentra en disposición de atacar directamente los segmentos de cualquier display a leds de ánodo común, cuyo consumo por segmento no sobrepase los 10 mA.

El contador de seis dígitos constituye la parte más importante del frecuencímetro digital, aunque falta un pequeño circuito que introduzca en el mismo los impulsos de "reset" y "memoria", espaciados exactamente un segundo entre sí, con el fin de que la lectura en los displays coincida exactamente con la frecuencia generada. Este circuito está formado por un circuito oscilador aestable del tipo 555 de elevada exactitud y un desplazador decimal del tipo 4017.

Puesto que, tanto el impulso de reset como el de memoria, que precisan estos circuitos contadores, deben ser de muy corta duración, se han instalado dos circuitos diferenciadores en estas dos salidas de bando. El primero proporciona a la salida un nivel bajo en ausencia de señal, con breves picos positivos correspondientes con los flancos positivos de la señal entrante. El segundo realiza la función inversa, es decir, proporciona un nivel alto en ausencia de señal, con breves picos de tensión nula correspondiendo con los flancos negativos de la señal de entrada. Estas distintas polaridades de los impulsos de mando del frecuencímetro, responden a la lógica que exigen los circuitos contadores.

FUENTE DE ALIMENTACION

Una vez realizadas todas las funciones del vobulador, sólo nos resta el diseño de una fuente que nos alimente a todos los circuitos.

Esta debe proporcionar tensiones de 5 voltios para los circuitos digitales y tensiones simétricas para los circuitos analógicos. El resto de las tensiones de referencia que utilizan el circuito han sido obtenidas a partir de las proporcionadas por la fuente, utilizando diodos zener en su correspondiente placa.

La red de energía eléctrica normalmente disponible, suministra una tensión alterna. La utilización de estas tensiones es bien conocida, pero la mayor parte de los circuitos electrónicos requieren para su funcionamiento una tensión continua. Aunque en algunos equipos electrónicos normalmente equipos

portátiles de bajo consumo, se utilizan pilas o baterías, con la ventaja de su facilidad de transporte y con el inconveniente de su relativamente rápido agotamiento.

En este caso se precisa de un sistema electrónico que convierta la energía alterna en características fijas de tensión y frecuencia.

La fuente de alimentación está formada básicamente por un transformador, y un rectificador. La función del transformador es la de disminuir el nivel de la tensión de la red, normalmente 220 voltios, a niveles adecuados. El rectificador tendrá como función la de convertir esta tensión de doble polaridad a una sola polaridad.

El rectificador que se ha utilizado está formado por un simple puente de diodos, el cual va a convertir los semiciclos negativos de la tensión alterna en positivos.

El ideal es retener exclusivamente una componente continua. Es obvio pues el emplear un filtro

paso bajo si se desea reducir el factor de rizado de la onda. La frecuencia de corte de dicho filtro debe ser inferior a la frecuencia fundamental de la señal del rectificador.

El filtro utilizado es el denominado de condensador. Para conseguir un bajo rizado y asegurar una buena regulación, este condensador debe ser de gran capacidad. Estos condensadores de tan alta capacidad suelen ser electrolíticos. Las ventajas que presentan son un pequeño rizado y una tensión de salida alta con cargas pequeñas.

Sin embargo la tensión continua disponible a la salida del filtro del rectificador puede que no sea lo suficientemente buena, debido al rizado, o que varie su magnitud ante determinados tipos de perturbaciones que puedan afectar al sistema.

Este punto se ha resuelto utilizando reguladores de tensión monolíticos dado su bajo coste y sencilla implementación.

Los reguladores monolíticos utilizados

pertenecen a la serie de circuitos integrados 7800. Para las tensiones simétricas se utilizaron los circuitos 7818, regulador positivo de 18 voltios y el 7918, regulador negativo de 18 voltios. Para las tensiones que van a alimentar los circuitos digitales se utilizó el circuito integrado 7805, regulador positivo de 5 voltios.

El consumo total del circuito es de unos 500 mA para cada tensión simétrica, y de unos 800 mA para los circuitos digitales.

Para reducir al máximo las oscilaciones se ha colocado un filtro a la salida de cada regulador. El rizado que se obtiene a la salida del conjunto será inferior a 0,01 %.

MODO DE FUNCIONAMIENTO

El vobulador de audiofrecuencias ha sido especialmente diseñado para que su utilización sea lo más simple posible. Se ha procurado en su realización, que su uso en la obtención de espectros, y como generador, requiera el mínimo número de de aparatos de laboratorio adicionales. Tanto es así, que a no ser que se requieran medidas de precisión, como las obtenidas por un analizador de onda, el trabajo con el vobulador de audio solo necesita del trazador grafico para el cual ha sido diseñado.

El tipo de trazador gráfico ha sido escogido en función de sus prestaciones y facilidad de manejo. Este equipo de registro esta provisto de dos entradas analógicas de tensión, que son las que determinan la posición de la aguja tanto horizontalmente, como verticalmente.

Para el posicionamiento horizontal, está dotado de un generador de rampa, que determina el eje de tiempo, como en un osciloscopio. Aunque se podría haber utilizado esta ventaja, se ha preferido que la tensión del eje de tiempo sea generada por nuestro equipo, para evitar problemas a la hora de inicializar una medida.

El modo de operación para realizar un barrido en frecuencia es el siguiente: En primer monento se ha de colocar el papel sobre la superficie del registrador. Este puede ser calibrado o no. La única diferencia estriba en que se ha de cuidar el ajuste del cero en el caso de estar calibrado. Una vez colocado y sujeto, se debe ajustar el inicio de la pluma, la cual se puede mover utilizando los potenciometros que están colocados en los mandos de cada eje.

Antes de inicializar un barrido se debe hacer una simulación con la pluma en alto. Para que se pueda realizar el barrido por la pluma, los dos ejes de dibujo deben estar en posición "record". Una vez cumplidos todos estos requisitos se debe conectar la

salida del barrido horizontal en la entrada de eje X del trazador, y la salida del barrido vertical en la entrada del eje Y.

El equipo que se va a analizar debe estar conectado de la siguiente forma. La salida de tensiones de frecuencias variables del generador debe ser conectada a la entrada del equipo test. De la salida del equipo test se debe introducir la señal de nuevo en la entrada del vobulador. De esta forma la señal será tratada y su resultado irá a parar al registrador a través de la salida de barrido horizontal.

Hay que tener en cuenta el tipo de equipo que estamos analizando, si amplifica o atenúa, o si sus impedancias de entrada o salida son adecuadas para ser estudiado con el vobulador. Si no tenemos en cuenta esto podremos obtener resultados erróneos producidos por saturaciones, cargas de un equipo a otro, etc.

Para realizar la primera simulación se debe colocar al vobulador en el modo automático, con el

conmutador automático-manual. Se debe pulsar una vez el interruptor de inicio, para situar la pluma en el cero. Una vez colocada la pluma y pulsando de nuevo el interruptor de inicio comenzará el barrido.

La primera simulación nos va ha servir para ajustar el nivel de amplitud de la señal, y la velocidad de barrido, de manera que la curva que se vaya a obtener sea de nuestro agrado. Para la selección de la velocidad contamos con un conmutador de cuatro posiciones para cuatro tiempos de barrido. Para la selección de la amplitud contamos con los cnmutadores de entrada-salida, para ajustar el nivel de entrada al equipo test, y el nivel de salida al registrador.

Para utilizar el generador de barridos como un generador de onda senoidal de frecuencia seleccionable, o para buscar los puntos de interes dentro de una curva, colocaremos el conmutador de modo manual-automático en el modo manual. Pulsando el boton de avance conseguiremos movernos en frecuencia, y en el caso de estar sobre la grafica, movernos en ésta.

Para poder movernos hacia adelante o hacia atrás, utilizaremos el boton de arriba-abajo, el cual nos facilitará el posicionarnos sobre un punto deseado.

Para movernos más rápidamente sobre la curva sin necesidad de variar la escala de velocidad del barrido se utilizará el conmutador de rapido-lento.

El frecuencimetro digital nos permite determinar en que punto de frecuencia nos encontramos, lo cual facilitara, junto con todas la posibilidades de movimiento que el equipo incluye, la localización y utilización de una frecuencia discreta.

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APENDICE

INVENTARIO DE COMPONENTES

CODIGO	CLASE		PRECIO
R1	Resistencia	620 ohm.	10 pts.
R2	"	620 "	"
R3	"	30K "	"
R4	"	10K "	"
R5	"	30K "	"
R6	"	15K "	"
R7	"	220 "	"
R8	"	220 "	"
R9	"	100K "	"
R10	"	10K "	"
R11	"	100K "	"
R12	"	220 "	"
R13	"	220 "	"
R14	"	100K "	"
R15	"	10K "	"
R16	"	100K "	"

R17	Resistencia	220 ohm.	10 pts.
R18	"	220 "	"
R19	"	10K "	"
R20	"	100k "	"
R21	"	10K "	"
R22	"	7K5 "	"
R23	"	1M1 "	"
R24	"	12K "	"
R25	"	130K "	"
R26	"	11K "	"
R27	"	4.7K "	"
R28	"	11K "	"
R29	"	51K "	"
R30	"	2.2K "	"
R31	"	130K "	"
R32	"	5K1 "	"
R33	"	2.2K "	"
R34	"	110K "	"
R35	"	100K "	"
R36	"	10K "	"
R37	"	12K "	"
R38	"	51K "	"
R39	"	50K "	"
R40	"	50K "	"

R41	Resistencia	500K ohm.	10 pts
R42	"	200 "	"
R43	"	2K5 "	"
R44	"	2K2 "	"
R45	"	2K2 "	"
R46	"	3K "	"
R47	"	10K "	"
R48	"	200 "	"
R49	"	1K8 "	"
R50	"	2.7 "	"
R51	"	2.7 "	"
R52	"	51 "	"
R53	"	91K "	"
R54	"	1M "	"
R55	"	500K "	"
R56	"	100K "	"
R57	"	10K "	"
R58	"	10K "	"
R59	"	4K7 "	"
R60	"	51K "	"
R61	"	200K "	"
R62	"	51K "	"
R63	"	200K "	"
R64	"	51K "	"

R65	Resistencia	51k	ohm	10 pts
R66	"	1K5	"	"
R67	"	25K	"	"
R68	"	5K1	"	"
R69	"	5K1	"	"
R70	"	5K1	"	"
R71	"	5K	"	"
R72	"	5K1	"	"
R73	"	5K1	"	"
R74	"	5K1	"	"
R75	"	5K	"	"
R76	"	1K1	"	"
R77	"	1K1	"	"
R78	"	6K2	"	"
R79	"	6K2	"	"
R80	"	6K2	"	"
R81	"	6K2	"	"
R82	"	6K2	"	"
R83	"	2K2	"	"
R84	"	30K	"	"
R85	"	2K2	"	"
R86	"	5K1	"	"
R87	"	871K	"	"
R88	"	13K	"	"

R89	Resistencia	5K1 ohm.	10 pts.
R90	"	7K5 "	"
R91	"	5K1 "	"
R92	"	4K "	"
R93	"	62K "	"
R94	"	100K "	"
R95	"	820 "	"
R96	"	1K5 "	"
R97	"	1K3 "	"
R98	"	1K "	"
R99	"	3K "	"
R100	"	2K "	"
R101	"	2K "	"
R102	"	2K "	"
R103	"	9K1 "	"
C1	Condensador	300pF	40 pts.
C2	"	300p "	"
C3	"	300p "	"
C4	"	300p "	"
C5	"	1000u "	275 "
C6	"	68n "	50 "
C7	"	50n "	80 "
C8	"	2p "	40 "
C9	"	10n "	50 "

C10	Condensador	100n F	50 Pts
C11	"	100n "	40 "
C12	"	10n "	40 "
C13	"	100n "	50 "
C14	"	100n "	50 "
C15	"	680n "	60 "
C16	"	"	"
C17	"	"	"
C18	"	"	"
C19	"	"	"
C20	"	100n "	50 "
C21	"	470n "	50 "
TR1	Transistor	2N3819	180 "
TR2	"	2N3083	210 "
TR3	"	2N4037	210 "
TR4	"	BC108	90 "
D1	Diodo	1n4148	40 "
D2	"	1n4148	40 "
D3	"	Z 3volt.	80 "
D4	"	1n4148	40 "
D5	"	"	"
D6	"	"	"
D7	"	"	"
D8	"	Z 10volt.	80 "

D9	Diodos	1n4148	40 "
D10	"	"	"
D11	"	Z 3volt.	80 "
IC1	C. Integrado	LM13600	430 "
IC2	"	"	"
IC3	"	uA741	"
IC4	"	TL084	210 "
IC5	"	"	"
IC6	"	uA741	430 "
IC7	"	CA080	350 "
IC8	"	TL084	210 "
IC9	"	74191	320 "
IC10	"	"	"
IC11	"	"	"
IC12	"	"	"
IC13	"	DAC08	610 "
IC14	"	"	"
IC15	"	TL084	210 "
IC16	"	7473	380 "
IC17	"	uA555	180 "
IC18	"	7408	230 "
IC19	"	7400	230 "
IC20	"	74125	380 "
Transformador		2 Amperios	2.300 "

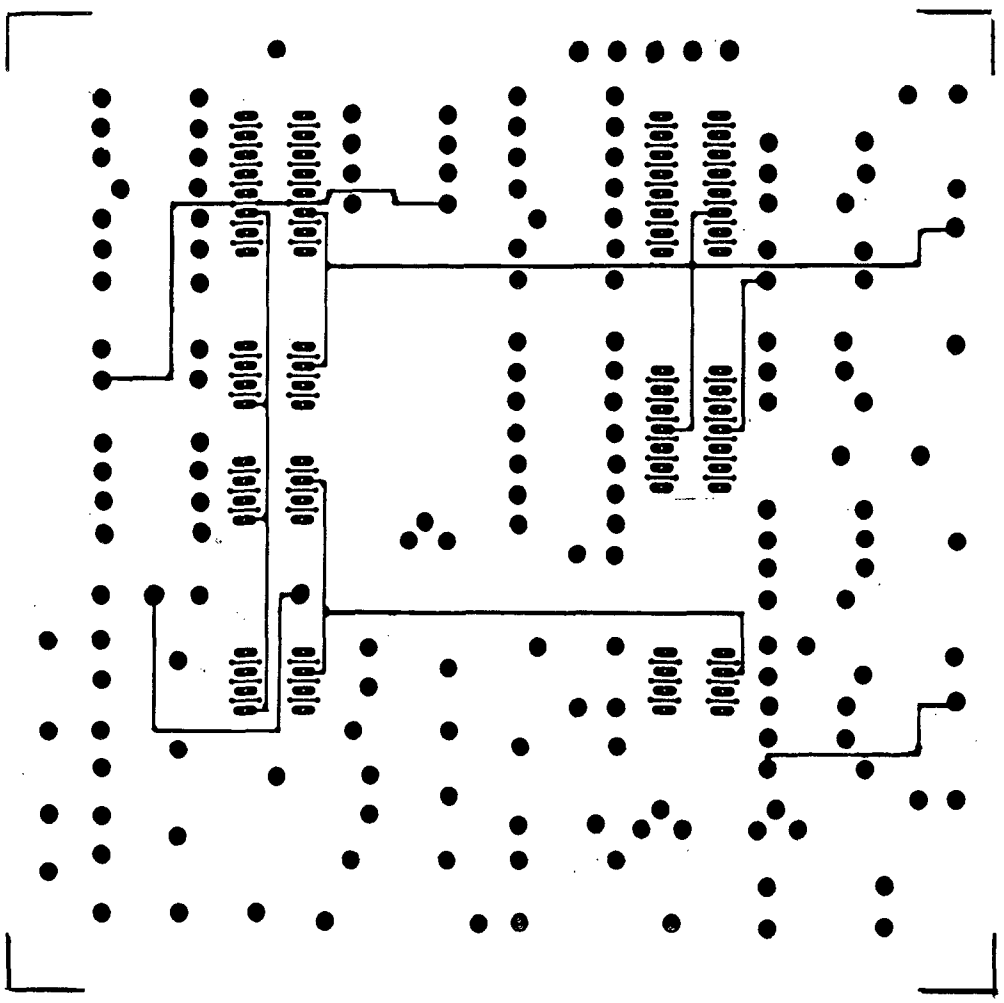
Conmutadores	950 Pts
Pulsadores	620 "
Portafusibles	500 "
Caja metálica	4.300 "
Conectores BNC	1.400 "
Conector alimentación	720 "

Presupuesto total 21.635 Pts

CIRCUITO IMPRESO

Oscilador Controlado por Tensión, Control Automático de Ganancia y Ampligicador de Salida.

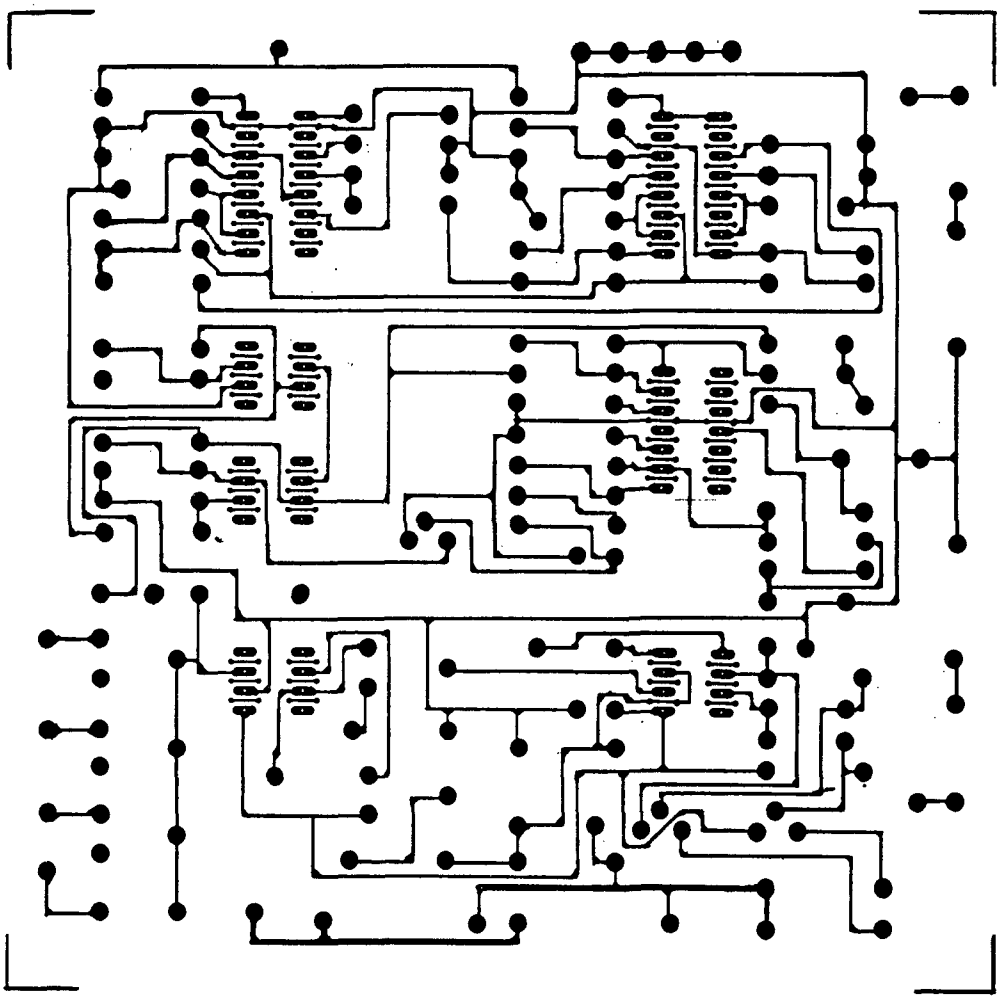
Cara de Componentes, vista superior.



CIRCUITO IMPRESO

Oscilador Controlado por Tensión, Control Automático de Ganancia y Ampligicador de Salida.

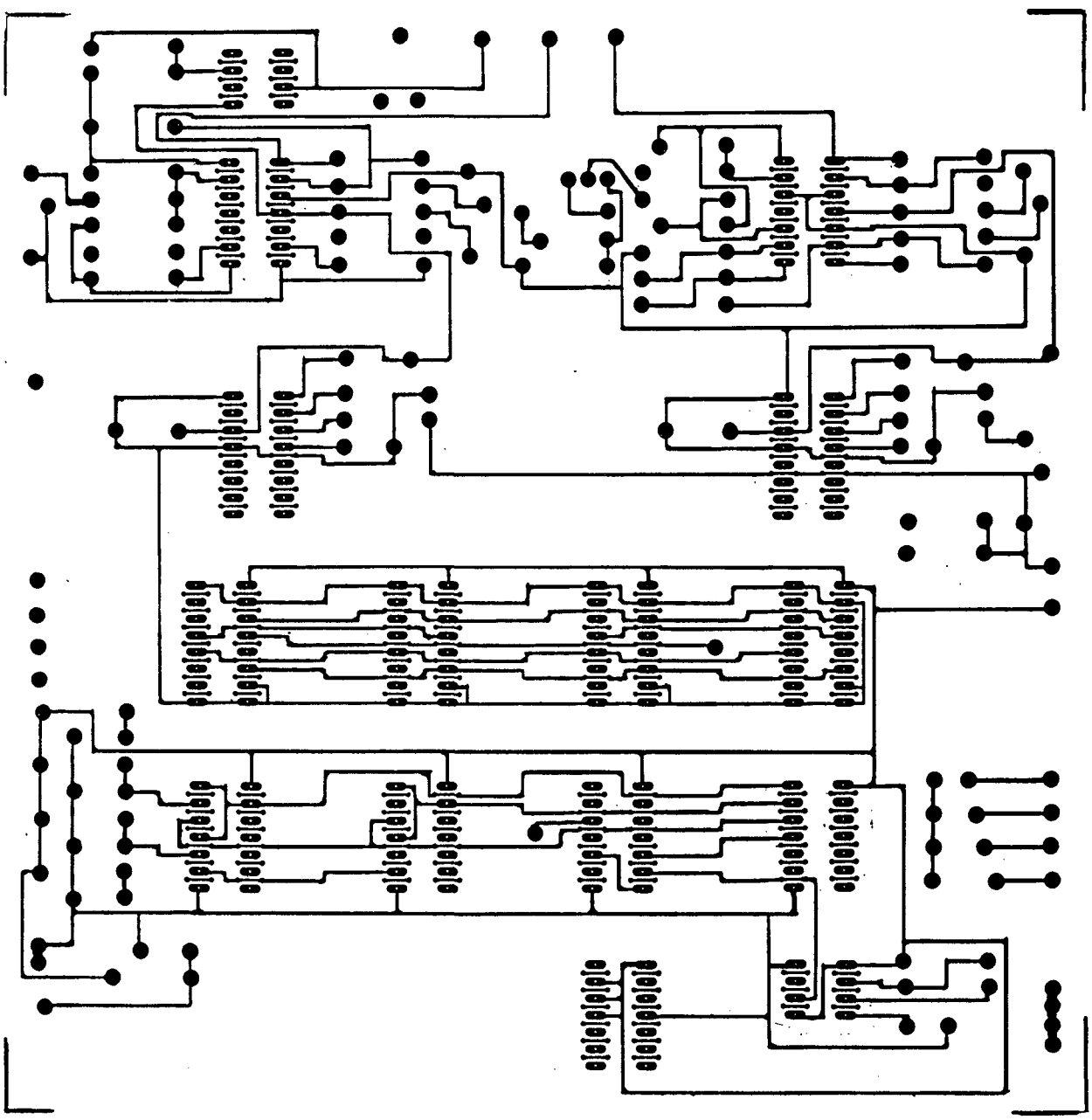
Cara de soldaduras, vista superior.



CIRCUITO IMPRESO

Tensión de Polarización, Lógica de Control, y Ampiflicador Lineal y Logarítmico.

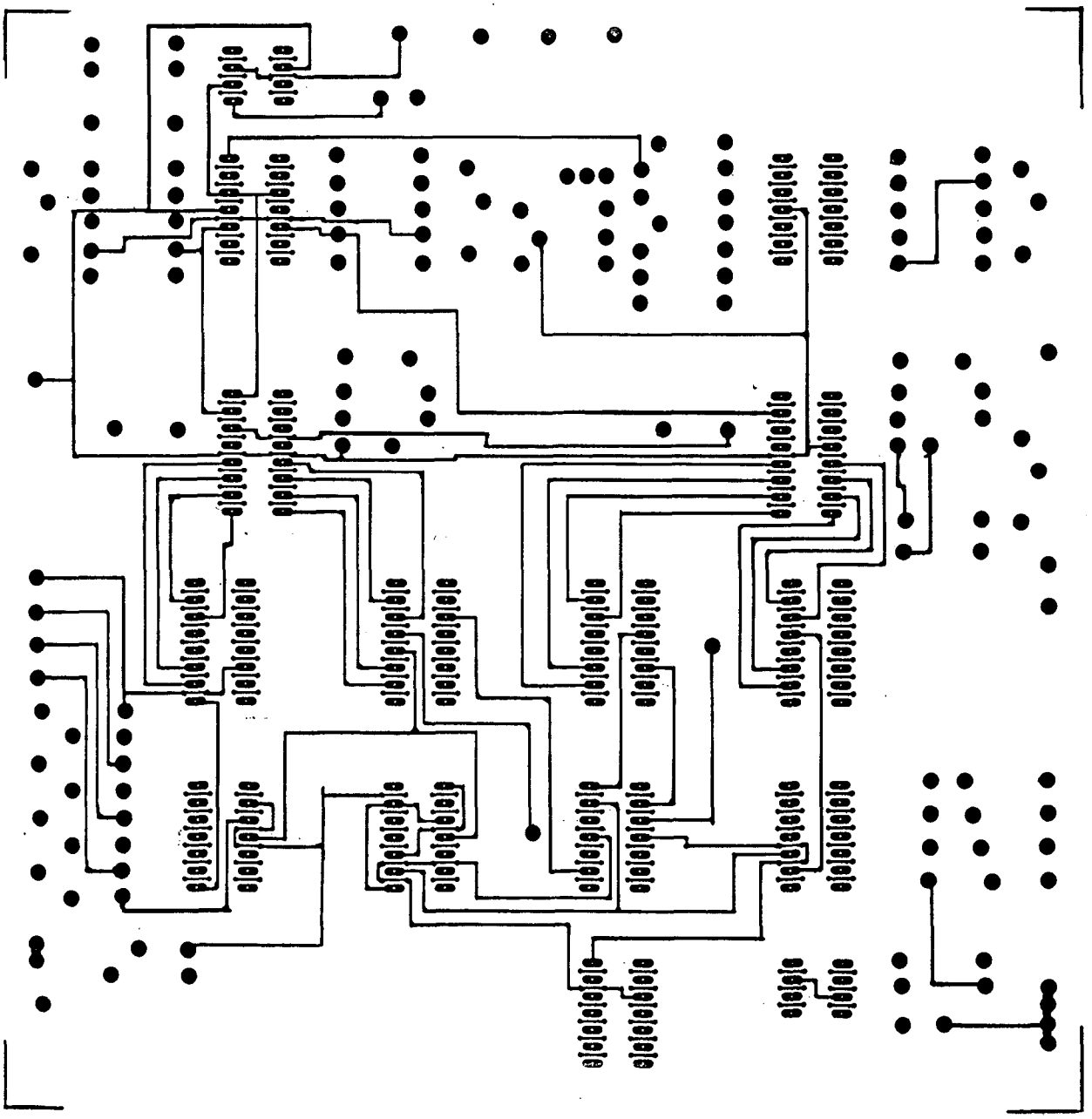
Cara de soldaduras, vista superior.



CIRCUITO IMPRESO

Tensión de Polarización, Lógica de Control, y Ampiflicador Lineal y Logarítmico.

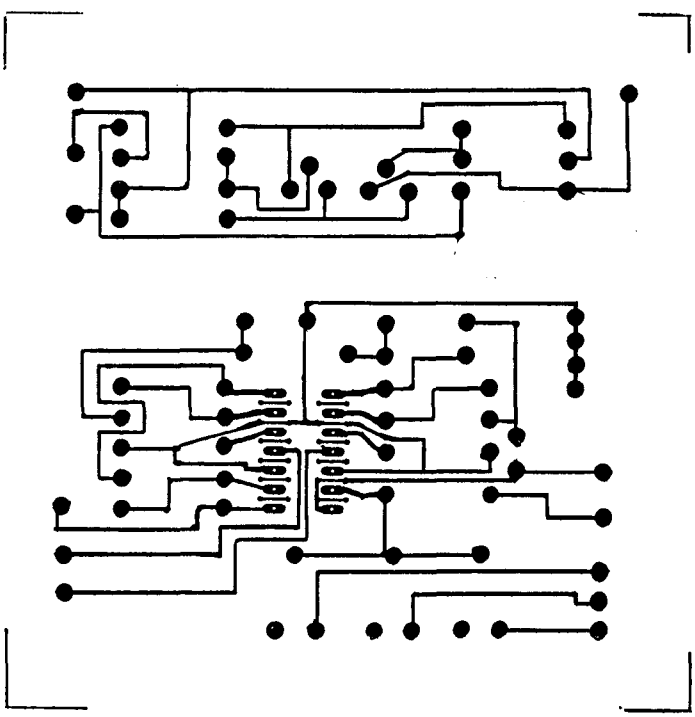
Cara de Componentes, vista superior.



CIRCUITO IMPRESO

Amplificador de Entrada, Rectificador, y Trigger Smith.

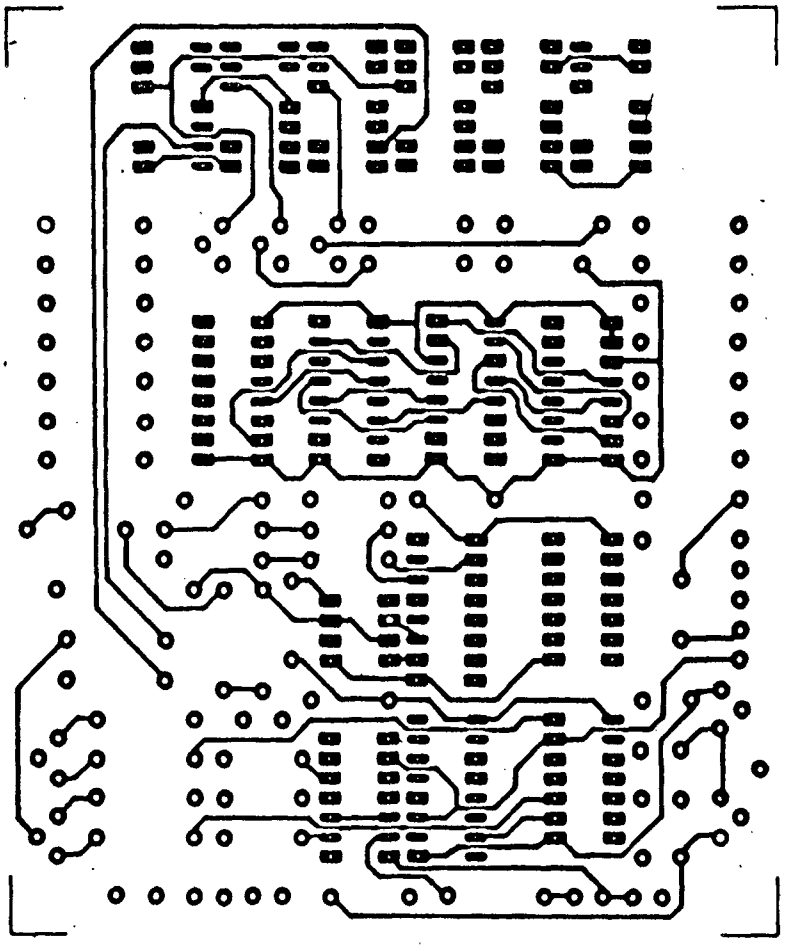
Cara de Soldaduras, vista superior.



CIRCUITO IMPRESO

Frecuencímetro Digital.

Cara de Componentes, vista superior.



CIRCUITO IMPRESO

Frecuencímetro Digital.

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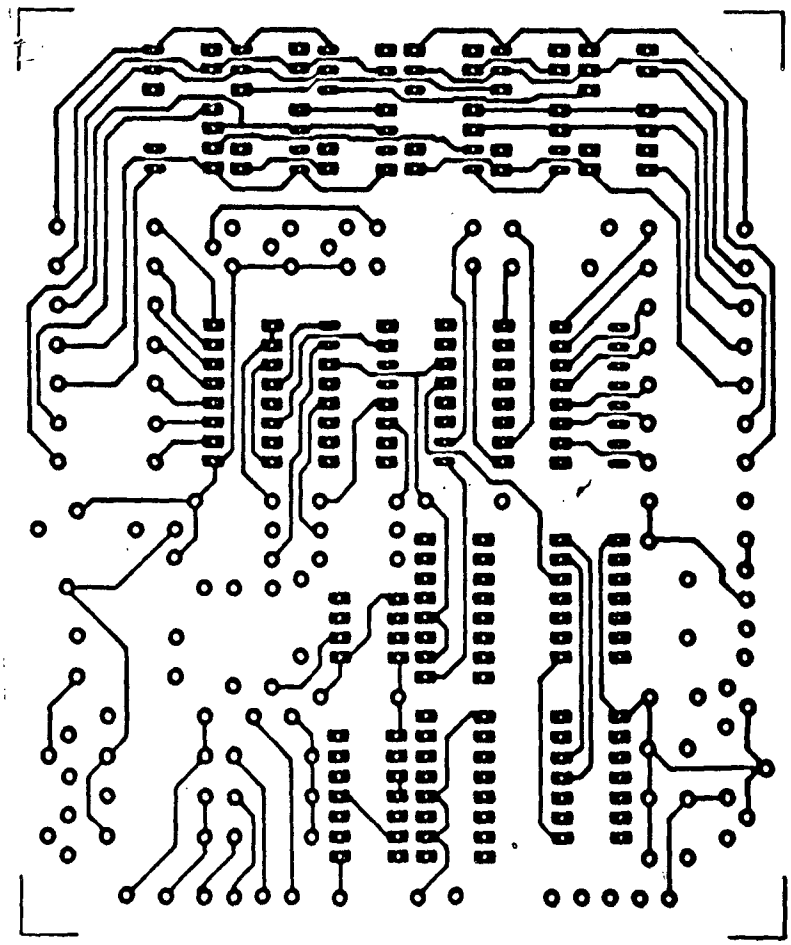


National Semiconductor

Audio/Radio Circuits

LM13600/LM13600A/LM11600A Dual Operational Transconductance Amplifiers With Linearizing Diodes and Buffers

General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The results is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers.

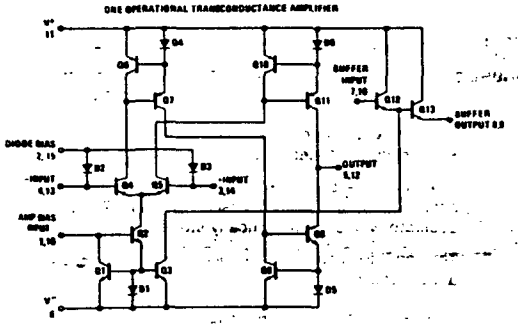
Features

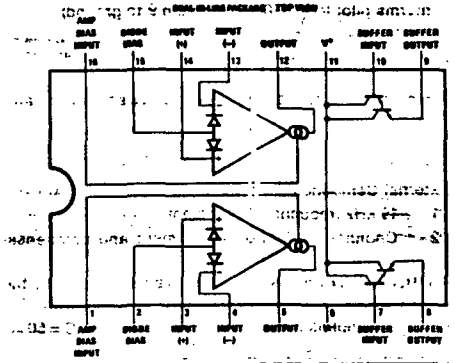
- gm adjustable over 6 decades
- Excellent gm linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedance buffers
- High output signal to noise ratio
- Wide supply range ± 2V to ± 22V.

Applications

- Current controlled amplifiers
- Current controlled impedances
- Current controlled filters
- Current controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Schematic and Connection Diagrams





Order Number LM13600J or LM11600AJ
See NS Package J16A

Order Number LM13600N or LM13600AN
See NS Package N16A

Absolute Maximum Ratings

Supply Voltage (Note 1)	
LM13600	36 V_{DC} or ± 18 V
LM13600A, LM11600A	44 V_{DC} or ± 22 V
Power Dissipation (Note 2) $T_A = 25°C$	
LM13600N, LM13600AN	570 mW
LM13600J, LM11600AJ	600mW
Differential Input Voltage	± 5 V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Indefinite
Buffer Output Current (Note 3)	20 mA
Operating Temperature Range	
LM13600N, LM13600AN	0° C to + 70° C
LM13600J, LM11600AJ	-55° C to + 125° C
DC Input Voltage	+ V_S to - V_S
Storage Temperature Range	-65° C to + 150° C
Lead Temperature (Soldering, 10 seconds)	300° C

Electrical Characteristics (Note 4)

Parameters	Conditions	LM13600			LM13600A LM11600A			Units
		Min	Typ	Max	Min	Typ	Max	
Input Offset Voltage (V_{OS})			0.4	4		0.4	1	mV
	Over Specified Temperature Range						2	mV
	I_{ABC} 5 μA		0.3	4		0.3	1	mV
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input Offset Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1	3		0.1	1	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	8		1	7	μA
Forward Transconductance(gm)		6700	9600	13000	7700	9600	12000	μmho
	Over specified Temp Range	5400			4000			μmho
gm Tracking			0.3			0.3		dB
Peak Output Current	RL = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	μA
	RL = 0, Over Specified Temp Range	300			300			μA
Peak Output Voltage								
Positive	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+ 12	+ 14.2		+ 12	+ 14.2		V
Negative	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	- 12	- 14.4		- 12	- 14.4		V
Supply Current	I_{ABC}=500μA,Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	Δ V_{OS}/Δ V+		20	150		20	150	μV/V
Negative	Δ V_{OS}/Δ V-		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common Mode Range		± 12	± 13.5		± 12	± 13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 KHz		100			100		dB
Diff.Input Current	I_{ABC} = 0, Input = ± 4 V		0.02	100		0.02	10	nA
Leakage Current	I_{ABC} = 0 (Refer To Test Circuit)		0.2	100		0.2	5	nA
Input Resistance		10	26		10	26		KΩ
Open Loop Bandwith			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μSec
Buff. Input Current	*(Note 5, Except I_{ABC} = 0 μA)*		0.2	0.4		0.2	0.4	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

Note 1. For selections to a supply voltage above ± 22V, contact factory.

Note 2. For operating at high temperatures, the device must be derated based on a 150° C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.

Note 3. Buffer output current should be limited so as to not exceed package dissipation.

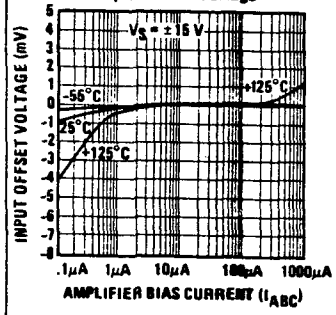
Note 4. These specifications apply for V_S = ± 15 V, T_A = 25° C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5. These specifications apply for V_S = ± 15V, I_{ABC} = 500 μA, R_{OUT} = 5 KΩ connected from the buffer output to - V_S and the input of the buffer is connected to the transconductance amplifier output.

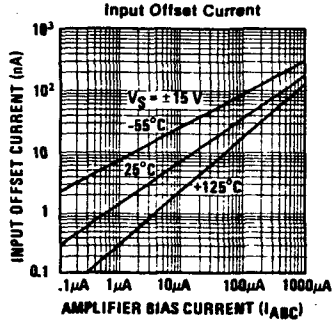
LM13600/LM13600A/LM11600A

Typical Performance Characteristics

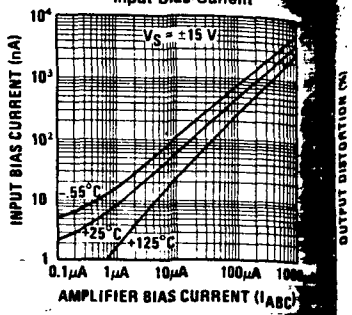
Input Offset Voltage



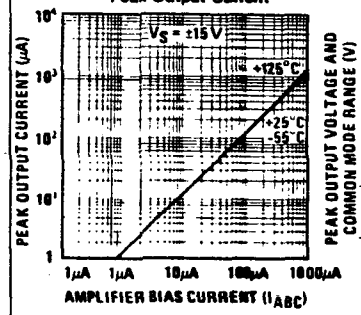
Input Offset Current



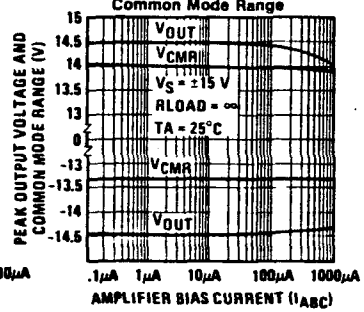
Input Bias Current



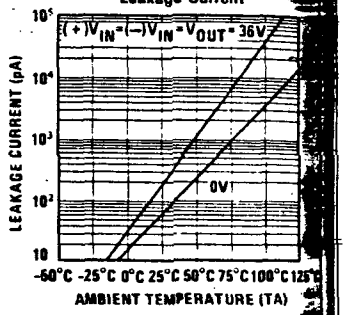
Peak Output Current



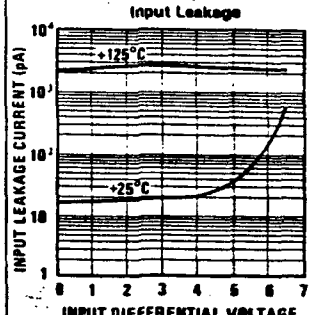
Peak Output Voltage and Common Mode Range



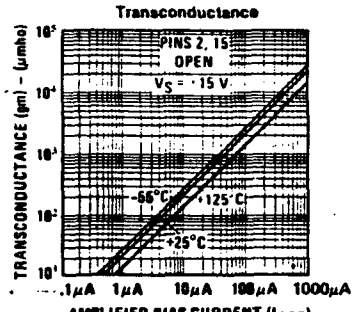
Leakage Current



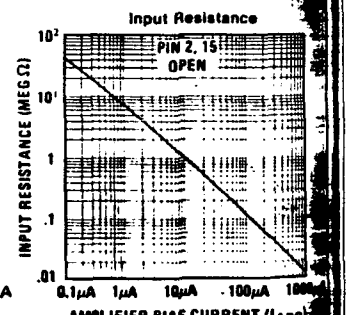
Input Leakage



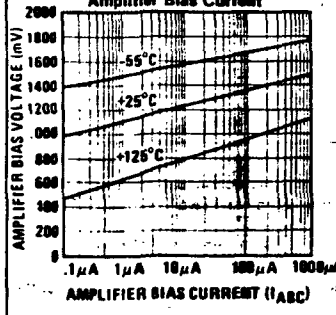
Transconductance



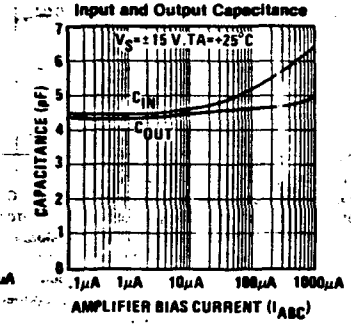
Input Resistance



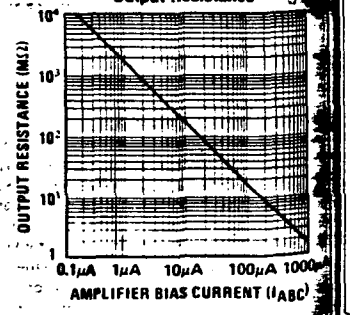
Amplifier Bias Voltage vs Amplifier Bias Current



Input and Output Capacitance

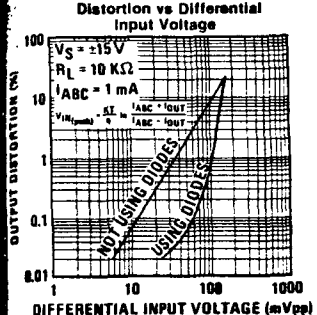


Output Resistance

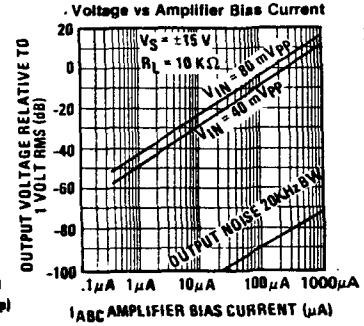


Typical Performance Characteristics (Cont'd)

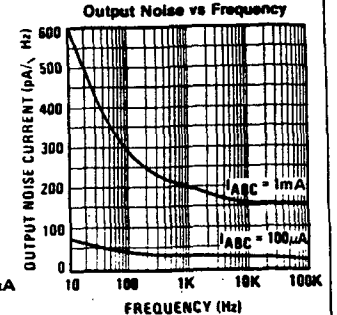
Distortion vs Differential Input Voltage

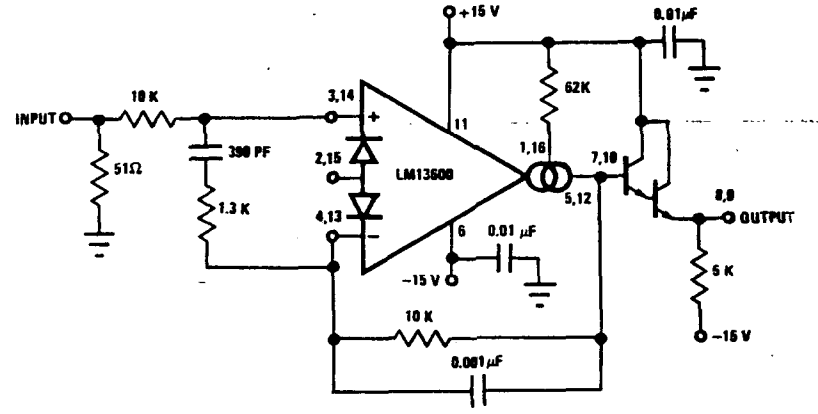


Voltage vs Amplifier Bias Current

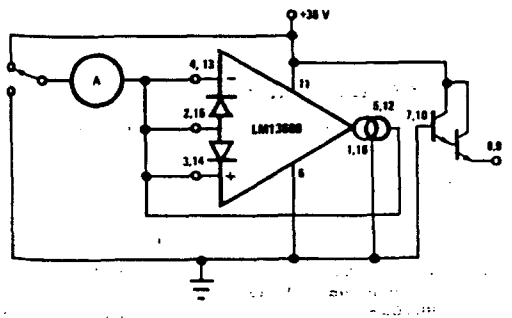


Output Noise vs Frequency

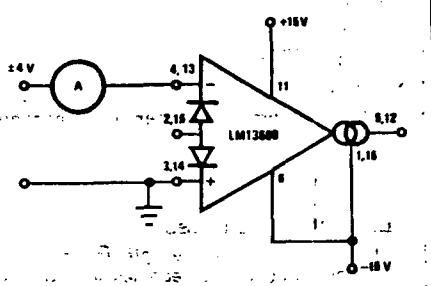




UNITY GAIN FOLLOWER



LEAKAGE CURRENT TEST CIRCUIT



DIFFERENTIAL INPUT CURRENT TEST CIRCUIT

Circuit Description

The differential transistor pair Q_4 and Q_5 form a transconductance stage in that the ratio of their collector currents is defined by the differential input voltage according to the transfer function:

$$V_{IN} = \frac{KT}{q} \ln \frac{I_5}{I_4} \quad (1)$$

where V_{IN} is the differential input voltage, KT/q is approximately 26 mV at 25° C and I_5 and I_4 are the collector currents of transistors Q_5 and Q_4 respectively. With the exception of Q_3 and Q_{13}, all transistors and diodes are identical in size. Transistors Q_1 and Q_2 with Diode D_1 form a current mirror which forces the sum of currents I_4 and I_5 to equal I_{ABC}:

$$I_4 + I_5 = I_{ABC} \quad (2)$$

where I_{ABC} is the amplifier bias current applied to the gain pin.

For small differential input voltages the ratio of I_4 and I_5 approaches unity and the Taylor series of the ln function can be approximated as:

$$\frac{KT}{q} \ln \frac{I_5}{I_4} \approx \frac{KT}{q} \frac{I_5 - I_4}{I_4} \quad (3)$$

$$I_4 \approx I_5 \approx \frac{I_{ABC}}{2}$$

$$V_{IN} \left[\frac{I_{ABC}\, q}{2KT}\right] = I_5 - I_4 \quad (4)$$

Collector currents I_4 and I_5 are not very useful by themselves and it is necessary to subtract one current from the other. The remaining transistors and diodes form three current mirrors that produce an output current equal to I_5 minus I_4 thus:

$$V_{IN} \left[\frac{I_{ABC}\, q}{2KT}\right] = I_{OUT} \quad (5)$$

The term in brackets is then the transconductance of the amplifier and is proportional to I_{ABC}.

Linearizing Diodes

For differential voltages greater than a few millivolts, Equation 3 becomes less valid and the transconductance becomes increasingly nonlinear. Figure 1 demonstrates how the internal diodes can linearize the transfer function of the amplifier. For convenience assume the diodes are biased with current sources and the input signal is in the form of current I_S. Since

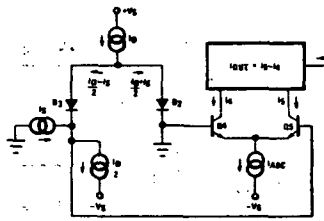


Figure 1. Linearizing Diodes

the sum of I_4 and I_5 is I_{ABC} and the difference is I_{OUT}, currents I_4 and I_5 can be written as follows:

$$I_4 = \frac{I_{ABC}}{2} - \frac{I_{OUT}}{2}, \quad I_5 = \frac{I_{ABC}}{2} + \frac{I_{OUT}}{2}$$

Since the diodes and the input transistors have identical geometries and are subject to similar voltages and temperatures, the following is true:

$$\frac{KT}{q} \ln \frac{\frac{I_D}{2} + I_S}{\frac{I_D}{2} - I_S} = \frac{KT}{q} \ln \frac{\frac{I_{ABC}}{2} + \frac{I_{out}}{2}}{\frac{I_{ABC}}{2} - \frac{I_{out}}{2}}$$

$$\therefore I_{out} = I_S \left(\frac{2I_{ABC}}{I_D}\right) \quad \text{for } |I_S| < \frac{I_D}{2} \quad (6)$$

Notice that in deriving Equation 6 no approximations have been made and there are no temperature dependent terms. The limitations are that the signal current not exceed $I_D/2$ and that the diodes be biased with currents. In practice, replacing the current sources with resistors will generate insignificant errors.

Controlled Impedance Buffers

The upper limit of transconductance is defined by the maximum value of I_{ABC} (2 mA). The lowest value of I_{ABC} for which the amplifier will function therefore determines the overall dynamic range. At very low values of I_{ABC}, a buffer which has very low input bias current is desirable. A FET follower satisfies the low input current requirement, but is somewhat nonlinear for large voltage swing. The controlled impedance buffer is a Darlington which modifies its input bias current to suit the need. For low values of I_{ABC}, the buffer's input current is minimal. At higher levels of I_{ABC} transistor Q_3 biases up Q_{12} with a current proportional to I_{ABC} for fast slew rate.

Applications/Voltage Controlled Amplifiers

Figure 2 shows how the linearizing diodes can be used in a voltage controlled amplifier. To understand the input biasing, it is best to consider the 13 KΩ resistor as a current source and use a Thevenin equivalent circuit as shown in Figure 3. This circuit is similar to Figure 1 and operates the same. The potentiometer in Figure 2 is adjusted to minimize the effects of the control signal at the output.

For optimum signal-to-noise performance, I_{ABC} should be as large as possible as shown by the Output Voltage vs. Amplifier Bias Current graph. Larger amplitudes of input signal also improve the S/N ratio. The linearizing diodes help here by allowing larger input signals for the same output distortion as shown by the Distortion vs. Differential Input Voltage graph. S/N may be optimized by adjusting the magnitude of the input signal via R_{IN} (Figure 2)until the output distortion is below some desired level. The output voltage swing can then be set at any level by selecting R_L.

Although the noise contribution of the linearizing diodes is negligible relative to the contribution of the amplifier's internal transistors, I_D should be as large as possible. This minimizes the dynamic junction resistance of the diodes (r_e) and maximizes their linearizing action when balanced against R_{IN}. A value of 1 mA is recommended for I_D unless the specific application demands otherwise.

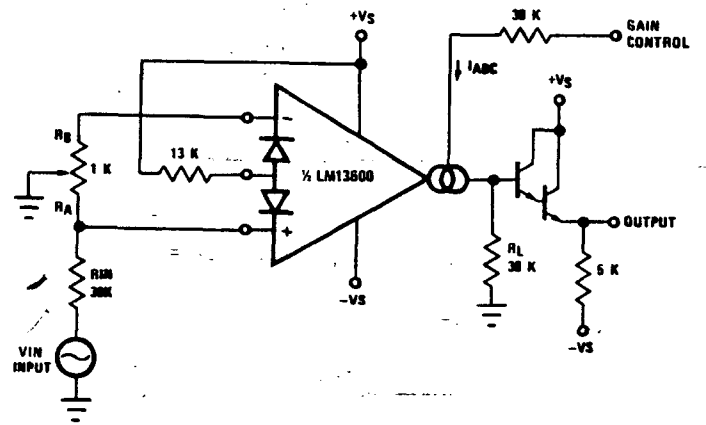


Figure. 2 Voltage Controlled Amplifier

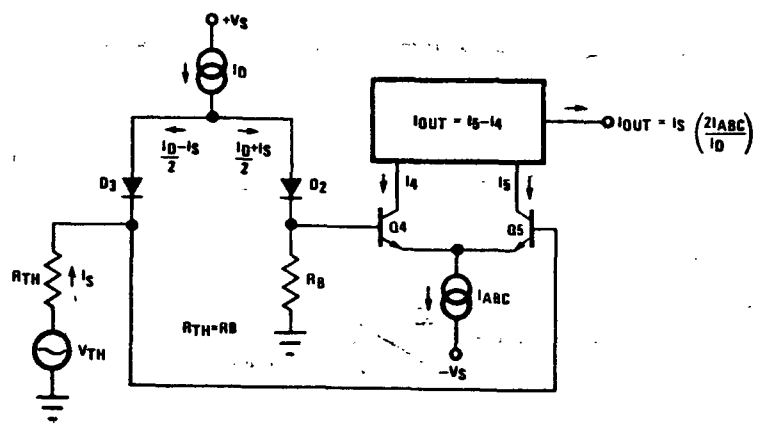


Figure 3. Equivalent VCA Input Circuit

Stereo Volume Control

The circuit of Figure 4 uses the excellent matching of the two LM13600 amplifiers to provide a Stereo Volume Control with a typical channel-to-channel gain tracking of 0.3 dB. Rp is provided to minimize the output offset voltage and may be replaced with two 510Ω resistors in AC-coupled applications. For the component values given, amplifier gain is derived from Figure 2 as being:

$$\frac{V_O}{V_{IN}} = 940 \times I_{ABC}$$

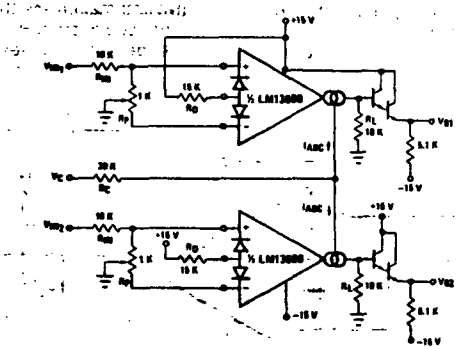


Figure 4. Stereo Volume Control

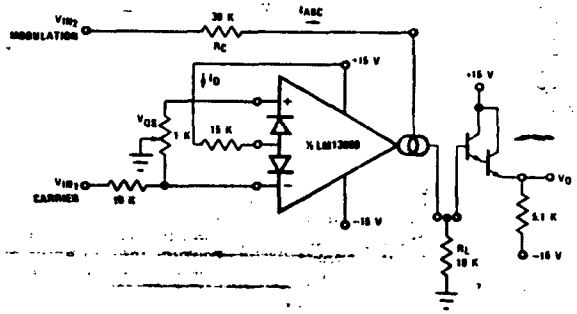


Figure 5. Amplitude Modulator

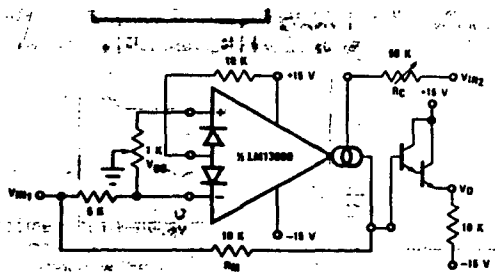


Figure 6. Four-Quadrant Multiplier

If V_C is derived from a second signal so... then the circuit becomes an amplitu... modulator or two-quadrant multiplier as sh... in Figure 5, where:

$$I_O = \frac{-2I_S}{I_D}(I_{ABC}) = \frac{-2I_S}{I_D}\frac{V_{IN2}}{R_C} - \frac{2I_S}{I_D}\frac{(V^+ ...}{R_C}$$

The constant term in the above equation... be cancelled by feeding $I_S \times I_D R_C/2(V^+ + 1.4V)$ to I_O. The circuit of Figure 6 adds R_M to pro...

this current, resulting in a four-quadrant multiplier where R_C is trimmed such that $V_O = 0V$ for $V_{IN2} = 0V$. R_M also serves as the load resistor for I_O.

Noting that the gain of the LM13600 amplifier of Figure 3 may be controlled by varying the linearizing diode current I_D as well as by varying I_{ABC}, Figure 7 shows an AGC Amplifier using this approach. As V_O reaches a high enough amplitude ($3V_{BE}$) to turn on the Darlington transistors and the linearizing diodes, the increase in I_D reduces the amplifier gain so as to hold V_O at that level.

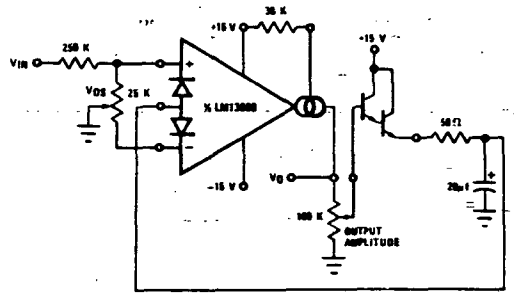
Voltage Controlled Resistors

An Operational Transconductance Amplifier (OTA) may be used to implement a Voltage Controlled Resistor as shown in Figure 8. A signal voltage applied at R_X generates a V_{IN} to the LM13600 which is then multiplied by the gm of the amplifier to produce an output current, thus:

$$R_X = \frac{R + R_A}{gmR_A}$$

where gm ≈ $19.2I_{ABC}$ at 25°C. Note that the attenuation of V_O by R and R_A is necessary to maintain V_{IN} within the linear range of the LM13600 input.

Figure 9 shows a similar VCR where the linearizing diodes are added, essentially improving the noise performance of the resistor. A floating VCR



7. AGC Amplifier

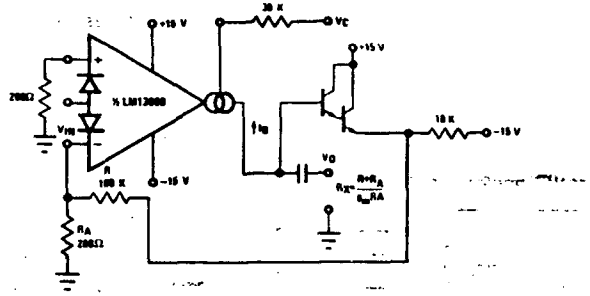


Figure 8. Voltage Controlled Resistor, Single-Ended

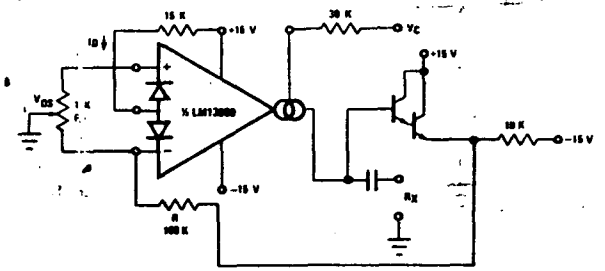


Figure 9. Voltage Controlled Resistor With Linearizing Diodes

shown in Figure 10, where each "end" of the resistor" may be at any voltage within the output voltage range of the LM13600.

Voltage Controlled Filters

OTA's are extremely useful for implementing voltage controlled filters, with the LM13600 having the advantage that the required buffers are included on the I.C. The VC Lo-Pass Filter Figure 11 performs as a unity-gain buffer amplifier at frequencies below cut-off, with the cut-off frequency being the point at which X_C/gm equals the closed-loop gain of (R/R_A). At frequencies above cut-off the circuit provides a single RC roll-off (6 dB per octave) of the input signal amplitude with a -3 dB point defined by the given equation.

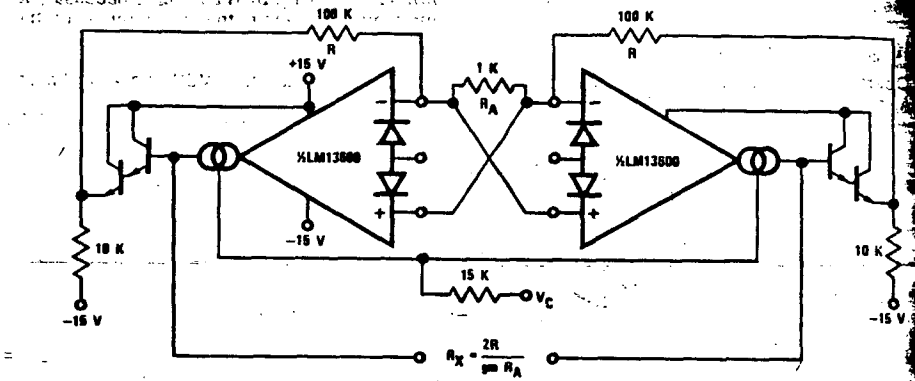


Figure 10. Floating Voltage Controlled Resistor

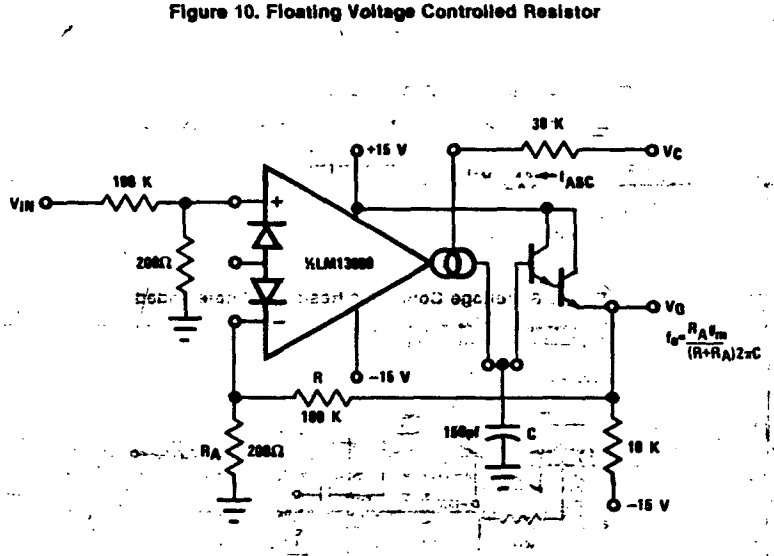


Figure 11. Voltage Controlled Low-Pass Filter

where gm is again 19.2 x I_{ABC} at room temperature. Figure 12 shows a VC High-Pass Filter which operates in much the same manner, providing a single RC roll-off below the defined cut-off frequency.

Additional amplifiers may be used to implement higher order filters as demonstrated by the two-pole Butterworth Lo-Pass Filter of Figure 13 and the state variable filter of Figure 14. Due to the excellent gm tracking of the two amplifiers and the varied bias of the buffer Darlingtons, these filters perform well over several decades of frequency.

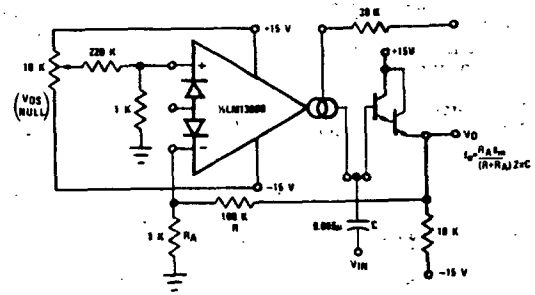


Figure 12. Voltage Controlled Hi-Pass Filter

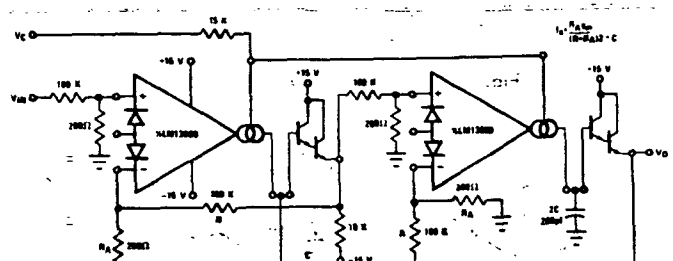


Figure 13. Voltage Controlled 2-pole Butterworth Lo-Pass Filter

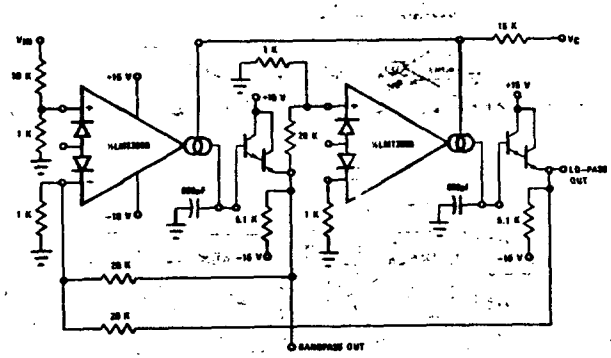


Figure 14. Voltage Controlled State Variable Filter

Voltage Controlled Oscillators

The classic Triangular/Square Wave VCO of Figure 15 is one of a variety of Voltage Controlled Oscillators which may be built utilizing the LM13600. With the component values shown, this oscillator provides signals from 200 kHz to below 2 Hz as I_C is varied from 1mA to 10nA. The output amplitudes are set by $I_A \times R_A$. Note that the peak differential input voltage must be less than 5 volts to prevent zenering the inputs.

A few modifications to this circuit produce the ramp/pulse VCO of Figure 16. When V_{O2} is high, I_F is added to I_C to increase amplifier A1's bias current and thus to increase the charging rate of capacitor C. When V_{O2} is low, I_F goes to zero and the capacitor discharge current is set by I_C.

The VC Lo-Pass Filter of Figure 11 may be used to produce a high-quality sinusoidal VCO. The circuit of Figure 16 employs two LM13600 packages, with three of the amplifiers configured as lo-pass filters and the fourth as a limiter/inverter. The circuit oscillates at the frequency at which the loop phase-shift is 360° or 180° for the inverter and 60° per filter stage. This VCO operates from 5 Hz to 50 kHz with less than 1% THD.

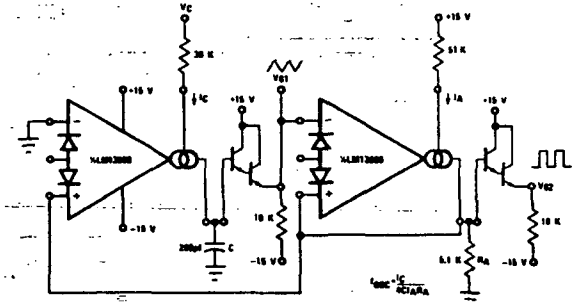


Figure 15. Triangular/Square-Wave VCO

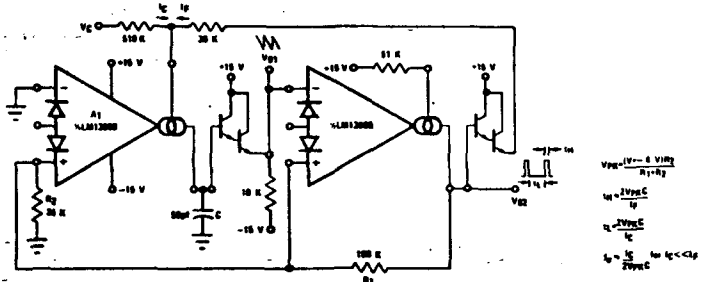


Figure 16. Ramp/Pulse VCO

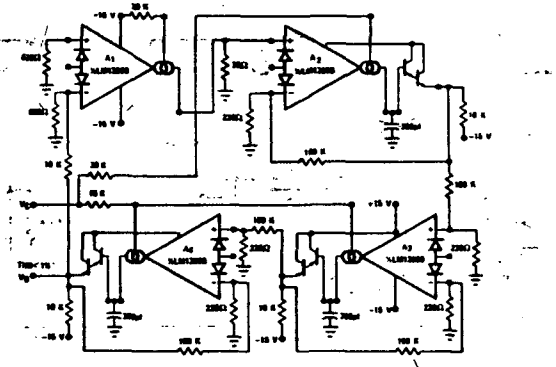


Figure 17. Sinusoidal VCO

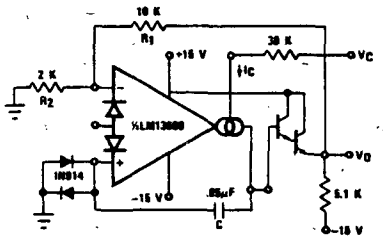


Figure 18. Single Amplifier VCO

Figure 18 shows how to build a VCO using one amplifier when the other amplifier is needed for another function.

Additional Applications

Figure 19 presents an interesting one-shot which draws no power supply current until it is triggered. A positive-going trigger pulse of at least 2V amplitude turns on the amplifier through R_B and pulls the non-inverting input high. The amplifier regenerates and latches its output high until capacitor C charges to the voltage level on the non-inverting input. The output then switches low, turning off the amplifier and discharging the capacitor. The capacitor discharge rate is speeded up by shorting the diode bias pin to the inverting input so that an additional discharge current flows through D_1 when the amplifier output switches low. A special feature of this timer is that the other amplifier, when biased from V_O, can perform another function and draw zero stand-by power as well.

The operation of the multiplexer of Figure 20 is very straightforward. When A1 is turned on it holds V_O equal to V_{IN1} and when A2 is supplied with bias current then it controls V_O. C_C and R_C serve to stabilize the unity-gain

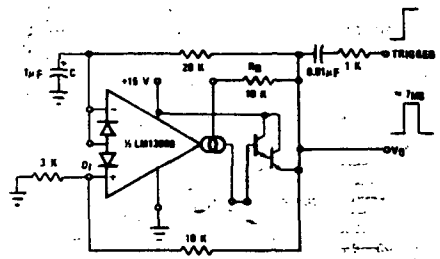


Figure 19. Zero Stand-by Power Timer

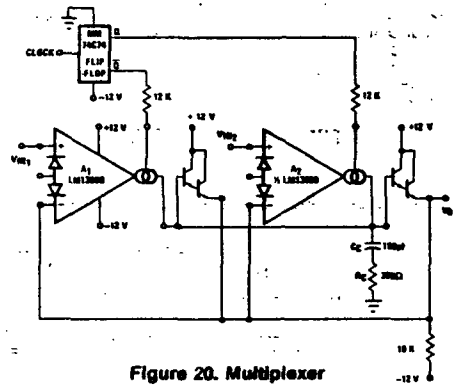


Figure 20. Multiplexer

configuration of amplifiers A1 and A2. The maximum clock rate is limited to about 200 KHz by the LM13600 slew rate into 150 pF when the $(V_{IN1}-V_{IN2})$ differential is at its maximum allowable value of 5 volts.

The Phase-Locked Loop of Figure 21 uses the four-quadrant multiplier of Figure 6 and the V_{CO} of Figure 18 to produce a PLL with a ± 5% hold-in range and an input sensitivity of about 300 mV.

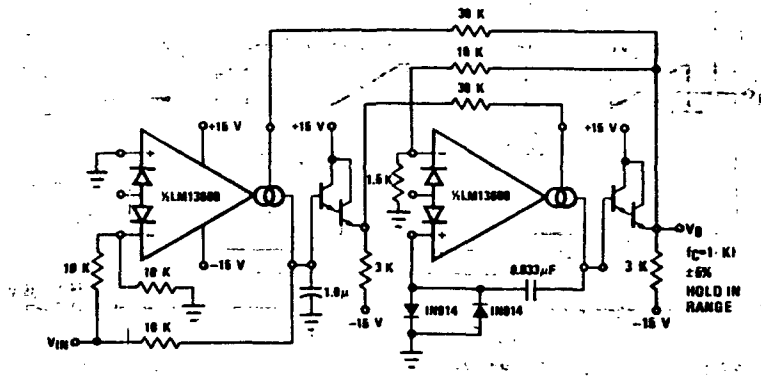


Figure 21. Phase Lock Loop

Schmitt Trigger of Figure 22 uses the amplifier output current into R to set the hysteresis of the comparator; thus $V_H = 2 \times R \times I_B$. Varying I_B will produce a Schmitt Trigger with variable hysteresis.

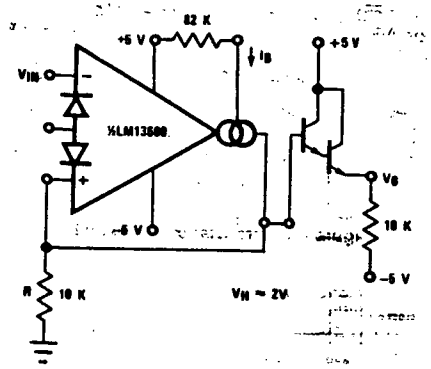


Figure 22. Schmitt Trigger

Figure 23 shows a Tachometer or Frequency-to-Voltage converter. Whenever A1 is toggled by a positive-going input, an amount of charge equal to $(V_H - V_L)\ C_t$ is sourced into C_f and R_t. This once per cycle charge is then balanced by the current of V_O/R_t. The maximum F_{IN} is limited by the amount of time required to charge C_t from V_L to V_H with a current of I_B, where V_L and V_H represent the maximum low and maximum high output voltage swing of the LM13600. D1 is added to provide a discharge path for C_t when A1 switches low.

The Peak Detector of Figure 24 uses A2 to turn on A1 whenever V_{IN} becomes more positive than V_O. A1 then charges storage capacitor C to hold V_O equal to $V_{IN}PK$. One precaution to observe when using this circuit: the Darlington transistor used must be on the same side of the package as A2 since the A1 Darlington will be turned on and off with A1. Pulling the output of A2 low through D1 serves to turn off A1 so that V_O remains constant.

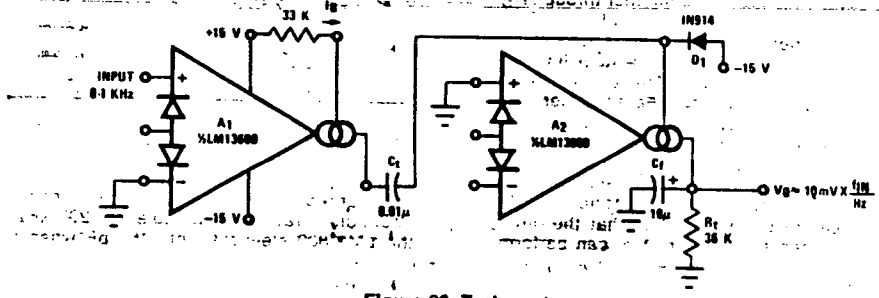


Figure 23. Tachometer

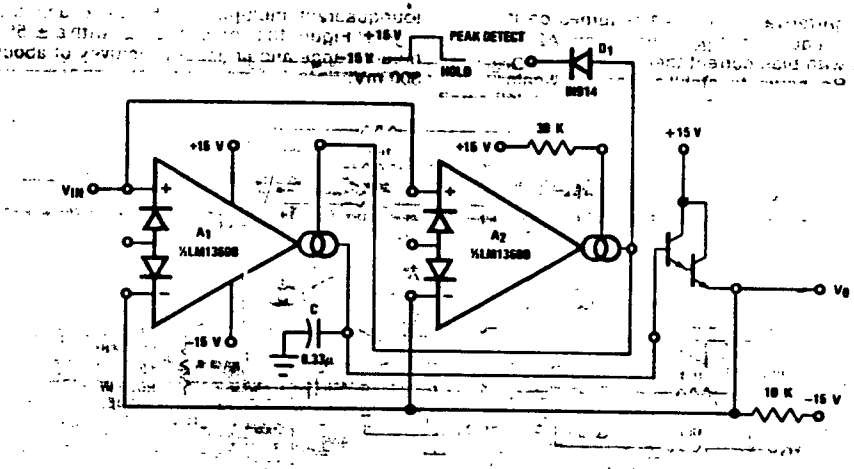


Figure 24. Peak Detector and Hold Circuit

The Sample-Hold circuit of Figure 25 also requires that the Darlington buffer used be from the other (A2) half of the package and that the corresponding amplifier be biased on continuously.

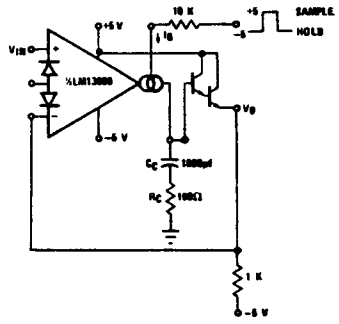


Figure 25. Sample-Hold Circuit

The Ramp-and-Hold of Figure 26 sources I_B into capacitor C whenever the input to A1 is brought high, giving a ramp-rate of about 1V/ms for the component values shown.

The true RMS converter of Figure 27 is essentially an automatic gain control amplifier which adjusts its gain such that the AC power at the output of amplifier A1 is constant. The output power of amplifier A1 is monitored by squaring amplifier A2 and the average compared to a reference voltage with amplifier A3. The output of A3 provides bias current to the diodes of A1 to attenuate the input signal. Because the output power of A1 is held constant, the RMS value is constant and the attentuation is directly proportional to the RMS value of the input voltage. The attenuation is also proportional to the diode bias current. Amplifier A4 adjusts the ratio of currents through the diodes to be equal and therefore the voltage at the output of A4 is proportional to the RMS value of the input voltage. The calibration potentiometer is set such that V_O reads directly in RMS volts.

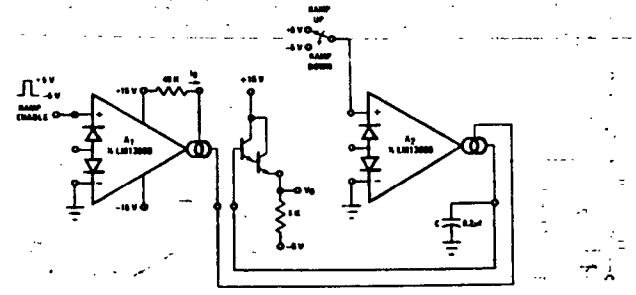


Figure 26. Ramp and Hold

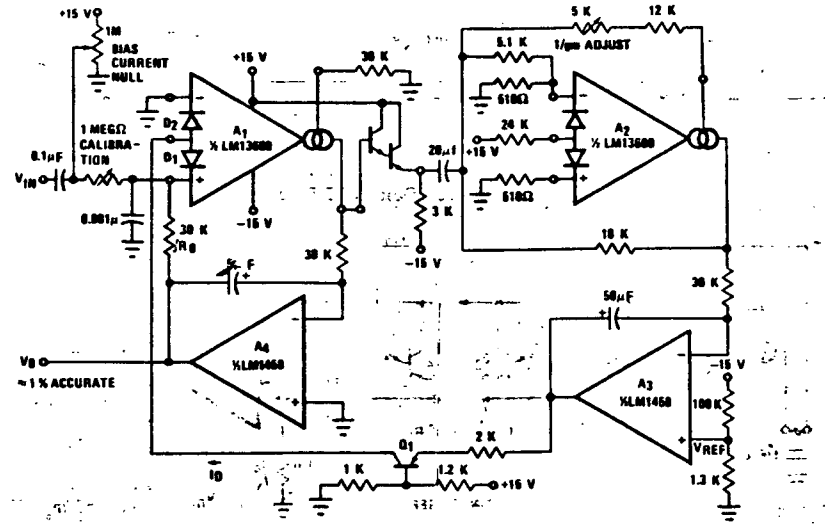


Figure 27. True RMS Converter

The circuit of Figure 28 is a voltage reference of variable Temperature Coefficient. The 100 KΩ potentiometer adjusts the output voltage which has a positive TC above 1.2 volts, zero TC at about 1.2 volts and negative TC below 1.2 volts. This is accomplished by balancing the TC of the A2 transfer function against the complementary TC of D1.

The log amplifier of Figure 29 responds to the ratio of current through buffer transistors Q3 and Q4. Zero temperature dependence for V_{OUT} is ensured in that the TC of the A2 transfer function is equal and opposite to the TC of the logging transistors Q3 and Q4.

The wide dynamic range of the LM13600 allows easy control of the output pulse width in the Pulse Width Modulator of Figure 30.

For generating I_{ABC} over a range of 4 to 6 decades of current, the system of Figure 31 provides a logarithmic current out for a linear voltage in.

Since the closed-loop configuration ensures that the input to A2 is held equal to 0V, the output current of A1 is equal to $I_3 = -V_C/R_C$.

The differential voltage between Q1 and Q2 is attenuated by the R1,R2 network so that A1 may be assumed to be operating within its linear range. From equation (5), the input voltage to A1 is:

$$V_{IN1} = \frac{-2KTI_3}{qI_2} = \frac{2KTV_C}{qI_2R_C}$$

The voltage on the base of Q1 is then

$$V_{B1} = \frac{(R_1+R_2)\,V_{IN1}}{R_1}$$

The ratio of the Q1 to Q2 collector currents is defined by:

$$V_{B1} = \frac{KT}{q}\ln\frac{I_{C2}}{I_{C1}} \approx \frac{KT}{q}\ln\frac{I_{ABC}}{I_1}$$

Combining and solving for I_{ABC} yields:

$$I_{ABC} = I_{1e}^{\frac{2(R_1+R_2)\,V_C}{R_1I_2R_C}}$$

This logarithmic current can be used to bias the circuit of Figure 4 to provide temperature independent stereo attenuation characteristic.

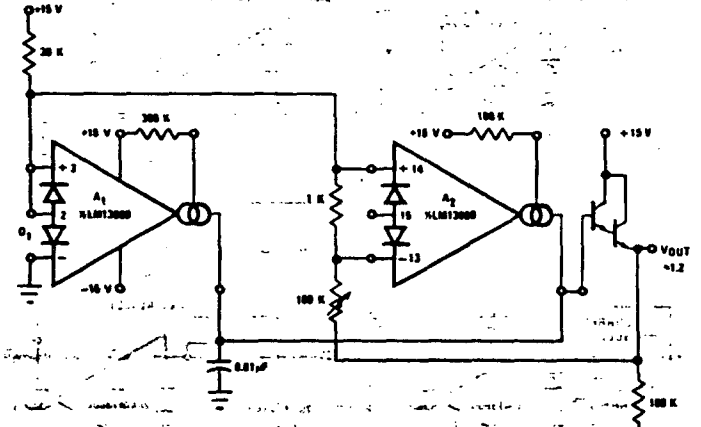
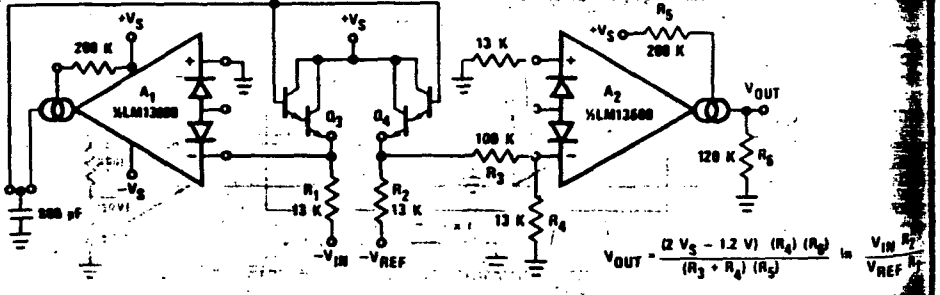


Figure 28. Delta VBE Reference



$$V_{OUT} = \frac{(2\,V_S - 1.2\,V)\,(R_4)\,(R_6)}{(R_3+R_4)\,(R_5)}\ln\frac{V_{IN}}{V_{REF}}\frac{R_2}{R_1}$$

Figure 29. Log Amplifier

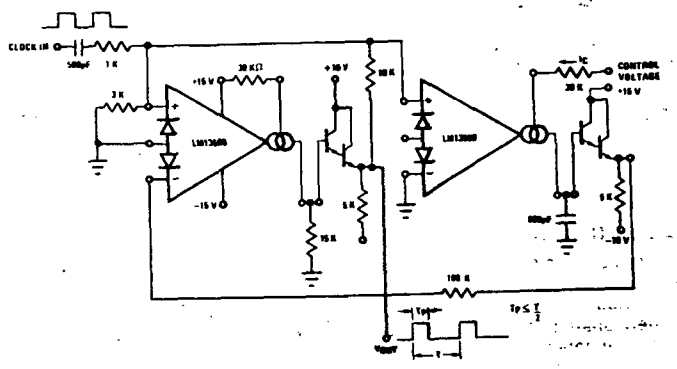


Figure 30. Pulse Width Modulator

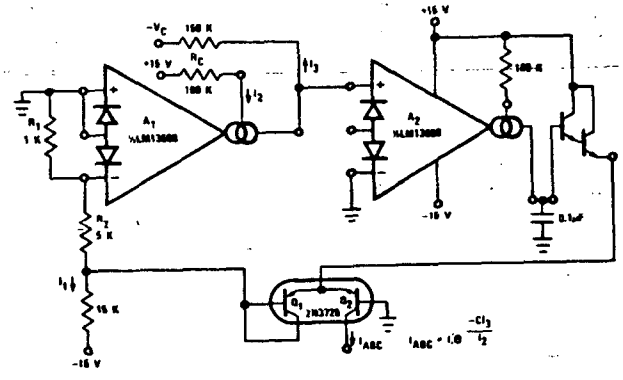


Figure 31. Logarithmic Current Source

LM555/LM555C Timer

General Description

The LM555 is a highly stable device for generating accurate time delays or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and duty cycle are accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output circuit can source or sink up to 200 mA or drive TTL circuits.

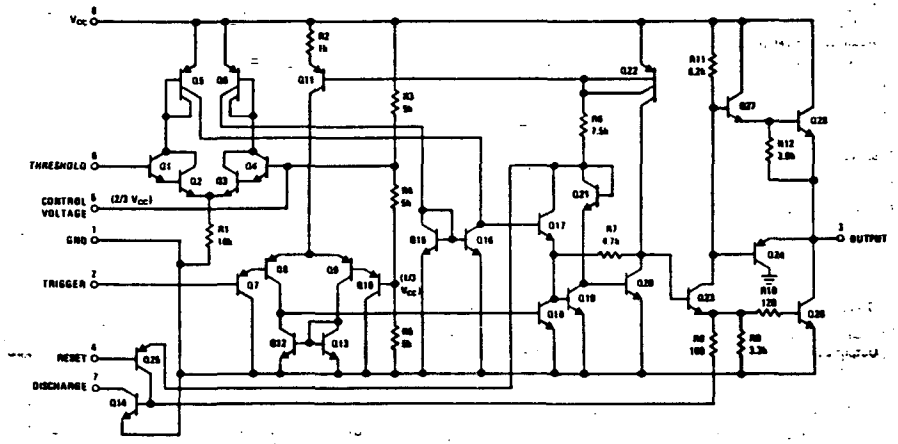
Features

- Direct replacement for SE555/NE555
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

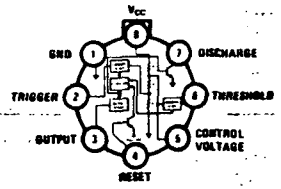
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagrams

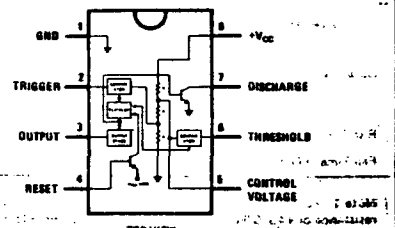
Metal Can Package



TOP VIEW

Order Number LM555H, LM555CH
See NS Package H08C

Dual-In-Line Package



TOP VIEW

Order Number LM555CN
See NS Package N08B
Order Number LM555J or LM555CJ
See NS Package J08A

Absolute Maximum Ratings

Supply Voltage	+18V
Power Dissipation (Note 1)	600 mW
Operating Temperature Ranges	
LM555C	0°C to +70°C
LM555	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (T_A = 25°C, V_{CC} = +5V to +15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LM555			LM555C			
		MIN	TYP	MAX	MIN	TYP	MAX	
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V, R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V, R_L = ∞ (Low State) (Note 2)		10	12		10	15	mA
Timing Error, Monostable								
Initial Accuracy			0.5			1		%
Drift with Temperature	R_A, R_B = 1k to 100 k, C = 0.1μF, (Note 3)		30			50		ppm/°C
Accuracy over Temperature			1.5			1.5		%
Drift with Supply			0.05			0.1		%/V
Timing Error, Astable								
Initial Accuracy			1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Accuracy over Temperature			2.5			3.0		%
Drift with Supply			0.15			0.30		%/V
Threshold Voltage			0.667			0.667		x V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		V
Trigger Current			0.01	0.5		0.5	0.9	μA
Reset Voltage		0.4	0.5	1	0.4	0.5	1	V
Reset Current			0.1	0.4		0.1	0.4	mA
Threshold Current	(Note 4)		0.1	0.25		0.1	0.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	V
Pin 7 Leakage Output High			1	100		1	100	nA
Pin 7 Sat (Note 5)								
Output Low	V_{CC} = 15V, I_7 = 15 mA		150			180		mV
Output Low	V_{CC} = 4.5V, I_7 = 4.5 mA		70	100		80	200	mV
Output Voltage Drop (Low)	V_{CC} = 15V							
	I_{SINK} = 10 mA		0.1	0.15		0.1	0.25	V
	I_{SINK} = 50 mA		0.4	0.5		0.4	0.75	V
	I_{SINK} = 100 mA		2	2.2		2	2.5	V
	I_{SINK} = 200 mA		2.5			2.5		V
	V_{CC} = 5V							
	I_{SINK} = 8 mA		0.1	0.25				V
	I_{SINK} = 5 mA					0.25	0.35	V
Output Voltage Drop (High)	I_{SOURCE} = 200 mA, V_{CC} = 15V		12.5			12.5		V
	I_{SOURCE} = 100 mA, V_{CC} = 15V	13	13.3		12.75	13.3		V
	V_{CC} = 5V	3	3.3		2.75	3.3		V
Rise Time of Output			100			100		ns
Fall Time of Output			100			100		ns

Note 1: For operating at elevated temperatures the device must be derated based on a +150°C maximum junction temperature and a thermal resistance of +45°C/W junction to case for TO-5 and +150°C/W junction to ambient for both packages.

Note 2: Supply current when output high typically 1 mA less at V_{CC} = 5V.

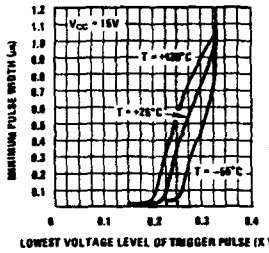
Note 3: Tested at V_{CC} = 5V and V_{CC} = 15V.

Note 4: This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total ($R_A + R_B$) is 20 MΩ.

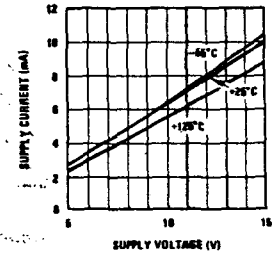
Note 5: No protection against excessive pin 7 current is necessary providing the package dissipation rating will not be exceeded.

Typical Performance Characteristics

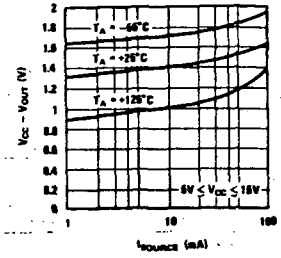
Minimum Pulse Width Required for Triggering



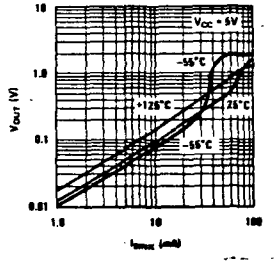
Supply Current vs Supply Voltage



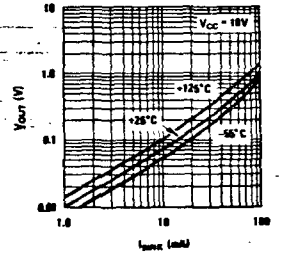
High Output Voltage vs Output Source Current



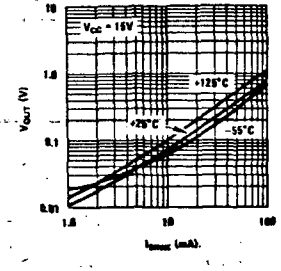
Low Output Voltage vs Output Sink Current



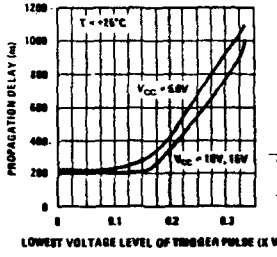
Low Output Voltage vs Output Sink Current



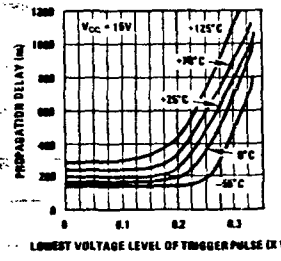
Low Output Voltage vs Output Sink Current



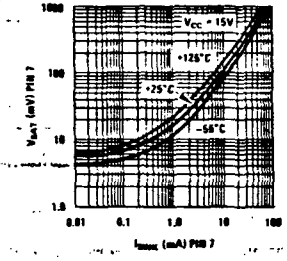
Output Propagation Delay vs Voltage Level of Trigger Pulse



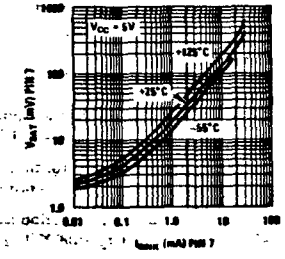
Output Propagation Delay vs Voltage Level of Trigger Pulse



Discharge Transistor (Pin 7) Voltage vs Sink Current



Discharge Transistor (Pin 7) Voltage vs Sink Current



Applications Information

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (*Figure 1*). The external capacitor is initially held discharged by a transistor inside the timer. Upon application of a negative trigger pulse of less than 1/3 V_{CC} to pin 2, the flip-flop is set which both releases the short circuit across the capacitor and drives the output high.

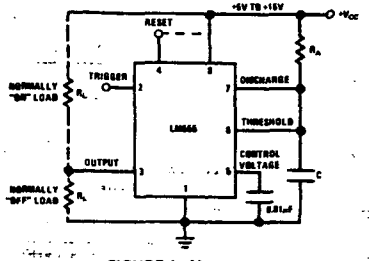


FIGURE 1. Monostable

The voltage across the capacitor then increases exponentially for a period of $t = 1.1\ R_A C$, at the end of which time the voltage equals 2/3 V_{CC}. The comparator then resets the flip-flop which in turn discharges the capacitor and drives the output to its low state. *Figure 2* shows the waveforms generated in this mode of operation. Since the charge and the threshold level of the comparator are both directly proportional to supply voltage, the timing internal is independent of supply.

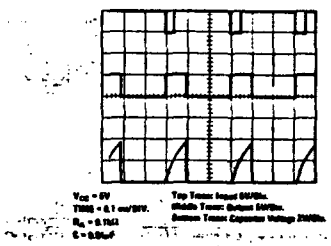


FIGURE 2. Monostable Waveforms

During the timing cycle when the output is high, the further application of a trigger pulse will not effect the circuit. However the circuit can be reset during this time by the application of a negative pulse to the reset terminal (pin 4). The output will then remain in the low state until a trigger pulse is again applied.

When the reset function is not in use, it is recommended that it be connected to V_{CC} to avoid any possibility of false triggering.

Figure 3 is a nomograph for easy determination of R, C values for various time delays.

NOTE: In monostable operation, the trigger should be driven high before the end of timing cycle.

ASTABLE OPERATION

If the circuit is connected as shown in *Figure 4* (pins 2 and 6 connected) it will trigger itself and free run as a

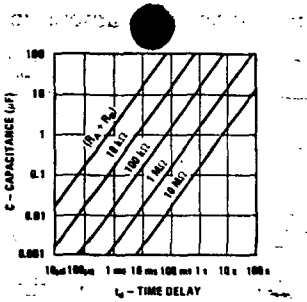


FIGURE 3. Time Delay

multivibrator. The external capacitor charges through $R_A + R_B$ and discharges through R_B. Thus the duty cycle may be precisely set by the ratio of these two resistors.

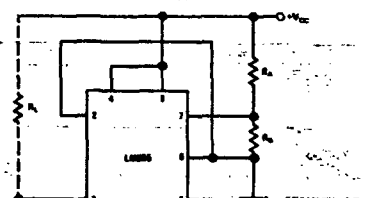


FIGURE 4. Astable

In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

Figure 5 shows the waveforms generated in this mode of operation.

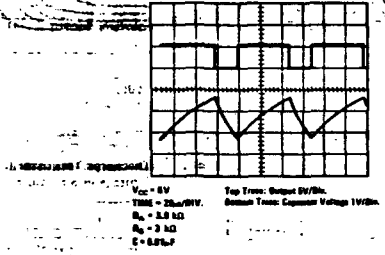


FIGURE 5. Astable Waveforms

The charge time (output high) is given by:

$$t_1 = 0.693\ (R_A + R_B)\ C$$

And the discharge time (output low) by:

$$t_2 = 0.693\ (R_B)\ C$$

Thus the total period is:

$$T = t_1 + t_2 = 0.693\ (R_A + 2R_B)\ C$$

Applications Information (Continued)

The frequency of oscillation is:

$$f = \frac{1}{T} = \frac{1.44}{(R_A + 2R_B)\ C}$$

Figure 6 may be used for quick determination of these RC values.

The duty cycle is:

$$D = \frac{R_B}{R_A + 2R_B}$$

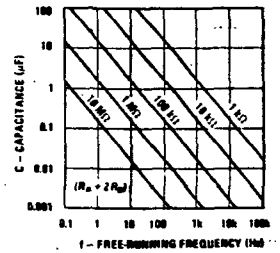


FIGURE 6. Free Running Frequency

FREQUENCY DIVIDER

The monostable circuit of *Figure 1* can be used as a frequency divider by adjusting the length of the timing cycle. *Figure 7* shows the waveforms generated in a divide by three circuit.

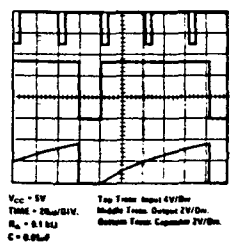


FIGURE 7. Frequency Divider

PULSE WIDTH MODULATOR

When the timer is connected in the monostable mode and triggered with a continuous pulse train, the output pulse width can be modulated by a signal applied to pin 5. *Figure 8* shows the circuit, and in *Figure 9* are some waveform examples.

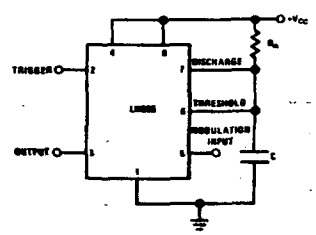


FIGURE 8. Pulse Width Modulator

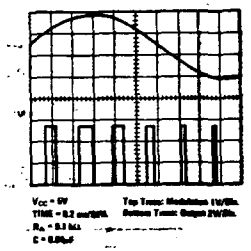


FIGURE 9. Pulse Width Modulator

PULSE POSITION MODULATOR

This application uses the timer connected for astable operation, as in *Figure 10*, with a modulating signal again applied to the control voltage terminal. The pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied. *Figure 11* shows the waveforms generated for a triangle wave modulation signal.

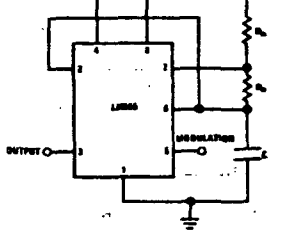


FIGURE 10. Pulse Position Modulator

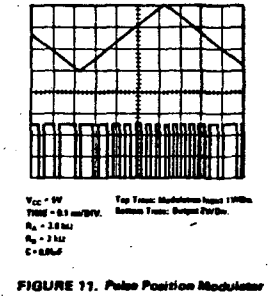


FIGURE 11. Pulse Position Modulator

LINEAR RAMP

When the pullup resistor, R_A, in the monostable circuit is replaced by a constant current source, a linear ramp is

Applications Information (Continued)

generated. *Figure 12* shows a circuit configuration that will perform this function.

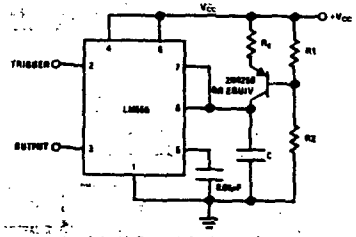


FIGURE 12.

Figure 13 shows waveforms generated by the linear ramp.

The time interval is given by:

$$T = \frac{2/3\ V_{CC}\ R_E\ (R_1 + R_2)\ C}{R_1\ V_{CC} - V_{BE}\ (R_1 + R_2)}$$

$V_{BE} \simeq 0.6V$

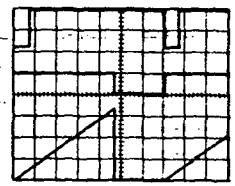


FIGURE 13. Linear Ramp

50% DUTY CYCLE OSCILLATOR

For a 50% duty cycle, the resistors R_A and R_B may be connected as in *Figure 14*. The time period for the output high is the same as previous, $t_1 = 0.693\ R_A\ C$. For the output low it is $t_2 =$

$$[(R_A\ R_B)/(R_A + R_B)]\ C \ln\left[\frac{R_B - 2R_A}{2R_B - R_A}\right]$$

Thus the frequency of oscillation is $f = \frac{1}{t_1 + t_2}$

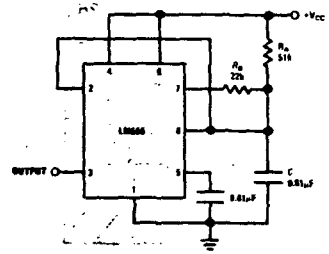


FIGURE 14. 50% Duty Cycle Oscillator

Note that this circuit will not oscillate if R_B is greater than 1/2 R_A because the junction of R_A and R_B cannot bring pin 2 down to 1/3 V_{CC} and trigger the lower comparator.

ADDITIONAL INFORMATION

Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is 0.1μF in parallel with 1μF electrolytic.

Lower comparator storage time can be as long as 10μs when pin 2 is driven fully to ground for triggering. This limits the monostable pulse width to 10μs minimum.

Delay time reset to output is 0.47μs typical. Minimum reset pulse width must be 0.3μs, typical.

Pin 7 current switches within 30 ns of the output (pin 3) voltage.

National Semiconductor

LM556/LM556C Dual Timer

General Description

The LM556 Dual timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 200 mA.

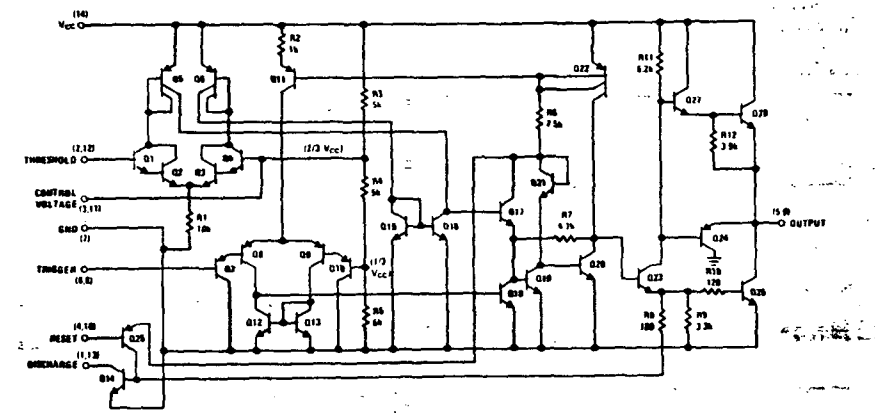
Features

- Direct replacement for SE556/NE556
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Replaces two 555 timers
- Adjustable duty cycle
- Output can source or sink 200 mA
- Output and supply TTL compatible
- Temperature stability better than 0.005% per °C
- Normally on and normally off output

Applications

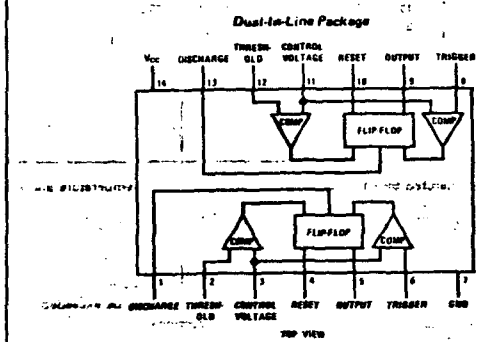
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Linear ramp generator

Schematic Diagram



Connection Diagram

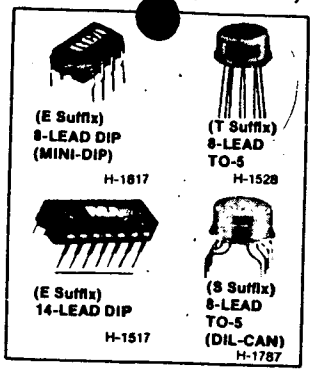
Dual-In-Line Package



Order Number LM556CN
See NS Package N14A

Order Number LM556J or LM556CJ
See NS Package J14A

CA741, CA747, CA748, CA1158, CA1558 Types



Operational Amplifiers

High-Gain Single and Dual Operational Amplifiers
For Military, Industrial and Commerical Applications

Features:

- *Input bias current (all types): 500 nA max.*
- *Input offset current (all types): 200 nA max.*

Applications:

- *Comparator*
- *DC amplifier*
- *Integrator or differentiator*
- *Multivibrator*
- *Narrow-band or band-pass filter*
- *Summing amplifier*

The RCA-CA1458, CA1558 (dual types); CA741C, CA741 (single-types); CA747C, CA747 (dual types); and CA748C, CA748 (single types) are general-purpose, high-gain operational amplifiers for use in military, industrial, and commercial applications.

These monolithic silicon integrated-circuit devices provide output short-circuit protection and latch-free operation. These types also feature wide common-mode and differential-mode signal ranges and have low-offset voltage nulling capability when used with an appropriately valued potentiometer. A 5-megohm potentiometer is used for offset nulling types CA748C, CA748 (See Fig. 10); a 10-kilohm potentiometer is used for offset nulling types CA741C, CA741, CA747CE, CA747E (See Fig. 9); and types CA1458, CA1558, CA747CT, have no specific terminals for offset nulling. Each type consists of a differential-input amplifier that effectively drives a gain and level-shifting stage having a complementary emitter-follower output.

This operational amplifier line also offers the circuit designer the option of operation with internal or external phase compensation.

Types CA748C and CA748, which are externally phase compensated (terminals 1 and 8) permit a choice of operation for improved bandwidth and slew-rate capabilities. Unity gain with external phase compensation can be obtained with a single 30-pF capacitor. All the other types are internally phase-compensated.

RCA's manufacturing process make it possible to produce IC operational amplifiers with low-burst ("popcorn") noise characteristics. Type CA6741, a low-noise version of the CA741, gives limit specifications for burst noise in the data bulletin, File No. 530. Contact your RCA Sales Representative for information pertinent to other operational amplifier types that meet low-burst noise specifications.

RCA Type No.	No. of Ampl.	Phase Comp.	Offset Voltage Null	Min. A_{OL}	Max. V_{IO} (mV)	Operating-Temperature Range (°C)
CA1458	dual	int.	no	20k	6	0 to +70▲
CA1558	dual	int.	no	50k	5	−55 to +125
CA741C	single	int.	yes	20k	6	0 to +70▲
CA741	single	int.	yes	50k	5	−55 to +125
CA747C	dual	int.	yes*	20k	6	0 to +70▲
CA747	dual	int.	yes*	50k	5	−55 to +125
CA748C	single	ext.	yes	20k	6	0 to +70▲
CA748	single	ext.	yes	50k	5	−55 to +125

*In the 14-lead dual-in-line plastic package only.

▲All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.

CA741, CA747, CA748, CA1458, CA1558 Types

ORDERING INFORMATION

When ordering any of these types, it is important that the appropriate suffix letter for the package required be affixed to the type number. For example: If a CA1458 in a straight-lead TO-5 style package is desired, order CA1458T.

TYPE NO.	PACKAGE TYPE AND SUFFIX LETTER							FIG. NO.
	TO-5 STYLE			PLASTIC		CHIP	BEAM-LEAD	
	8L	10L	DIL-CAN	8L	14L			
CA1458	T		S	E		H		1d, 1h
CA1558	T		S	E				1d, 1h
CA741C	T		S	E		H		1a, 1e
CA741	T		S	E			L	1a, 1e
CA747C		T			E	H		1b, 1f
CA747		T			E			1b, 1f
CA748C	T		S	E		H		1c, 1g
CA748	T		S	E				1c, 1g

MAXIMUM RATINGS, *Absolute-Maximum Values at T_A = 25°C:*

DC Supply Voltage (between V^+ and V^- terminals):
- CA741C, CA747C▲, CA748C, CA1458▲ . . . 36 V
- CA741, CA747▲, CA748, CA1558▲ . . . 44 V

Differential Input Voltage . . . ±30 V
DC Input Voltage* . . . ±15 V
Output Short-Circuit Duration . . . Indefinite
Device Dissipation:
- Up to 70°C (CA741C, CA748C) . . . 500 mW
- Up to 75°C (CA741, CA748) . . . 500 mW
- Up to 30°C (CA747) . . . 800 mW
- Up to 25°C (CA747C) . . . 800 mW
- Up to 30°C (CA1558) . . . 680 mW
- Up to 25°C (CA1458) . . . 680 mW

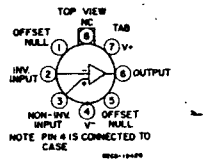
For Temperatures Indicated Above . . . Derate linearly 6.67 mW/°C
Voltage between Offset Null and V^- (CA741C, CA741, CA747CE) . . . ±0.5 V
Ambient Temperature Range:
- Operating — CA741, CA747E, CA748, CA1558 . . . −55 to +125 °C
- CA741C, CA747C, CA748C, CA1458 . . . 0 to +70 °C†
- Storage . . . −65 to +150 °C

Lead Temperature (During Soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 seconds max. . . . 265 °C

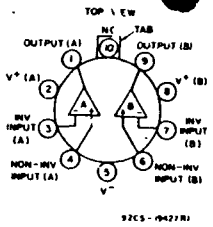
* If Supply Voltage is less than ± 15 volts, the Absolute Maximum Input Voltage is equal to the Supply Voltage.

▲ Voltage values apply for each of the dual operational amplifiers.

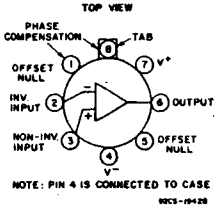
† All types in any package style can be operated over the temperature range of −55 to +125°C, although the published limits for certain electrical specifications apply only over the temperature range of 0 to +70°C.



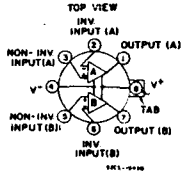
1a.—CA741CS, CA741CT, CA741S, & CA741T with internal phase compensation.



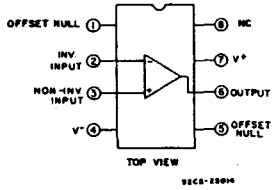
1b.—CA747CT and CA747T with internal phase compensation.



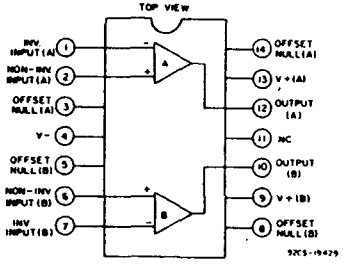
1c.—CA748CS, CA748CT, CA748S, and CA748T with external phase compensation.



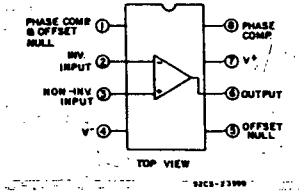
1d.—CA1458S, CA1458T, CA1558S, and CA1558T and internal phase compensation.



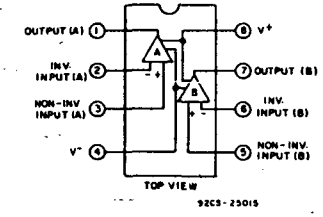
1e.—CA741C and CA741E with internal phase compensation.



1f.—CA747CE and CA747E with internal phase compensation.



1g.—CA748CE and CA748E with external phase compensation.



1h.—CA1458E and CA1558E with internal phase compensation.

Fig. 1 — Functional diagrams.

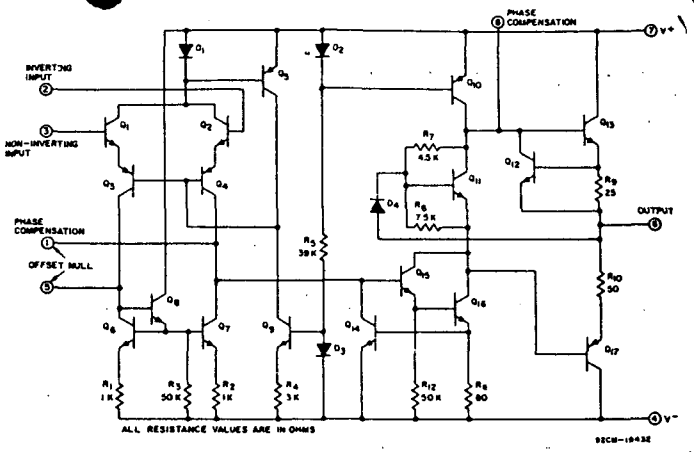


Fig. 2—Schematic diagram of operational amplifier with external phase compensation for CA748C and CA748.

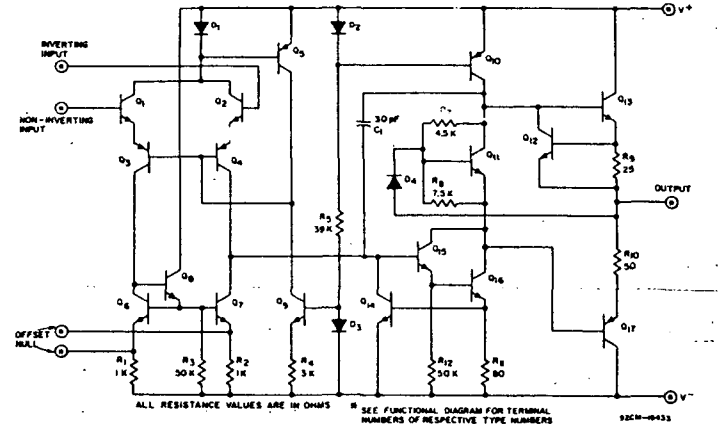


Fig. 3—Schematic diagram of operational amplifiers with internal phase compensation for CA741C, CA741, and for each amplifier of the CA747C, CA747, CA1458, and CA1558.

ELECTRICAL CHARACTERISTICS
Typical Values Intended Only for Design Guidance

CHARACTERISTIC	TEST CONDITIONS $V\pm = \pm 15$ V	TYP. VALUES ALL TYPES	UNITS
Input Capacitance, C_I		1.4	pF
Offset Voltage Adjustment Range		±15	mV
Output Resistance, R_O		75	Ω
Output Short-Circuit Current		25	mA
Transient Response: Rise Time, t_r	Unity gain, V_I = 20 mV, R_L = 2 kΩ, $C_L \leq$ 100 pF	0.3	μs
Transient Response: Overshoot		5	%
Slew Rate, SR: Closed-loop	$R_L \geq$ 2 kΩ	0.5	V/μs
Slew Rate, SR: Open-loop▲		40	V/μs

▲ Open-loop slew rate applies only for types CA748C and CA748.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V; Ambient Temperature, T_A	LIMITS CA741C, CA747C*, CA748C, CA1458* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S \leq$ 10 kΩ, 25 °C	–	2	6	mV
	$R_S \leq$ 10 kΩ, 0 to 70 °C	–	–	7.5	mV
Input Offset Current, I_{IO}	25 °C	–	20	200	nA
	0 to 70 °C	–	–	300	nA
Input Bias Current, I_{IB}	25 °C	–	80	500	nA
	0 to 70 °C	–	–	800	nA
Input Resistance, R_I		0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V_O = ±10 V, 25 °C	20,000	200,000	–	
	$R_L \geq$ 2 kΩ, V_O = ±10 V, 0 to 70 °C	15,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}	25 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ, 25 °C	70	90	–	dB
Supply-Voltage Rejection Ratio, PSRR	$R_S \leq$ 10 kΩ, 25 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq$ 10 kΩ, 25 °C	±12	±14	–	V
	$R_L \geq$ 2 kΩ, 25 °C	±10	±13	–	V
	$R_L \geq$ 2 kΩ, 0 to 70 °C	±10	±13	–	V
Supply Current, $I^{\pm}$	25 °C	–	1.7	2.8	mA
Device Dissipation, P_D	25 °C	–	50	85	mW

* Values apply for each section of the dual amplifiers.

ELECTRICAL CHARACTERISTICS
For Equipment Design

CHARACTERISTIC	TEST CONDITIONS Supply Voltage, V^+ = 15 V, V^- = −15 V; Ambient Temperature, T_A	LIMITS CA741, CA747*, CA748, CA1558* Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S \leq$ 10 kΩ, 25 °C	–	1	5	mV
	$R_S \leq$ 10 kΩ, −55 to +125 °C	–	1	6	mV
Input Offset Current, I_{IO}	25 °C	–	20	200	nA
	−55 °C	–	85	500	nA
	+125 °C	–	7	200	nA
Input Bias Current, I_{IB}	25 °C	–	80	500	nA
	−55 °C	–	300	1500	nA
	+125 °C	–	30	500	nA
Input Resistance, R_I		0.3	2	–	MΩ
Open-Loop Differential Voltage Gain, A_{OL}	$R_L \geq$ 2 kΩ, V_O = ±10 V, 25 °C	50,000	200,000	–	
	$R_L \geq$ 2 kΩ, V_O = ±10 V, −55 to +125 °C	25,000	–	–	
Common-Mode Input Voltage Range, V_{ICR}	−55 to +125 °C	±12	±13	–	V
Common-Mode Rejection Ratio, CMRR	$R_S \leq$ 10 kΩ, −55 to +125 °C	70	90	–	dB
Supply Voltage Rejection Ratio, PSRR	$R_S \leq$ 10 kΩ, −55 to +125 °C	–	30	150	μV/V
Output Voltage Swing, V_{OPP}	$R_L \geq$ 10 kΩ, −55 to +125 °C	±12	±14	–	V
	$R_L \geq$ 2 kΩ, −55 to +125 °C	±10	±13	–	V
Supply Current, $I^{\pm}$	25 °C	–	1.7	2.8	mA
	−55 °C	–	2	3.3	mA
	+125 °C	–	1.5	2.5	mA
Device Dissipation, P_D	25 °C	–	50	85	mW
	−55 °C	–	60	100	mW
	+125 °C	–	45	75	mW

* Values apply for each section of the dual amplifiers.

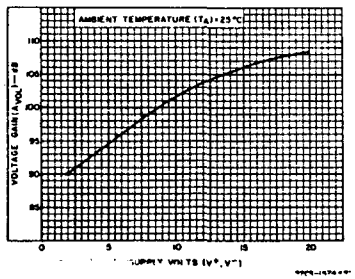


Fig. 4—Open-loop voltage gain vs. supply voltage for all types except CA748 and CA748C.

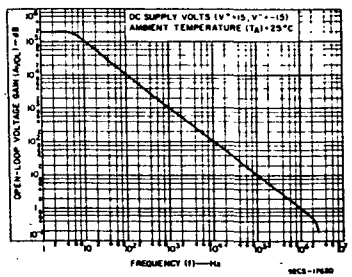


Fig. 5—Open-loop voltage gain vs. frequency for all types except CA748 and CA748C.

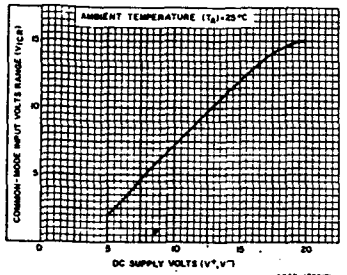


Fig.6—Common-mode input voltage range vs. supply voltage for all types.

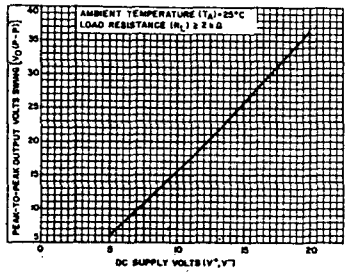


Fig.7—Peak-to-peak output voltage vs. supply voltage for all types except CA748 and CA748C.

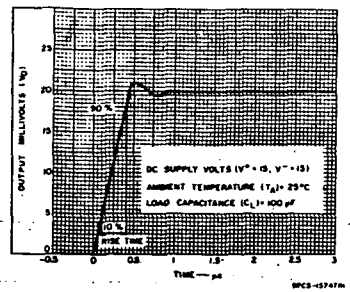


Fig.8—Output voltage vs. transient response time for CA741C and CA741.

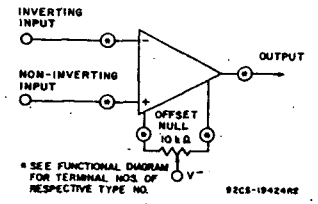


Fig.9—Voltage offset null circuit for CA741C, CA741, CA747CE, and CA747E.

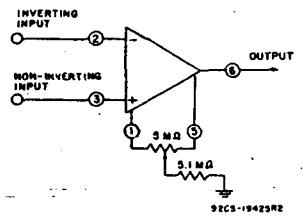


Fig.10—Voltage offset null circuit for CA748C and CA748.

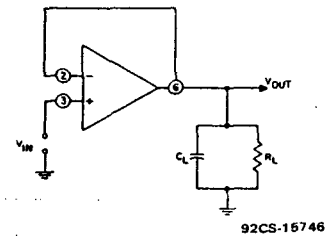
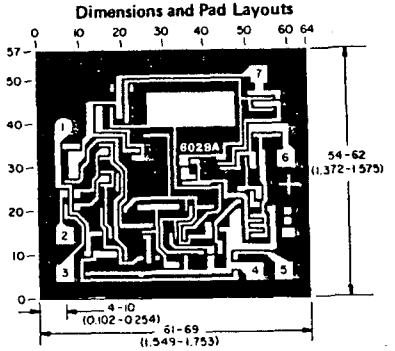


Fig.11—Transient response test circuit for all types.

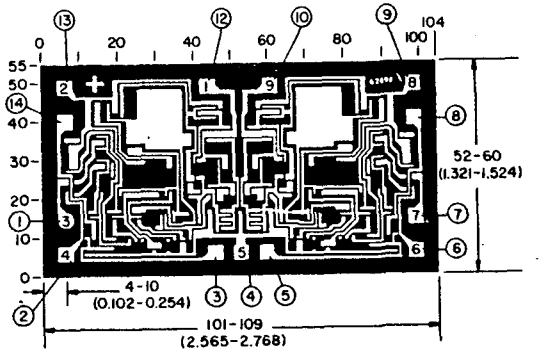
CHIP PHOTOS

Dimensions and Pad Layouts

CA741CH

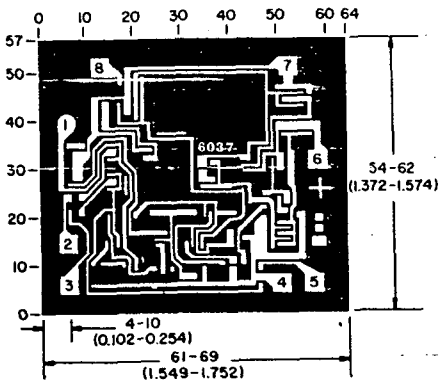


CA747CH

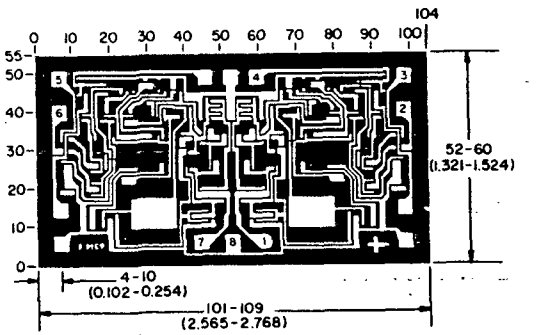


NOTE: NOS. IN PADS ARE FOR 10-LEAD TO-5
NOS. OUTSIDE OF CHIP ARE FOR 14-LEAD DIP

92CM-33260

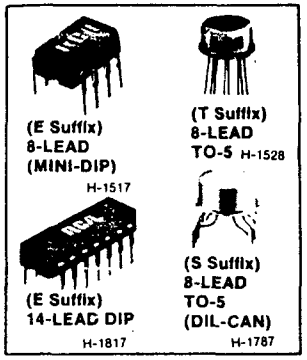


CA748CH



CA1458H

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).



BiMOS Operational Amplifiers

With MOS/FET Input, Composite Bipolar/MOS Output

Single Amplifier: CA080, CA081
Dual Amplifier: CA082, CA083
Quad Amplifier: CA084

Features:

- *Very low input bias and offset currents*
- *Input impedance typically 1.5 x 10^{12} Ω*
- *Low input offset voltage*
- *Wide common-mode input voltage range*
- *Low power consumption*
- *Fast slew rate*
- *Unity-gain bandwidth = 5 MHz (typ.)*
- *Wide output voltage swing*
- *Low distortion*
- *Continuous short circuit protection*
- *Direct replacement for industry type TL080 series in most applications*

The RCA-CA080, CA081, CA082, CA083, and CA084 BiMOS operational amplifiers combine the advantages of MOS and bipolar transistors on the same monolithic chip. The gate-protected MOS/FET (PMOS) input transistors provide high input impedance and a wide common-mode input voltage range. The bipolar and MOS output transistors allow a wide output voltage swing and provide a high output current capability.

Applications:

- *Inverters*
- *High-Q notch filters*
- *IC preamplifiers*
- *Unity Gain Absolute Value Amplifiers*
- *Sample and hold amplifiers*
- *Active filters*

The CA080 is externally phase-compensated, and the CA081, CA082, CA083, and CA084 are internally phase-compensated. All types except the CA082 have provisions for external offset nulling.

The CA080, CA081, CA082, CA083, and CA084 are available in chip form (H Suffix).

Package Selection Chart

Type No.	Package Type & Suffix			
	8L TO-5	DIL-CAN	Mini-DIP	14L DIP
CA080	T	S	E	
CA080A	T	S	E	
CA080B			E	
CA080C	T	S		
CA081	T	S	E	
CA081A	T	S	E	
CA081B			E	
CA081C	T	S		
CA082	T	S	E	
CA082A	T	S	E	
CA082B			E	
CA082C	T	S		
CA083				E
CA083A				E
CA083B				E
CA084				E
CA084A				E
CA084B				E

Operating Temperature Ranges:

-55 to +125°C	0 to +70°C
CA080T, CA080S	CA080CT, CA080CS
CA080AT, CA080AS	CA080BE
CA081T, CA081S	CA081CT, CA081CS
CA081AT, CA081AS	CA081BE
CA082T, CA082S	CA082CT, CA082CS
CA082AT, CA082AS	CA082BE
	CA083BE, CA083AE
	CA083BE
	CA084, CA084AE
	CA084BE

CA080, CA081, CA082, CA083, CA084 Series

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY VOLTAGE V± ..... ±18 V
DIFFERENTIAL INPUT VOLTAGE ..... ±18 V
INPUT VOLTAGE RANGE ..... ± 15 V
INPUT CURRENT ..... 1 mA
OUTPUT SHORT-CIRCUIT DURATION ..... UNLIMITED*
POWER DISSIPATION, PD:
At TA = 25°C:
E Suffix ..... 625 mW
T Suffix ..... 680 mW
Derating Factors:
Mini-DIP ..... Derate linearly at 6.67 mW/°C above 56°C
14-Lead DIP ..... Derate linearly at 6.67 mW/°C above 56°C
TO-5 ..... Derate linearly at 6.67 mW/°C above 56°C
AMBIENT TEMPERATURE RANGE:
CT, CS, E, Suffixes ..... 0 to +70°C
T, S, Suffixes ..... -55 to +125°C
STORAGE TEMPERATURE RANGE, ALL TYPES ..... -65 to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 (1.59 ± 0.79 mm) from case for 10 seconds max. ..... +265°C

* The output may be shorted to ground or either supply if the maximum temperature and dissipation ratings are observed.

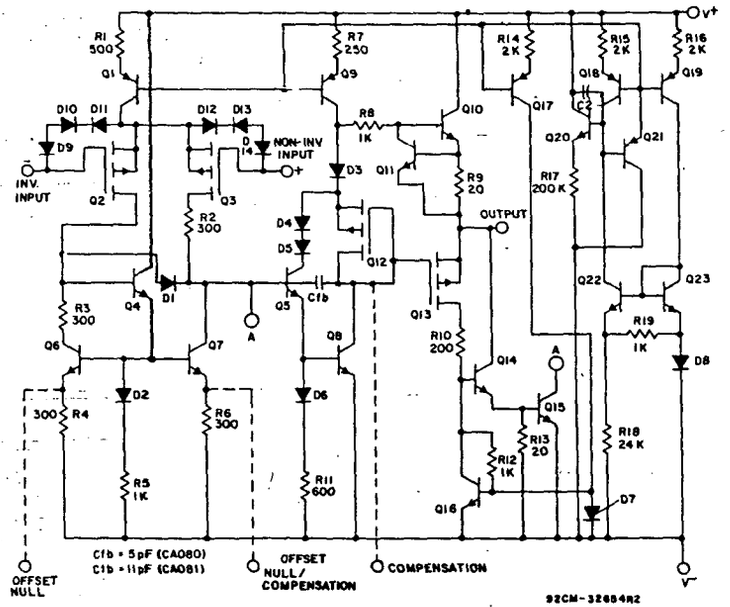
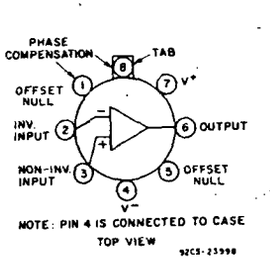


Fig. 1 - Schematic diagram of the CA080, CA081, CA082, CA083, and CA084.

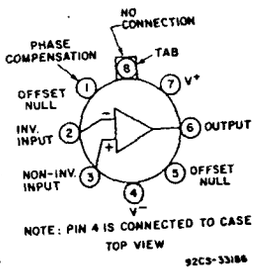
CA080, CA081, CA082, CA083, CA084 Series

Texas Instruments-to-RCA Package Suffix Cross Reference Chart

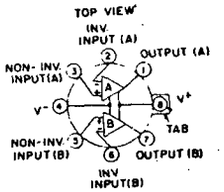
Texas Instruments Suffix	Texas Instruments Description	RCA Suffix	RCA Description
ACJG	Ceramic DIL	AS	DILCAN TO-5
ACL	TO-5	AT	TO-5
ACN	Plastic DIL	AE	Plastic DIL
ACP	Plastic DIL	AE	Plastic DIL
CJG	Ceramic DIL	CS	DILCAN TO-5
CL	TO-5	CT	TO-5
CN	Plastic DIL	E	Plastic DIL
CP	Plastic DIL	E	Plastic DIL
IJG	Ceramic DIL	S	DILCAN TO-5
IL	TO-5	T	TO-5
IP	Plastic DIL	E	DILCAN TO-5
MJG	Ceramic DIL	S	DILCAN TO-5
ML	TO-5	T	TO-5
AML	TO-5	AT	TO-5
BCP	Plastic DIL	BE	Plastic DIL



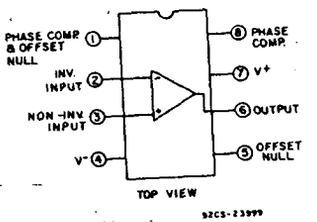
CA080
T, S Suffixes



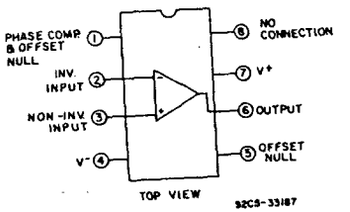
CA081
T, S Suffixes



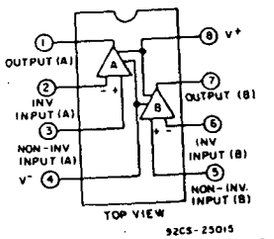
CA082
T, S Suffixes



CA080
E Suffix



CA081
E Suffix



CA082
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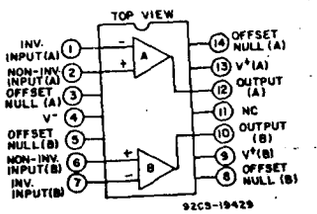

CA083
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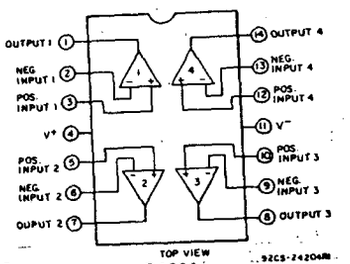


CA084
E Suffix

Fig. 2 - Terminal assignments.

TYPICAL OPERATING CHARACTERISTICS at $V\pm = 15\ V, T_A = 25°C$

CHARACTERISTIC	TEST CONDITIONS	VALUE	UNITS
Slew Rate at Unity Gain, SR	$V_I = 10\ V, R_L = 2\ k\Omega, C_L = 100\ pF, A_{VD} = 1$	13	V/μs
Rise Time, t_r	$V_I = 10\ V, R_L = 2\ k\Omega, C_L = 100\ pF, A_{VD} = 1$	0.1	μs
Overshoot Factor		10	%
Equivalent Input Noise Voltage, e_n	$R_S = 100\ \Omega, f = 1\ kHz$	40	nV/√Hz

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$ and $T_A = -55$ to $+125°C$ for types supplied in TO-5 style packages (T, S Suffixes). $V^+ = \pm 15\ V$

This does not include CA080C, CA081C, or CA082C. These types are supplied in TO-5 packages, but they are specified over the range of 0 to 70°C, and their limits are the same as those for the CA080, CA081, CA082, and CA083 in plastic packages over the range 0 to 70°C.

CHARACTERISTIC	TEST CONDITIONS	−55 to +125°C	+25°C	LIMITS: CA080T, S CA081T, S CA082T, S Min.	Typ.	Max.	LIMITS: CA080AT, S CA081AT, S CA082AT, S Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S = 50\Omega$	X		—	3	6	—	2	3	mV
			X	—	—	9	—	—	5	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	$R_S = 50\ \Omega$		X	—	10	—	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	20	—	5	20	pA
			X	—	—	4	—	—	2	nA
Input Current		X		—	15	40	—	15	40	pA
			X	—	—	10	—	—	5	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±12	—	—	±12	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	$R_L = 10\ k\Omega$	X		24	27	—	24	27	—	V
	$R_L > 10\ k\Omega$		X	24	—	—	24	—	—	
	$R_L \geq 2\ k\Omega$		X	20	24	—	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	$R_L \geq 2\ k\Omega$, $V_O = \pm 10V$	X		50	200	—	50	200	—	V/mV
			X	25	—	—	25	—	—	
Unity-Gain Bandwidth		X		—	5	—	—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\ k\Omega$	X		80	86	—	80	86	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+ / \pm \Delta V_{IO}$)	$R_S \leq 10\ k\Omega$	X		80	86	—	80	86	—	dB
Supply Current, I^+ (per amp., CA082, CA083)	No load, No Signal	X		—	1.4	2.8	—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps., CA082, CA083)	$A_{VD} = 100$	X		—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS at $T_A = 25°C$, $T_A = 0$ to $+70°C$ for types supplied in plastic dual-in-line packages (E Suffix). $V^+ = \pm 15\ V$

CHARACTERISTIC	TEST CONDITIONS	0 to 70°C	+25°C	LIMITS: CA080BE CA081BE CA082BE CA083BE CA084BE Min.	Typ.	Max.	LIMITS: CA080AE CA081AE CA082AE CA083AE CA084AE Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	$R_S = 50\Omega$	X		—	2	3	—	3	6	mV
			X	—	—	5	—	—	7.5	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	$R_S = 50\ \Omega$		X	—	10	—	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	10	—	5	20	pA
			X	—	—	0.4	—	—	0.6	nA
Input Current		X		—	15	30	—	15	40	pA
			X	—	—	0.7	—	—	1	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±12	—	—	±12	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	$R_L = 10\ k\Omega$	X		24	27	—	24	27	—	V
	$R_L > 10\ k\Omega$		X	24	—	—	24	—	—	
	$R_L \geq 2\ k\Omega$		X	20	24	—	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	$R_L \geq 2\ k\Omega$, $V_O = \pm 10V$	X		50	200	—	50	200	—	V/mV
			X	—	—	—	—	—	—	
Unity-Gain Bandwidth		X		—	5	—	—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	$R_S \leq 10\ k\Omega$	X		80	86	—	80	86	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+ / \pm \Delta V_{IO}$)	$R_S \leq 10\ k\Omega$	X		80	86	—	80	86	—	dB
Supply Current, I^+ (per amp., CA082, CA083, CA084)	No load, No Signal	X		—	1.4	2.8	—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps., CA082, CA083)	$A_{VD} = 100$	X		—	120	—	—	120	—	dB

ELECTRICAL CHARACTERISTICS at T_A = 25°C, T_A = 0 to 70°C for types supplied in plastic dual-in-line packages (E Suffix). V^+ = ±15 V

The limits for the CA080C, CA081C, and CA082C in TO-5 packages are the same as those for the types in this chart.

CHARACTERISTIC	TEST CONDITIONS	0 to 70°C	+25°C	LIMITS CA080E, T CA081E, T CA082E, T CA083E CA084E Min.	Typ.	Max.	UNITS
Input Offset Voltage, V_{IO}	R_S = 50Ω	X		—	5	15	mV
			X	—	—	20	
Temperature Coefficient of Input Offset Voltage, αV_{IO}	R_S = 50 Ω		X	—	10	—	μV/°C
Input Offset Current, I_{IO}		X		—	5	30	pA
			X	—	—	1	nA
Input Current		X		—	15	50	pA
			X	—	—	2	nA
Common-Mode Input Voltage Range, V_{ICR}		X		±10	—	—	V
Maximum Output Voltage Swing, V_{OP-P}	R_L = 10 kΩ	X		24	27	—	V
	R_L ≥ 10 kΩ		X	24	—	—	
	R_L ≥ 2 kΩ		X	20	24	—	
Large-Signal Differential Voltage Gain, A_{VD}	R_L ≥ 2 kΩ, V_O = ±10V	X		25	200	—	V/mV
			X	—	—	—	
Unity-Gain Bandwidth		X		—	5	—	MHz
Input Resistance, R_I		X		—	1.5	—	TΩ
Common-Mode Rejection Ratio, CMRR	R_S ≤ 10 kΩ	X		70	76	—	dB
Power Supply Rejection Ratio, PSRR ($\Delta V^+ / \pm \Delta V_{IO}$)	R_S ≤ 10 kΩ	X		70	76	—	dB
Supply Current, I^+ (per amp., CA082, CA083)	No load, No Signal	X		—	1.4	2.8	mA
Channel Separation, V_{O1}/V_{O2} (between amps., CA082, CA083)	A_{VD} = 100	X		—	120	—	dB

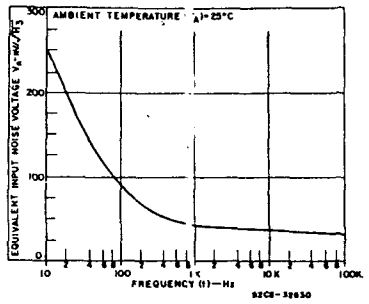


Fig. 3 – Noise voltage as a function of frequency.

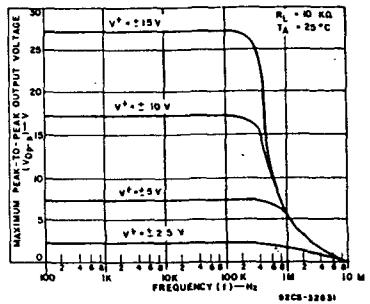


Fig. 4 – Output voltage as a function of frequency.

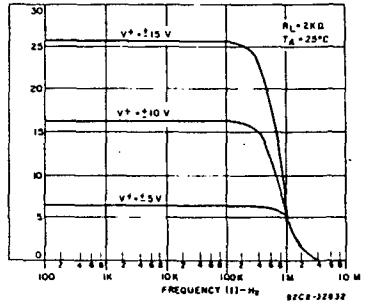


Fig. 5 – Output voltage as a function of frequency.

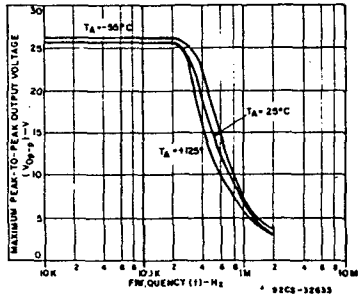


Fig. 6 – Output voltage as a function of frequency.

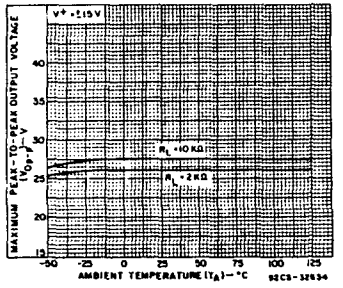


Fig. 7 – Output voltage as a function of ambient temperature.

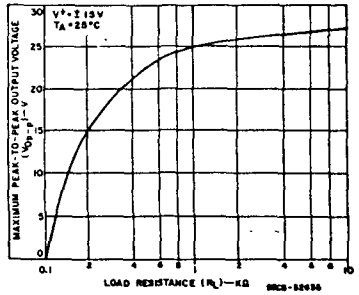


Fig. 8 – Output voltage as a function of load resistance.

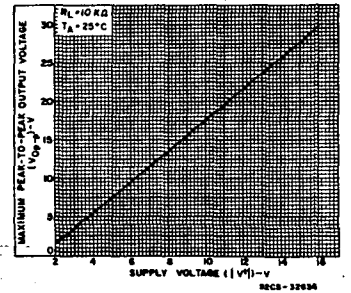


Fig. 9 – Output voltage as a function of supply voltage.

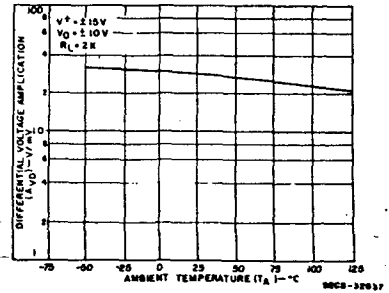


Fig. 10 – Differential voltage amplification as a function of ambient temperature.

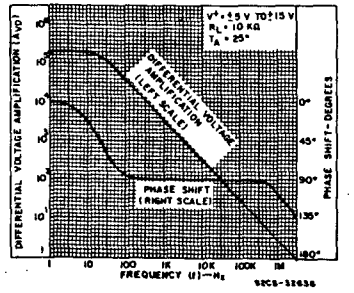


Fig. 11 - Differential voltage amplification as a function of frequency.

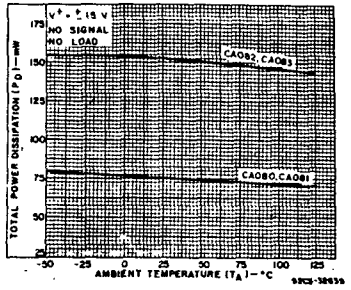


Fig. 12 - Total power dissipation as a function of ambient temperature.

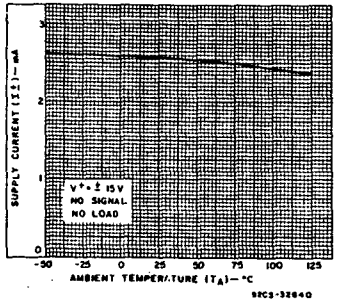


Fig. 13 - Supply current as a function of ambient temperature.

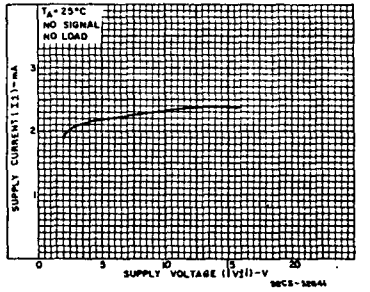


Fig. 14 - Supply current as a function of supply voltage.

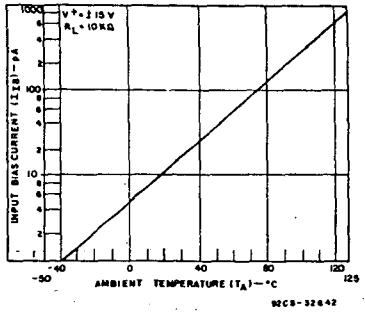


Fig. 15 - Input bias current as a function of ambient temperature.

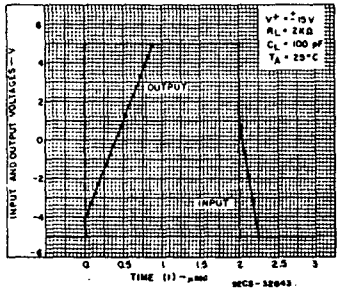


Fig. 16 - Voltage follower large-signal pulse response.

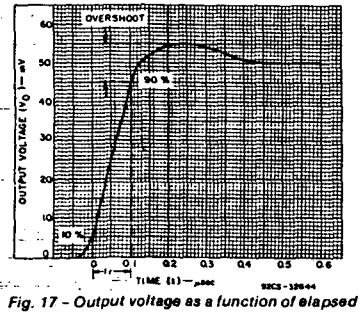


Fig. 17 - Output voltage as a function of elapsed time.

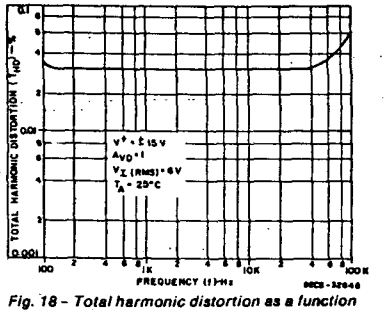


Fig. 18 - Total harmonic distortion as a function of frequency.

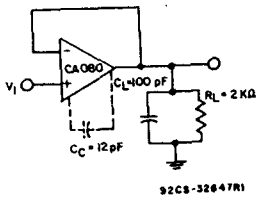


Fig. 19 - Unity-gain amplifier.

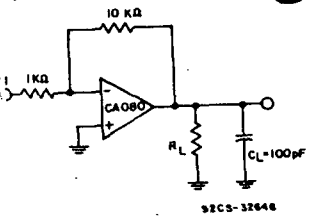


Fig. 20 - 10X inverting amplifier.

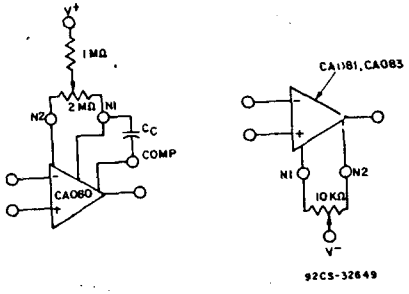


Fig. 21 - Input-offset voltage null circuits.

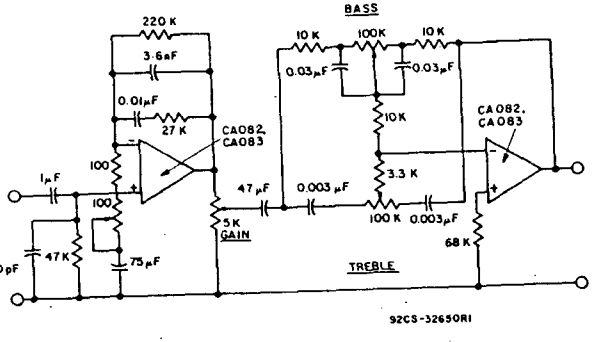


Fig. 22 - IC preamplifier.

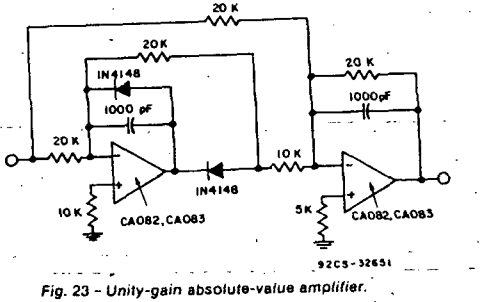


Fig. 23 - Unity-gain absolute-value amplifier.

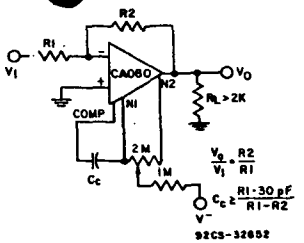


Fig. 24 - Inverting amplifier with single-pole compensation and offset adjustment.

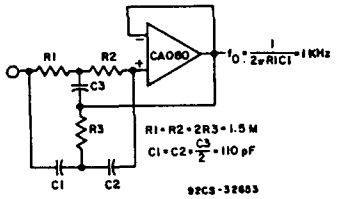


Fig. 25 - High Q notch filter.

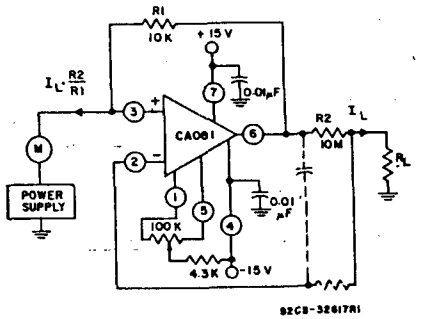


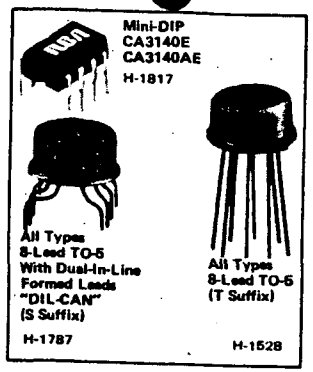
Fig. 26 - Basic current amplifier for low-current measurement systems.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA081 makes it ideal for use in current-amplifier applications such as the one shown in Fig.26. In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.



BiMOS Operational Amplifiers

With MOSFET Input/Bipolar Output

FEATURES:

- *MOS/FET input Stage*
  - *(a) Very high input impedance (Z_{IN}) — 1.5 TΩ typ.*
  - *(b) Very low input current (I_I) — 10 pA typ. at ± 15 V*
  - *(c) Low input-offset voltage (V_{IO}) — to 2 mV max.*
  - *(d) Wide common-mode input-voltage range (V_{ICR})— can be swung 0.5 volt below negative supply-voltage rail*
  - *(e) Output swing complements input common-mode range*
  - *(f) Rugged input stage — bipolar diode protected*
- *Directly replaces industry type 741 in most applications*
- *Includes numerous industry operational amplifier categories such as general-purpose, FET input, wideband (high slew rate)*
- *Operation from 4-to-44 volts Single or Dual supplies*
- *Internally compensated*
- *Characterized for ± 15-volt operation and for TTL supply systems with operation down to 4 volts*
- *Wide bandwidth — 4.5 MHz unity gain at ± 15 V or 30 V; 3.7 MHz at 5 V*
- *High voltage-follower slew rate — 9 V/μs*
- *Fast setting time — 1.4 μs typ. to 10 mV with a 10-V_{p-p} signal*
- *Output swings to within 0.2 volt of negative supply*
- *Strobable output stage*

APPLICATIONS:

- *Ground-referenced single-supply amplifiers in automobile and portable instrumentation*
- *Sample and hold amplifiers*
- *Long-duration timers/multivibrators (microseconds—minutes—hours)*
- *Photocurrent instrumentation*
- *Peak detectors* ■ *Active filters*
- *Comparators*
- *Interface in 5 V TTL systems & other low-supply voltage systems*
- *All standard operational amplifier applications*
- *Function generators* ■ *Tone controls*
- *Power supplies* ■ *Portable instruments*
- *Intrusion alarm systems*

The CA3140B, CA3140A, and CA3140 are integrated-circuit operational amplifiers that combine the advantages of high-voltage PMOS transistors with high-voltage bipolar transistors on a single monolithic chip. Because of this unique combination of technologies, this device can now provide designers, for the first time, with the special performance features of the CA3130 COS/MOS operational amplifiers and the versatility of the 741 series of industry-standard operational amplifiers.

The CA3140, CA3140A, and CA3140 BiMOS operational amplifiers feature gate-protected MOS/FET (PMOS) transistors in the input circuit to provide very-high-input impedance, very-low-input current, and high-speed performance. The CA3140B operates at supply voltages from 4 to 44 volts; the CA3140A and CA3140 from 4 to 36 volts (either single or dual supply). These operational amplifiers are internally phase-compensated to achieve stable operation in unity-gain follower operation, and, additionally, have access terminals for a supplementary external capacitor if additional frequency roll-off is desired. Terminals are also provided for use in applications requiring input offset-voltage nulling. The use of PMOS field-effect transistors in the input stage results in common-mode input-voltage capability down to 0.5 volt below the negative-supply terminal, an important attribute for single-supply applications. The output stage uses bipolar transistors and includes built-in protection against damage from load-terminal short-circuiting to either supply-rail or to ground.

The CA3140 Series has the same 8-lead terminal pin-out used for the "741" and other industry-standard operational amplifiers. They are supplied in either the standard 8-lead TO-5 style package (T suffix), or in the 8-lead dual-in-line formed-lead TO-5 style package "DIL-CAN" (S suffix). The CA3140 is available in chip form (H suffix). The CA3140A and CA3140 are also available in an 8-lead dual-in-line plastic package (Mini-DIP-E suffix). The CA3140B is intended for operation at supply voltages ranging from 4 to 44 volts, for applications requiring premium-grade specifications. The CA3140A and CA3140 are for operation at supply voltages up to 36 volts (±18 volts). All types can be operated safely over the temperature range from -55°C to +125°C.

TYPICAL ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		TEST CONDITIONS V^+ = +15 V, V^- = −15 V, T_A = 25°C		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage Adjustment Resistor		Typ. Value of Resistor Between Term. 4 and 5 or 4 and 1 to Adjust Max. V_{IO}		43	18	4.7	kΩ
Input Resistance	R_I			1.5	1.5	1.5	TΩ
Input Capacitance	C_I			4	4	4	pF
Output Resistance	R_O			60	60	60	Ω
Equivalent Wideband Input Noise Voltage (See Fig. 39)	e_n	BW = 140 kHz, R_S = 1 MΩ		48	48	48	μV
Equivalent Input Noise Voltage (See Fig.10)	e_n	f = 1 kHz	R_S = 100 Ω	40	40	40	nV/√Hz
		f = 10 kHz		12	12	12	
Short-Circuit Current to Opposite Supply	Source I_{OM^+}			40	40	40	mA
	Sink I_{OM^-}			18	18	18	mA
Gain-Bandwidth Product, (See Figs. 5 &18)	f_T			4.5	4.5	4.5	MHz
Slew Rate, (See Fig.6)	SR			9	9	9	V/μs
Sink Current From Terminal 8 To Terminal 4 to Swing Output Low				220	220	220	μA
Transient Response: Rise Time	t_r	R_L = 2 kΩ, C_L = 100 pF		0.08	0.08	0.08	μs
Overshoot (See Fig. 37)				10	10	10	%
Settling Time at 10 V_{p-p}, (See Fig.17)	t_s 1 mV	R_L = 2 kΩ, C_L = 100 pF, Voltage Follower		4.5	4.5	4.5	μs
	t_s 10 mV			1.4	1.4	1.4	

ELECTRICAL CHARACTERISTICS FOR EQUIPMENT DESIGN

At $V^+ = 15$ V, $V^- = 15$ V, $T_A = 25^oC$ Unless Otherwise Specified

CHARACTERISTIC	LIMITS									UNITS
	CA3140B			CA3140A			CA3140			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Input Offset Voltage, $\|V_{IO}\|$	–	0.8	2	–	2	5	–		15	mV
Input Offset Current, $\|I_{IO}\|$	–	0.5	10	–	0.5	20	–	0.5	30	pA
Input Current, I_I	–	10	30	–	10	40	–	1.0	50	pA
Large-Signal Voltage Gain, A_{OL}● (See Figs. 4,18)	50 k	100 k	–	20 k	100 k	–	20 k	100 k	–	V/V
	94	100	–	86	100	–	86	100	–	dB
Common-Mode Rejection Ratio, CMRR (See Fig.9)	–	20	50	–	32	320	–	32	320	μV/V
	86	94	–	70	90	–	70	90	–	dB
Common-Mode Input-Voltage Range, V_{ICR} (See Fig.20)	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	12	−15	−15.5 to +12.5	11	V
Power-Supply Rejection Ratio, PSRR $\Delta V_{IO}/\Delta V$ (See Fig.11)	–	32	100	–	100	150	–	100	150	μV/V
	80	90	–	76	80	–	76	80	–	dB
Max. Output Voltage● V_{OM}^+ (See Figs.13,20) V_{OM}^-	+12	13	–	+12	13	–	+12	13	–	V
	−14	−14.4	–	−14	−14.4	–	−14	−14.4	–	
Supply Current, I^+ (See Fig.7)	–	4	6	–	4	6	–	4	6	mA
Device Dissipation, P_D	–	120	180	–	120	180	–	120	180	mW
Input Offset Voltage Temp. Drift, $\Delta V_{IO}/\Delta T$	–	5	–	–	6	–	–	8	–	μV/°C
Max. Output Voltage,★ V_{OM}^+	+19	+19.5	–	–	–	–	–	–	–	V
V_{OM}^-	−21	−21.4	–	–	–	–	–	–	–	
Large-Signal Voltage Gain, A_{OL}♦★	20 k	50 k	–	–	–	–	–	–	–	V/V
	86	94	–	–	–	–	–	–	–	dB

● At $V_O = 26V_{p-p}$, +12V, −14V and $R_L = 2\,k\Omega$.

■ At $R_L = 2\,k\Omega$.

♦ At $V_O = +19$ V, −21 V, and $R_L = 2\,k\Omega$.

★ At $V^+ = 22$ V, $V^- = 22$ V.

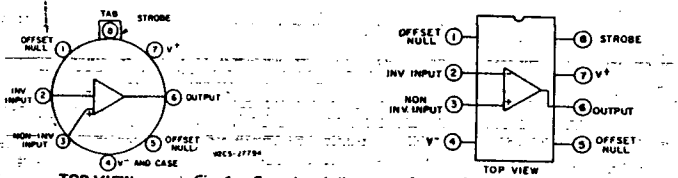


Fig. 1 – Functional diagrams of the CA3140 series.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

	CA3140, CA3140A	CA3140B
DC SUPPLY VOLTAGE (BETWEEN V^+ AND V^- TERMINALS)	36 V	44 V
DIFFERENTIAL-MODE INPUT VOLTAGE	±8 V	±8 V
COMMON-MODE DC INPUT VOLTAGE	(V^+ +8 V) to (V^- −0.5 V)	
INPUT-TERMINAL CURRENT	1 mA	
DEVICE DISSIPATION:		
WITHOUT HEAT SINK –		
UP TO 55°C	630 mW	
ABOVE 55°C	Derate linearly 6.67 mW/°C	
WITH HEAT SINK –		
Up to 55°C	1 W	
Above 55°C	Derate linearly 16.7 mW/°C	
TEMPERATURE RANGE:		
OPERATING (ALL TYPES)	−55 to + 125°C	
STORAGE (ALL TYPES)	−65 to +150°C	
OUTPUT SHORT-CIRCUIT DURATION*	INDEFINITE	
LEAD TEMPERATURE (DURING SOLDERING):		
AT DISTANCE 1/16 ± 1/32 INCH (1.59 ± 0.79 MM) FROM CASE FOR 10 SECONDS MAX.	+265°C	

* Short circuit may be applied to ground or to either supply.

TYPICAL ELECTRICAL CHARACTERISTICS FOR DESIGN GUIDANCE

At $V^+ = 5$ V, $V^- = 0$ V, $T_A = 25^oC$

CHARACTERISTIC		CA3140B (T,S)	CA3140A (T,S,E)	CA3140 (T,S,E)	UNITS
Input Offset Voltage	$\|V_{IO}\|$	0.8	2	5	mV
Input Offset Current	$\|I_{IO}\|$	0.1	0.1	0.1	pA
Input Current	I_I	2	2	2	pA
Input Resistance		1	1	1	TΩ
Large-Signal Voltage Gain	A_{OL}	100 k	100 k	100 k	V/V
(See Figs.4,18)		100	100	100	dB
Common-Mode Rejection Ratio,	CMRR	20	32	32	μV/V
		94	90	90	dB
Common-Mode Input-Voltage Range	V_{ICR}	−0.5	−0.5	−0.5	V
(See Fig.20)		2.6	2.6	2.6	
Power-Supply Rejection Ratio	$\Delta V_{IO}/\Delta V^+$	32	100	100	μV/V
		90	80	80	dB
Maximum Output Voltage	V_{OM}^+	3	3	3	V
(See Figs.13,20)	V_{OM}^-	0.13	0.13	0.13	
Maximum Output Current:					
Source	I_{OM}^+	10	10	10	mA
Sink	I_{OM}^-	1	1	1	
Slew Rate (See Fig.6)		7	7	7	V/μs
Gain-Bandwidth Product (See Fig.5)	f_T	3.7	3.7	3.7	MHz
Supply Current (See Fig.7)	I^+	1.6	1.6	1.6	mA
Device Dissipation	P_D	8	8	8	mW
Sink Current from Term. 8 to Term. 4 to Swing Output Low		200	200	200	μA

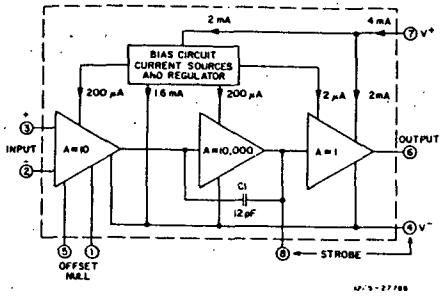


Fig.2 – Block diagram of CA3140 series.

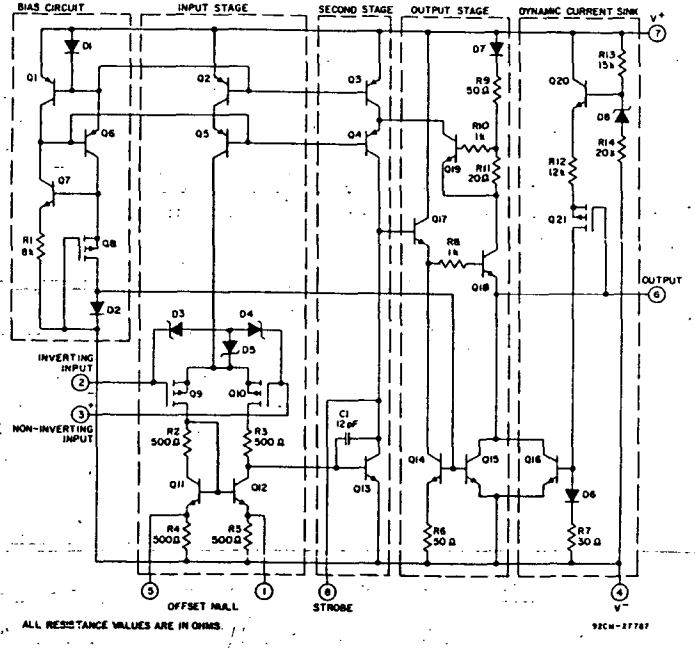


Fig.3 – Schematic diagram of CA3140 series.

CIRCUIT DESCRIPTION

Fig.2 is a block diagram of the CA3140 Series PMOS Operational Amplifiers. The input terminals may be operated down to 0.5 V below the negative supply rail. Two class A amplifier stages provide the voltage gain, and a unique class AB amplifier stage provides the current gain necessary to drive low-impedance loads.

A biasing circuit provides control of cascoded constant-current flow circuits in the first and second stages. The CA3140 includes an on-chip phase-compensating capacitor that is sufficient for the unity gain voltage-follower configuration.

Input Stages – The schematic circuit diagram of the CA3140 is shown in Fig.3. It consists of a differential-input stage using PMOS field-effect transistors (Q9, Q10) working into a mirror pair of bipolar transistors (Q11, Q12) functioning as load resistors together with resistors R2 through R5. The mirror-pair transistors also function as a differential-to-single-ended converter to provide base-current drive to the second-stage bipolar transistor (Q13). Offset nulling, when desired, can be effected with a 10-kΩ potentiometer connected across terminals 1 and 5 and with its slider arm connected to terminal 4. Cascode-connected bipolar transistors Q2, Q5 are the constant-current source for the input stage. The base-biasing circuit for the constant-current source is described subsequently. The small diodes D3, D4, D5 provide gate-oxide protection against high-voltage transients, e.g., static electricity.

Second Stage – Most of the voltage gain in the CA3140 is provided by the second amplifier stage, consisting of bipolar transistor Q13 and its cascode-connected load resistance provided by bipolar transistors Q3, Q4. On-chip phase compensation, sufficient for a majority of the applications is provided by C1. Additional Miller-Effect compensation (roll-off) can be accomplished, when desired, by simply connecting a small capacitor between terminals 1 and 8. Terminal 8 is also used to strobe the output stage into quiescence. When terminal 8 is tied to the negative supply rail (terminal 4) by mechanical or electrical means, the output terminal 6 swings low, i.e., approximately to terminal 4 potential.

Output Stage – The CA3140 Series circuits employ a broadband output stage that can sink loads to the negative supply to complement the capability of the PMOS input stage when operating near the negative rail. Quiescent current in the emitter-follower cascade circuit (Q17, Q18) is established by transistors (Q14, Q15) whose base-currents are "mirrored" to current flowing through diode D2 in the bias circuit section. When the CA3140 is operating such that output terminal 6 is sourcing current, transistor Q18 functions as an emitter-follower to source current from the V+ bus (terminal 7), via D7, R9, and R11. Under these conditions, the collector potential of Q13 is sufficiently high to permit the necessary flow of base current to emitter follower Q17 which, in turn, drives Q18.

When the CA3140 is operating such that output terminal 6 is sinking current to the V– bus, transistor Q16 is the current-sinking element. Transistor Q16 is mirror-connected to D6, R7, with current fed by way of Q21, R12, and Q20. Transistor Q20, in turn, is biased by current-flow through R13, zener D8, and R14. The dynamic current-sink is controlled by voltage-level sensing. For purposes of explanation, it is assumed that output terminal 6 is quiescently established at the potential mid-point between the V+ and V– supply rails. When output-current sinking-mode operation is required, the collector potential of transistor Q13 is driven below its quiescent level, thereby causing Q17, Q18 to decrease the output voltage at terminal 6. Thus, the gate terminal of PMOS transistor Q21 is displaced toward the V– bus, thereby reducing the channel resistance of Q21. As a consequence, there is an incremental increase in current flow through Q20, R12, Q21, D6; R7, and the base of Q16. As a result, Q16 sinks current from terminal 6 in direct response to the incremental change in output voltage caused by Q18. This sink current flows regardless of load; any excess current is internally supplied by the emitter-follower Q18. Short-circuit protection of the output circuit is provided by Q19, which is driven into conduction by the high voltage drop developed across R11 under output short-circuit conditions. Under these conditions, the collector of Q19 diverts current from Q4 so as to reduce the base-current drive from Q17, thereby limiting current flow in Q18 to the short-circuited load terminal.

Bias Circuit – Quiescent current in all stages (except the dynamic current sink) of the CA3140 is dependent upon bias current flow in R1. The function of the bias circuit is to establish and maintain constant-current flow through D1, Q6, Q8 and D2. D1 is a diode-connected transistor mirror-connected in parallel with the base-emitter junctions of Q1, Q2, and Q3. D1 may be considered as a current-sampling diode that senses the emitter current of Q6 and automatically adjusts the base current of Q6 (via Q1) to maintain a constant current through Q6, Q8, D2. The base-currents in Q2, Q3 are also determined by constant-current flow D1. Furthermore, current in diode-connected transistor D2 establishes the currents in transistors Q14 and Q15.

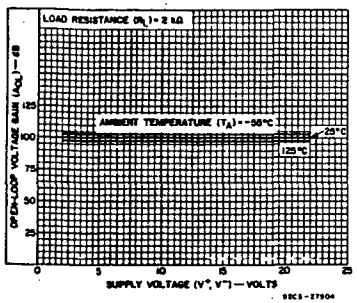


Fig.4 – Open-loop voltage gain vs supply voltage and temperature.

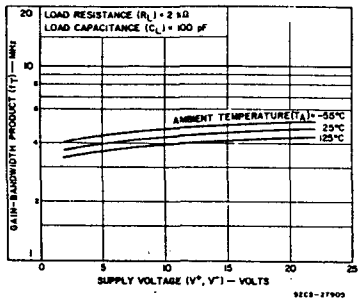


Fig.5 – Gain-bandwidth product vs supply voltage and temperature.

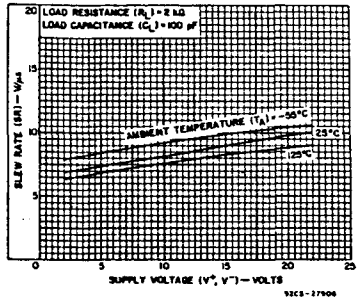


Fig.6 – Slew rate vs supply voltage and temperature.

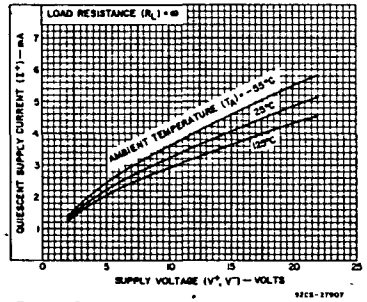


Fig.7 – Quiescent supply current vs supply voltage and temperature.

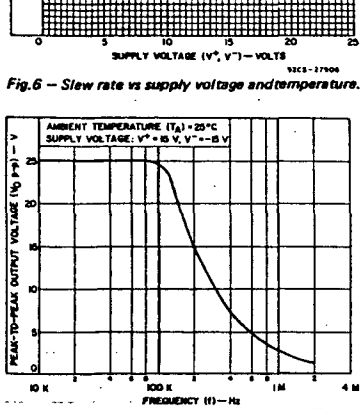


Fig.8 – Maximum output voltage swing vs frequency.

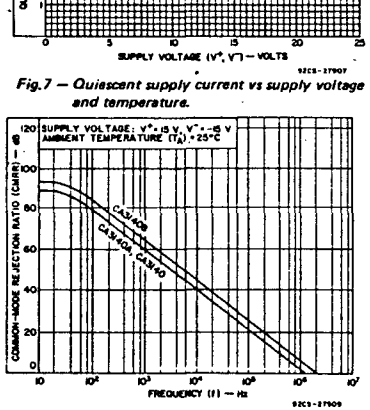


Fig.9 – Common-mode rejection ratio vs frequency.

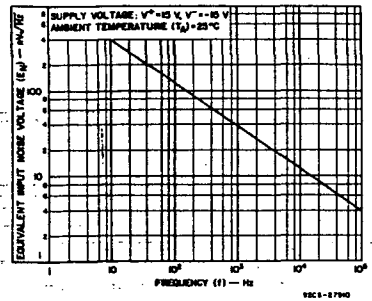


Fig.10 – Equivalent input noise voltage vs frequency.

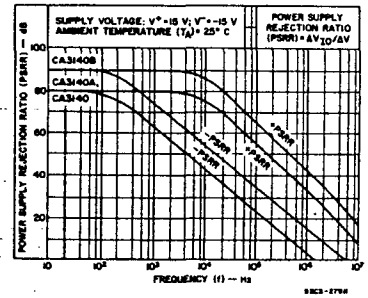


Fig.11 – Power supply rejection ratio vs frequency.

APPLICATIONS CONSIDERATIONS

Wide dynamic range of input and output characteristics with the most desirable high input-impedance characteristic is achieved in the CA3140 by the use of an unique design based upon the PMOS-Bipolar process. Input-common-mode voltage range and output-swing capabilities are complementary, allowing operation with the single supply down to four volts.

The wide dynamic range of these parameters also means that this device is suitable for many single-supply applications, such as, for example, where one input is driven below the potential of terminal 4 and the phase sense of the output signal must be maintained – a most important consideration in comparator applications.

OUTPUT CIRCUIT CONSIDERATIONS

Excellent interfacing with TTL circuitry is easily achieved with a single 6.2-volt zener diode connected to terminal 8 as shown in Fig.12. This connection assures that the maximum output signal swing will not go more positive than the zener voltage minus two base-to-emitter voltage drops within the CA3140. These voltages are independent of the operating supply voltage.

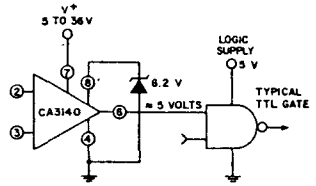


Fig.12 – Zener clamping diode connected to terminals 8 and 4 to limit CA3140 output swing to TTL levels.

Fig.13 shows output current-sinking capabilities of the CA3140 at various supply voltages. Output voltage swing to the negative supply rail permits this device to operate both power transistors and thyristors directly without the need for level-shifting circuitry usually associated with the 741 series of operational amplifiers.

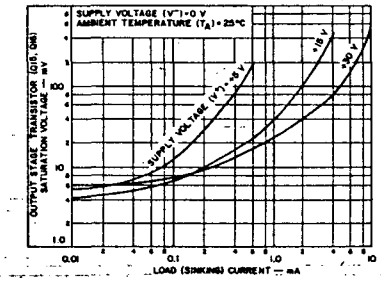


Fig.13 – Voltage across output transistors Q15 and Q16 vs load current.

Fig.16 show some typical configurations. Note that a series resistor, R_L, is used in both cases to limit the drive available to the driven device. Moreover, it is recommended that a series diode and shunt diode be used at the thyristor input to prevent large negative transient surges that can appear at the gate of thyristors, from damaging the integrated circuit.

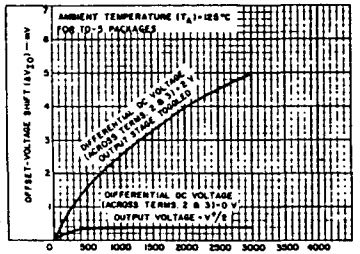


Fig.14 – Typical incremental offset-voltage shift vs operating life.

OFFSET-VOLTAGE NULLING

The input-offset voltage can be nulled by connecting a 10-kΩ potentiometer between terminals 1 and 5 and returning its wiper arm to terminal 4, see Fig.15a. This technique, however, gives more adjustment range than required and therefore, a considerable portion of the potentiometer rotation is not fully utilized. Typical values of series resistors that may be placed at either end of the potentiometer, see Fig.15b, to optimize its utilization range are given in the table "Typical Electrical Characteristics" shown in this bulletin.

An alternate system is shown in Fig.15c. This circuit uses only one additional resistor of approximately the value shown in the table. For potentiometers, in which the resistance does not drop to zero ohms at either end of rotation, a value of resistance 10% lower than the values shown in the table should be used.

LOW-VOLTAGE OPERATION

Operation at total supply voltages as low as 4 volts is possible with the CA3140. A current regulator based upon the PMOS threshold voltage maintains reasonable constant operating current and hence consistent performance down to these lower voltages.

The low-voltage limitation occurs when the upper extreme of the input common-mode voltage range extends down to the voltage at terminal 4. This limit is reached at a total

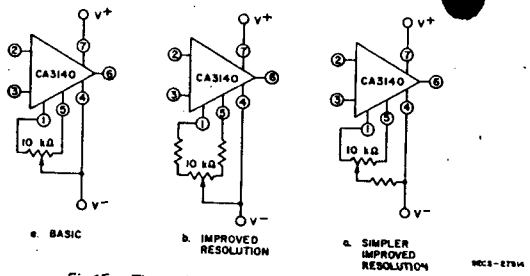


Fig.15 – Three offset-voltage nulling methods.

supply voltage just below 4 volts. The output voltage range also begins to extend down to the negative supply rail, but is slightly higher than that of the input. Fig.20 shows these characteristics and shows that with 2-volt dual supplies, the lower extreme of the input common-mode voltage range is below ground potential.

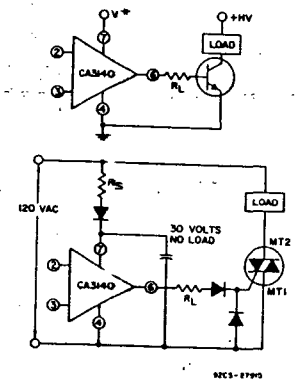


Fig.16 – Methods of utilizing the $V_{CE(sat)}$ sinking-current capability of the CA3140 series.

BANDWIDTH AND SLEW RATE

For those cases where bandwidth reduction is desired, for example, broadband noise reduction, an external capacitor connected between terminals 1 and 8 can reduce the open-loop −3 dB bandwidth. The slew rate will, however, also be proportionally reduced by using this additional capacitor. Thus, a 20% reduction in bandwidth by this technique will also reduce the slew rate by about 20%.

Fig.17 shows the typical settling time required to reach 1 mV or 10 mV of the final value for various levels of large signal inputs for the voltage-follower and inverting unity-gain amplifiers. The exceptionally fast setting time characteristics are largely due to the high combination of high gain and wide bandwidth of the CA3140; as shown in Fig. 18.

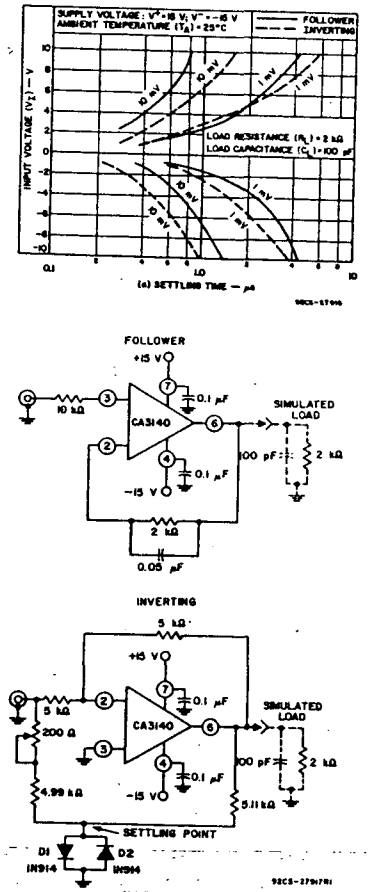


Fig.17 – Input voltage vs settling time.

INPUT CIRCUIT CONSIDERATIONS

As mentioned previously, the amplifier inputs can be driven below the terminal 4 potential, but a series current-limiting resistor is recommended to limit the maximum input terminal current to less than 1 mA to prevent damage to the input protection circuitry.

Moreover, some current-limiting resistance should be provided between the inverting input and the output when the CA3140 is used as a unity-gain voltage follower. This resistance prevents the possibility of extremely large input-signal transients from forcing a signal through the input-protection network and directly driving the internal constant-current source which could result in positive feedback via the output terminal. A 3.9-kΩ resistor is sufficient.

The typical input current is in the order of 10 pA when the inputs are centered at nominal device dissipation. As the output supplies load current, device dissipation will increase, raising the chip temperature and resulting in increased input current. Fig.19 shows typical input-terminal current versus ambient temperature for the CA3140.

It is well known that MOS/FET devices can exhibit slight changes in characteristics (for example, small changes in input offset voltage) due to the application of large differential input voltages that are sustained over long periods at elevated temperatures.

Both applied voltage and temperature accelerate these changes. The process is reversible and offset voltage shifts of the opposite polarity reverse the offset. Fig.14 shows the typical offset voltage change as a function of various stress voltages at the maximum rating of 125°C (for TO-5); at lower temperatures (TO-5 and plastic), for example, at 85°C, this change in voltage is considerably less. In typical linear applications, where the differential voltage is small and symmetrical, these incremental changes are of about the same magnitude as those encountered in an operational amplifier employing a bipolar a transistor input stage.

SUPER SWEEP FUNCTION GENERATOR

A function generator having a wide tuning range is shown in Fig.21. The 1,000,000/1 adjustment range is accomplished by a single variable potentiometer or by an auxiliary sweeping signal. The CA3140 functions as a non-inverting read-out amplifier of the triangular signal developed across the integrating capacitor network connected to the output of the CA3080A current source.

Buffered triangular output signals are then applied to a second CA3080 functioning as a high-speed hysteresis switch. Output from the switch is returned directly back to the

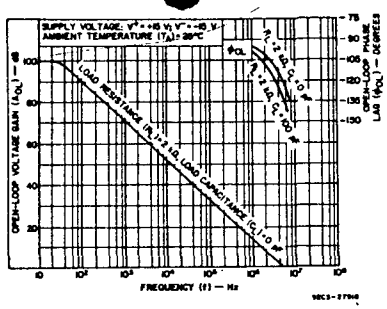


Fig.18 – Open-loop voltage gain and phase lag vs frequency.

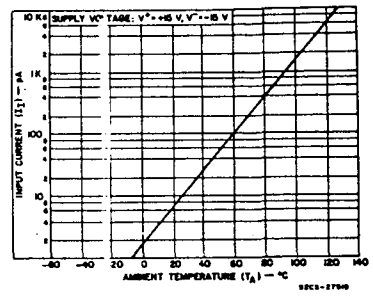


Fig.19 – Input current vs ambient temperature.

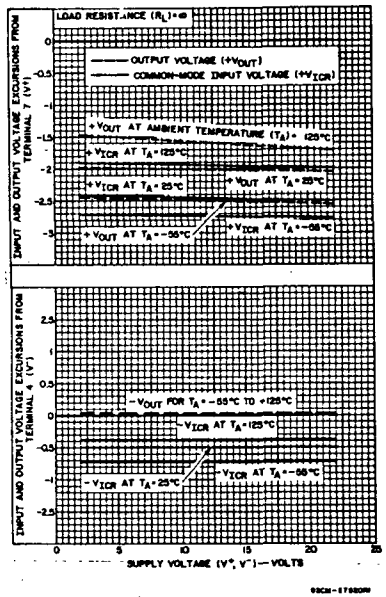


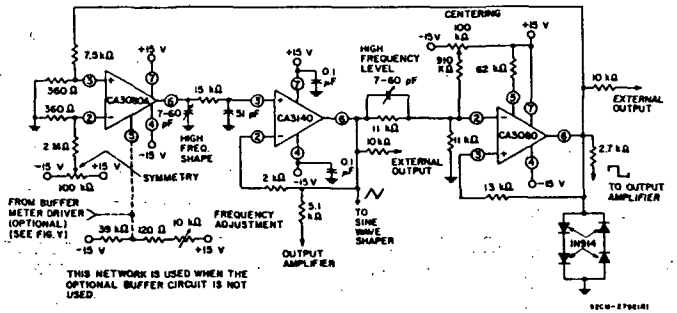
Fig.20 – Output-voltage-swing capability and common-mode input-voltage range vs supply voltage and temperature.

inp it of the CA3080A current source, thereby, completing the positive feedback loop.

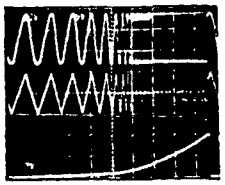
The triangular output level is determined by the four 1N914 level-limiting diodes of the second CA3080 and the resistor-divider network connected to terminal No.2 (input) of the CA3080. These diodes establish the input trip level to this switching stage and, therefore, indirectly determine the amplitude of the output triangle.

Compensation for propagation delays around the entire loop is provided by one adjustment on the input of the CA3080. This adjustment, which provides for a constant generator amplitude output, is most easily made while the generator is sweeping. High-frequency ramp linearity is adjusted by the single 7-to-60 pF capacitor in the output of the CA3080A.

It must be emphasized that only the CA-3080A is characterized for maximum output linearity in the current-generator function.

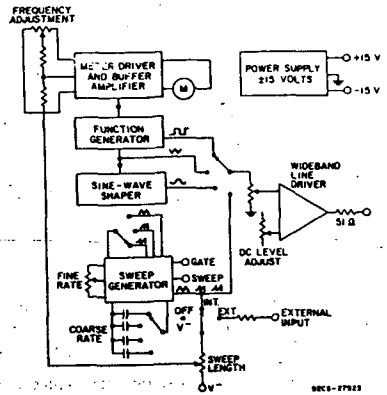


(a) Circuit

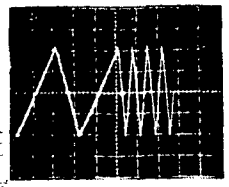


TOP TRACE: OUTPUT AT JUNCTION OF 2.7 Ω AND 51 Ω RESISTORS
5 V/DIV AND 500 ms/DIV
CENTER TRACE: EXTERNAL OUTPUT OF TRIANGULAR FUNCTION GENERATOR
2 V/DIV AND 500 ms/DIV
BOTTOM TRACE: OUTPUT OF "LOG" GENERATOR
10 V/DIV AND 500 ms/DIV

(b1) Function generator sweeping



(c) Interconnections



1V/DIV and 1 sec/DIV

Three tone test signals, highest frequency > 0.5 MHz. Note the slight assymmetry at the three-second/cycle signal. This assymmetry is due to slightly different positive and negative integration from the CA3080A and from the pc board and component leakages at the 100-pA level.

(b2) Function generator with fixed frequencies

Fig. 21 – Function generator.

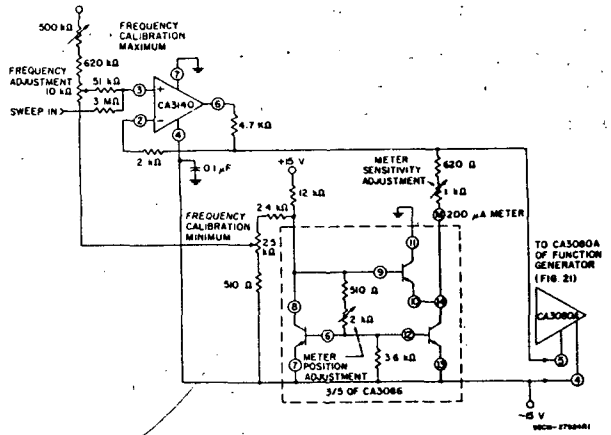


Fig. 22 – Meter driver and buffer amplifier.

METER DRIVER AND BUFFER AMPLIFIER

Fig. 22 shows the CA3140 connected as a *meter driver and buffer amplifier*. Low driving impedance is required of the CA-3080A current source to assure smooth operation of the Frequency Adjustment Control. This low-driving impedance requirement is easily met by using a CA3140 connected as a voltage follower. Moreover, a meter may be placed across the input to the CA3080A to give a logarithmic analog indication of the function generators frequency.

Analog frequency readout is readily accomplished by the means described above because the output current of the CA3080A varies approximately one decade for each 60-mV change in the applied voltage, V_{ABC} (voltage between terminals 5 and 4 of the CA3080A of the function generator). Therefore, six decades represent 360-mV change in V_{ABC}.

Now, only the reference voltage must be established to set the lower limit on the meter. The three remaining transistors from the CA3086 Array used in the sweep generator are used for this reference voltage. In addition, this reference generator arrangement tends to track ambient temperature variations, and thus compensates for the effects of the normal negative temperature coefficient of the CA3080A V_{ABC} terminal voltage.

Another output voltage from the reference generator is used to insure temperature tracking of the lower end of the Frequency Adjustment Potentiometer. A large series resistance simulates a current source, assuring similar temperature coefficients at both ends of the Frequency Adjustment Control.

To calibrate this circuit, set the Frequency Adjustment Potentiometer at its low end. Then adjust the Minimum Frequency Calibration Control for the lowest frequency. To establish the upper frequency limit, set the Frequency Adjustment Potentiometer to its upper end and then adjust the Maximum Frequency Calibration Control for the maximum frequency. Because there is interaction among these controls, repetition of the adjustment procedure may be necesary.

Two adjustments are used for the meter. The meter sensitivity control sets the meter-scale width of each decade, while the meter position control adjusts the pointer on the scale with negligible effect on the sensitivity adjustment. Thus, the meter sensitivity adjustment control calibrates the meter so that it deflects 1/6 of full scale for each decade change in frequency.

SINE-WAVE SHAPER

The circuit shown in Fig. 23 uses a CA3140 as a voltage follower in combination with diodes from the CA3019 Array to convert the triangular signal from the function generator to a sine-wave output signal having typically less than 2% THD. The basic zero-crossing slope is established by the 10-kΩ potentiometer connected between terminals 2 and 6 of the CA3140 and the 9.1-kΩ resistor and 10-kΩ potentiometer from terminal 2 to ground. Two break points are established by diodes D_1 through D_4. Positive feedback via D_5 and D_6 establishes the zero slope at the maximum and minimum levels of the sine wave. This technique is necessary because the voltage-follower configuration approaches unity gain rather than the zero gain required to shape the sine wave at the two extremes.

This circuit can be adjusted most easily with a distortion analyzer, but a good first approximation can be made by comparing the output signal with that of a sine-wave generator. The initial slope is adjusted with the potentiometer R_1, followed by an adjustment of R_2. The final slope is established by adjusting R_3, thereby adding additional segments that are contributed by these diodes. Because there is some interaction among these controls, repetition of the adjustment procedure may be necessary

SWEEPING GENERATOR

Fig. 24 shows a sweeping generator. Three CA3140's are used in this circuit. One CA3140 is used as an integrator, a second device is used as a hysteresis switch that determines the starting and stopping points of the sweep. A third CA3140 is used as a logarithmic shaping network for the log function. Rates and slopes, as well as sawtooth, triangle, and logarithmic sweeps are generated by this circuit.

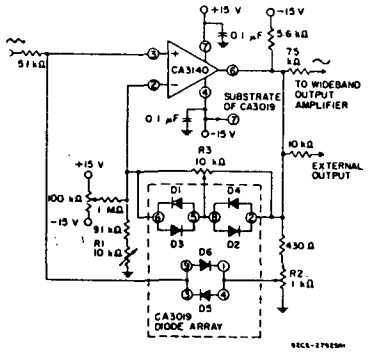


Fig. 23 — Sine-wave shaper.

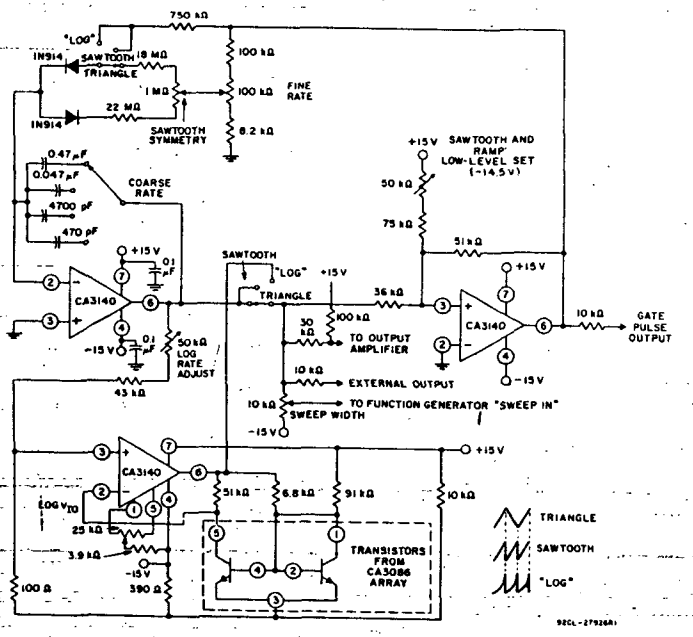


Fig. 24 — Sweeping generator.

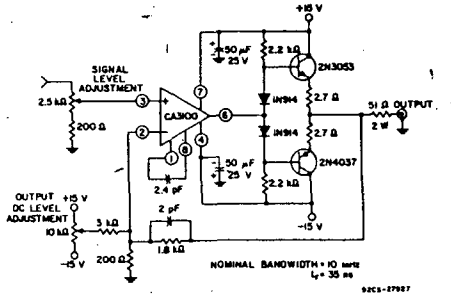


Fig. 25 — Wideband output amplifier.

WIDEBAND OUTPUT AMPLIFIER

Fig. 25 shows a high-slew-rate, wideband amplifier suitable for use as a 50-ohm transmission-line driver. This circuit, when used in conjunction with the function generator and sine-wave shaper circuits shown in Figs. 21 and 23 provides 18 volts peak-to-peak output open-circuited, or 9 volts peak-to-peak output when terminated in 50 ohms. The slew rate required of this amplifier is 28 volts/μs (18 volts peak-to-peak x π x 0.5 MHz).

POWER SUPPLIES

High input-impedance, common-mode capability down to the negative supply and high output-drive current capability are key factors in the design of wide-range output-voltage supplies that use a single input voltage to provide a regulated output voltage that can be adjusted from essentially 0 to 24 volts.

Unlike many regulator systems using comparators having a bipolar transistor-input stage, a high-impedance reference-voltage divider from a single supply can be used in connection with the CA3140 (see Fig. 26).

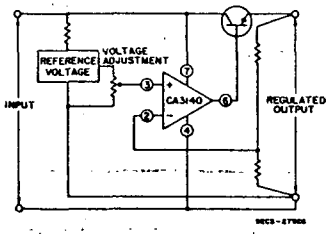


Fig. 26 — Basic single-supply voltage regulator showing voltage-follower configuration.

Essentially, the regulators, shown in Figs. 27 and 28, are connected as non-inverting power operational amplifiers with a gain of 3.2. An 8-volt reference input yields a maximum output voltage slightly greater than 25 volts. As a voltage follower, when the reference input goes to 0 volts the output will be 0 volts. Because the offset voltage is also multiplied by the 3.2 gain factor, a potentiometer is needed to null the offset voltage.

Series pass transistors with high I_{CBO} levels will also prevent the output voltage from reaching zero because there is a finite voltage drop (V_{CE}sat) across the output of the CA3140 (see Fig.13). This saturation voltage level may indeed set the lowest voltage obtainable.

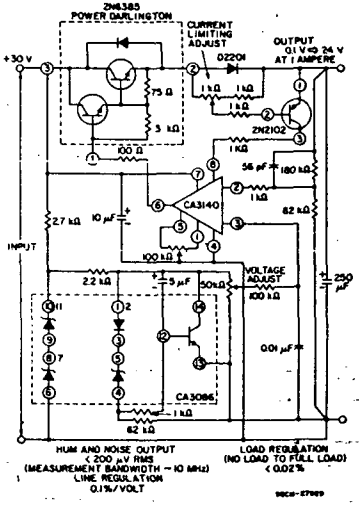


Fig. 27 — Regulated power supply.

The high impedance presented by terminal 8 is advantageous in effecting current limiting. Thus, only a small signal transistor is required for the current-limit sensing amplifier. Resistive decoupling is provided for this transistor to minimize damage to it or the CA3140 in the event of unusual input or output transients on the supply-rail.

Figs. 27 and 28, show circuits in which a D2201 high-speed diode is used for the current sensor. This diode was chosen for its slightly higher forward-voltage drop characteristic thus giving greater sensitivity. It must be emphasized that heat sinking of this diode is essential to minimize variation of the current trip point due to internal heating of the diode. That is, 1 ampere at 1 volt forward drop represents one watt which can result in significant regenerative changes in the current trip point as the diode temperature rises. Placing the small-signal reference amplifier in the proximity of the current-sensing diode also helps minimize the variability in the trip level due to the negative temperature coefficient of the diode. In spite of those limitations, the current limiting point can easily be adjusted over the range from 10 mA to 1 ampere with a single adjustment potentiometer. If the temperature stability of the current-limiting system is a serious consideration, the more usual current-sampling resistor-type of circuitry should be employed.

A power Darlington transistor (in a heat sink TO-3 case), is used as the series-pass element for the conventional current-limiting system, Fig. 27, because high-power Darlington dissipation will be encountered at low output voltage and high currents.

A small heat-sink VERSAWATT transistor is used as the series-pass element in the foldback current system, Fig.28, since dissipation levels will only approach 10 watts. In this system, the D2201 diode is used for current sampling. Foldback is provided by the 3 kΩ and 100 kΩ divider network connected to the base of the current-sensing transistor.

Both regulators, Figs. 27 and 28, provide better than 0.02% load regulation. Because there is constant loop gain at all voltage settings, the regulation also remains constant. Line regulation is 0.1% per volt. Hum and noise voltage is less than 200 μV as read with a meter having a 10-MHz bandwidth.

Fig.31 (a) shows the turn ON and turn OFF characteristics of both regulators. The slow turn-on rise is due to the slow rate of rise of the reference voltage. Fig. 29 (b) shows the transient response of the regulator with the switching of a 20-Ω load at 20 volts output.

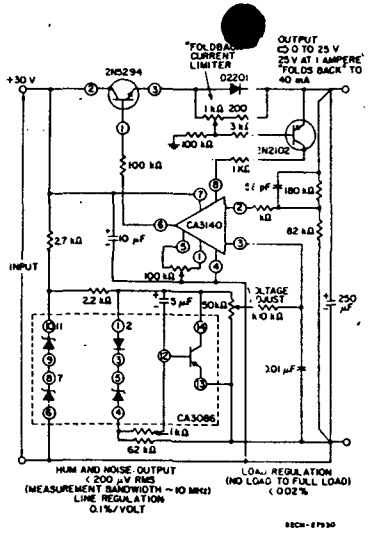
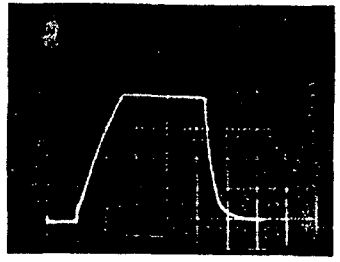
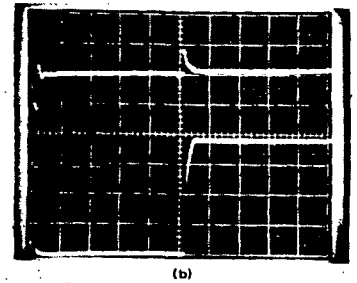


Fig. 28 – Regulated power supply with "foldback" current limiting.



(a)

SUPPLY TURN-ON AND TURN-OFF CHARACTERISTICS
(5 VOLTS/DIV AND 1 s/DIV.)
92CS-27882



(b)

TRANSIENT RESPONSE
TOP TRACE: OUTPUT VOLTAGE
(200 mV/DIV AND 5 μs/DIV)
BOTTOM TRACE: COLLECTOR OF LOAD SWITCHING TRANSISTOR, LOAD = 1 AMPERE
(5 VOLTS/DIV AND 5 μs/DIV)
92CS-27881

Fig. 29 – Waveforms of dynamic characteristics of power supply currents shown in Figs. 29 and 30.

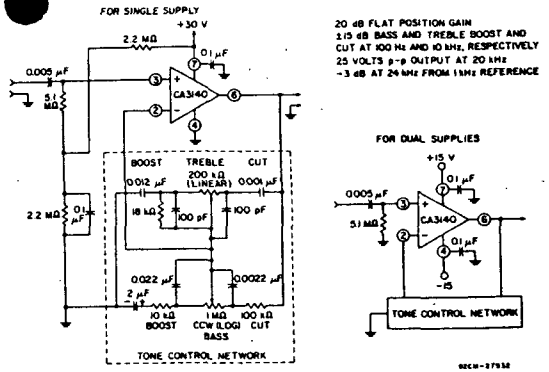


Fig. 30 – Tone control circuit using CA3130 series (20-dB midband gain).

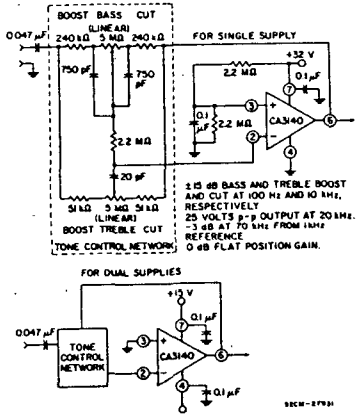


Fig. 31 – Baxandall tone control circuit using CA3140 series.

TONE CONTROL CIRCUITS

High-slew-rate, wide-bandwidth, high-output voltage capability and high input impedance are all characteristics required of tone-control amplifiers. Two tone control circuits that exploit these characteristics of the CA3140 are shown in Figs. 30 and 31.

The first circuit, shown in Fig. 31, is the Baxandall tone-control circuit which provides unity gain at midband and uses standard linear potentiometers. The high input impedance of the CA3140 makes possible the use of low-cost, low-value, small-size capacitors, as well as reduced load of the driving stage.

Bass treble boost and cut are ± 15 dB at 100 Hz and 10 kHz, respectively. Full peak-to-peak output is available up to at least 20 kHz due to the high slew rate of the CA3140. The amplifier gain is −3 dB down from its "flat" position at 70 kHz.

Fig. 30 shows another tone-control circuit with similar boost and cut specifications. The wideband gain of this circuit is equal to the ultimate boost or cut plus one, which in this case is a gain of eleven. For 20-dB boost and cut, the input loading of this circuit is essentially equal to the value of the resistance from terminal No.3 to ground. A detailed analysis of this circuit is given in "An IC Operational Transconductance Amplifier (OTA) With Power Capability" by L. Kaplan and H. Wittlinger, IEEE Transactions on Broadcast and Television Receivers, Vol. BTR-18, No.3, August, 1972.

WIEN BRIDGE OSCILLATOR

Another application of the CA3140 that makes excellent use of its high input-impedance, high-slew-rate, and high-voltage qualities is the Wien Bridge sine-wave oscillator. A basic Wien Bridge oscillator is shown in Fig. 32. When $R_1 = R_2 = R$ and $C_1 = C_2 = C$, the frequency equation reduces to the familiar $f = 1/2\pi RC$ and the gain required for oscillation, A_{OSC} is equal to 3. Note that if C_2 is increased by a factor of four and R_2 is reduced by a factor of four, the gain required for oscillation becomes 1.5, thus per-

mitting a potentially higher operating frequency closer to the gain-bandwidth product of the CA3140.

Oscillator stabilization takes on many forms. It must be precisely set, otherwise the amplitude will either diminish or reach some form of limiting with high levels of distortion. The element, R_S, is commonly replaced with some variable resistance element. Thus, through some control means, the value of R_S is adjusted to maintain constant oscillator output. A FET channel resistance, a thermistor, a lamp bulb, or other device whose resistance is made to increase as the output amplitude is increased are a few of the elements often utilized.

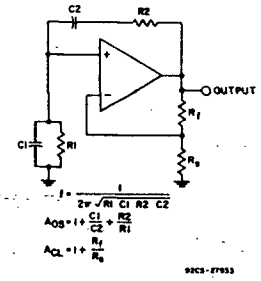


Fig. 32 – Basic Wien bridge oscillator circuit using an operational amplifier.

Fig. 33 shows another means of stabilizing the oscillator with a zener diode shunting the feedback resistor (R_f of Fig. 32). As the output signal amplitude increases, the zener diode impedance decreases resulting in more feedback with consequent reduction in gain; thus stabilizing the amplitude of the output signal. Furthermore, this combination of a monolithic zener diode and bridge rectifier circuit tends to provide a zero temperature coefficient for this regulating system. Because this bridge rectifier system has no time constant, i.e., thermal time constant for the lamp bulb, and RC time constant for filters often used in detector networks, there is no lower frequency limit. For example, with 1-μF polycarbonate capacitors and 22 MΩ for the frequency determining network, the operating frequency is 0.007 Hz.

As the frequency is increased, the output amplitude must be reduced to prevent the output signal from becoming slew-rate limited. An output frequency of 180 kHz will reach a slew rate of approximately 9 volts/μs when its amplitude is 16 volts peak-to-peak.

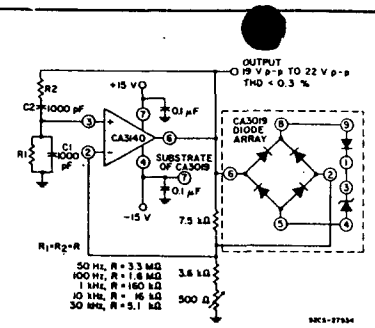


Fig. 33 – Wien bridge oscillator circuit using CA3140 series.

SIMPLE SAMPLE-AND-HOLD SYSTEM

Fig. 34 shows a very simple sample-and-hold system using the CA3140 as the readout amplifier for the storage capacitor. The CA3080A serves as both input buffer amplifier and low feed-through transmission switch.* System offset nulling is accomplished with the CA3140 via its offset nulling terminals. A typical simulated load of 2 kΩ and 30 pF is shown in the schematic.

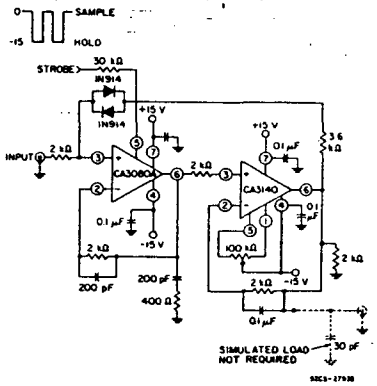
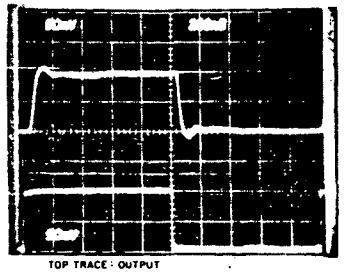


Fig. 34 – Sample-and hold circuit.

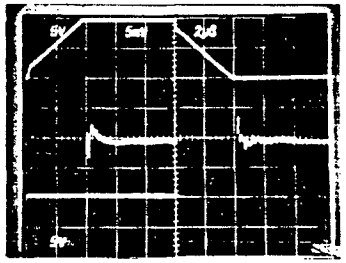
In this circuit, the storage compensation capacitance (C_1) is only 200 pF. Larger value capacitors provide longer "hold" periods but with slower slew rates. The slew rate $\frac{dv}{dt} = \frac{i}{c} = 0.5\ mA/200\ pF = 2.5\ V/\mu s$.

* ICAN-6668 "Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers".

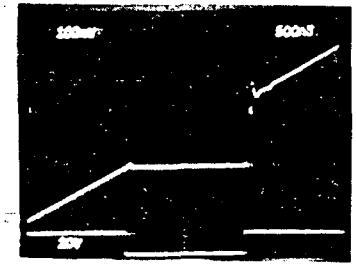
Pulse "droop" during the hold interval is 170 pA/200 pF which is = 0.85 μV/μs; (i.e., 170 pA/200 pF). In this case, 170 pA represents the typical leakage current of the CA3080A when strobed off. If C_1 were increased to 2000 pF, the "hold-droop" rate will decrease to 0.085 μV/μs, but the slew rate would decrease to 0.25 V/μs. The parallel diode network connected between terminal 3 of the CA3080A and terminal 6 of the CA3140 prevents large input-signal feedthrough across the input terminals of the CA3080A to the 200 pF storage capacitor when the CA3080A is strobed off. Fig. 35 shows dynamic characteristic waveforms of this sample-and-hold system.



TOP TRACE: OUTPUT
(50 mV/DIV. AND 200 ns/DIV.)
BOTTOM TRACE: INPUT
(50 mV/DIV. AND 200 ns/DIV.)
92CS-27883



LARGE-SIGNAL RESPONSE AND SETTLING TIME
TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5 V/DIV. AND 2 μs/DIV.)
CENTER TRACE: DIFFERENCE OF INPUT AND OUTPUT SIGNALS THROUGH TEKTRONIX AMPLIFIER 7A13
(5 mV/DIV. AND 2 μs/DIV.) 92CS-27884



SAMPLING RESPONSE
TOP TRACE: SYSTEM OUTPUT
(100 mV/DIV. AND 500 ns/DIV.)
BOTTOM TRACE: SAMPLING SIGNAL
(20 V/DIV. AND 500 ns/DIV.)
92CS-27885

Fig. 35 – Sample-and hold system dynamic characteristics waveforms.

CURRENT AMPLIFIER

The low input-terminal current needed to drive the CA3140 makes it ideal for use in current-amplifier applications such as the one shown in Fig. 36.* In this circuit, low current is supplied at the input potential as the power supply to load resistor R_L. This load current is increased by the multiplication factor R2/R1, when the load current is monitored by the power supply meter M. Thus, if the load current is 100 nA, with values shown, the load current presented to the supply will be 100 μA; a much easier current to measure in many systems.

Note that the input and output voltages are transferred at the same potential and only the output current is multiplied by the scale factor.

The dotted components show a method of decoupling the circuit from the effects of high output-load capacitance and the potential oscillation in this situation. Essentially, the necessary high-frequency feedback is provided by the capacitor with the dotted series resistor providing load decoupling.

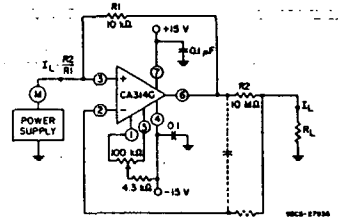


Fig. 36 – Basic current amplifier for low-current measurement systems.

Fig. 37 shows a single-supply, absolute-value, ideal full-wave rectifier with associated waveforms. During positive excursions, the input signal is fed through the feedback network directly to the output. Simultaneously, the positive excursion of the input signal also drives the output terminal (No.6) of the inverting amplifier in a negative-going excursion such that the 1N914 diode effectively disconnects the amplifier from the signal path. During a negative-going excursion of the input signal, the CA3140 functions as a normal inverting amplifier with a gain equal to −R2/R1. When the equality of the two equations shown in Fig. 37 is satisfied, the full-wave output is symmetrical.

• "Operational Amplifiers Design and Applications", J. G. Graeme, McGraw-Hill Book Company, page 308 – "Negative Immittance Converter Circuits".

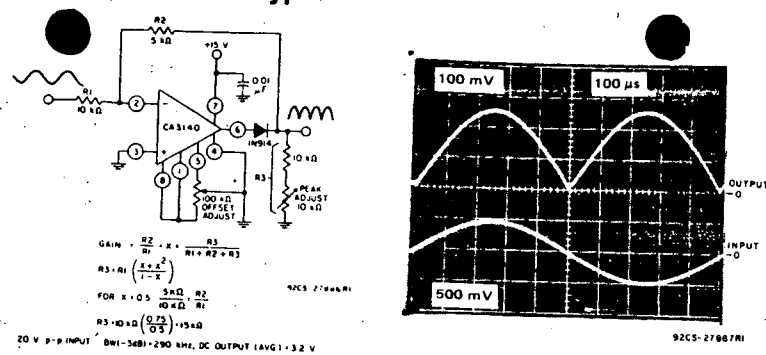
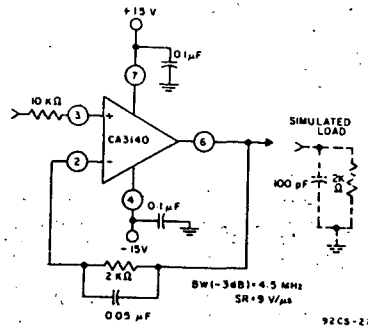
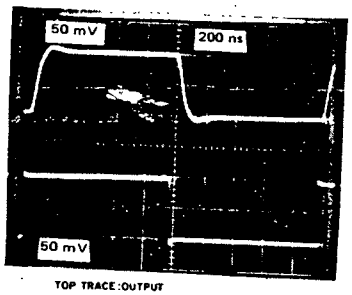
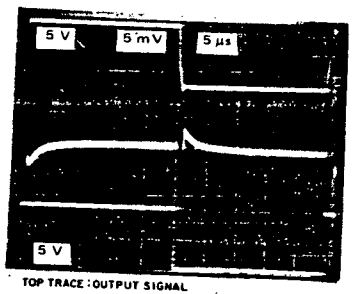


Fig. 37 – Single-supply, absolute-value, ideal full-wave rectifier with associated waveforms.





TOP TRACE: OUTPUT
(50 mV/DIV AND 200 ns/DIV)
BOTTOM TRACE: INPUT
(50 mV/DIV AND 200 ns/DIV)
(a) SMALL-SIGNAL RESPONSE
(50 mV/DIV AND 200 ns/DIV)
92CS-27879



TOP TRACE: OUTPUT SIGNAL
(5 V/DIV. AND 5 µs/DIV.)
CENTER TRACE: DIFFERENCE SIGNAL
(5m V/DIV. AND 5 µs/DIV.)
BOTTOM TRACE: INPUT SIGNAL
(5 V/DIV. AND 5 µs/DIV)
(b) INPUT-OUTPUT DIFFERENCE SIGNAL SHOWING SETTLING TIME (MEASUREMENT MADE WITH TEKTRONIX 7A13 DIFFERENTIAL AMPLIFIER)
92CS-27880

Fig. 38 – Split-supply voltage-follower test circuit and associated waveforms.

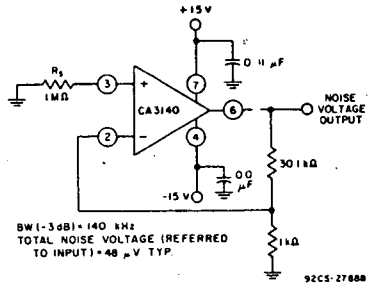
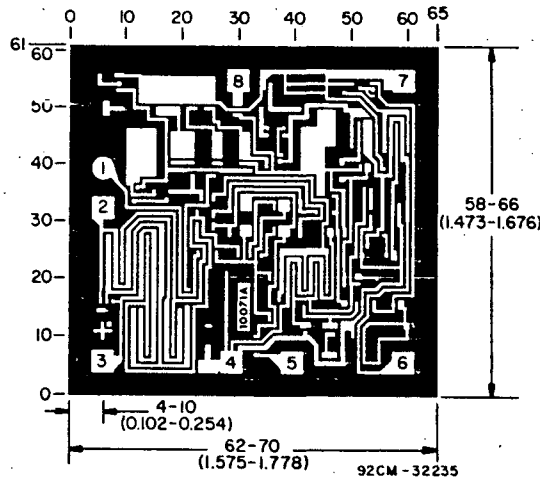


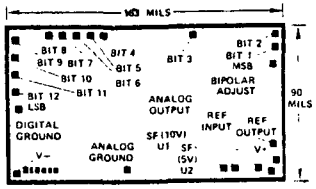
Fig. 39 – Test circuit amplifier (30-dB gain) used for wideband noise measurement.



The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17 mm) larger in both dimensions.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

DICE DIMENSIONS

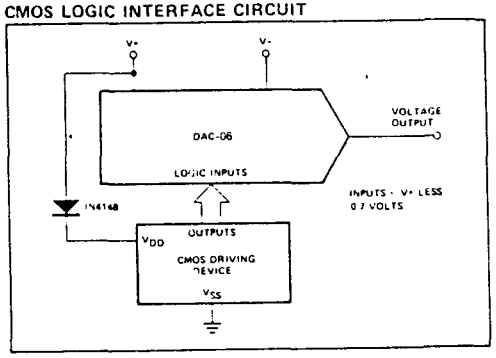


INTERFACING WITH CMOS LOGIC

The DAC-06's logic input stages require about 1μA and are capable of operation with inputs between −5 volts and V+ less 0.7 volt. This wide input voltage range allows direct CMOS interfacing in most applications, the exception being where the CMOS logic and D/A converter must use the same positive power supply.

In this special case, a diode should be placed in series with the CMOS driving device's V_{DD} lead as shown in Figure 1. The diode limits V_D to V+ less 0.7 volt — since the output from the CMOS device cannot exceed this value, the DAC's maximum input voltage rule is satisfied. Summarizing: in all applications, the DAC-06 requires either no interfacing components, or at most a single inexpensive diode for full CMOS compatibility.

CMOS LOGIC INTERFACE CIRCUIT



DAC-08

8-BIT HIGH-SPEED MULTIPLYING D/A CONVERTER

UNIVERSAL DIGITAL LOGIC INTERFACE

FEATURES

- Fast Settling Output Current 85ns
- Full Scale Current Prematched to ±1 LSB
- Direct Interface to TTL, CMOS, ECL, HTL, PMOS
- Nonlinearity to ±0.1% Maximum Over Temperature Range
- High Output Impedance and Compliance ..... −10V to +18V
- Differential Current Outputs
- Wide Range Multiplying Capability ... 1MHz Bandwidth
- Low FS Current Drift ..... ±10ppm/°C
- Wide Power Supply Range ..... ±4.5V to ±18V
- Low Power Consumption ..... 33mW @ ±5V
- Low Cost

GENERAL DESCRIPTION

The DAC-08 series of 8-bit monolithic Digital-to-Analog Converters provide very high-speed performance coupled with low cost and outstanding applications flexibility.

Advanced circuit design achieves 85ns settling times with very low glitch and at low power consumption. Monotonic multiplying performance is attained over a wide 40 to 1 reference current range. Matching to within 1 LSB between reference and full scale currents eliminates the need for full scale trimming in most applications. Direct interface to all popular logic families with full noise immunity is provided by the high swing, adjustable threshold logic inputs.

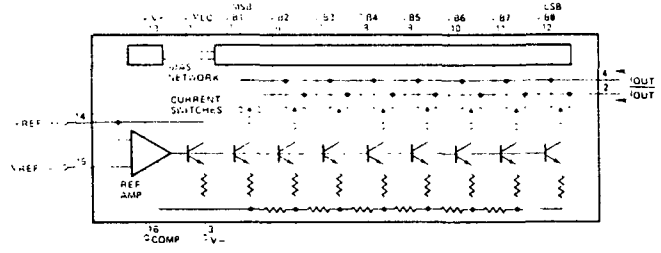
High-voltage compliance dual-complementary current outputs are provided, increasing versatility and enabling differential operation to effectively double the peak-to-peak output swing. In many applications, the outputs can be directly converted to voltage without the need for an external op amp.

All DAC-08 series models guarantee full 8-bit monotonicity, and nonlinearities as tight as ±0.1% over the entire operating temperature range are available. Device performance is essentially unchanged over the ±4.5 to ±18V power supply range, with 33mW power consumption attainable at ±5V supplies.

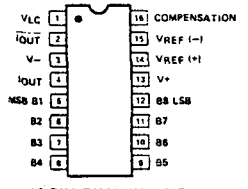
The compact size and low power consumption make the DAC-08 attractive for portable and military/aerospace applications. devices processed to MIL-STD-883, Level B are available.

DAC-08 applications include 8-bit, 1μs A/D converters, servo motor and pen drivers, waveform generators, audio encoders and attenuators, analog meter drivers, programmable power supplies, CRT display drivers, high-speed modems and other applications where low cost, high speed and complete input/output versatility are required.

EQUIVALENT CIRCUIT



ORDERING INFORMATION & PIN CONNECTION



16-PIN DUAL-IN-LINE

Q — Hermetic Package P — Plastic Package

MODEL	TEMP RANGE	NONLINEARITY
DAC-08AQ	−55°/+125°C	±0.1%
DAC-08Q	−55°/+125°C	±0.19%
DAC-08HQ	0°/+70°C	±0.1%
DAC-08EQ	0°/+70°C	±0.19%
DAC-08CQ	0°/+70°C	±0.39%
DAC-08HP	0°/+70°C	±0.10%
DAC-08EP	0°/+70°C	±0.19%
DAC-08CP	0°/+70°C	±0.39%

Military Temperature Range Devices With MIL-STD-883B Class B Processing

ORDER: DAC08AQ/883
DAC08Q/883

FOR QPL-38510 PARTS REFER TO JM38510/11301/11302 DATA SHEET

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- DAC-08AQ, Q ..... −55°C to +125°C
- DAC-08HQ, EQ, CQ ..... 0°C to +70°
- Storage Temperature ..... −65°C to 150°C
- Power Dissipation* 500mW
- Derate above 100°C ..... 10mW/°C
- Lead Soldering Temperature (60 sec.) ..... 300°C

*Over full operating range

V+ Supply to V− Supply 36V
Logic Inputs ..... V− to V− plus 36V
V_{LC} ..... V− to V+
Analog Current Outputs ..... See Figure 12
Reference Inputs (V_{14} to V_{15}) ..... V− to V+
Reference Input Differential Voltage (V_{14} to V_{15}) ..... ±18V
Reference Input Current (I_{14}) 5.0mA

ELECTRICAL CHARACTERISTICS

at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = -55°C$ to $+125°C$ unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

PARAMETER	SYMBOL	CONDITIONS	DAC-08A MIN	DAC-08A TYP	DAC-08A MAX	DAC-08 MIN	DAC-08 TYP	DAC-08 MAX	UNITS
Resolution			8	8	8	8	8	8	Bits
Monotonicity			8	8	8	8	8	8	Bits
Nonlinearity		$T_A = -55°C$ to $+125°C$	—	—	±0.1	—	—	±0.19	%FS
Settling Time	t_s	To ±½ LSB, all bits switched ON or OFF, $T_A = 25°C$ (See Note)	—	85	135	—	85	150	ns
Propagation Delay									
Each bit	t_{PLH}	$T_A = 25°C$	—	35	60	—	35	60	ns
All bits switched	t_{PHL}	(See Note)	—	35	60	—	35	60	ns
Full Scale Tempco	TC_{FS}	(See Note)	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance (True Compliance)	V_{OC}	Full scale current change < ½ LSB, R_{OUT} > 20MΩ typical	−10	—	+18	−10	—	+18	Volts
Full Range Current	I_{FR4}	$I_{REF} = 2mA$, $T_A = +25°C$	1.984	1.992	2.000	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} - I_{FR2}$	—	±0.5	±4.0	—	±1.0	±8.0	µA
Zero Scale Current	I_{ZS}		—	0.1	1.0	—	0.2	2.0	µA
Output Current Range	I_{OR_1}	R_{14}, $R_{15} = 5.000k\Omega$, $V_{REF} = +15.0V$, $V- = -10V$	2.1	—	—	2.1	—	—	mA
	I_{OR_2}	$V_{REF} = +25.0V$, $V- = -12V$	4.2	—	—	4.2	—	—	
Logic Input Levels									
Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	Volts
Logic Input "1"	V_{IH}		2.0	—	—	2.0	—	—	
Logic Input Current		$V_{LC} = 0V$							
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	—	−2.0	−10	—	−2.0	−10	µA
Logic Input "1"	I_{IH}	$V_{IN} = 2.0V$ to $18V$	—	0.002	10	—	0.002	10	
Logic Input Swing	V_{IS}	$V- = -15V$	−10	—	+18	−10	—	+18	Volts
Logic Threshold Range	V_{THR}	$V_S = \pm 15V$	−10	—	+13.5	−10	—	+13.5	Volts
Reference Bias Current	I_{15}		—	−1.0	−3.0	—	−1.0	−3.0	µA
Reference Input Slew Rate	dI/dt	$R_{EQ} = 200\Omega$, $R_L = 100\Omega$, $C_L = 0pF$ — See fast pulsed into following Elect. Characteristics	4.0	8.0	—	4.0	8.0	—	mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$	$V+ = 4.5V$ to $18V$, $V- = -4.5$ to $-18V$, $I_{REF} = 1.0mA$	—	±0.0003	±0.01	—	±0.0003	±0.01	%/%ΔV+
	$PSSI_{FS-}$		—	±0.002	±0.01	—	±0.002	±0.01	%/%ΔV−
Power Supply Current	I+	$V_S = \pm 5V$, $I_{REF} = 1.0mA$	—	2.3	3.8	—	2.3	3.8	mA
	I−		—	−4.3	−5.8	—	−4.3	−5.8	
	I+	$V_S = +5V$, $-15V$, $I_{REF} = 2.0mA$	—	2.4	3.8	—	2.4	3.8	
	I−		—	−6.4	−7.8	—	−6.4	−7.8	
	I+	$V_S = \pm 15V$, $I_{REF} = 2.0mA$	—	2.5	3.8	—	2.5	3.8	
	I−		—	−6.5	−7.8	—	−6.5	−7.8	
Power Dissipation	P_d	±5V, $I_{REF} = 1.0mA$	—	33	48	—	33	48	mW
		+5V, −15V, $I_{REF} = 2.0mA$	—	103	136	—	108	136	
		±15V, $I_{REF} = 2.0mA$	—	135	174	—	135	174	

NOTE: Parameter not 100% tested; guaranteed by design.

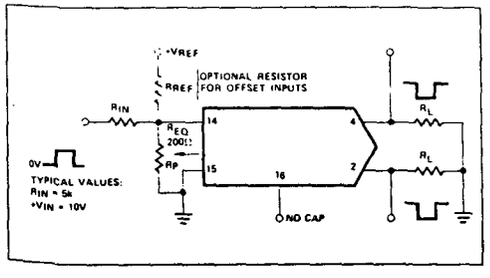
ELECTRICAL CHARACTERISTICS

at $V_S = \pm 15V$, $I_{REF} = 2.0mA$, $T_A = 0°C$ to $+70°C$ unless otherwise noted. Output characteristics refer to both I_{OUT} and $\overline{I_{OUT}}$.

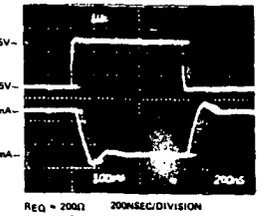
PARAMETER	SYMBOL	CONDITIONS	DAC-08H MIN	DAC-08H TYP	DAC-08H MAX	DAC-08E MIN	DAC-08E TYP	DAC-08E MAX	DAC-08C MIN	DAC-08C TYP	DAC-08C MAX	UNITS
Resolution			8	8	8	8	8	8	8	8	8	Bits
Monotonicity			8	8	8	8	8	8	8	8	8	Bits
Nonlinearity		$T_A = 0°C$ to $70°C$	—	—	±0.1	—	—	±0.19	—	—	±0.39	%FS
Settling Time	t_s	To ±½ LSB, all bits switched ON or OFF, $T_A = 25°C$ (See Note)	—	85	135	—	85	150	—	85	150	ns
Propagation Delay												
Each bit	t_{PLH}	$T_A = 25°C$	—	35	60	—	35	60	—	35	60	ns
All bits switched	t_{PHL}	(See Note)	—	35	60	—	35	60	—	35	60	ns
Full Scale Tempco	TC_{FS}		—	±10	±50	—	±10	±50	—	±10	±80	ppm/°C
Output Voltage Compliance (True Compliance)	V_{OC}	Full scale current change < ½ LSB, R_{OUT} > 20MΩ typical	−10	—	+18	−10	—	+18	−10	—	+18	Volts
Full Range Current	I_{FR4}	$V_{REF} = 10.000V$, R_{14}, $R_{15} = 5.000k\Omega$, $T_A = +25°C$	1.984	1.992	2.000	1.94	1.99	2.04	1.94	1.99	2.04	mA
Full Range Symmetry	I_{FRS}	$I_{FR4} - I_{FR2}$	—	±0.5	±4.0	—	±1.0	±8.0	—	±2.0	±16.0	µA
Zero Scale Current	I_{ZS}		—	0.1	1.0	—	0.2	2.0	—	0.2	4.0	µA
Output Current Range	I_{OR_1}	R_{14}, $R_{15} = 5.000k\Omega$, $V_{REF} = +15.0V$, $V- = -10V$	2.1	—	—	2.1	—	—	2.1	—	—	mA
	I_{OR_2}	$V_{REF} = +25.0V$, $V- = -12V$	4.2	—	—	4.2	—	—	4.2	—	—	
Logic Input Levels												
Logic "0"	V_{IL}	$V_{LC} = 0V$	—	—	0.8	—	—	0.8	—	—	0.8	Volts
Logic Input "1"	V_{IH}		2.0	—	—	2.0	—	—	2.0	—	—	
Logic Input Current		$V_{LC} = 0V$										
Logic "0"	I_{IL}	$V_{IN} = -10V$ to $+0.8V$	—	−2.0	−10	—	−2.0	−10	—	−2.0	−10	µA
Logic Input "1"	I_{IH}	$V_{IN} = 2.0V$ to $18V$	—	0.002	10	—	0.002	10	—	0.002	10	
Logic Input Swing	V_{IS}	$V- = -15V$	−10	—	+18	−10	—	+18	−10	—	+18	Volts
Logic Threshold Range	V_{THR}	$V_S = \pm 15V$	−10	—	+13.5	−10	—	+13.5	−10	—	+13.5	Volts
Reference Bias Current	I_{15}		—	−1.0	−3.0	—	−1.0	−3.0	—	−1.0	−3.0	µA
Reference Input Slew Rate	dI/dt	$R_{EQ} = 200\Omega$, $R_L = 100\Omega$, $C_C = 0pF$ — See fast pulsed ref. into below	4.0	8.0	—	4.0	8.0	—	4.0	8.0	—	mA/µs
Power Supply Sensitivity	$PSSI_{FS+}$	$V+ = 4.5V$ to $18V$, $V- = -4.5V$ to $-18V$, $I_{REF} = 1.0mA$	—	±0.0003	±0.01	—	±0.0003	±0.01	—	±0.0003	±0.01	%/%ΔV+
	$PSSI_{FS-}$		—	±0.002	±0.01	—	±0.002	±0.01	—	±0.002	±0.01	%/%ΔV−
Power Supply Current	I+	$V_S = \pm 5V$, $I_{REF} = 1.0mA$	—	2.3	3.8	—	2.3	3.8	—	2.3	3.8	mA
	I−		—	−4.3	−5.8	—	−4.3	−5.8	—	−4.3	−5.8	
	I+	$V_S = +5V$, $-15V$, $I_{REF} = 2.0mA$	—	2.4	3.8	—	2.4	3.8	—	2.4	3.8	
	I−		—	−6.4	−7.8	—	−6.4	−7.8	—	−6.4	−7.8	
	I+	$V_S = \pm 15V$, $I_{REF} = 2.0mA$	—	2.5	3.8	—	2.5	3.8	—	2.5	3.8	
	I−		—	−6.5	−7.8	—	−6.5	−7.8	—	−6.5	−7.8	
Power Dissipation	P_d	±5V, $I_{REF} = 1.0mA$	—	33	48	—	33	48	—	33	48	mW
		+5V, −5V, $I_{REF} = 2.0mA$	—	108	136	—	108	136	—	108	136	
		±15V, $I_{REF} = 2.0mA$	—	135	174	—	135	174	—	135	174	

NOTE: Parameter not 100% tested; guaranteed by design

PULSED REFERENCE OPERATION



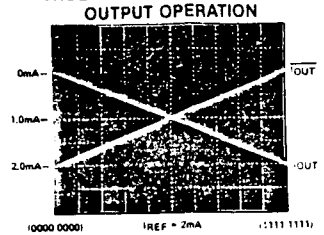
FAST PULSED REFERENCE OPERATION



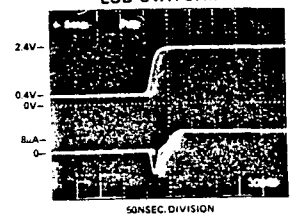
REQ = 200Ω
RL = 100Ω
CC = 0

200NSEC/DIVISION

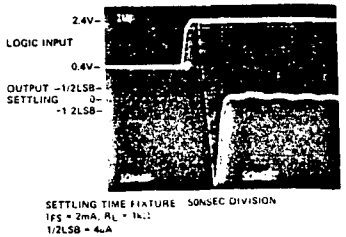
TRUE AND COMPLEMENTARY OUTPUT OPERATION



LSB SWITCHING

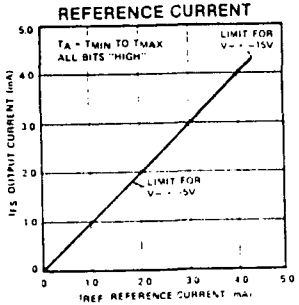


FULL SCALE SETTLING TIME

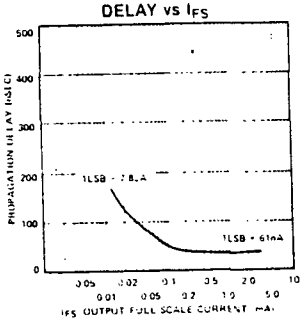


TYPICAL PERFORMANCE CURVES

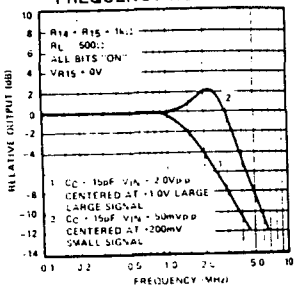
FULL SCALE CURRENT vs REFERENCE CURRENT



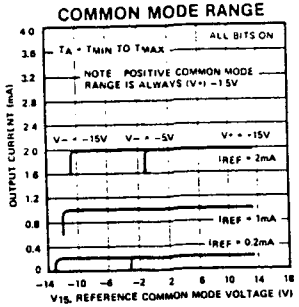
LSB PROPAGATION DELAY vs I_{FS}



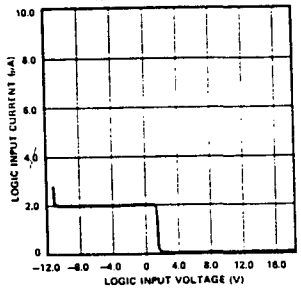
REFERENCE INPUT FREQUENCY RESPONSE



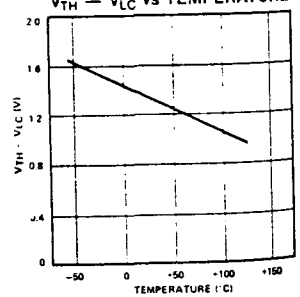
REFERENCE AMP COMMON MODE RANGE



LOGIC INPUT CURRENT vs INPUT VOLTAGE

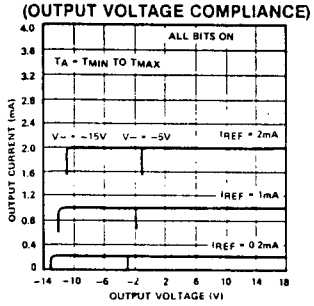


V_{TH} — V_{LC} vs TEMPERATURE

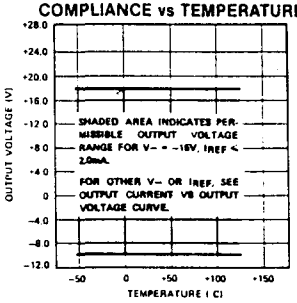


TYPICAL PERFORMANCE CURVES

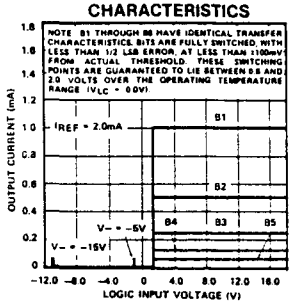
OUTPUT CURRENT vs OUTPUT VOLTAGE (OUTPUT VOLTAGE COMPLIANCE)



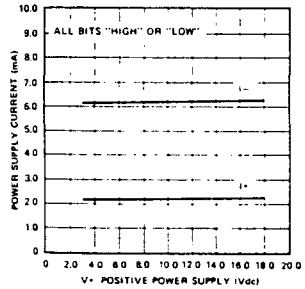
OUTPUT VOLTAGE COMPLIANCE vs TEMPERATURE



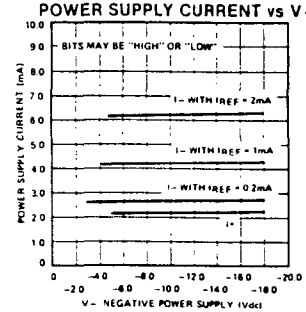
BIT TRANSFER CHARACTERISTICS



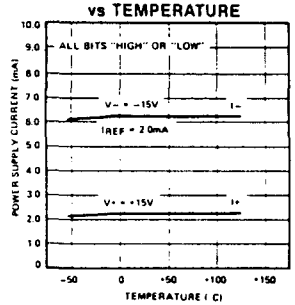
POWER SUPPLY CURRENT vs V+



POWER SUPPLY CURRENT vs V–

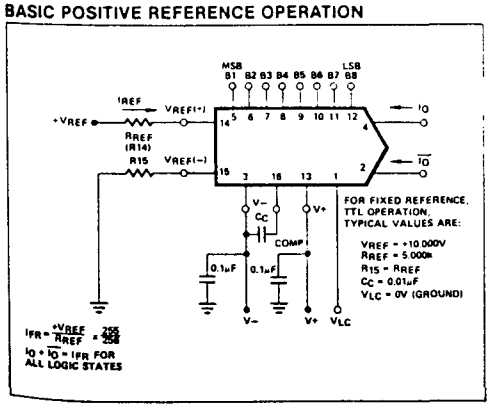


POWER SUPPLY CURRENT vs TEMPERATURE

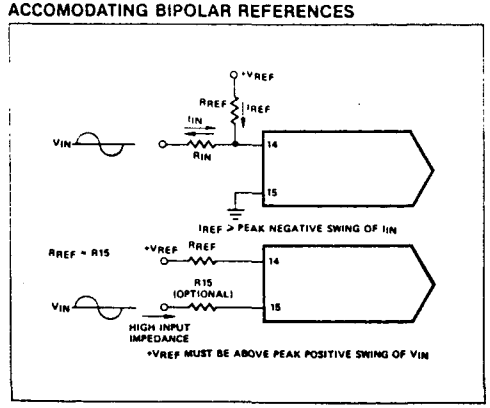


BASIC CONNECTIONS

BASIC POSITIVE REFERENCE OPERATION

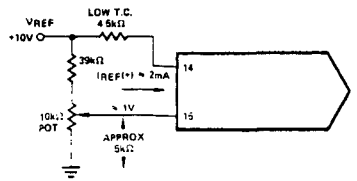


ACCOMODATING BIPOLAR REFERENCES

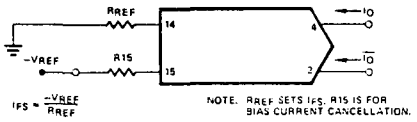


BASIC CONNECTIO

RECOMMENDED FULL SCALE ADJUSTMENT CIRCUIT

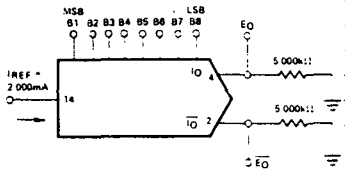


BASIC NEGATIVE REFERENCE OPERATION



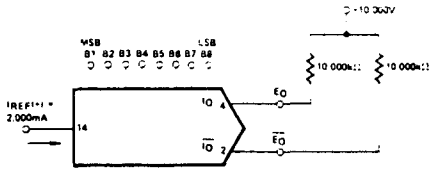
NOTE: RREF SETS IFS. R15 IS FOR BIAS CURRENT CANCELLATION.

BASIC UNIPOLAR NEGATIVE OPERATION



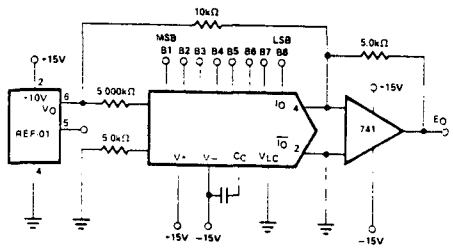
	B1	B2	B3	B4	B5	B6	B7	B8	I_OmA	$I_{\overline{O}}$mA	E_O	$E_{\overline{O}}$
FULL RANGE	1	1	1	1	1	1	1	1	1.992	000	−9.960	− 000
HALF SCALE +LSB	1	0	0	0	0	0	0	1	1.008	984	−5.040	−4.920
HALF SCALE	1	0	0	0	0	0	0	0	1.000	992	−5.000	−4.960
HALF SCALE −LSB	0	1	1	1	1	1	1	1	992	1.000	−4.960	−5.000
ZERO SCALE +LSB	0	0	0	0	0	0	0	1	008	1.984	− 040	−9.920
ZERO SCALE	0	0	0	0	0	0	0	0	000	1.992	000	−9.960

BASIC BIPOLAR OUTPUT OPERATION



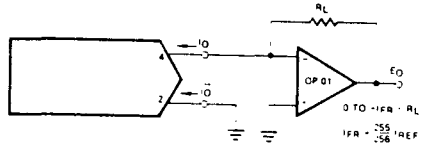
	B1	B2	B3	B4	B5	B6	B7	B8	E_O	$E_{\overline{O}}$
POS FULL RANGE	1	1	1	1	1	1	1	1	+9.920	+10.000
POS FULL RANGE −LSB	1	1	1	1	1	1	1	0	+9.840	+ 9.920
ZERO SCALE +LSB	1	0	0	0	0	0	0	1	−0.080	+ 0.160
ZERO SCALE	1	0	0	0	0	0	0	0	0.000	− 0.080
ZERO SCALE −LSB	0	1	1	1	1	1	1	1	+0.080	0.000
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	−9.920	− 9.840
NEG FULL SCALE	0	0	0	0	0	0	0	0	+10.000	− 9.920

OFFSET BINARY OPERATION



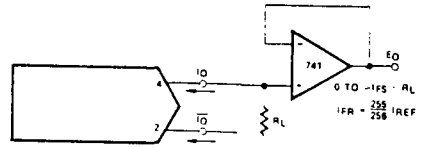
	B1	B2	B3	B4	B5	B6	B7	B8	E_O
POS FULL RANGE	1	1	1	1	1	1	1	1	+4.960
ZERO SCALE	1	0	0	0	0	0	0	0	0.00
NEG FULL SCALE +1 LSB	0	0	0	0	0	0	0	1	−4.960
NEG FULL SCALE	0	0	0	0	0	0	0	0	−5.000

POSITIVE LOW IMPEDANCE OUTPUT OPERATION



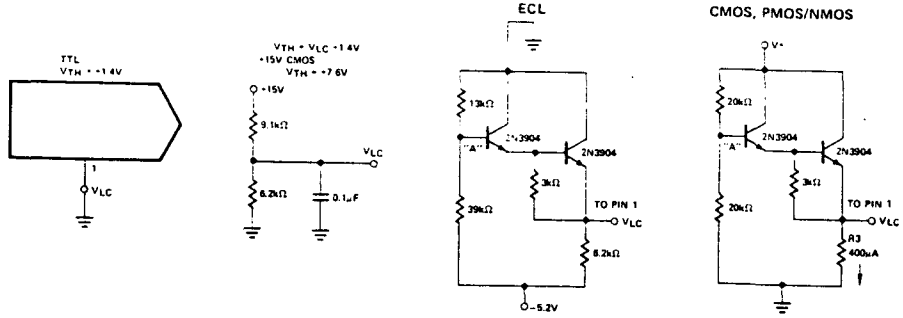
FOR COMPLEMENTARY OUTPUT OPERATION AS A NEGATIVE LOGIC DAC CONNECT INVERTING INPUT OF OP AMP TO $\overline{IO}$ PIN 2; CONNECT IO PIN 4 TO GROUND

NEGATIVE LOW IMPEDANCE OUTPUT OPERATION



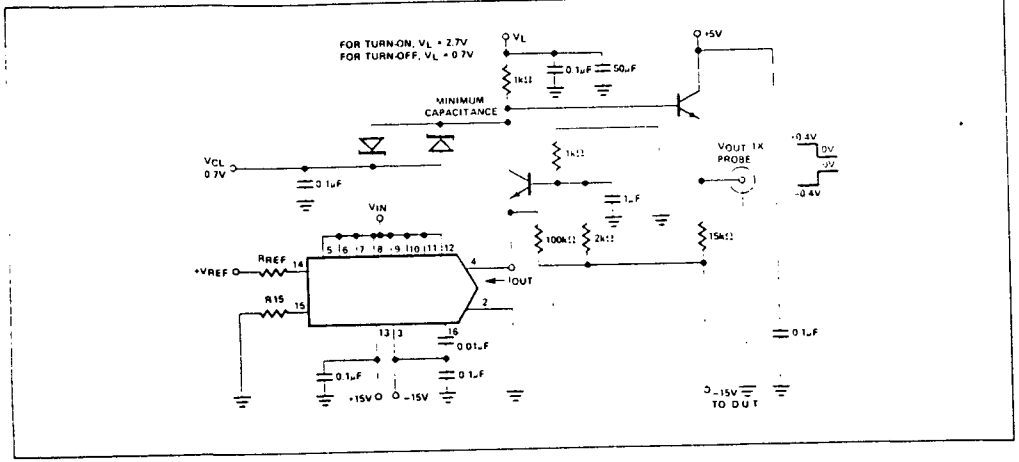
FOR COMPLEMENTARY OUTPUT OPERATION AS A NEGATIVE LOGIC DAC CONNECT NON-INVERTING INPUT OF OP AMP TO IO PIN 2; CONNECT IO PIN 4 TO GROUND

INTERFACING WITH VARIOUS LOGIC FAMILIES



TEMPERATURE COMPENSATING VLC CIRCUITS

SETTLING TIME MEASUREMENT



APPLICATIONS INFORMATION

REFERENCE AMPLIFIER SETUP

The DAC-08 is a multiplying D/A converter in which the output current is the product of a digital number and the input reference current. The reference current may be fixed or may vary from nearly zero to +4.0mA. The full scale output current is a linear function of the reference current and is given by:

$$I_{FS} = \frac{255}{256} \times I_{REF} \text{ where } I_{REF} = I_{14}.$$

In positive reference applications, an external positive reference voltage forces current through R_{14} into the $V_{REF(+)}$ terminal (pin 14) of the reference amplifier. Alternatively, a negative reference may be applied to $V_{REF(-)}$ at pin 15; reference current flows from ground through R_{14} into $V_{REF(+)}$ as in the positive reference case. This negative reference connection has the advantage of a very high impedance presented at pin 15. The voltage at pin 14 is equal to and tracks the voltage at pin 15 due to the high gain of the internal reference amplifier. R_{15} (nominally equal to R_{14}) is used to cancel bias current errors; R_{15} may be eliminated with only a minor increase in error.

Bipolar references may be accomodated by offsetting V_{REF} or pin 15. The negative common mode range of the reference amplifier is given by: $V_{CM-} = V- \text{ plus } (I_{REF} \times 1k\Omega)$ plus 2.5V. The positive common mode range is V+ less 1.5V.

When a DC reference is used, a reference bypass capacitor is recommended. A 5.0V TTL logic supply is not recommended as a reference. If a regulated power supply is used as a reference, R_{14} should be split into two resistors with the junction bypassed to ground with a 0.1μF capacitor.

For most applications the tight relationship between I_{REF} and I_{FS} will eliminate the need for trimming I_{REF}. If required, full scale trimming may be accomplished by adjusting the value of R_{14}, or by using a potentiometer for R_{14}. An improved method of full scale trimming which eliminates potentiometer T.C. effects is shown in the recommended full scale adjustment circuit.

Using lower values of reference current reduces negative power supply current and increases reference amplifier negative common mode range. The recommended range for operation with a DC reference current is +0.2mA to +4.0mA.

The reference amplifier must be compensated by using a capacitor from pin 16 to V−. For fixed reference operation, a 0.01μF capacitor is recommended. For variable reference applications, see section entitled "Reference Amplifer Compensation for Multiplying Applications".

MULTIPLYING OPERATION

The DAC-08 provides excellent multiplying performance with an extremely linear relationship between I_{FS} and I_{REF} over a range of 4mA to 4μA. Monotonic operation is maintained over a typical range of I_{REF} from 100μA to 4.0mA.

REFERENCE AMPLIFIER COMPENSATION FOR MULTIPLYING APPLICATIONS

AC reference applications will require the reference amplifer to be compensated using a capacitor from pin 16 to V−. The value of this capacitor depends on the the impedance presented to pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

For fastest response to a pulse, low values of R_{14} enabling small C_C values should be used. If pin 14 is driven by a high impedance such as a transistor current source, none of the above values will suffice and the amplifier must be heavily compensated which will decrease overall bandwidth and slew rate. For $R_{14} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns.

Operation with pulse inputs to the reference amplifier may be accomodated by an alternate compensation scheme. This technique provides lowest full scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. Full scale transition (0 to 2mA) occurs in 120ns when the equivalent impedance at pin 14 is 200Ω and $C_C = 0$. This yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

LOGIC INPUTS

The DAC-08 design incorporates a unique logic input circuit which enables direct interface to all popular logic families and provides maximum noise immunity. This feature is made possible by the large input swing capability, 2μA logic input current and completely adjustable logic threshold voltage. For V− = −15V, the logic inputs may swing between −10V and +18V. This enables direct interface with +15V CMOS logic, even when the DAC-08 is powered from a +5V supply. Minimum input logic swing and minimum logic threshold voltage are given by: V− plus ($I_{REF} \times 1k\Omega$) plus 2.5V. The logic threshold may be adjusted over a wide range by placing an appropriate voltage at the logic threshold control pin (pin 1, V_{LC}). The appropriate graph shows the relationship between V_{LC} and V_{TH} over the temperature range, with V_{TH} nominally 1.4 above V_{LC}. For TTL and DTL interface, simply ground pin 1. When interfacing ECL, an $I_{REF} = 1mA$ is recommended. For interfacing other logic families, see previous page. For general setup of the logic control circuit, it should be noted that pin 1 will source 100μA typical; external circuitry should be designed to accomodate this current.

Fastest settling times are obtained when pin 1 sees a low impedance. If pin 1 is connected to a 1kΩ divider, for example, it should be bypassed to ground by a 0.01μF capacitor.

ANALOG OUTPUT CURRENTS

Both true and complemented output sink currents are provided where $I_O + \overline{I_O} = I_{FS}$. Current appears at the "true" output when a "1" is applied to each logic input. As the binary count increases, the sink current at pin 4 increases proportionally, in the fashion of a "positive logic" D/A converter. When a "0" is applied to any input bit, that current is turned off at pin 4 and turned on at pin 2. A decreasing logic count increases I_O as in a negative or inverted logic D/A converter. Both outputs may be used simultaneously. If one of the outputs is not required it must still be connected to ground or to a point capable of sourcing I_{FS}; do not leave an unused output pin open.

Both outputs have an extremely wide voltage compliance enabling fast direct current-to-voltage conversion through a resistor tied to ground or other voltage source. Positive compliance is 36V above V− and is independent of the positive supply. Negative compliance is given by V− plus ($I_{REF} \times 1k\Omega$) plus 2.5V.

The dual outputs enable double the usual peak-to-peak load swing when driving loads in quasi-differential fashion. This feature is especially useful in cable driving, CRT deflection and in other balanced applications such as driving center-tapped coils and transformers.

POWER SUPPLIES

The DAC-08 operates over a wide range of power supply voltages from a total supply of 9V to 36V. When operating at supplies of ±5V or less, $I_{REF} \leq 1mA$ is recommended. Low *reference current operation decreases power consumption* and increases negative compliance, reference amplifer negative common mode range, negative logic input range, and negative logic threshold range; consult the various figures for guidance. For example, operation at −4.5V with $I_{REF} = 2mA$ is not recommended because negative output compliance would be reduced to near zero. Operation from lower supplies is possible, however at least 8V total must be aplied to insure turn-on of the internal bias network.

Symetrical supplies are not required, as the DAC-08 is quite insensitive to variations in supply voltage. Battery operation is feasible as no ground connection is required; however, an artificial ground may be used to insure logic swings, etc. remain between acceptable limits.

Power consumption may be calculated as follows:

$P_d = (I+)(V+) + (I+)(V-) + (2\ I_{REF})(V-)$. A useful feature of the DAC-08 design is that supply current is constant and independent of input logic states; this is useful in cryptographic applications and further serves to reduce the size of the power supply bypass capacitors.

TEMPERATURE PERFORMANCE

The nonlinearity and monotonicity specifications of the DAC-08 are guaranteed to apply over the entire rated operating temperature range. Full scale output current drift is tight, typically ±10ppm/°C, with zero scale output current and drift essentially negligible compared to 1/2 LSB.

The temperature coefficient of the reference resistor R_{14} should match and track that of the output resistor for minimum overall full scale drift. Settling times of the DAC-08 decrease approximately 10% at −55°C; at +125°C an increase of about 15% is typical.

One benefit is not immediately apparent and deserves special mention. In all of these applications, the digital input words can be CMOS, TTL, DTL, NMOS, or MECL, because the DAC-08 interfaces with all of those logic families. In fact, the two input words may even be from different logic families to eliminate special level translators or interface circuitry. (See AN-17 "DAC-08 Applications Collection.")

The first arithmetic application is shown in Figure 17. Two DAC-08s perform a fast algebraic summation with a direct analog output. The circuit works by paralleling the outputs of two DAC-08s and summing their currents while driving a balanced load. The output is the algebraic sum of word "A" and word "B" in all four quadrants.

FOUR-QUADRANT DIGITAL MULTIPLICATION

High-speed multiplication of two 8-bit digital words with an analog output usually requires several logic packages and a D/A converter. The circuit in Figure 18 performs this function using only three ICs.

In Figure 18 DAC-08 number 1 and number 2 are connected as previously shown, and DAC-08 number 3 provides the analog reference inputs to DAC-08 number 1 and number 2. Those reference inputs are determined by digital input word "A." The circuit's output, I_{01}-I_{02}, is a differential current output which may be used to drive a balanced load.

Four-quadrant multiplication is thus performed by adding one more DAC-08 to the basic four-quadrant multiplying connection.

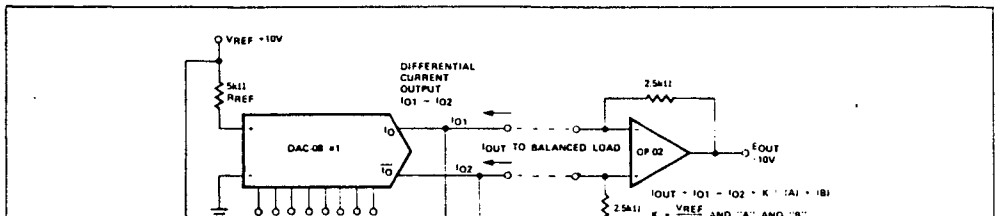


Figure 17. Four-Quadrant Algebraic Digital Computation

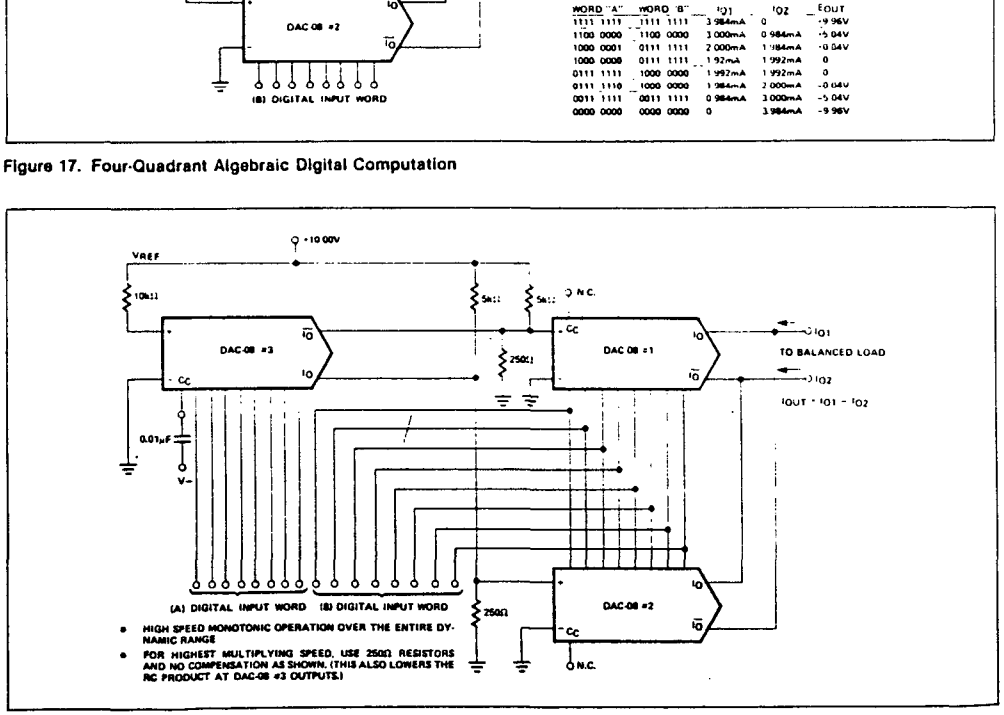


Figure 18. Four-Quadrant 8-Bit × 8-Bit Digital Multiplier

APPLICATION NOTE 20

EXPONENTIAL DIGITALLY CONTROLLED OSCILLATOR USING DAC-76

By Donn Soderquist

Here is a 4-IC, microprocessor-controlled oscillator with a 8159 to 1 frequency range covering 2.5Hz to 20kHz. An exponential, current output IC DAC functioning as a programmable current source alternately charges and discharges a capacitor between precisely-controlled upper and lower limits. This circuit features instantaneous frequency change, operates with +5V ±1V and −15V ±3V supplies, and provides monotonic frequency changes over a 78dB range — the dynamic range of a 13-bit DAC.

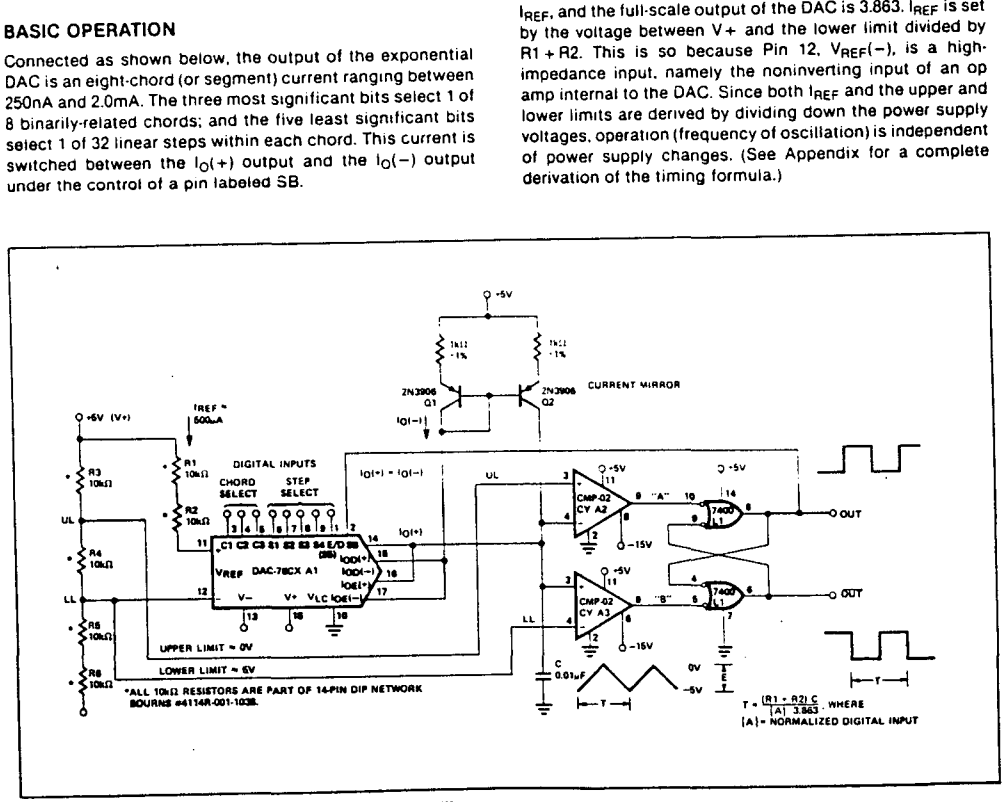
BASIC OPERATION

Connected as shown below, the output of the exponential DAC is an eight-chord (or segment) current ranging between 250nA and 2.0mA. The three most significant bits select 1 of 8 binarily-related chords; and the five least significant bits select 1 of 32 linear steps within each chord. This current is switched between the $I_O(+)$ output and the $I_O(-)$ output under the control of a pin labeled SB.

When SB is low, $I_O(-)$ is selected, and the DAC's output current drives a current mirror which ramps the timing capacitor in a positive direction until an upper limit of 0V is sensed by A2. At this time the set-resist flip-flop (L1) is set, SB becomes a "1", and the DAC's output current is switched to the $I_O(+)$ output. Now the capacitor is charged to a lower limit of −5V, the flip-flop is reset, and the cycle repeats itself.

REFERENCE SETUP

The multiplying relationship between the reference current, I_{REF}, and the full-scale output of the DAC is 3.863. I_{REF} is set by the voltage between V+ and the lower limit divided by R1 + R2. This is so because Pin 12, $V_{REF}(-)$, is a high-impedance input, namely the noninverting input of an op amp internal to the DAC. Since both I_{REF} and the upper and lower limits are derived by dividing down the power supply voltages, operation (frequency of oscillation) is independent of power supply changes. (See Appendix for a complete derivation of the timing formula.)



Circuit Diagram Exponential Digitally-Controlled Oscillator

current compensation for the DAC reference amplifier is accomplished by R4.

Figures 1b, 1c, and 1d show dynamic performance of circuit 1a when the digital inputs are swept by an external BCD up-counter with codes of 0000 0001 through 1001 1001 (division by zero is not allowed).

THEORY OF OPERATION (—A/X)

The circuit configuration for the —A/X function is shown in Figure 2a. It is quite similar to that of Figure 1a with both the DAC reference amplifier and output amplifier terminals reversed. Capacitors C1 and C2 provide phase compensation. Figures 2b, 2c, and 2d show dynamic performance of circuit 2a.

DESIGN CONSIDERATIONS

1. Circuit speed and settling time are dictated by output op amp slew rate, scale factor, and compensation. Use of slower amplifiers considerably increases the illustrated settling times. Effective slew rate of circuit 1a is 3V/μs, while circuit 2a slews 0.6V/μs.
2. Layout and breadboarding of high gain, wide-bandwidth devices necessitates considerable care with a ground plane with single point grounding being highly desirable. Decoupling capacitors located close to the devices' supply inputs are essential.
3. Accuracy of the circuit is within 1% over the 0°C to +70°C temperature range with 1% metal film resistors R1, R2 and R3. DAC linearity becomes an important factor as the divisor decreases; for this reason 1/4 LSB linear DAC's are recommended
4. Binary coding may be accomplished by substituting an 8-bit binary-coded DAC-08EX for the two-digit BCD-coded DAC-20EX. In addition to adjusting circuit values however, a higher performance op amp such as the OP-17F is desirable because the output amplifier's input offset voltage drift becomes a more significant error source for overall scale factor stability over temperature. This is due to the increased resolution of the binary coding.

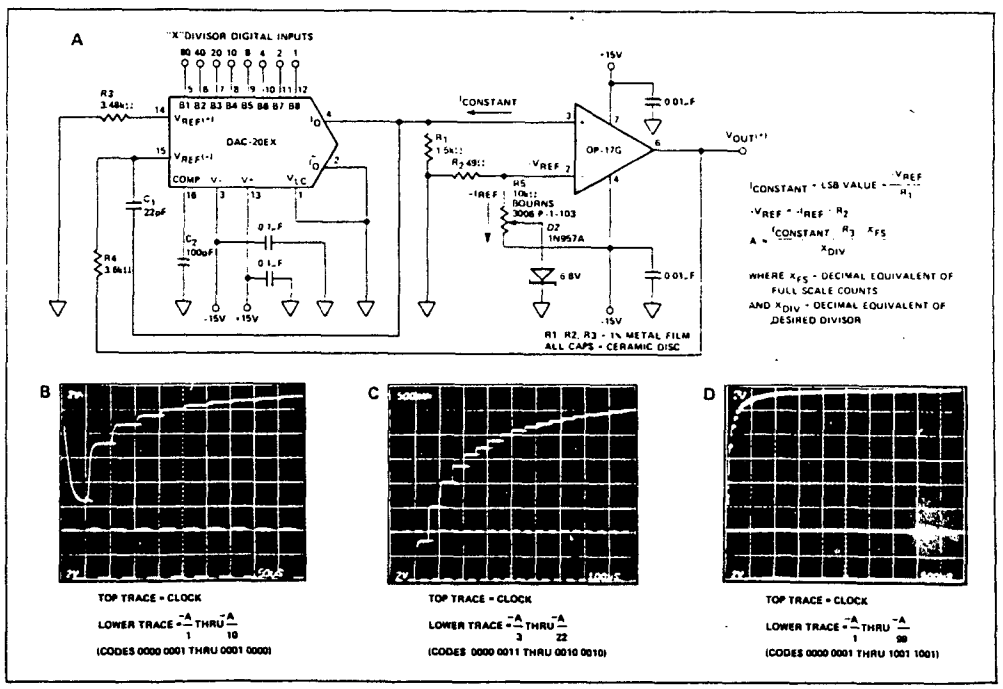


Figure 2. —A/X Function Generator

APPLICATION NOTE 24

THE OP-17, OP-16, OP-15 AS OUTPUT AMPLIFIERS FOR HIGH SPEED D/A CONVERTERS

by George Erdi

This application note shows how to make high speed, voltage output D/A converters using the DAC-08 and OP-15/16/17 precision BIFET op amps. Designs are optimized for highest speed (OP-17), lowest drift (OP-16) and for lowest power (OP-15). Although the DAC-08 is used as an example, the same configurations work with DAC-20 and DAC-76.

Converting the current output of a fast IC DAC to a voltage while maintaining fast settling time is difficult. The full scale current of the DAC-08 settles in 85ns. It can be terminated with a load resistance, as shown in Figure 1, to give a 10V output. However, in this configuration the settling time will be dominated by the RC time constant of R_1 and the DAC-08's output capacitance ($T = R_1C_0 = 5k\Omega \times 15pF = 75ns$). It requires 6.2 time constants to settle within 0.2% of full scale (1/2 least significant bit of an 8-bit converter). Therefore, the settling time is 500ns including the DAC-08's 35ns propagation delay

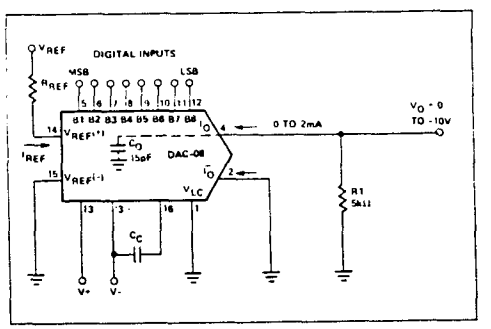


Figure 1. DAC-08 with Resistive Termination Settling Time = 500ns for 0 to -10V

Due to this RC time constant, current-to-voltage conversion is usually accomplished with a transimpedance amplifier as shown in Figure 2. The output's response is now limited by the amplifier's slew rate and settling time. However, an additional pole is introduced at $\frac{1}{2\pi R2C1}$, where C1 is the sum of the DAC's output capacitance and the op amp's input capacitance. The frequency of this pole is likely to be at an inopportune location for fast amplifiers, creating an underdamped response or even oscillation.

The circuit of Figure 3 resolves this problem. It can be shown that if R1C1 = R2C2, the effect of the two capacitors is

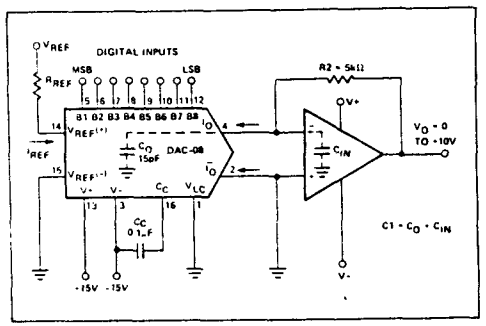


Figure 2. Voltage Output DAC with Transimpedance Amplifier

completely cancelled, and the overall settling will be determined by the amplifier's behavior only. In addition, C2 can be varied to fine tune the system's response and minimize settling time to compensate for the op amp's possibly underdamped or overdamped characteristics. The disadvantage of this circuit compared to that of Figure 2 is that all input errors, and in particular input offset voltage (V_{OS}), are amplified by the factor $(1 + \frac{R2}{R1})$.

The optimum speed is obtained — at low cost — by using the OP-17, fast, precision, BIFET-input op amp, stable only at closed-loop gains of five or more. Therefore, the R2/R1 ratio

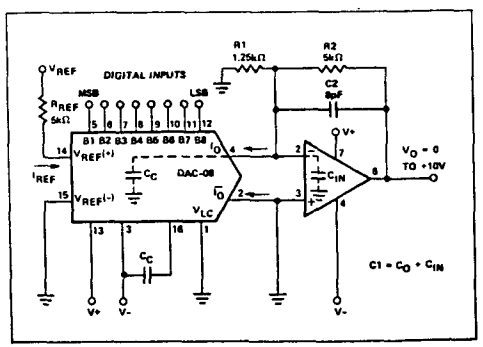


Figure 3. Voltage Output DAC with Response Shaping

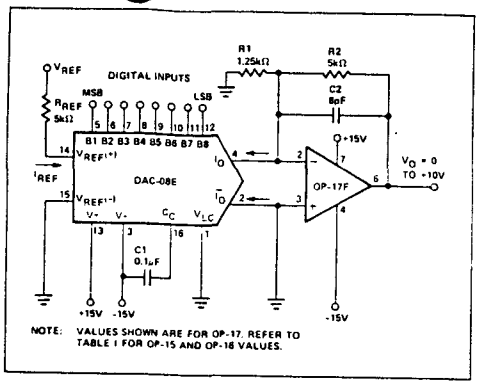


Figure 4. 0 to -10V Connection, Settling Time = 380ns

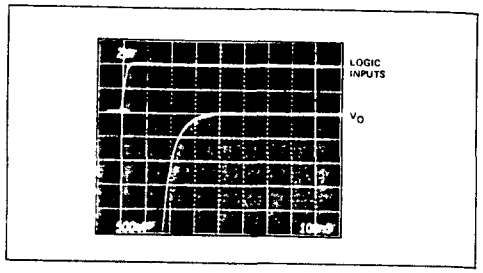


Figure 5. Settling Time of Figure 4 Circuit Using OP-17

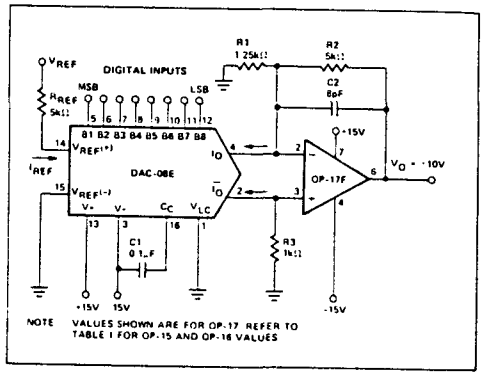


Figure 6. ±10V Connection, Settling Time = 450ns

is set at four (Figure 4). Settling time to 0.2% is 380ns with all bits turning ON (0 to 10V), or all bits turning OFF (10V to 0). The last 2.5 volts of the rising waveform are shown in the photograph of Figure 5. The three grades of the OP-17 are specified at V_{OS} = 0.5mV maximum (OP-17E), 1.0mV maximum (OP-17F), and 3.0mV maximum (OP-17G). Even though V_{OS} is multiplied five times its effect is still less than 0.2% or 20mV. The OP-17E's contribution will be only 1/4 LSB even on a 10-bit system. The offset voltage can also be trimmed to zero, then the TCV_{OS}, at 2 to 4μV/°C, typically, will be the limiting factor. The complementary output of the DAC-08 can be used for a -10V to +10V system as depicted in Figure 6. Settling time is only slightly increased because of the time required to slew the additional ten volts. Since 1/2 LSB is now 40mV, the non-slew portion is decreased by 70ns.

The OP-16 is slower than the OP-17 but it is stable in unity gain. Therefore, improved output-referred error can be traded off for increased settling time. The OP-15 is a lower power dissipation model, but again this improvement is obtained at the expense of settling time. Table 1 summarizes the resistor and capacitor values for the various amplifiers in the circuits of Figure 4 and Figure 6, the settling times obtained in these circuits, and the output-referred offset errors.

Table 1. OP-17/16/15 Performance as Output Op Amp for DAC-08

	OP-17		OP-16		OP-15	
	0 to 10V Figure 4	-10 to +10V Figure 6	0 to 10V Figure 4	-10 to +10V Figure 6	0 to 10V Figure 4	-10 to +10V Figure 6
R_1	1.25kΩ	1.25kΩ	10kΩ	10kΩ	10kΩ	10kΩ
R_2	5kΩ	5kΩ	5kΩ	5kΩ	5kΩ	5kΩ
R_3	—	1kΩ	—	3.3kΩ	—	3.3kΩ
C_2	8pF	8pF	25pF	40pF	30pF	50pF
Settling time to ±0.2%	380ns	450ns	750ns	1100ns	900ns	1350ns
Slew Time	150ns	290ns	400ns	800ns	590ns	1170ns
1/2 LSB = 0.2%	20mV	40mV	20mV	40mV	20mV	40mV
Closed Loop Gain	5	5	1.5	1.5	1.5	1.5
Offset Error at Output						
E Grade Maximum	2.5mV	2.5mV	0.75mV	0.75mV	0.75mV	0.75mV
F Grade Maximum	5.0mV	5.0mV	1.5mV	1.5mV	1.5mV	1.5mV
G Grade Maximum	15.0mV	15.0mV	4.5mV	4.5mV	4.5mV	4.5mV
Supply Current Maximum	7mA	7mA	7mA	7mA	4mA	4mA

APPLICATION NOTE 25

THE OP-06 OP AMP AS A LOW-LEVEL COMPARATOR

By Shelby D. Givens

INTRODUCTION

The Precision Monolithics OP06 op amp makes an excellent comparator. In fact, for submillivolt signals, there is simply no comparator that performs as well. Using an external nulling potentiometer, the offset drift is typically 0.6μV/°C. With its high open loop gain of 1 million, only 30μV is required at the input to drive the output from one saturation level to the other. A 50°C change in temperature produces a 30μV change in V_{OS}; thus a *total* error band of 100μV *including temperature effects* is quite conservative. This performance is an order of magnitude better than other comparators. 100μV sensitivity is nice to have in 12-bit A/D converters, but it is essential in 14-bit converters. Where preamplifiers are typically needed with thermocouples and strain gauges, the OP06's sensitivity allows *direct* comparison of these low-level outputs. As a result system costs decrease, and reliability increases.

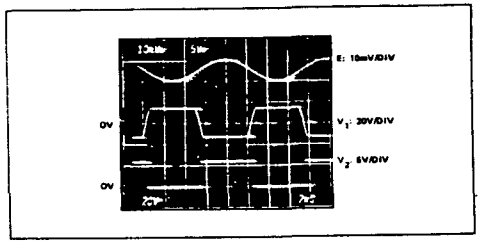


Figure 1. 100μV P-P Sine Wave Response (R_S: 100Ω)

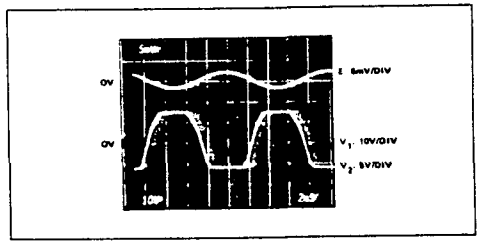
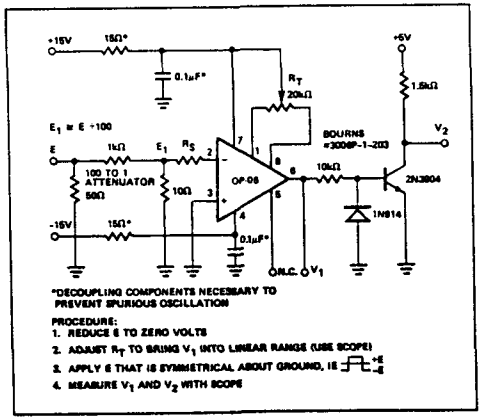


Figure 2. 40μV P-P Sine Wave Response (R_S: 100Ω)

LOW-LEVEL PERFORMANCE MEASUREMENTS

The low-level capabilities of the OP06 comparator are graphically illustrated in Figures 1 and 2 using the test circuit below. Comparator voltage input, applied through a 100 to 1 attenuator, is $100\mu V_{p\text{-}p}$ in Figure 1 and $40\mu V_{p\text{-}p}$ in Figure 2. Note that the op amp output still reaches both positive and negative saturation.

TEST CIRCUIT



COMPARATOR RESPONSE TIME

While most comparators are specified for 2mV to 5mV overdrive, the OP06 operates very reliably with only 0.5mV overdrive. Figures 3 and 4 show the response times for both positive going and negative going inputs with 500μV and 5mV overdrives as measured at the logic output.

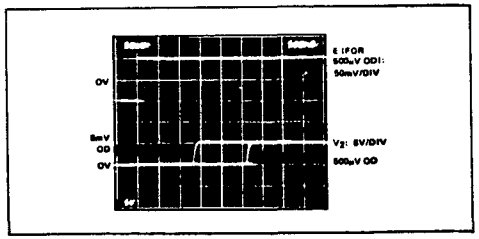


Figure 3. Positive Going Response Time (5mV and 500μV Overdrives)

demultiplexer, which will have its own break-before-make delay. An analog to digital system will have a sample/hold amplifier in front of the A/D converter. Since the equations which apply to these situations are different, they will be discussed separately. Figure 15 summarizes the conditions and the equations which apply to them.

Since there is no held voltage, then $N_H = 0$ in the multiplexer-demultiplexer system. This reduces N_O to the simple form shown in equation (1). S_1 and S_2 follow in equations (2) and (3). Since $t_1 = T_D$ (break-before-make time of the DEMUX), that time will have a significant effect on ACCT. The MUX-sample/hold system imposes the condition $S_1 = S_2 = P_2 = 0$; thus $N_O = N_H$. It will be instructive to compare the levels of ACCT in these two systems versus their appropriate times.

Figure 16 looks at a "typical" system which will give approximately one percent transmission error (33kΩ R_L and 300Ω R_{ON}), and has 50pF C_L. The value of C_L is somewhat on the high side (20pF being typical for MUX-08 connected to a buffer amp), but it does give a conservative value for analysis. What Figure 16 shows is rather startling. The adjacent channel crosstalk, while inherent in the multiplexer itself, can be eliminated in **both** systems by the proper timing. In the case of the sample/hold it is only necessary to delay the hold command for approximately 1.2μsec to have the ACCT vanish completely. This is no problem, since most sample/holds need at least 2.5sec to accurately acquire the signal (this is particularly true of monolithic devices). The plot for the MUX-DEMUX system relates to T_D, which is **not adjustable** for a given DEMUX. What is possible is to add some delay to the address change for the DEMUX. In this way, the DEMUX will not "look" at the MUX output until the charge from the previous channel has had a chance to dissipate.

CONCLUSION

Table II summarizes the forms of crosstalk and lists ways of coping with them. Reduction of R_{ON} is helpful in all three cases. While T_{BRK} should be minimized as much as possible, it is important that no two channels are ON at the same time. In some cases, T_{BRK} is chosen such that even over temperature extremes, the break-before-make feature is maintained. Since all three components of crosstalk are present in a dynamic multiplexer, the "careful circuit board layout" is important even though it is not listed in the ACCT section.

Table 2. How to Handle Crosstalk

Crosstalk Component	Variation with f_{SIG}	Ways to Minimize Effects
Static	6dB/octave	• Minimize R_{ON} • Reduce stray capacitance (C_{EQ}) by careful circuit board layout.
Dynamic	6dB/octave	• Minimize R_{ON} • Minimize f_{CLK} • Minimize T_{BRK}, but $T_{BRK} > 0$ is needed to prevent shorting channels together. • Minimize R_L • Reduce stray capacitance (C_{EQ}) by careful circuit board layout.
Adjacent Channel	NONE	• Minimize R_{ON} • Minimize f_{CLK} • Minimize T_{BRK}, but $T_{BRK} > 0$ is needed to prevent shorting channels together. • Minimize R_L and C_L • WAIT before allowing sample/hold or DEMUX to measure MUX output.

This paper has pointed out the fact that static crosstalk (given on multiplexer data sheets) is only **one** of the **three** components of crosstalk. The models for static and dynamic crosstalk are relatively simple and were discussed to show how they are related. The most troublesome component of crosstalk (adjacent channel crosstalk) was shown not to be quite so straight-forward. For one thing, adjacent channel crosstalk (ACCT) is **not signal frequency dependent** as are CT and DCT. The mechanism which governs this form of crosstalk is stored charge on the MUX node. While CT and DCT must be minimized by careful layout and once present in the multiplexer cannot be reduced, such is not the case with ACCT. Even though ACCT is present in the multiplexer, the proper timing of demultiplexer or sample/hold commands can effectively eliminate ACCT from the total system.

APPLICATION NOTE 36

DAC-08 CONTROL OF 555 TIMERS

by Kishor Patel

INTRODUCTION

This application note describes a digitally or microprocessor controlled one-shot and an astable multivibrator using two of the industry's most widely used low cost building blocks, the PMI DAC-08 8 bit DAC and the 555 timer. Digital control ranges of 255 to 1 and 510 to 1 are shown for one-shot and astable applications allowing periods of 18μsec to 1.4 seconds and frequencies of 1 Hz to 60 KHz.

ONE-SHOT LINEAR MODE OPERATION

In the one-shot mode of operation, the time delay or the one-shot period is determined by a constant current source and a capacitor. A digitally programmable constant current source is made using the DAC-08 and two PNP transistors. The DAC-08 is a current sink; the two PNP transistors are used as a current mirror which reverses the direction of the DAC's sink current forming a current source. The current source charges the timing capacitor, causing the voltage across the capacitor to increase linearly at the rate of $\left\{\frac{I_{OUT}}{C}\right\}$ volts per second from approximately zero volts to $\frac{2}{3} V_{CC}$ of the 555 timer.

The one-shot's period, T, is basically an RC product with two other control factors. The R is fixed and represented by R_{REF} which sets up the correct I_{REF} current for the DAC. With the fixed R_{REF}, the one-shot period is directly proportional to the value of the timing capacitor C (see Table 1). The other two controlling factors are the DAC's digital inputs and the ratio of the timer's V_{CC} to the DAC's V_{REF}. The one-shot period is inversely proportional to the normalized digital input value and directly proportional to the V_{CC} to V_{REF} ratio as illustrated in Fig. 2. When operated in the linear mode, a 255 to 1 control range of the one-shot's period is achieved.

BASIC DESIGN

As shown in Fig. 1, this design involves a series of conversions from a digital input to an analog current to a threshold voltage and finally to a time delay or a frequency. A DAC-08 converts the digital input to an analog current

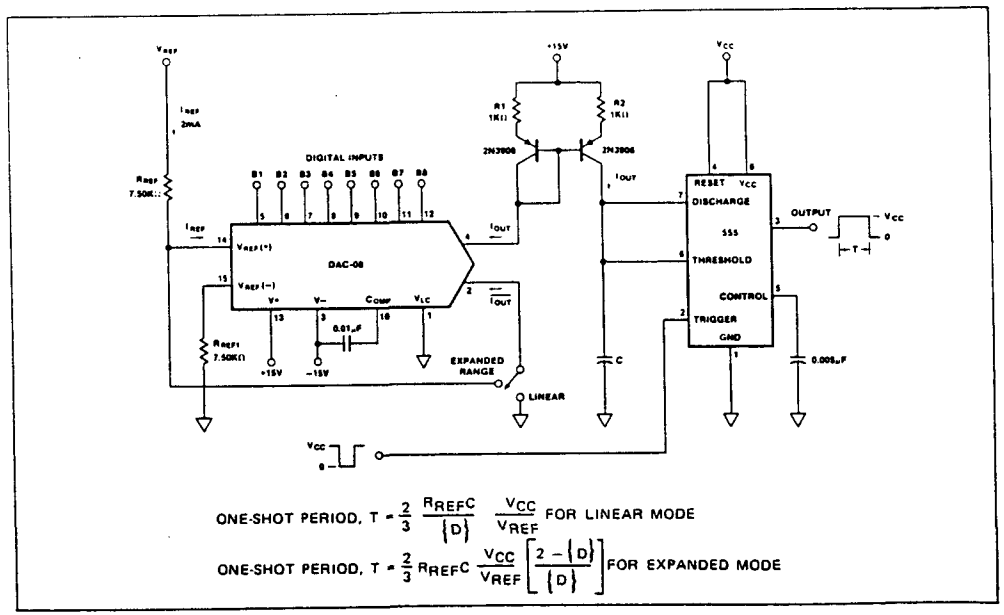


Figure 1. Digitally Controlled One-Shot

Table 1. One-Shot Linear Mode Timing Table

	ONE-SHOT PERIOD (msec)					
	V_{CC} = 15V V_{REF} = 15V			V_{CC} = 5V V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
11 11 11 11	5.2	0.505	0.049	1.72	0.160	0.0176
00 00 00 01	1440	134	13.8	455	43	4.8

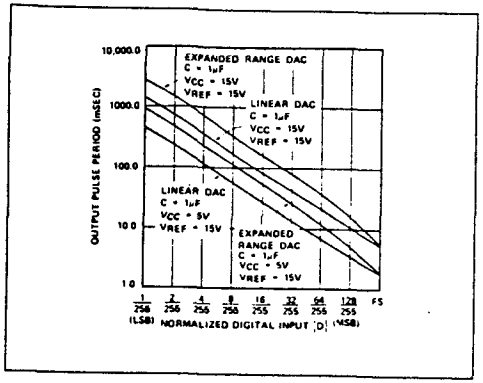


Figure 2. One-Shot Period vs Digital Input

which is then converted to a voltage by a two transistor current source and a capacitor. The voltage is then converted to a time delay or frequency by a timing capacitor and the 555 timer.

ONE-SHOT EXPANDED MODE OPERATION

Range is doubled to 510 to 1 by operating the DAC in the expanded range mode with the DAC's I_{OUT} fed forward from the reference input node of the DAC. Expanded range mode timing is shown in Table 2 and in the graph of Fig. 2.

ASTABLE MODE OPERATION

An astable multivibrator is made in a similar fashion in Fig. 3. A DAC-08 and two PNP's form a current source driving the timing capacitor (C) and a discharge resistor (R_B). The timing capacitor is charged linearly by the current source and discharged exponentially through R_B. Once again, the

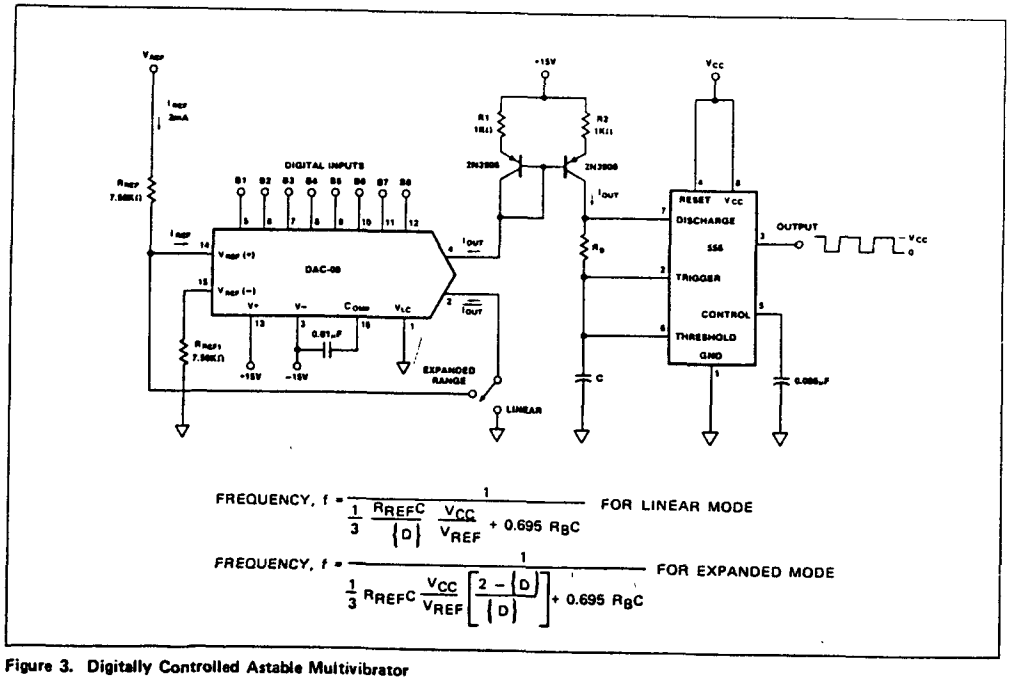


Figure 3. Digitally Controlled Astable Multivibrator

digital DAC input and the ratio of the timer V_{CC} to the DAC's V_{REF} provide additional control on the multivibrator's frequency. The digital input has directly proportional control while the V_{CC} to V_{REF} ratio has an inversely proportional control of frequency.

Frequency range is not fully 255 to 1 as expected but approximately 220 to 1, because the discharge time (output low) of a cycle is invariable for any digital input being determined by the product of R_B and C. Frequency is shown in Table 3 and in Fig. 4. Expanded range operation doubles frequency range as it did in the one-shot application. Frequency is shown in Table 4.

MICROPROCESSOR CONTROL

Both the one-shot and the astable multivibrator can be microprocessor controlled. Fig. 5 shows the implementation of a microprocessor controlled one-shot. The eight bit latch (74LS377) is used to interface between the data bus and the DAC. Stable data is latched in by a positive going edge of an address coincident pulse. After the data is latched, a buffered negative going address coincident pulse can be used to trigger the one-shot. The astable multivibrator is implimented similarly except for elimination of the buffer and the trigger pulses which are not required.

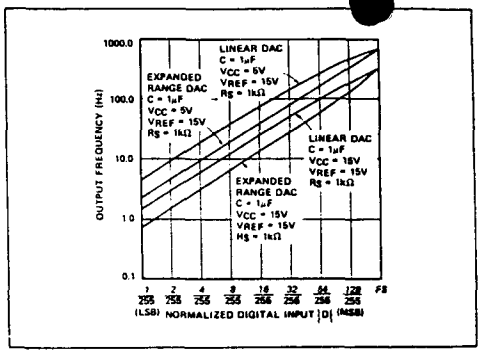


Figure 4. Multivibrator Frequency vs Digital Input

CONCLUSION

Digitally controlled one-shot and astable multivibrator with a wide range of outputs have been implemented. The one-shot has a 255 to 1 (8 Bit dynamic) time period range and the astable multivibrator a 220 to 1 frequency range. When the DAC is operated in the expanded modes, these ranges are doubled.

Table 2. One-Shot Expanded Mode Timing Table

	ONE-SHOT PERIOD (msec)					
	V_{CC} = 15V V_{REF} = 15V			V_{CC} = 5V V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
11 11 11 11	5.2	0.495	0.049	1.72	0.160	0.0176
00 00 00 01	2900	280	26	970	87	8.4

Table 3. Astable Linear Mode Frequency Table

	ASTABLE MULTIVIBRATOR FREQUENCY (Hz)					
	R_B = 1kΩ; V_{CC} = 15V; V_{REF} = 15V			R_B = 1kΩ; V_{CC} = 5V; V_{REF} = 15V		
Input Digital Code	C = 1μF	C = 0.1μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
00 00 00 01	1.49	14.7	156	4.86	49.8	433
11 11 11 11	328	3,279	33,333	717	7,273	60,241

Table 4. Astable Expanded Mode Frequency Table

	ASTABLE MULTIVIBRATOR FREQUENCY (Hz)					
	R_B = 1kΩ; V_{CC} = 15V; V_{REF} = 15V			R_B = 1kΩ; V_{CC} = 5V; V_{REF} = 10V		
Input Digital Code	C = 1μF	C = 0.10μF	C = 0.01μF	C = 1μF	C = 0.1μF	C = 0.01μF
00 00 00 01	0.74	7.69	79.9	2.42	24.7	217
11 11 11 11	328	3,279	33,333	714	7,299	60,241

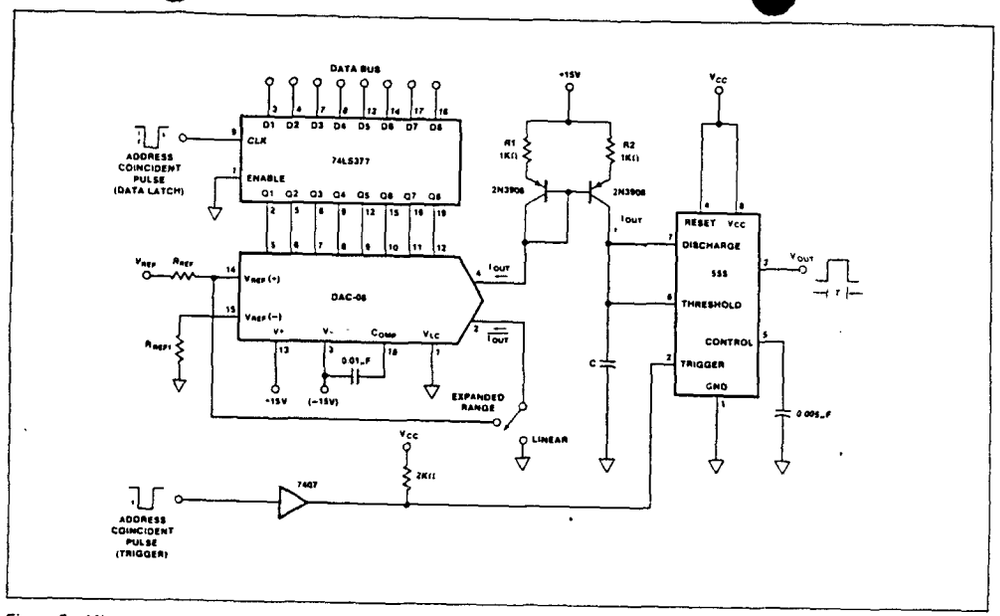


Figure 5. Microprocessor Controlled One-Shot

APPLICATION NOTE 40

A BUFFER APPLICATIONS COLLECTION

by Shelby D. Givens

INTRODUCTION

This Application Note consists of a collection of circuits which apply buffers to the solutions of a variety of problems. As will be shown, buffers may be used to make filters, current sources, cable drivers, sample and holds, high speed instrumentation amplifiers, line drivers for multiplexers, current boosters for voltage references, and high speed voltage output DACs.

INDUCTORS AND FILTERS

The active inductor in Figure 1 is realized with an eight-lead IC, two carbon resistors, and a small capacitor. A commercial inductor of 50 henries may occupy up to five cubic inches.

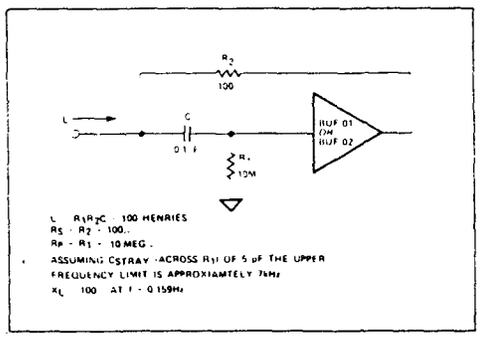


Figure 1. Active Inductor

The tuned circuit shown in Figure 2 uses the simulated inductor of Figure 1 (R_1, R_2, C_1) and C_2. Depending upon whether the circuit is driven at E_1 or E_2 the responses of Figures 3 or 4 result. The resonant response in both cases is

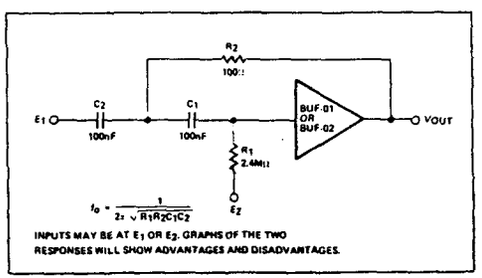


Figure 2. Tuned Circuit

+ 38dB at 103Hz. The Figure 3 response is + 2.5dB at 200Hz and − 10dB at 50Hz. On the other hand, the Figure 4 response is − 9dB at 200Hz and + 2.5dB at 50Hz.

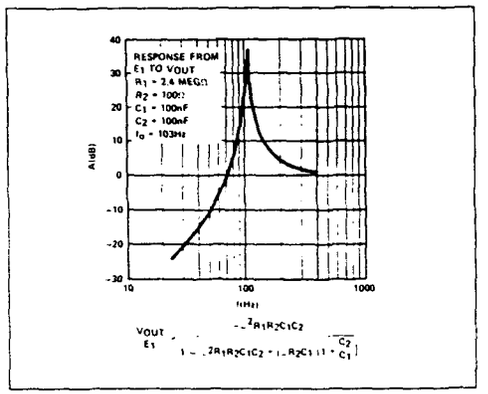


Figure 3. Response from E_1 to V_{out}

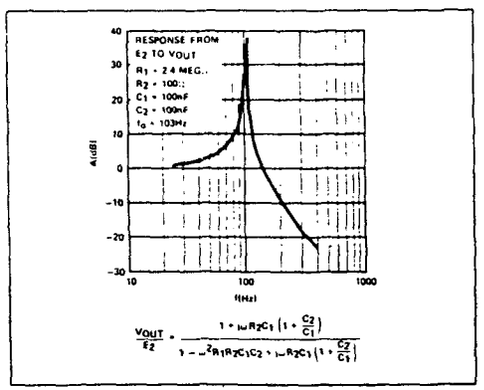


Figure 4. Response from E_2 to V_{out}

Figure 5 shows a low pass filter realized for f_o of 1MHz. What is remarkable about this filter is most ICs do not have the full power bandwidth to handle 1MHz signals in the 5 to 10 Volt range, while the BUF-03 has a greater than 4MHz full power bandwidth for a $20V_{p-p}$ sinewave. Similar comments apply to the filter in Figure 6. In other words, the extreme bandwidth of the BUF-03 extends the bandwidth capability of certain classes of active filters.

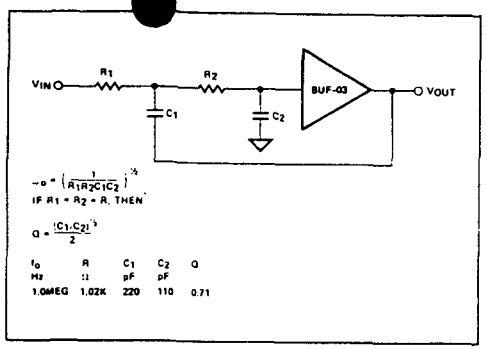
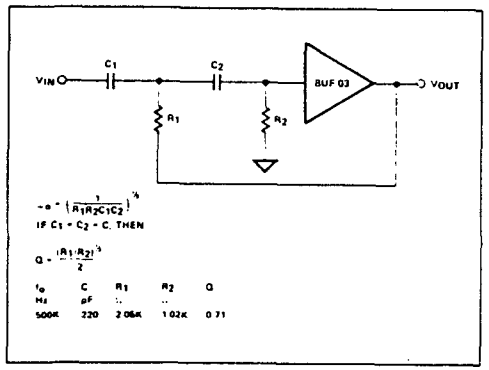


Figure 5. Low Pass Filter (High Frequency)



Figrue 6. High Pass Filter (High Frequency)

The BUF-03 can be used to make a 4.5MHz trap for use in TV. This circuit is shown in Figure 7, and the elements are chosen such that no capacitor is less than 100pF.

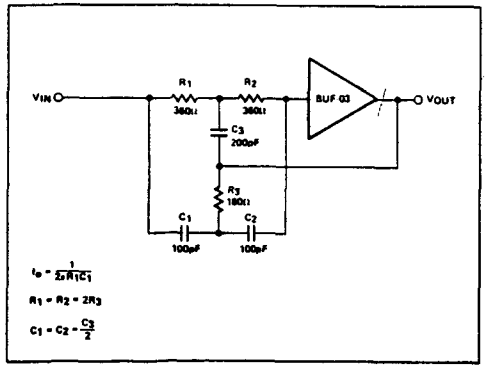


Figure 7. Notch Filter at 4.5MHz

HIGH SPEED CURRENT SOURCES

The BUF-03 in combination with an OP-16 produces a bipolar voltage-controlled current source. The circuits shown in Figures 8 and 9 were breadboarded and found to have rise times of approximately 1μsec. Since the waveforms had definite RC characteristics, layout was suspected as contributing primarily to the rise times observed. Figure 8 shows the inverting connection, while Figure 9 shows the noninverting connection.

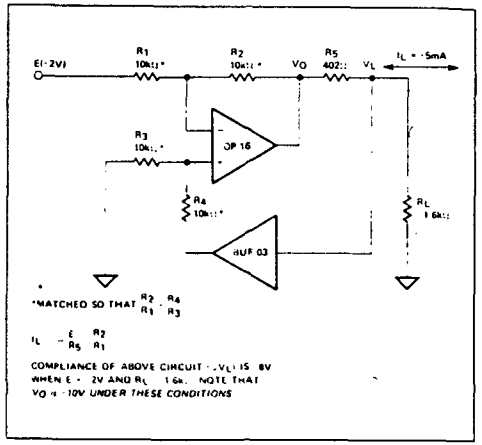


Figure 8. Inverting Bipolar Current Source (High Speed)

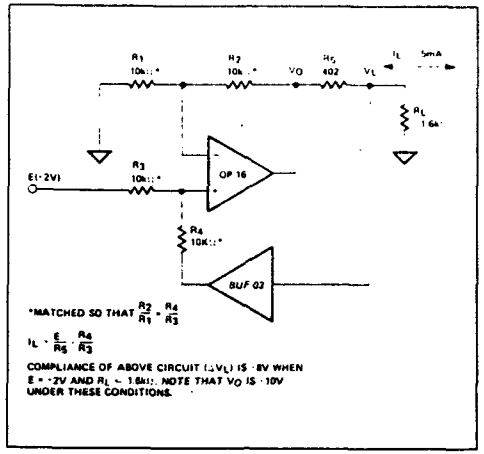


Figure 9. Noninverting Bipolar Current Source

DATA ACQUISITION SYSTEM APPLICATIONS

Because of the speed of these devices, the BUF-03 and OP-17 allow the fabrication of a high speed instrumentation amplifier as shown in Figure 10. The output of the instrumentation amplifier will likely be multiplexed onto a common data line. Here the BUF-02 or BUF-03 can be used as the data line drivers because of their speed and current capabilities. The connection for this application is shown in Figure 11. The realization of a high speed sample and hold is possible using the BUF-03 and suitable analog switches. The circuit shown in Figure 12 provides the highest speed because there are no feedback loops to slow down the settling times. Typically the sample and hold is followed by a successive approximation analog-to-digital converter (ADC).

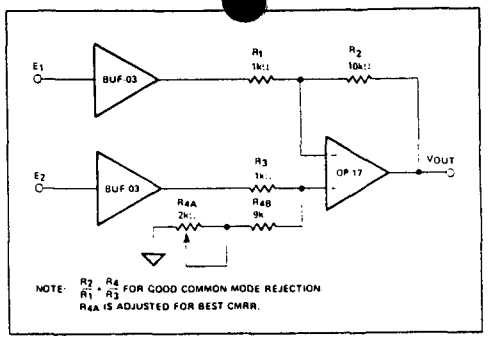


Figure 10. High Speed Instrumentation Amplifier

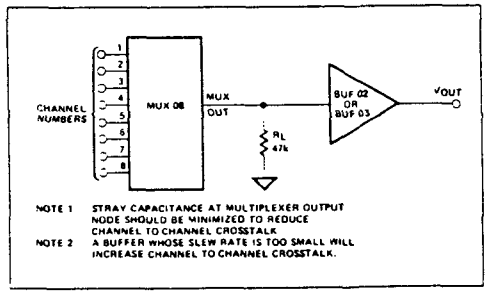


Figure 11. High Speed Line Driver for Multiplexers

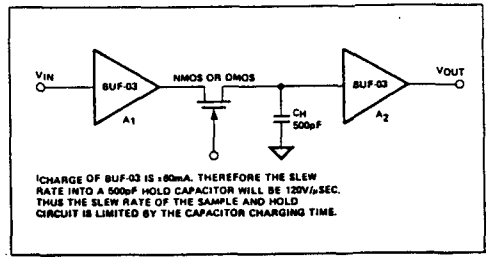


Figure 12. High Speed Sample and Hold

The BUF-01 is shown in Figure 13 as the input buffer for a 14-bit ADC. Because of its extreme accuracy, the BUF-01 can resolve ½LSB of a 10V, 14-bit system. The final application involves the BUF-03 and the DAC-08 (digital-to-analog converter). Figure 14 shows how it is possible to develop both V_{out} and $\overline{V}_{out}$. The output capacitance of the DAC-08 is approximately 15pF, thus as R_O increases in value, so does the settling time for V_{out} (and $\overline{V}_{out}$).

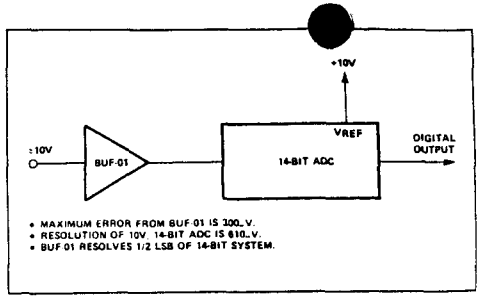


Figure 13. High Resolution ADC Input Buffer

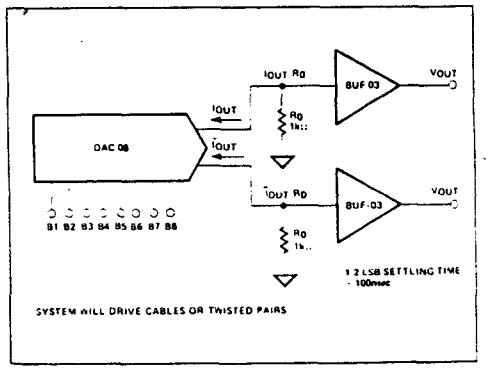


Figure 14. High Speed Voltage Output DAC

LINE DRIVER APPLICATIONS

If your BIFET "line driver" has the speed but not the stability or the current capability to drive coaxial cables, its output may be buffered with a BUF-03 as shown in Figure 15. Figure

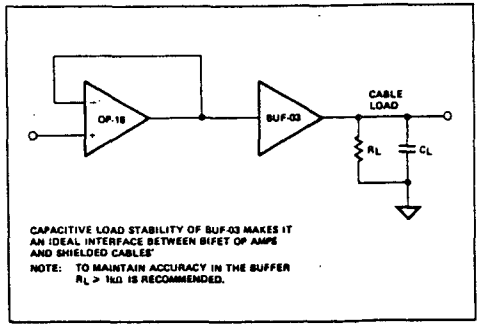


Figure 15. Convert BIFET Into Cable Driver

16 shows an alternative connection when better accuracy and more current capability is needed. Note that the limitation on R_L being greater than 1K does not apply in this case since the added error caused by lower impedances is imbedded inside the feedback loop of the op amp.

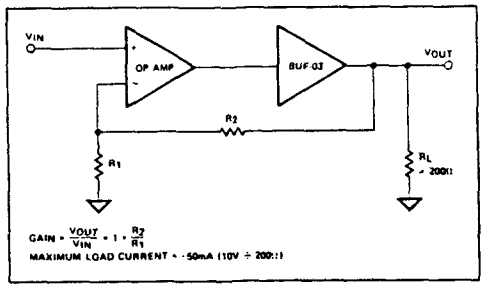


Figure 16. Current Booster

MISCELLANEOUS USES OF BUFFERS

An accurate buffer can be useful for isolating a reference zener from load fluctuations. In this way the same zener can be used in a variety of reference situations. The circuit shown in Figure 17 can supply up to 10mA (5mA for the BUF-02) to a load using a BUF-01. Single supply applications can be realized using either the BUF-02 or the BUF-03 as shown in Figure 18.

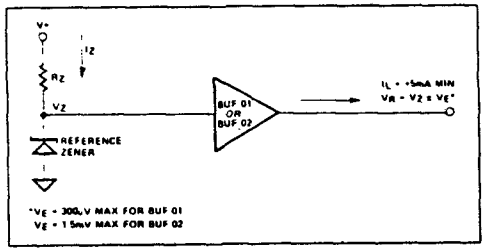


Figure 17. Buffered Voltage Reference

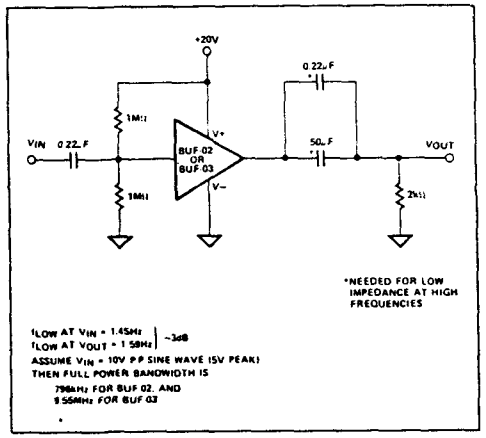


Figure 18. Single Supply AC Buffer (High Speed)

CONCLUSION

While the list is by no means all inclusive, this application note has attempted to point out some of the myriad of uses for the IC buffer. In particular, the BUF-03 makes possible a whole new class of high frequency filters and high speed current sources. Many problems in data acquisition systems can be solved by the use of buffers. In addition, the BUF-03 is useful in providing increased drive current, as well as the ability to drive long cables without instability. Finally, the versatility of the reference zener can be increased by using buffers, and for AC applications the buffer can be used on single power supplies.

APPLICATION NOTE 43

THE DAC-76 IN CONTROL APPLICATIONS

by Mike Parsin

This note describes a companding D/A converter that is ideally suited for industrial control applications using 8-bit microprocessor bus structures. Features, such as 4-channel demultiplexing, a reference amplifier that accepts various levels of DC or AC for multiplying, and both encode or decode capabilities are on-board the COMDAC®. Twelve-bit accuracy can be obtained with a logrithmic 7-bit plus sign microprocessor compatible D/A converter.

The DAC-76 is at its best when measurement and control become critical as the signal approaches zero volts. Not all control systems that require precise control need the accuracy of a 12-bit digital-to-analog converter over their entire range of operation. In fact, the non-linearity of a 7-bit companding D/A converter can be quite an advantage.

COMDAC® CHARACTERISTICS

The term "companding" comes from compression/expansion which is used extensively in the telecommunication industry. Compression is performed in the encode or analog-to-digital conversion mode, and expansion occurs during decode or D/A conversion. The A/D transfer characteristic is seen in Figure 1. Eight points which are referred to as chords or segments are selected by a 3-bit binary code. Within each chord are 16 steps selected by a 4-bit binary code. Each chord segment is linear to 1/2LSB. Step size varies from 0.025% in chord 0 to 3.2% of full scale in chord 7 (see Table 1).

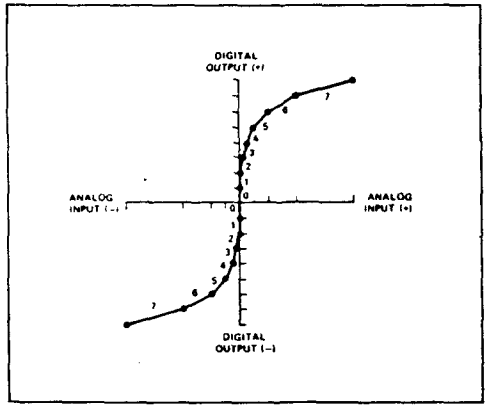


Figure 1. Transfer Characteristic

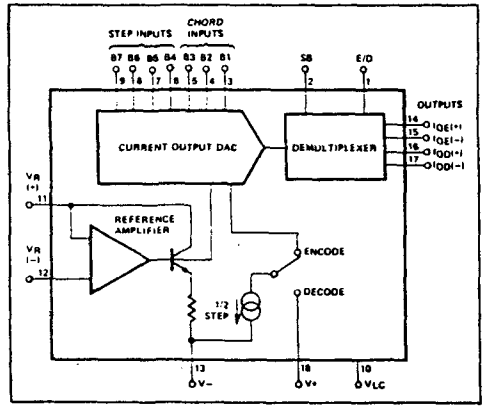


Figure 2. DAC-76 Equivalent Circuit

Table 1. Step Size Summary Table Decode Output (Sign Bit Excluded)

CHORD	STEP SIZE NORMALIZED TO FULL SCALE	STEP SIZE IN μA WITH 2007.75μA F.S.	STEP SIZE AS A % OF FULL SCALE	STEP SIZE IN dB AT CHORD ENDPOINTS	STEP SIZE AS A % OF READING AT CHORD ENDPOINTS	RESOLUTION & ACCURACY OF EQUIVALENT BINARY DAC
0	2	0.5	0.025%	0.60	6.67%	SIGN + 12 BITS
1	4	1.0	0.05%	0.38	4.30%	SIGN + 11 BITS
2	8	2.0	0.1%	0.32	3.65%	SIGN + 10 BITS
3	16	4.0	0.2%	0.31	3.40%	SIGN + 9 BITS
4	32	8.0	0.4%	0.29	3.28%	SIGN + 8 BITS
5	64	16	0.8%	0.28	3.23%	SIGN + 7 BITS
6	128	32	1.6%	0.28	3.20%	SIGN + 6 BITS
7	256	64	3.2%	0.28	3.19%	SIGN + 5 BITS

BIPOLAR REFERENCES

Operation with bipolar references is achieved by modulating I_{REF} as shown in Figure 5. To aid in understanding bipolar operation, see the equivalent circuit in Figure 4. The reference inputs of the DAC-08 are op amp inputs — $V_{REF}(+)$ being the inverting input and $V_{REF}(-)$ being the noninverting input. Excellent gain linearity of the reference amplifier allows multiplying operation over a range of I_{REF} of 4μA to 4mA with monotonic operation from less than 100μA to 4mA.

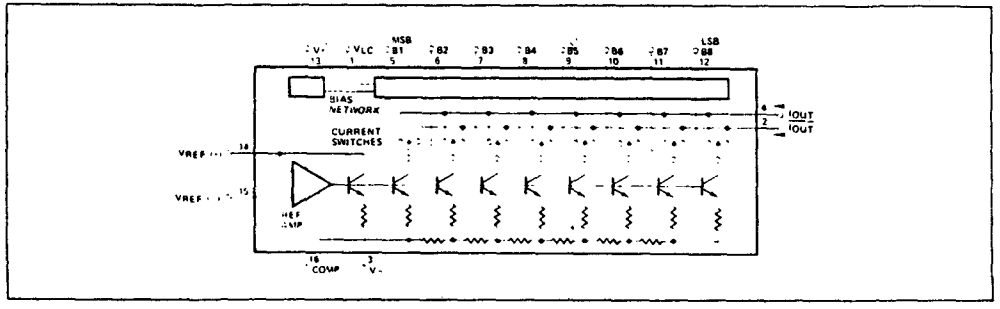


Figure 4. DAC-08 Equivalent Circuit

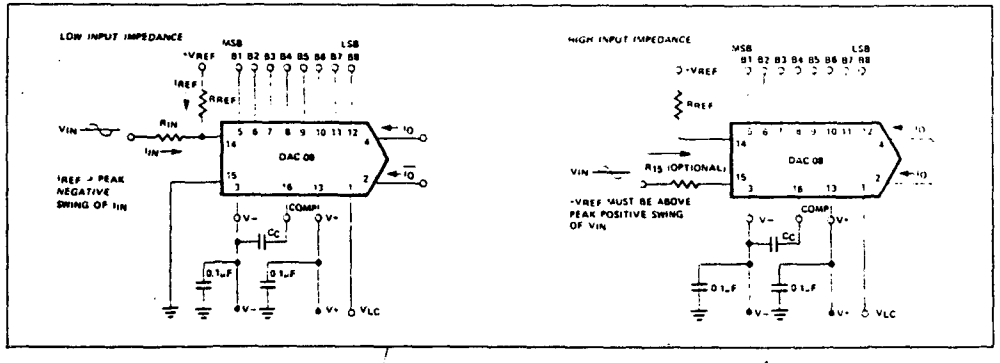


Figure 5. Bipolar Reference Connections

REFERENCE AMPLIFIER COMPENSATION

AC reference applications will require the reference amplifier to be compensated using a capacitor from Pin 16 to V−. The value of this capacitor depends on the impedance presented to Pin 14: for R_{14} values of 1.0, 2.5 and 5.0kΩ, minimum values of C_C are 15, 37, and 75pF. Larger values of R_{14} require proportionately increased values of C_C for proper phase margin.

FAST PULSED OPERATION

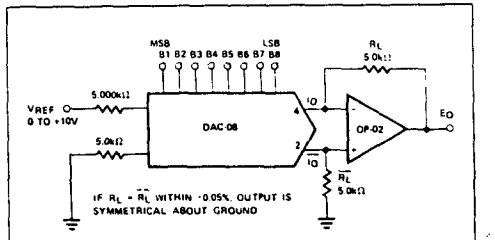
For fastest multiplying response, low values of R_{14} enabling small C_C values should be used. For $R_{14} = 1k\Omega$ and $C_C = 15pF$, the reference amplifier slews at 4mA/μs enabling a transition from $I_{REF} = 0$ to $I_{REF} = 2mA$ in 500ns. If R_{14} or the parallel equivalent resistance at Pin 14 is less than 200Ω, no compensation capacitor is necessary, and a full-scale transition requires only 16ns.

TWO-QUADRANT MULTIPLICATION

There are two forms of two-quadrant multiplication: bipolar digital, where the digital input word controls output polarity, and bipolar analog, where the analog reference input controls output polarity.

Bipolar digital two-quadrant mutliplication is shown in Figure 6 with the output polarity being controlled by an offset-binary-coded digital input word.

Bipolar analog two-quadrant multiplication is shown in Figure 7. A bipolar reference voltage is connected to the upper DAC-08 and modulates the reference current by ±1.0mA around a quiescent current of 1.1mA. The lower DAC-08 also has a reference current of 1.1mA; due to the parallel digital inputs, the lower DAC-08 effectively subtracts out the quiescent 1.1mA of the upper DAC-08's reference current at all input codes, since the voltage across R3 varies between −10V and 0V. Thus, the output voltage, E_O, is a product of a digital input word and a bipolar analog reference voltage.



	B1	B2	B3	B4	B5	B6	B7	B8	I_O mA	$I_{\overline{O}}$ mA	E_O (V)
POS FULL SCALE	1	1	1	1	1	1	1	1	1.992	0.000	+9.96
POS FULL SCALE −LSB	1	1	1	1	1	1	1	0	1.984	0.008	+9.88
(+) ZERO SCALE	1	0	0	0	0	0	0	0	1.000	0.992	−0.040
(−) ZERO SCALE	0	1	1	1	1	1	1	1	0.992	1.000	−0.040
NEG FULL SCALE +LSB	0	0	0	0	0	0	0	1	0.008	1.984	−9.88
NEG FULL SCALE	0	0	0	0	0	0	0	0	0.000	1.992	−9.96

Figure 6. Bipolar Digital Two-Quadrant Multiplication (Symmetrical Offset Binary)

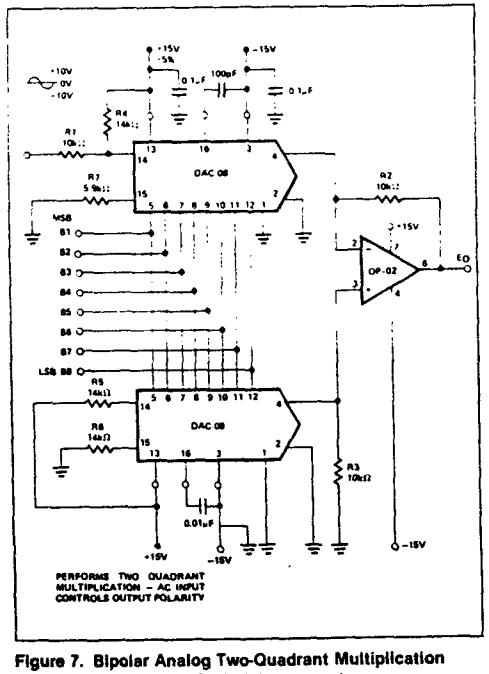


Figure 7. Bipolar Analog Two-Quadrant Multiplication (DC-Coupled Digital Attenuator)

FOUR-QUADRANT MUTLIPLICATION

Four-quadrant multiplication combines the two forms of two-quadrant multiplication. Output analog polarity is controlled by either the analog input reference or by the offset binary digital input word. One implementation of this function with the DAC-08 is shown in Figure 8 with output current values listed in Table 1.

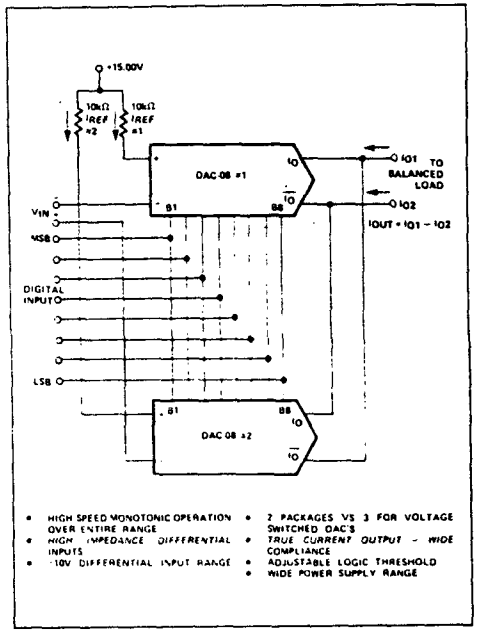


Figure 8. Four-Quadrant Multiplying DAC with with Impedance Input

The four-quadrant multiplying DAC circuit shown accepts a differential voltage input and produces a differential current output. An output op amp is not shown because it is not always required; many applications are more suited for high output compliance (−10V to +18V) differential current outputs. Typical balanced loads include transformers, transducers, transmission lines, bridges and servos.

Operation of the four-quadrant multiplier may be more easily visualized by considering that if either $V_{IN} = 0V$ or the offset binary digital input code is at midscale (corresponding to zero), then a change in the other input will not affect the output. Zero multiplied by any number equals zero.

A common mode current will be present at the output and must be accommodated by the balanced load. A pair of matched resistors may be used at the outputs to shunt most of the common mode current to ground, thus reducing the common mode voltage swing at the output.

Table 1. Four-Quadrant Multiplying Current Values in Figure 8.

DIGITAL INPUT	$V_{IN}(+)$	$V_{IN}(-)$	V_{IN} DIFF.	I_{REF} #1 (mA)	I_{REF} #2 (mA)	I_O#1 (mA)	I_O#2 (mA)	I_{01} (mA)	I_O#2 (mA)	I_O#1 (mA)	I_{02} (mA)	I_{OUT} DIFF.
1111 1111	+5V	−5V	+10V	2.000	1.000	1.992	0	1.992	0.996	0	0.996	0.996mA
1000 0000	+5V	−5V	+10V	2.000	1.000	1.000	0.496	1.496	0.500	0.992	1.492	0.004mA
0111 1111	+5V	−5V	+10V	2.000	1.000	0.992	0.500	1.492	0.496	1.000	1.496	−0.004mA
0000 0000	+5V	−5V	+10V	2.000	1.000	0	0.996	0.996	0	1.992	1.992	−0.996mA
1111 1111	0V	0V	0V	1.500	1.500	1.494	0	1.494	1.494	0	1.494	0.000mA
1000 0000	−10V	−10V	0V	2.500	2.500	1.250	1.240	2.490	1.250	1.240	2.490	0.000mA
0111 1111	+10V	+10V	0V	0.500	0.500	0.248	0.250	0.498	0.248	0.250	0.498	0.000mA
0000 0000	0V	0V	0V	1.500	1.500	0	1.494	1.494	0	1.494	1.494	0.000mA
1111 1111	−5V	+5V	−10V	1.000	2.000	0.996	0	0.996	1.992	0	1.992	−0.996mA
1000 0000	−5V	+5V	−10V	1.000	2.000	0.500	0.992	1.492	1.000	0.496	1.496	−0.004mA
0111 1111	−5V	+5V	−10V	1.000	2.000	0.496	1.000	1.496	0.992	0.500	1.492	0.004mA
0000 0000	−5V	+5V	−10V	1.000	2.000	0	1.992	1.992	0	0.996	0.996	0.996mA

HIGHEST SPEED FOUR-QUADRANT MULTIPLYING CONSIDERATIONS

The configuration shown in Figure 10 makes use of the DAC-08's ability to operate in a fast-pulsed reference mode without compensation capacitors. This technique provides lowest full-scale transition times. An internal clamp allows quick recovery of the reference amplifier from a cutoff ($I_{REF} = 0$) condition. This connection yields a reference slew rate of 16mA/μs which is relatively independent of R_{IN} and V_{IN} values.

Input resistances are not limited to 10kΩ. For example, 100kΩ resistors for R_{IN1} and R_{IN2} allow ±100V reference voltage inputs making this connection especially useful in high common mode voltage environments. Except for different reference treatment, operation and digital input coding are identical in the circuits shown in Figure 8 and in Figure 10; both have the transfer function shown in Figure 9.

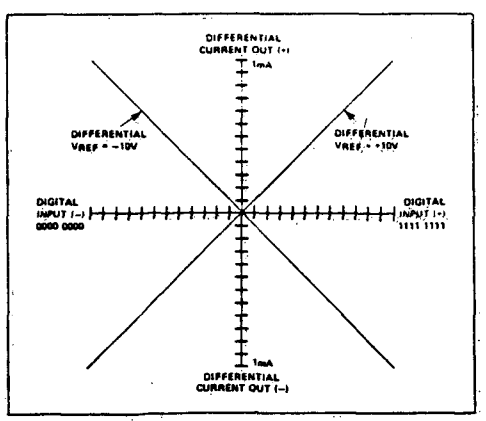


Figure 9. Four-Quadrant Multiplying DAC Transfer Function

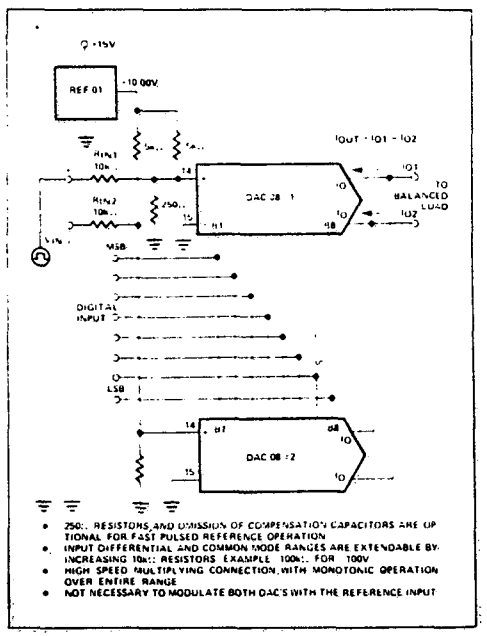


Figure 10. Four-Quadrant Multiplying DAC with Extendable Input Range and Highest Speed

AC-COUPLED MULTIPLICATION

Some multiplying DAC applications are more easily achieved with AC coupling. At the same time, a high impedance input is often required to avoid loading a relatively high source impedance. Both requirements are met by the circuits shown in Figure 11 and Figure 12 which use the compensation

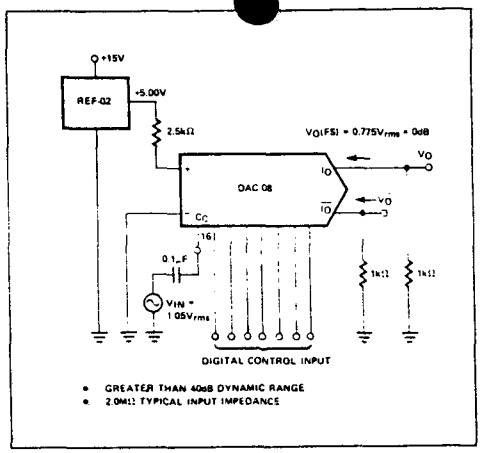


Figure 11. High Input Impedance AC-Coupled Multiplication (Audio Frequency Digital Attenuator)

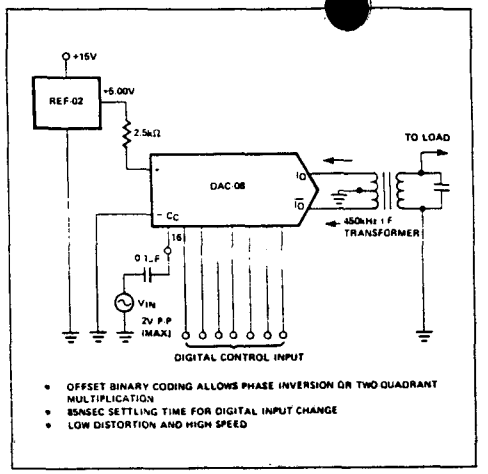


Figure 12. High Input Impedance AC-Coupled Multiplication (I.F. Amplifier/Digital Attenuator)

capacitor terminal (C_C) as an input. This is possible because C_C is the base of a transistor whose emitter is one diode drop (0.7V) away from the R-2R ladder network common baseline internal to the DAC-08.

With a full-scale input code the output, V_O, is flat to >200kHz and is 3dB down at approximately 1.0MHz making this type of multiplying connection useful even beyond the audio frequency range. Such a connection is illustrated in Figure 12 operating at 455kHz, the highest recommended operating frequency in this connection.

DIFFERENTIAL AND RATIOMETRIC A/D CONVERSION

Complementary/differential current-source outputs and multiplying capability allow the DAC-08 to be used in differential and ratiometric A/D converter designs directly without signal conditioning amplifiers. This group of applications begins with the basic differential A/D converter and ratiometric A/D conveter connections followed by more specific applications.

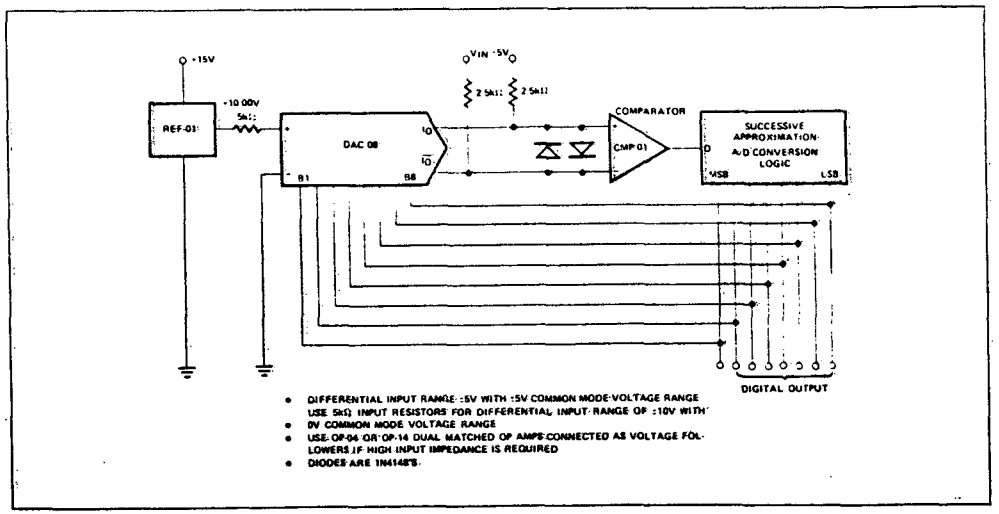


Figure 13. Differential Input A/D Conversion Basic Connections

These are extremely cost-effective designs due to their low parts count and simplicity. Alternative designs performing identical functions require instrumentation amplifiers for the differential-to-single-ended input signal conditioning and analog multipliers or dividers for the arithmetic functions.

DIFFERENTIAL A/D CONVERSION

The circuit in Figure 13 uses the high voltage compliance current output capability of the DAC-08 and the high common mode voltage rejection of the CMP-01 to construct a differential input ADC without input signal conditioning.

A successive approximation ADC is constructed with four ICs: a REF-01 +10V reference, a 2502-type successive approximation register, a CMP-01 precision voltage comparator, and a DAC-08. As shown, the circuit converts an analog input in less than 2.0μs. For lower speed requirements, the A/D conversion logic can be the tracking or servo type consisting of up/down counters.

FOUR-QUADRANT RATIOMETRIC A/D CONVERSION

Ratiometric A/D conversion with fully differential X and Y inputs is accomplished with the circuit in Figure 14. Here, one set of inputs, V_X, is connected in a manner similar to the circuit in Figure 13, and the other set of inputs V_Y, is connected in a multiplying fashion. Operation is as follows: I_{REF} for both the upper and the lower DAC-08 is modulated between 1mA and 3mA; and the resulting output currents are differentially transformed into voltages by the 5kΩ resistors at the comparator's inputs and compared with the V_X differential input. When the conversion process is complete (comparator inputs differentially nulled to less than 1/2 LSB) a digital output is available which corresponds to the quotient of V_X/V_Y. Thus, four-quadrant ratiometric A/D conversion is achieved with four ICs and without instrumentation amplifiers.

BRIDGE TRANSDUCER NULL

In many control systems, bridges must be nulled, and a digital representation of the bridge's error must be provided for computer monitoring and control. The circuit in Figure 15 accomplishes both tasks by using the DAC-08 complementary/differential current outputs to null the bridge with the DAC-08 connected in a tracking differential A/D converter configuration. The REF-02 reference voltage source provides both the bridge excitation voltage and the positive reference voltage for the DAC-08. Some of the advantages of this circuit are listed at the bottom of Figure 15.

POWER MONITOR

Another differential current-input ADC is shown in Figure 16 with a transformer-coupled input. An up/down counter, a precision high-speed comparator, and the DAC-08 form a tracking A/D converter which continuously monitors the analog input. Two precautions must be observed: the common mode voltage at the comparator's inputs must not exceed ±10V; and the differential voltage must not exceed 11V. Voltage-limiting resistors at the comparator's inputs are recommended.

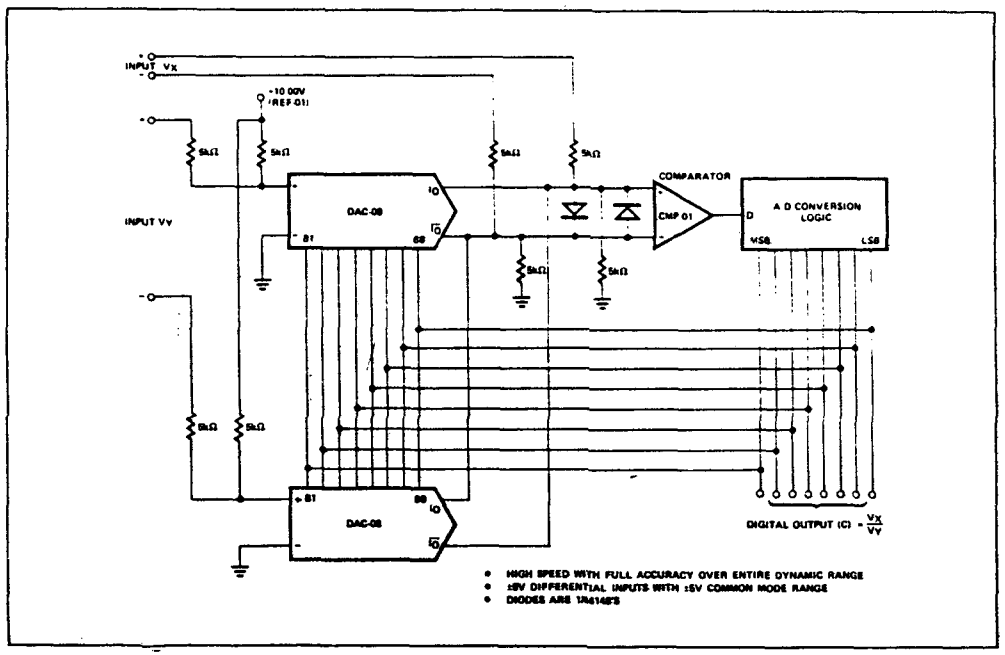


Figure 14. Four-Quadrant Ratiometric A/D Conversion Basic Connections

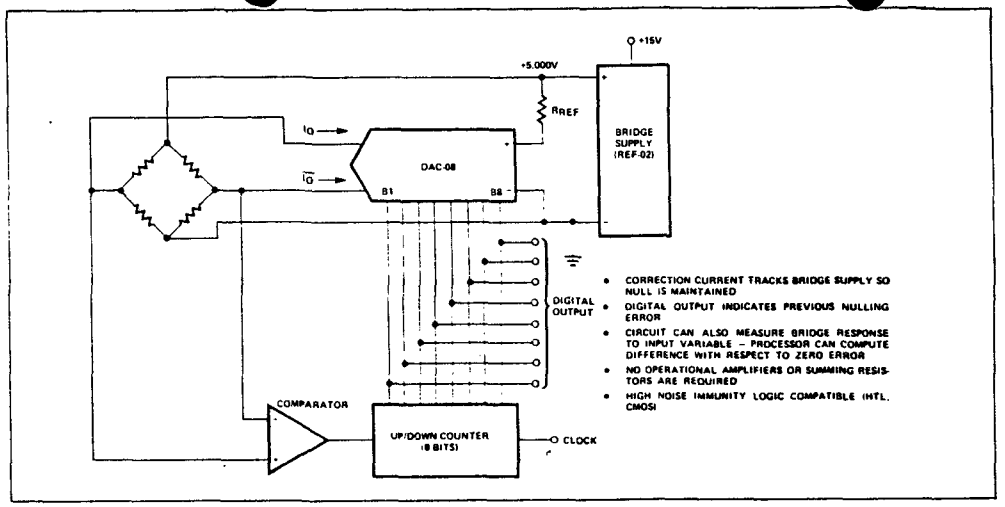


Figure 15. Bridge Transducer Null

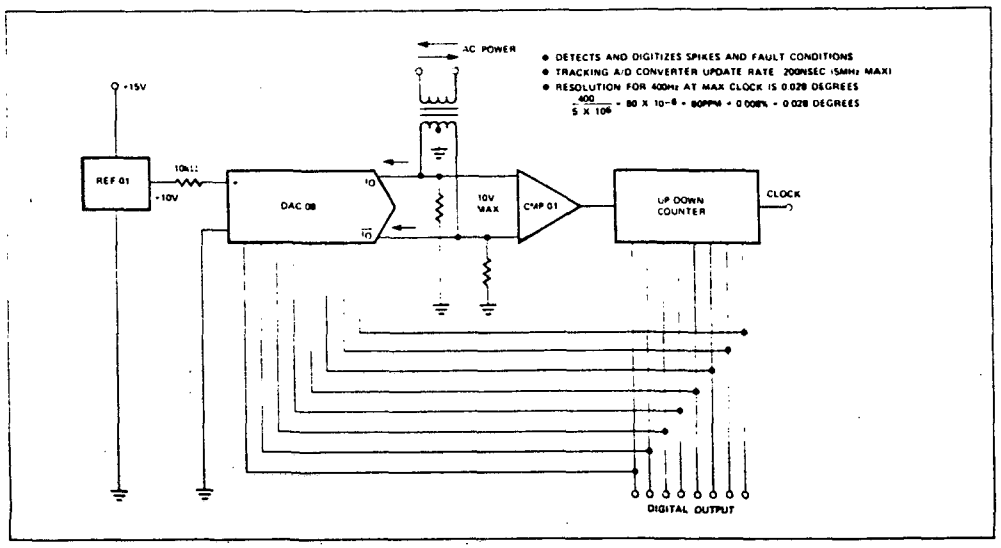


Figure 16. Power Fault Monitor and Detector

ALGEBRAIC DIGITAL COMPUTATION

Frequently, a digital arithmetic operation (addition, subtraction, multiplication, or division) must be performed, and an analog output must be provided. Traditionally, the arithmetic operations are performed with several ICs, and the output drives a D/A converter. This section decribes applications of the DAC-08 as an arithmetic building block, new design approaches that reduce the number of packages required in many applications. Today's low cost, versatile DACs merit a designer's consideration as arithmetic elements.