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# DC Gate Leakage Current Model Accounting for Trapping Effects in AlGaN/GaN HEMTs

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**Abstract:** A DC leakage current model accounting for trapping effects under the gate of AlGaN/GaN HEMTs on silicon has been developed. Based on TCAD numerical simulations (with Sentaurus Device), non-local tunneling under the Schottky gate is necessary to reproduce the measured transfer characteristics in a subthreshold regime. Once the trap concentration and distribution are determined in the device, the resulting gate leakage current is modeled making use of Verilog-A, for typical operation regimes.

**Keywords:** AlGaN/GaN HEMT; gate leakage current; traps; numerical simulation; modeling

## 1. Introduction

AlGaN/GaN devices grown on silicon substrates are the main candidates for power applications in the next generation of power converters [1–3]. Therefore, an accurate modeling of the AlGaN/GaN HEMT is essential in the design of circuits for both high power and radio frequency applications. On the other hand, simplification is mandatory when dealing with compact modeling for circuit simulation purposes. Thus, this paper is devoted to obtaining a simple analytical expression for the DC current of AlGaN/GaN HEMTs and, at the same time, accurately supporting the underlying physics.

Although GaN HEMTs are promising, the presence of traps during crystal growth and epitaxial processing implies not desired aspects such as leakage current and current collapse, among others [4]. A deeper understanding of trapping effects is essential for the electrical functionality and correct modeling of these devices, in order to achieve accurate circuit designs [5–7]. In fact, the etching process for Schottky gates together with electrical stress during normal device operation may provoke traps in barriers.

It is well known that there are four major mechanisms for gate leakage currents. Fowler-Nordheim (FN) [8] and Thermionic-Emission (TE) [9] are one-step tunneling processes taking place near the Fermi level and at higher energy levels, respectively. These high-energy mechanisms through the entire energy barrier can be accounted for more easily. Poole–Frenkel emission (PF) [10] is an emission transport through a continuum of trap states, which is sensitive to the temperature and the electric field and, therefore, difficult to identify at low bias in the subthreshold region. Finally, in Trap Assisted Tunneling (TAT) emission [11] most of tunneling takes place through a two-step tunneling via a mid-band state-layer of scattered traps within the AlGaN barrier layer [12].

Hopping through high-density surface electronic states in AlGaN is only significant for very short gate to drain distances, when its corresponding current approaches the more significant vertical

tunneling component of the leakage current [13]. This surface component can be easily controlled through proper passivation. Therefore, we focus our work on vertical leakage through traps.

In this work, the HEMT description is presented in Section 2. Section 3 is devoted to an evaluation of trap concentration and distribution, through numerical simulation. The model to account for the resulting gate leakage current is developed in Section 4, whose transfer characteristics are compared with those measured. Finally, conclusions are presented in Section 5.

## 2. Device Description

The long channel device under study is a normally-on HEMT on silicon (from a normally-off AlGaN/GaN HEMT using fluorine implantation below the channel [14]), based on the AlGaN/GaN system, 1000 µm wide, with the technological processing carried out at LAAS.

The device geometry and material composition are drawn in Figure 1. Corresponding donor doping concentrations, $N_D$, are also indicated. Notice that below the AlGaN barrier and GaN channel, 30 nm and 1.1 µm deep, respectively, a practically undoped GaN buffer (with similar electrothermal performance) substitutes the transition layers for simulation purposes.

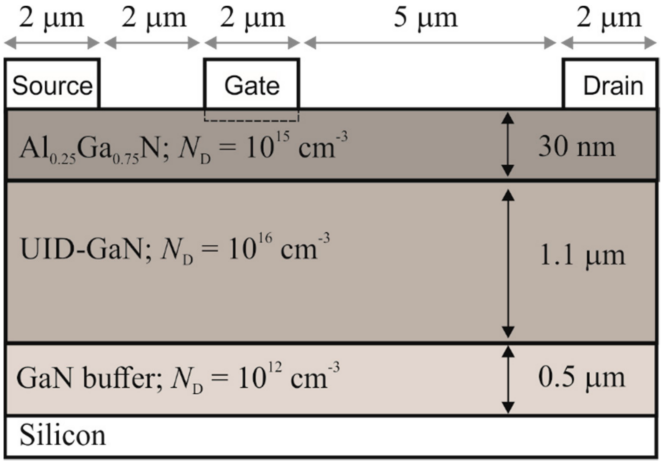


**Figure 1.** Simulated AlGaN/GaN HEMT. Below the gate, the donor trap layer is indicated with dashed lines.

Finally, it is known that the etching process in GaN-based devices during a Schottky gate contact formation, can lead to defective adhesion properties at the metal/semiconductor interface, originating traps under the gate and, therefore, a leakage current increment [15,16]. Thus, making use of deep-level transient spectroscopy (DLTS), N-vacancies (surface donors) were demonstrated to be formed under the gate in [15].

Additional trapping under the gate can be caused by electrical stress [17,18], which is present in the (across the barrier) gate edge region of the HEMT under study. Under electrical stress, the elastic energy in the high-field region increases on top of this. If the elastic energy exceeds a critical value, crystallographic defects are formed [19].

Thus, a trap concentration under the gate of the transistor investigated is considered, as indicated in Figure 1 with dashed lines.

## 3. Numerical Simulation

Numerical simulations have been performed with a Sentaurus Device (from Synopsys) [20]. The transistor DC response, at room temperature, is analyzed solving the Poisson and drift-diffusion equations, together with the heat equation as in [21], polarization charges [22], and the rest of physical parameters from [14]. A gate Schottky diode (i.e., thermionic emission, TE) with Poole–Frenkel (PF) is considered for all operating regimes [23].

Traps on the top of the AlGaN barrier, with a donor sheet density of $2.3 \times 10^{13}$ cm$^{-2}$ and an activation energy from the center of the band gap of 0.4 eV have been incorporated, as well as acceptor traps in the GaN buffer, with a concentration of $10^{17}$ cm$^{-3}$ and an activation energy from the valence band maximum of 0.368 eV [5].

In order to set the threshold voltage, no fitting for the polarization charge is needed (opposite to [14]) when traps under the gate are determined [19], as they (in volume) can modify the Fermi level position in the energy band diagram, or (when superficial) produce a straight-on threshold voltage displacement [24].

Regarding the device description, a layer of donor traps, 2 nm deep, just below the gate terminal, with an activation energy from the conduction band minimum of 0.2 eV, and capture cross-section of $10^{-15}$ cm$^{-2}$, is firstly assumed (according to [19]).

Then, for any trap concentration, $N_t$, ranging from $10^{19}$ cm$^{-3}$ to $3 \times 10^{20}$ cm$^{-3}$, transconductance ($\partial I_D / \partial V_{GS}$) in strong inversion regime is numerically reproduced, as Figure 2a shows, where measured (with symbols) and simulated (with lines) transfer characteristics are represented in linear scale. Notice that, for a trap concentration of $10^{19}$ cm$^{-3}$, the measured transfer characteristics above threshold voltage are well predicted, additionally.

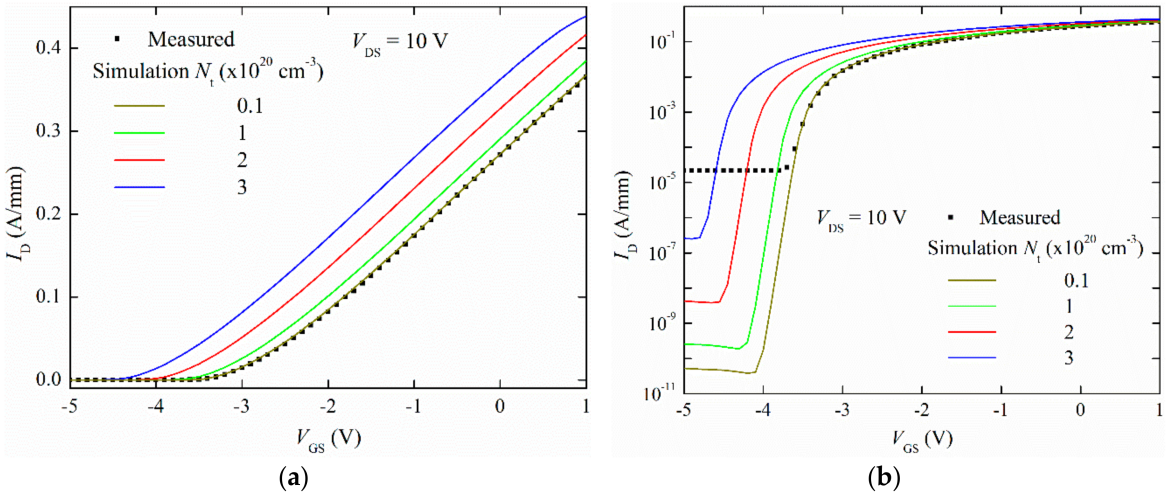


**Figure 2.** Measured (symbols) and simulated (lines) transfer characteristics for the AlGaN/GaN HEMT, for different traps concentration, with drain current in (**a**) linear scale and (**b**) logarithmic scale; $V_{DS}$ = 10 V.

However, when drain current of transfer characteristics is represented in logarithmic scale, Figure 2b, the existence in subthreshold regime of a constant leakage current, $I_{off}$, of 22.5 μA does show up, which is not being numerically reproduced.

To solve the problem of the adjustment of this gate leakage current behavior, without deteriorating the transfer characteristics in conduction regime (with gate-to-source voltage, $V_{GS}$, above threshold voltage), non-local tunneling incorporating FN emission through the gate is activated in simulations [19,23], with the donor layer thickness for traps, $t$, being varied from 2 nm to 5 nm. Figure 3 shows the resulting conduction band energy minimum profile below the gate ($E_C$, with colored lines), in depth ($z$). Notice how the transversal electric field ($|\partial E_C / \partial z|$) under the gate drastically increases with the thickness of the trap layer, deriving a higher leakage current by tunneling.

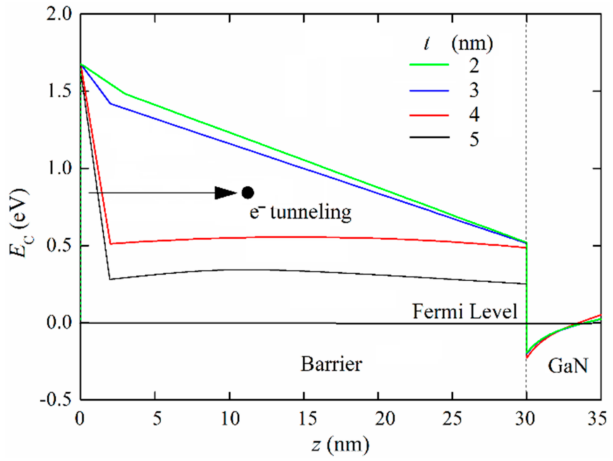


**Figure 3.** Conduction band energy minimum vs. depth under the gate, when varying the thickness of the donor traps layer beneath the gate: $t$ = 2, 3, 4, and 5 nm.

This effect is observed in Figure 4, where transfer characteristics (left axis) and corresponding gate current (right axis) are represented. Note that, in an off-state regime, gate and drain measured currents (with symbols) coincide, demonstrating that all leakage current through the gate is collected by the drain terminal. Numerical simulation data (with lines) show that the subthreshold current increases with the trap layer thickness, and, for a value of 4 nm, the difference between measured and simulated subthreshold current is reduced in more than five orders of magnitude, with a correct prediction in strong inversion regime being maintained. Higher values (e.g., $t$ = 5 nm) are not suitable because transfer characteristics deteriorate, since the threshold voltage suffers a considerable reduction not observed in measurements.

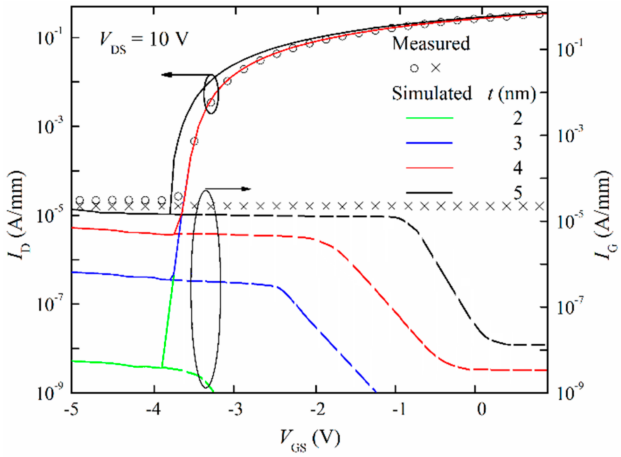


**Figure 4.** Measured (circles) and simulated (solid lines) transfer characteristics in logarithmic scale (left axis), and corresponding measured (crosses) and simulated (dashed lines) gate current (right axis).

It can be noticed that had TAT emission been considered, instead of FN emission, similar results would be obtained. However, with FN emission, there is no necessity of introducing TAT at room temperature, opposite to [25], in order to model drain current continuity.

## 4. Modeling

Most existing compact models for HEMT are based on a two-dimensional electron gas (2-DEG) precise description at the AlGaN-GaN heterojunction. Charge and current models tend to end up being complex and unattractive for circuit design, due to the evaluation of the Fermi level (i.e., the

charge in the channel) when considering the existence of several energy levels in the corresponding 2-DEG quantum well.

However, assuming a triangular quantum well potential with the contribution of the first energy level being the one taken into account, with most of the 2-DEG concentration, a simple relationship between the applied voltage and the 2-DEG concentration, $n$, can be established [26]:

$$n = DV_{\mathrm{TH}} \ln\left[\exp\left(\frac{E_F - E_0}{V_{\mathrm{TH}}}\right) + 1\right] \approx \frac{\varepsilon}{qd}(V_{\mathrm{G}} - V_{\mathrm{T}} - E_{\mathrm{F}}) \quad (1)$$

where $D$ represents the density of states, $V_{\mathrm{TH}}$ is the thermal voltage, $E_{\mathrm{F}}$ is the Fermi level, $E_0$ the position of the first energy level in the quantum well, $\varepsilon$ is the AlGaN barrier dielectric permittivity, $d$ the barrier thickness, $q$ the absolute charge of an electron and $V_{\mathrm{T}}$ is the transistor threshold voltage.

In addition, this gives, as a result, an analytical and simple model for the drain-to-source current, $I_{\mathrm{D}}$, through the GaN channel, maintaining the accuracy and covering all operating regimes for long channel devices, which is given by [26]:

$$I_{\mathrm{D}} = -\frac{q\mu W}{L}\left[\frac{qd}{2\varepsilon}\left(n_{\mathrm{D}}^2 - n_{\mathrm{S}}^2\right) + \frac{2}{5}\gamma_0\left(n_{\mathrm{D}}^{\frac{5}{3}} - n_{\mathrm{S}}^{\frac{5}{3}}\right) + V_{\mathrm{TH}}(n_{\mathrm{D}} - n_{\mathrm{S}})\right] \quad (2)$$

where $n_{\mathrm{S}}$ and $n_{\mathrm{D}}$ are the 2-DEG concentration at the source and drain terminals, respectively, $\mu$ is the electron mobility in the channel (evaluated as in [26]), $W$ is the gate width (1000 μm), $L$ the channel length (2 μm), and $\gamma_0$ is a fitting parameter. This model is suitable for different geometries and substrate materials, with the self-heating effects being incorporated through a device thermal resistance, $R_{\mathrm{TH}}$, as in [27], where the device temperature increment, $\Delta T$, respecting room temperature, is evaluated as the product $R_{\mathrm{TH}} I_{\mathrm{D}} V_{\mathrm{DS}}$. Compact model parameters used in this work are summarized in Table 1. For the thermal resistance, a realistic value of 52 K/W is assumed (30 K/W in [28], as the sum of the silicon substrate resistance, 17.4 K/W [23], and that for the semi-insulating transition layers of the GaN buffer-AlN, pGaN, etc., 0.5 μm thick in [29]).

**Table 1.** Compact model parameters.

| Parameter | Value | Unit |
|---|---|---|
| $d$ | 30 | nm |
| $V_{\mathrm{T}}$ | −3.8 | V |
| $\gamma_0$ | $2.12 \times 10^{-12}$ | $\mathrm{Vcm}^{4/3}$ |
| $R_{\mathrm{TH}}$ | 52 | K/W |

The large signal scheme of the compact model, which is implemented in the electrical simulator ADS (from Keysight) employing the industry modeling language for analog circuits and devices Verilog-A, is presented in Figure 5, where the Schottky gate is modeled through diodes $D_{\mathrm{gd}}$ and $D_{\mathrm{gs}}$, from gate-to-drain and gate-to-source intrinsic nodes, respectively.

Parasitic resistances in source and drain terminals, $R_{\mathrm{S}}$ and $R_{\mathrm{D}}$ (temperature-dependent), which are decisive for the DC performance evaluation of HEMTs, are incorporated with data extracted from simulations. Both of them, particularly $R_{\mathrm{D}}$, are higher as the device temperature increment rises, as Figure 6 shows (squares). A second-order polynomial is enough to fit this dependence (solid lines), that is $R_{\mathrm{S/D}} \approx a + b\Delta T + c\Delta T^2$; fitting parameters, $a$, $b$ and $c$, are indicated in Table 2.

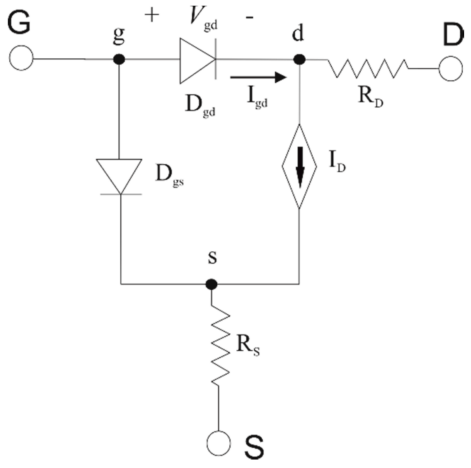


**Figure 5.** HEMT large signal equivalent circuit.

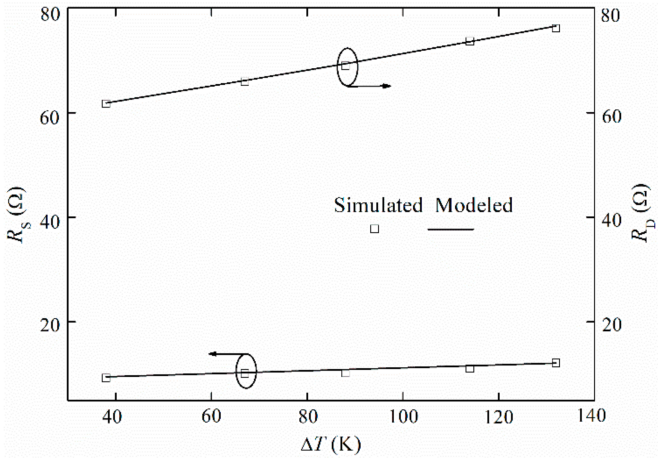


**Figure 6.** Numerical (symbols) and modeled (lines) $R_S$ (left axis) and $R_D$ (right axis) against device temperature increment.

**Table 2.** Fitting parameters for $R_S$ and $R_D$.

| | $R_S$ | $R_D$ |
|---|---|---|
| $a$ (Ω) | 8.1 | 56.4 |
| $b$ (Ω/K) | 0.03 | 0.13 |
| $c$ (Ω/K$^2$) | - | $1.4 \times 10^{-4}$ |

The gate leakage current could flow from gate to drain terminals through the top surface of the AlGaN barrier or, vertically, crossing the barrier through the GaN channel [19]. Numerical simulations with TE, PF and FN emissions show that the second case is taking place in the HEMT under study, as Figure 7 indicates for reverse-biased gate ($V_{GS} = -5$ V and $V_{DS} = 10$ V), with the current density flowing through the barrier, under the gate, by the drain side.

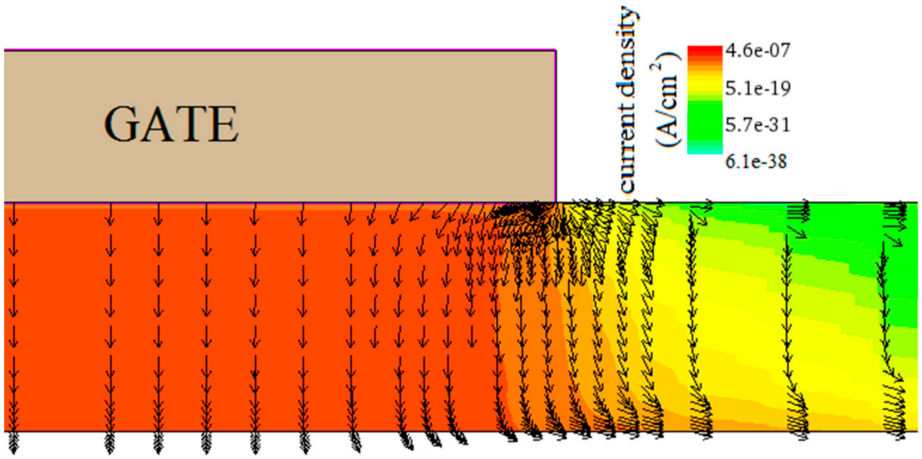


**Figure 7.** Current density flow through the barrier; $V_{GS} = -5$ V and $V_{DS} = 10$ V.

Gate leakage current has been already modeled analytically in a surface potential-based compact model [30], with TAT emission having been introduced in order to keep current continuity. However, for simplicity, it is proposed to introduce the gate leakage current into the compact model by a single and non-ideal continuous expression for the current of the gate-to-drain diode, which is given by:

$$I_{gd} = W \times L\left[j_s \times \left(exp\left(\frac{V_{gd}}{m \times V_{TH}}\right) - 1\right) - j_{off}\right] \quad (3)$$

where $j_{off}$ corresponds to the gate leakage current density in subthreshold regime by PF and FN emissions, $j_s$ is the reverse saturation TE current density, and $m$ is the non-ideality parameter for Schottky gates in AlGaN/GaN based HEMTs [30], which could be properly set when forward gate-to-drain current is available (which is not the case for typical operation regimes).

For typical operation regimes of the HEMT (off, linear and saturation regimes), when the Schottky gate is reverse-biased, the absolute value of the current density of the drain-to-gate diode, $j_{gd}$, can be approximated by

$$j_{gd} = j_s + j_{off} \quad (4)$$

condition for which measurements were collected. Then, equaling $j_{gd}$ (4) to the total measured reverse density current of the Schottky gate and attending that, from numerical simulations, the TE term represents 0.026% of the total reverse density current, 112 $\mu A \cdot cm^{-2}$ and 29 $nA \cdot cm^{-2}$ are obtained, respectively, for $j_{off}$ and $j_s$.

Thus, the resulting modeled (dashed line) and measured (symbols) transfer characteristics in saturation regime (left axis, with $V_{DS} = 10$ V), in logarithmic scale, are represented in Figure 8a, together with the corresponding gate current (right axis) in a similar way. A good correspondence between modeled and measured data has been achieved, with an average relative error of 8.3% (around $V_{GS} = 0$ V) and 0.6%, respectively, for the drain and gate current. And, again, drain and gate currents in subthreshold regime do match. Similarly, measured and modeled output characteristics (left axis), with the corresponding gate current (right axis), are represented in Figure 8b for different gate voltages. A good agreement is, again, observed, with an average relative error of 1.8% and 1% for the drain and gate current, respectively. Therefore, our model (4) can be considered appropriate for the leakage current of GaN-based HEMTs, through the Schottky gate, within typical operation regimes.

Other physics-based models accounting for reverse gate leakage current have been developed. In [31] the model is based on the characteristic energy related to the tunneling probability in the Wentzel–Kramers–Brillouin approximation, considers mainly TE based mechanisms, and the study is applied to leakage behavior in aged devices. In [32] the model is based on surface donor traps under the gate plus the volume density of bulk traps present in the AlGaN layer and the trap energy

dependent rate constant. Notice that the "two-step" gate metal surface traps (filled interface trap states) plus bulk traps tunneling (GaN on SiC process) of [32], is quantified in our work and also located in depth and thickness since a donor trap layer at defined depth emerge in simulations matching suggestions from device manufacturing (in a GaN on Silicon process). However, as simplification is mandatory in compact modeling for circuit designers, our model offers a simpler and differentiable analytical expression for the Schottky gate leakage current of GaN-based HEMTs, which is valid for circuit simulation purposes, while supporting accurately the underlying physics, including the relative weight of PF, FN and TE mechanisms.

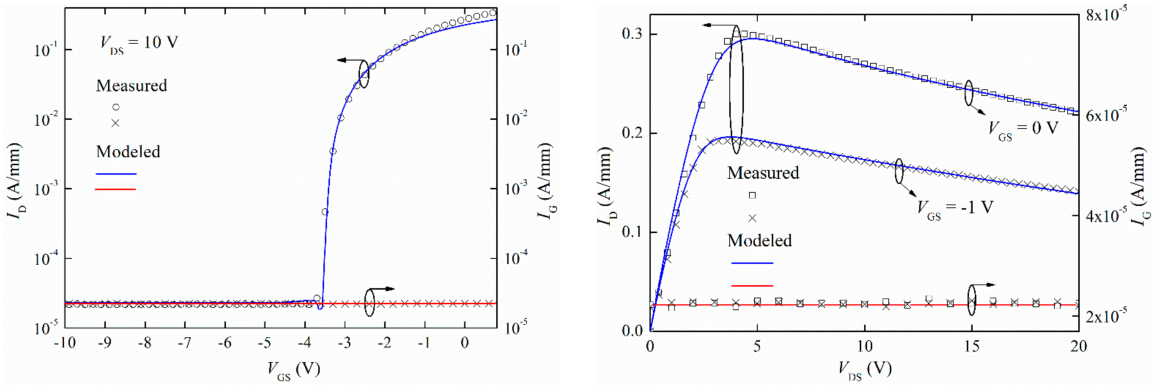


**Figure 8.** Measured (symbols) and modeled (lines) (**a**) transfer characteristic in saturation regime (left axis, with $V_{DS}$ = 10 V) and corresponding gate current (right axis), in logarithmic scale, and (**b**) output characteristics (left axis) and corresponding gate current (right axis), at different gate voltages: $V_{GS}$ = −1 and 0 V.

## 5. Conclusions

In this work, a gate leakage current in subthreshold regime for an AlGaN/GaN-based HEMT, grown on silicon, has been detected and quantified through measurements and numerical simulations. The gate leakage current is attributed to non-local FN tunneling and Poole–Frenkel emission, with donor trap concentration, activation energy, cross-section, and depth being set beneath the gate. Numerical simulations demonstrate that the gate leakage current flows across the barrier, towards the GaN channel, which has been successfully modeled making use of Verilog-A through a simple analytical expression, which is valid for circuit simulation purposes and typical operation regimes of the transistor, while accurately supporting the underlying physics. Relative errors between measured and modeled data for the gate leakage current demonstrate the validity of our model, which has been successfully incorporated into a DC compact model.

**Author Contributions:** R.R. developed the study, which was directed by B.G., J.G. aided to develop the model for the gate leakage current. F.M. provided the measurements, and G.T. and A.N. assisted on numerical simulations and trapping effects, respectively.

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**Conflicts of Interest:** The authors declare no conflict of interest.

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