A Wide-band Noise-Cancelling CMOS LNA based on Current Conveyors

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***Abstract*— In this paper, a Wide-band CMOS low-noise amplifier (LNA) based on Current Conveyors (CC) is presented, in which the thermal noise of the input MOSFET is cancelled by exploiting a noise-cancelling technique. This new LNA offers the following notable advantages over existing topologies: wideband performance, with a stable frequency response from 0 to 6.2GHz and wideband input matched impedance with a total absence of passive elements; a low Noise Figure (NF) and high linearity. Comparisons with other topologies prove the effectiveness of the new implementation.**

Index Terms— RFIC; low noise amplifier (LNA); Current Conveyor, Noise Cancelling; CMOS.

I. INTRODUCTION

One of the key elements within a wideband receiver is the Low Noise Amplifier (LNA). As the first element in the reception chain, its Noise Figure (NF) and gain affects the total performance more than the rest of the blocks. Therefore, it should exhibit the lowest NF and the greatest possible gain over a wide frequency range. Moreover, source impedance matching (i.e. $Z_{IN}=R_S$) is usually wanted to limit reflections.

Typical basic wideband LNAs such as the resistively terminated common-source (CS), the common-gate (CG), etc., have difficulties in meeting the above-mentioned requirements [1]. On the other hand, amplifiers exploiting global negative feedback achieve low NFs with good input matching, but they are prone to instability [2]. Other alternatives such as distributed amplifiers (DAs) [3] or cascode amplifiers with LC broad band input matching networks [4][5][6] provide good impedance matching and high gain over a wide range of frequencies, but require a large number of high-quality inductors, making it difficult to implement them in a small area.

Another topology that is being used to design wideband LNAs is based on the use of current conveyors (CC) [7][8][9]. Although they have a number of advantages such as good input matching, high linearity and low power consumption, the achieved NF is relatively high.

In this paper, the concept of noise cancellation [10][11][12] is applied to the design of a wideband LNA based on CC. Thus, the ultimate goal will be to present an amplifier which combines the benefits of having a topology based on CC and the possibility of reducing the NF at the output of the circuit.

Section II introduces the wideband amplifiers based on CC. In section III, the noise cancelling techniques for CG amplifiers are presented. Section IV presents the proposed amplifier based on CC with noise cancelling. Simulation results for the proposed LNA implemented in a 65nm CMOS process are reported in Section V. Finally, conclusions are given in Section VI.

II. CMOS CURRENT CONVEYOR LNA

This section briefly presents the amplifiers based on current conveyors using CMOS technology. Fig. 1 shows the basic topology with ideal current sources. It consists of an input CG gain stage (M1), followed by a source follower stage (M2) [8]. The transistors are biased by the current sources I01 and I02, which in the actual circuit will be realized by current mirrors.

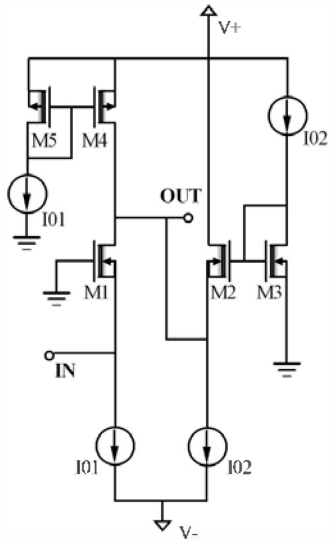

Fig. 1 LNA based on CC with ideal current sources.

The basic circuit can be described by the following equations:

1) DC gain :

$$G=\frac{gm1}{gm2} \qquad (1)$$

where gm1 and gm2 are M1 and M2 transconductances, respectively.

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2) Bandwidth:

$$f_{-3dB}=\frac{gm2}{2\pi C_T} \quad (2)$$

where C_T represents the total parasitic capacitance at the output node.

3) Noise Factor:

$$NF=1+\gamma\left(1+\frac{gm2}{gm1}+\frac{gm4}{gm1}\right) \quad (3)$$

being γ the excess noise factor which is a constant that depends on the transistor size.

4) Input and Output Impedances:

$$Zin=\frac{1}{gm1} \quad (4)$$

$$Zout=\frac{1}{gm2} \quad (5)$$

As can be seen, the transistor sizes and the bias currents affect all circuit parameters. There is a tradeoff between gm1 and gm2 and, as a consequence, between the transistor sizes and their bias currents.

I01 through gm1 affects the gain but has no effect on the bandwidth, whereas I02 controls both gain and bandwidth through gm2 so that, if I02 increases, the bandwidth increases, but the gain decreases.

On the other hand, equation (3) shows that the NF decreases when gm1 is increased. It can be done by increasing the size of M1 or the current I01. Also, the NF is reduced if M2 and M4 are smaller or biased with a lower I02.

Finally, the input and output impedances are directly related to their associated transistors and bias currents. For example, through I01, Zin can be matched to the source impedance without resorting to matching networks, enabling a much smaller circuit than conventional topologies. This is one of the main advantages of this topology.

Fig. 2 shows the actual schematic of the circuit where the ideal current sources have been substituted by current mirrors. As can be seen, the number of transistors has increased considerably, affecting the circuit performance, especially the bandwidth, the noise and the power consumption. Also, it is important to note that, in deep sub-micron technologies, due to the low output resistance of the transistors, the input impedance is deviated from the conventional value of 1/gm. This, rather than being a problem, can be useful for isolating the conditions of input matching with noise cancellation by importing one degree of freedom that is the load impedance in satisfying the input matching condition [13].

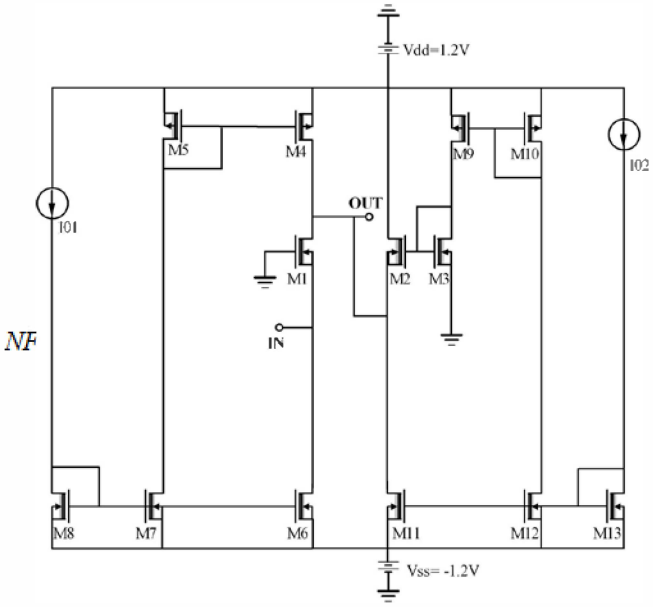


Fig. 2 LNA based on CC with current mirrors as current sources.

III. Noise Cancelling Technique applied to a CG-stage

As explained above, the main contributor to the noise is the input transistor (M1). This transistor is in common-gate configuration so, in this section, the noise cancellation techniques for CG amplifiers are presented [10][11][12].

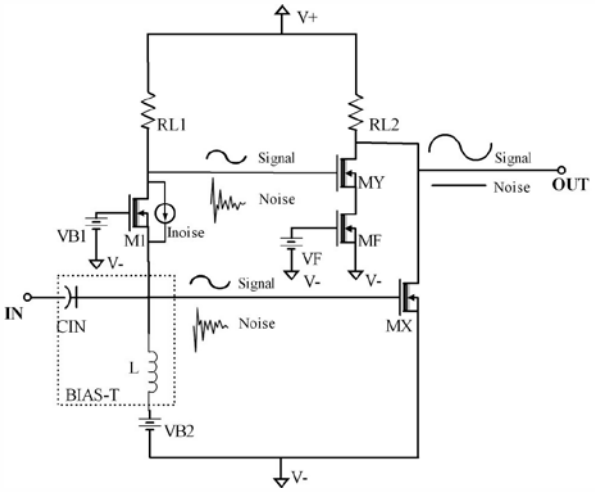


Fig. 3 The Noise Cancelling Technique applied to a CG-stage.

The typical noise-cancelling CG LNA is shown in Fig. 3. In this technique the noise of the input transistor after passing along two different paths, i.e. transistors MX and MY, is cancelled at the output while the input signal is boosted. This can be seen better in the inset of Fig. 3 where the noise and the signals are plotted on the schematic. The noise generated by M1 can be represented by a current source (i_{noise}) which generates a voltage at its source and a fully correlated voltage at its drain in anti-phase. After passing through the CS inverting stages MX and MY, these noise voltages are cancelled. On the other hand, the input signal is amplified via two paths, an inverting CG-CS path (transistors M1 and MY)

and an inverting CS path (transistor MX) so they are summed at the output.

For perfect noise cancelling, the two noise paths should present the same gain. For this reason, transistors MX and MY must be biased independently. Also it is important to note that the circuit elements used to cancel the noise of M1 (MX, MY and RL1) also introduce noise to the circuit. Thus, the key to a low overall NF has now shifted to a low noise implementation in the noise cancelling stage.

IV. LNA BASED ON CC WITH NOISE CANCELLING

The proposed LNA based on CC with noise cancelling is depicted in Fig. 4. This circuit combines the CC based LNA shown in Fig. 2 and the cancelling technique presented in Fig. 3. As explained above, the use of a CC based LNA as the input stage gives a degree of freedom in satisfying the input matching condition compared to a simple CG stage.

In the design of this circuit, the input stage should be sized to obtain a good input impedance matching over a wideband. The size and the bias of the noise cancelling stage must be chosen according to broadband noise cancellation as well as minimizing its noise. Also it should be sized to affect as little as possible the gain, the bandwidth, the power consumption and the input matching.

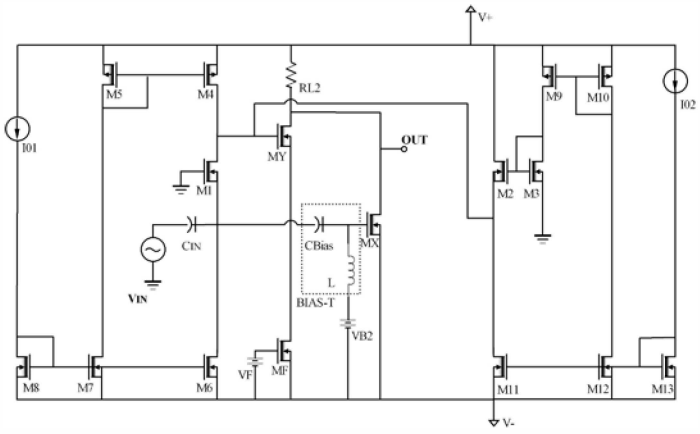


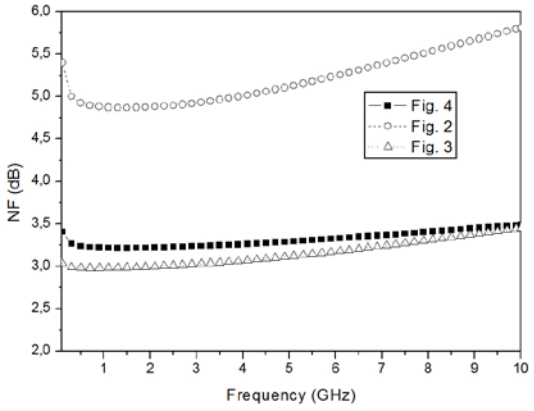
Fig. 4 Proposed LNA basedon CC with noise cancelling.

V. SIMULATION RESULTS

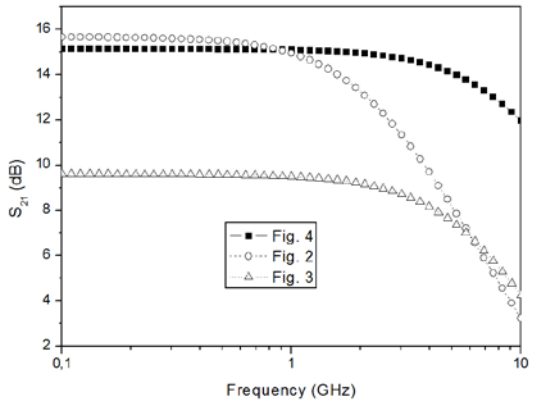
The circuits presented in this paper (Fig. 2, Fig. 3 and Fig. 4) have been designed using the UMC CMOS 65nm process under a ±1.2V supply voltage and simulated using Advanced Design System (ADS) software.

Fig. 5 shows the noise figure, the gain (S_{21}) and the input matching (S_{11}) for the three designs.

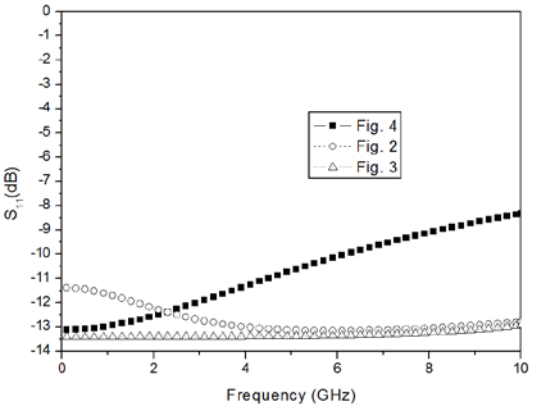
Fig. 5.a shows that without noise cancelling, the amplifier based on CC achieves a high NF and, when the noise cancelling technique is applied, the NF lowers to 3.5dB which is practically the same NF as a simple CG with noise cancelling.



(a)



(b)



(c)

Fig. 5 Comparison between the circuits presented in this paper (Fig. 2, Fig. 3 and Fig. 4): a) NF, b) S21 and c) S11.

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However, as shown in Fig. 5.b, the gain of the amplifiers based on CC is more than 5dB larger than the simple CG with noise cancelling.

Finally, Fig. 5.c shows that at low frequencies the three circuits achieve a good input matching with a S_{11} below -10dB. However at high frequencies (above 6.2GHz) the proposed amplifier input matching starts to get worse. This can be solved by simply increasing the bias current I02 at the expense of a slightly increased power consumption.

The performance of the proposed LNA and comparison with the previous designs and existing LNAs based on CC [9] or CG with noise cancelling [12] are summarised in Table 1. As shown in the table, the proposed LNA provides a good gain similar to the basic CC amplifier of Fig. 2 or [9], with a low NF comparable to the CG with noise cancelling of Fig. 3 or [12]. On the downside, the power consumption is slightly higher due to the increased number of transistors compared to the basic circuits.

Table 1: Performance summary of the proposed LNA and comparison with the existing work

Ref.	CMOS Technology	S_{11} (dB)	G_{MAX} (dB)	BW (GHZ)	NF (dB)	IIP3 (dBm)	Power (mW)
Fig. 4	**0.65 nm**	**-13**	**15.13**	**6.2**	**3.21 – 3.4**	**7.6**	**18.6**
Fig. 2	0.65 nm	-11.3	15.65	2.2	4.9 – 5.4	-3.4	12
Fig. 3	0.65 nm	-13.4	9.6	6	3 – 3.2	-	13.05
[9]	0.35 µm	-	10.2	3.1 – 10.6	5.1	-	5.6
[12]	0.18 µm	< -11	9.7	1.2 – 11.9	4.5 – 5.1	- 6.2	20

One important benefit of the proposed circuit is that its linearity is improved. This is due to the fact that the same mechanism leading to cancellation of the output noise due to the matching devices is also capable of partially cancelling the nonlinear distortions [13].

VI. Conclusions

In this paper, a wide-band CMOS LNA based on CC exploiting a noise cancelling technique is proposed. The concept of noise cancelling seen here consists of the following functional blocks: an amplifier stage providing the source impedance matching which is based on a CC amplifier; an auxiliary amplifier sensing the voltage (signal and noise) across the real input source; and a network combining the output of the two amplifiers, such that noise from the matching device cancels while signal contributions add.

Simulation results show that the proposed LNA achieves good input impedance matching, high gain and low noise figure in 0-6.2GHz frequency range, at the price of power dissipation in the auxiliary amplifier. Also, the linearity is improved because the noise-cancelling technique is also capable of partially cancelling the nonlinear distortions.

Acknowledgement

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