A Single-Capacitor Bootstrapped Power-Efficient CMOS Driver

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A Single Capacitor Bootstrapped Power Efficient CMOS Driver

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***Abstract*— A high speed and low power driver employing a single bootstrap capacitor is reported. It provides a six–fold improvement in the power dissipation, 15% higher speed, and 8.7% reduction in the active area when compared with the fastest reported driver [8] using bootstrap techniques, under similar loading conditions and circuit parameters.**

I. INTRODUCTION

Bootstrapping is an efficient technique for speed enhancement and power reduction. Most bootstrap circuits are based on BiCMOS technology [1] – [3]. But with reduction in supply voltage to less that 1.5 volts use of the conventional BiCMOS circuit design techniques are no longer possible.

With the widespread use of low voltage and low power CMOS circuits, research into design of drivers employing CMOS bootstrap circuits techniques has accelerated in the recent past [4] – [9]. CMOS bootstrapping requires access to bulk nodes of PMOS and NMOS devices. Designs in [5], [6], [8] and [9] rely on twin–well CMOS processes to provide access to the bulk nodes. Bootstrap design in [7] uses a p–well only process. It makes use of NMOS devices for both pull–down and pull–down switching operations. However, this will not allow for maximum voltage swing during the pull–up due to threshold voltage loss in the NMOS transistor. Designs in [4] – [8] achieve bootstrapping by an indirect technique. In the indirect technique the bootstrapping is applied to the gates of devices at the output stage of the driver to improve the drive capability during the switching transitions. However, since the threshold voltage of the MOS devices do not scale down with same factor as the power supply, the indirect bootstrapping may not be very effective in driving the large capacitive loads [9]. In [9] design of a direct bootstrap technique has been discussed. In the direct technique the bootstrapping is directly applied to the output node, thereby improving the driver speed.

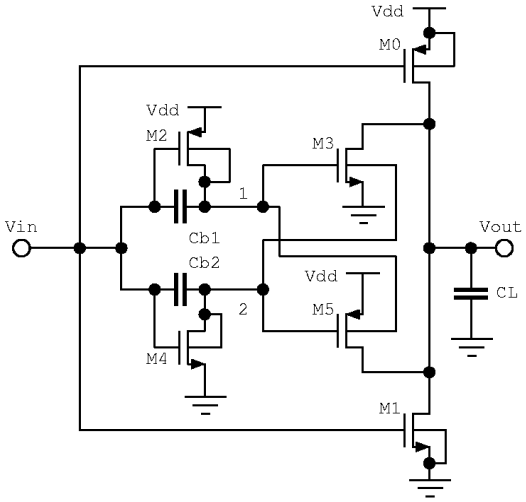

Figure 1. CMOS inverting *CK*–driver

CMOS bootstrap circuits reported in [4] – [9] require two bootstrap capacitors; one for bootstrapping during the low-to-high switching transition and one for the high-to-low.

In this paper, we provide a new bootstrap driver circuit, termed the *F*–driver, which offers improvements in terms of speed, power and area compared with the fastest CMOS indirect bootstrap driver circuit – the *CK*–driver [8] (Figure 1) and direct bootstrap driver circuit the *D*–driver [9] (Figure 2). In our proposed direct bootstrap technique, the voltage across bootstrap capacitor is directly coupled to the output node during the switching transitions. Furthermore our design requires only one bootstrap capacitor to achieve bootstrapping for both switching transitions.

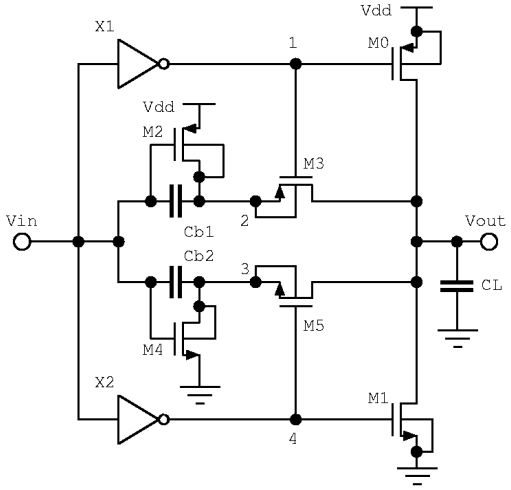

Figure 2. CMOS inverting *D*–driver

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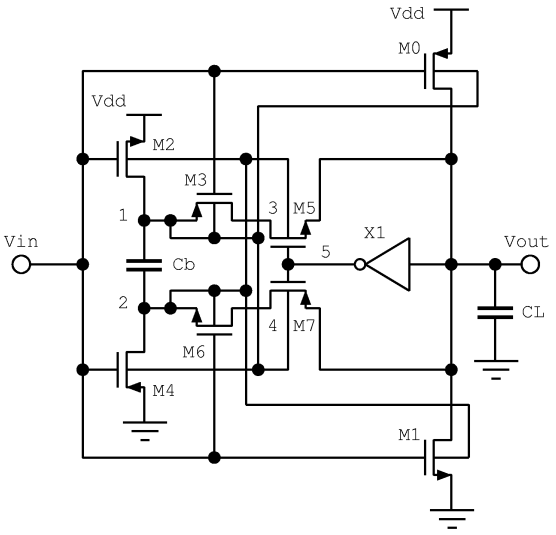

Figure 3. CMOS inverting *F*–driver

The rest of paper is organized as follows. In Section II we introduce the structure of the *F*–driver. In Section III we describe the principle of operation of the *F*–driver circuit. In Section IV we analyze the performance of the *F*–driver circuit and provide simulation results. Section V concludes the paper.

II. *F*–DRIVER CIRCUIT STRUCTURE

The circuit diagram of the *F*–driver is shown in Figure 3. This circuit provides a full logic swing at the output, and unlike other reported bootstrap designs, requires only a single bootstrap capacitor to couple the charge from the internal nodes 1 and 2 onto the output node. A single capacitor results in lower area and power dissipation.

The channel widths of M0, M1 are 100μm and 50μm, respectively. All other transistors have minimum sized channel width of 0.18μm. The channel length for all transistors is 0.18μm. The bootstrap capacitor Cb is realized using PMOSFET, with its drain, source and body terminals connected together with a channel width of 10μm.

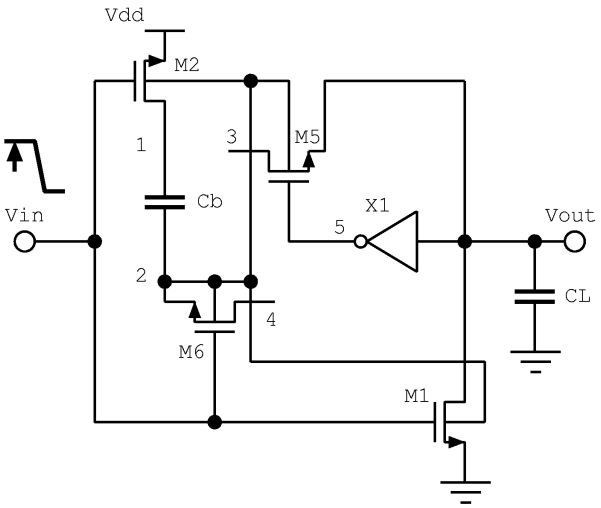

Figure 4. Equivalent inverting *F*–driver when input is high

To reduce power dissipation the circuit in Figure 3 is designed to confine the bootstrapping action to a narrow time window during the output transitions. The bootstrap capacitor Cb, is used for both pull–up and pull–down bootstrapping operations. In the circuit of Figure 3, the body terminals of PMOS transistors are connected to node 1 instead of the Vdd node, while the body terminals of NMOS transistors are connected to node 2 instead of the GND node. Thus, the internal voltage overshoot at node 1 and undershoot at node 2 do not cause forward biasing of source/drain–substrate junctions. The back gate capacitive coupling also, greatly enhances the bootstrapping during the output transitions.

III. *F*–DRIVER CIRCUIT OPERATION

The equivalent circuit diagram of the *F*–driver in Figure 3 when input is high is presented in Figure 4. As shown in Figure 4, when input is high M0 is turned off and M1 is turned on causing the output node to pull low. M2 is on charging node 1 to Vdd–VTn. M3 is off isolating node 1 from node 3. Inversion by the inverter X1 turns M5 on, pulling node 3 low. At the same time, M4 is off locking the charge on node 2. M6 is on shortening the path from node 2 to node 4. M7 is off isolating node 4 from the output.

Similar analysis can be applied to describe the circuit in Figure 3 when the input is low. Figure 5 illustrates the equivalent circuit for the *F*–driver when input is low. In that case, M1 is turned off and M0 is turned on causing the output node to pull high. M4 is on charging node 2 to VTp. M6 is off isolating node 2 from node 4. Inversion by the inverter X1 turns M7 on pulling node 4 high. At the same time, M2 is off locking the charge on node 1. M3 is on shortening the path from node 1 to node 3. M5 is off isolating node 3 from the output.

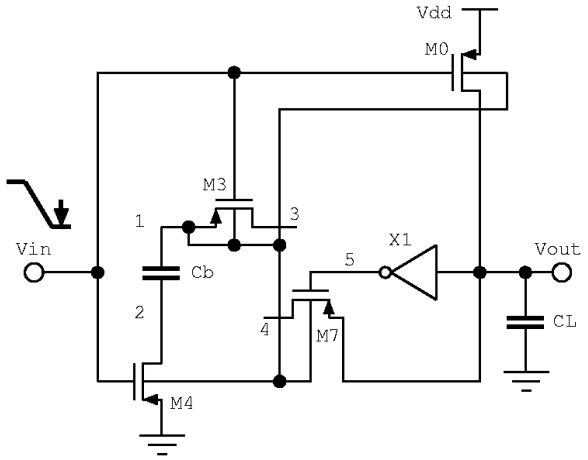

Figure 5. Equivalent inverting *F*–driver when input is low

The equivalent circuit diagram of the *F*–driver during the high to low transition at the input is shown in Figure 6. During this input transition, the delay across the inverter X1,

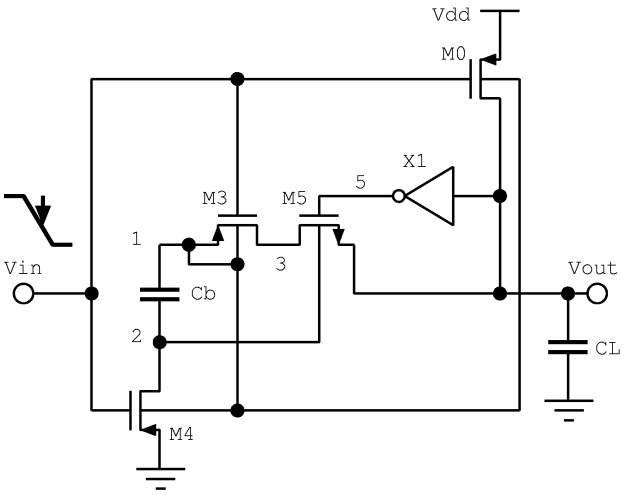

Figure 6. Equivalent inverting *F*–driver during input transition from high to low

presents a brief period of time when M3 and M5 are both simultaneously on, providing a path for coupling of high voltage across the bootstrap capacitor to the output node, resulting in the output node to go high quickly. Quick rise at the output causes the voltage at the node 1 to rise, to a value of 1.9V, due to the PN junction capacitance coupling across the drain and back gate terminals of transistor M0. Eventually, the transistor M5 turns off isolating the output from node 3. The rise at node 1 couples to node 2 across the bootstrap capacitor Cb resulting in an increase in the voltage at node 2 to VTp.

The similar equivalent circuit for the low to high transition at the input of the *F*–driver is illustrated in Figure 7. During this input transition, the delay across the inverter X1, presents a brief period of time when M6 and M7 are both simultaneously on, providing a path for coupling of high magnitude negative voltage across the bootstrap capacitor to the output node, resulting in the output node to go low quickly. Quick drop at the output causes the voltage

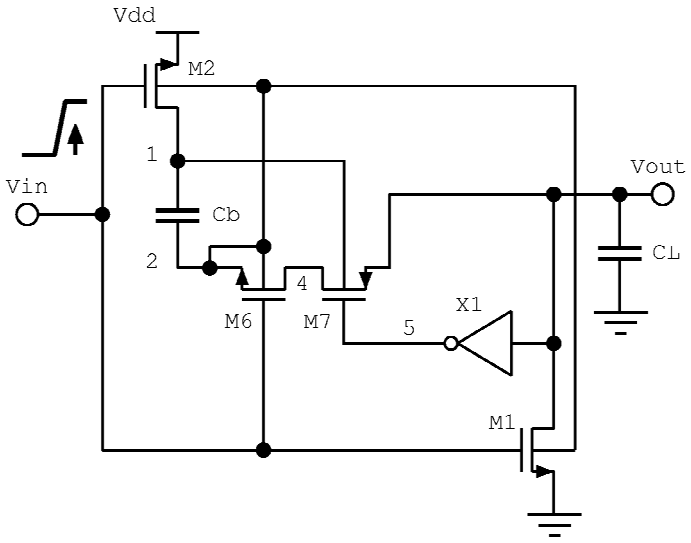

Figure 7. Equivalent inverting *F*–driver during input transition from low to high

at node 2 to drop to a value of –0.2V, due to the PN junction capacitance coupling across the drain and back gate terminals of transistor M1. Eventually, transistor M7 turns off isolating the output from node 4. The drop at node 2 couples to node 1 across the bootstrap capacitor Cb causing a drop in the voltage at node 1 to Vdd – VTn.

Further improvement in speed can be obtained by sizing the channel width of transistors M0, M1, M3 and M4. However, minimum sized values result in lowest area and power dissipation.

Figure 8 shows the transient waveforms of the *F*–driver with output load capacitance of 100fF at the input frequency of 500MHz.

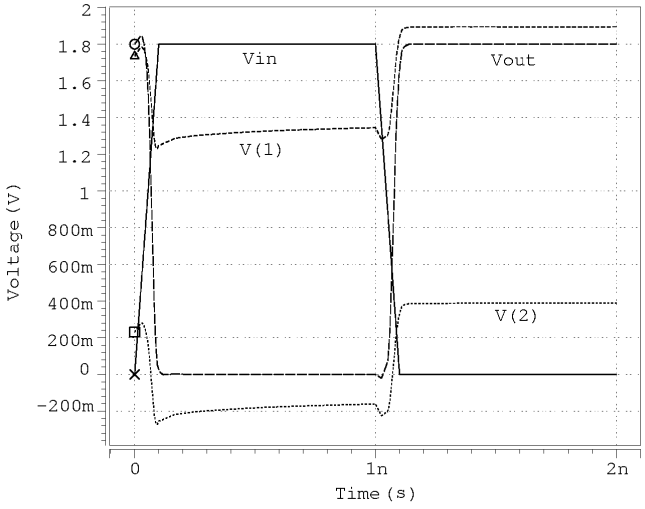

Figure 8. Transient waveforms of CMOS inverting *F*–driver

IV. COMPARISON AND DISCUSSION

To assess the performance of the *F*–driver, a test circuit based on 0.18μm Mixed–Signal SALICIDE process from TSMC has been designed. To compare our work with the *CK*–driver [8] and the *D*–driver [9], we reimplemented those designs using the same technology from TSMC. They were simulated at 500MHz input frequency with 100ps rise and fall times, a supply voltage of 1.8V, and the output capacitive load in the range of 10fF to 100fF.

The active area of the *F*–driver is 29.1μm^2 which is 8.7% less than the *CK*–driver. Figure 9 plots the propagation delay versus the output load. As seen the propagation of delay of the *F*–driver is 15% and 52% less than that of the *CK*–driver and the *D*–driver, respectively, over the range of output loads. According to our simulation, the *F*–driver provides an approximate power dissipation saving of 83% and 85% compared with the *CK*–driver and the *D*–driver, respectively, over the range of output loads.

We use the delay-area-power product as the figure of merit to provide an overall comparison between the various bootstrapping driver circuits. The figure of merit for the *F*–

driver is 6 – 7 times smaller than that of the *CK*–driver over the range of output loads and employing the same technology.

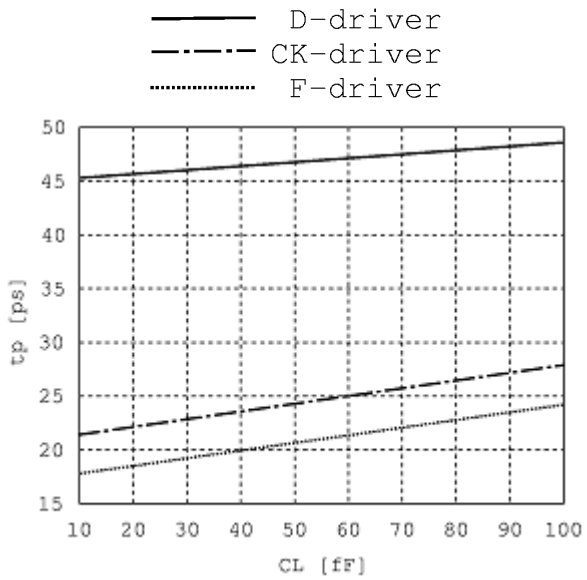

Figure 9. Propagation delay time versus output load capacitance

V. CONCLUSION

This paper presented the design for a novel single bootstrap capacitor driver. For a supply voltage of 1.8V, the *F*–driver reduces the power dissipation by a factor of 6 while keeping the speed and the area marginally lower than the *CK*–driver [8]. Furthermore, the *F*–driver demonstrate a superior performance over the *D*–driver [9].

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