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Conference Paper · June 2007

DOI: 10.1109/ISCAS.2007.378047 · Source: IEEE Xplore

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Adaptive Low/High Voltage Swing CMOS Driver for On–Chip Interconnects

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***Abstract*— This paper reports the design of a high performance, adaptive low/high swing CMOS driver circuit (*mj–driver*) suitable for driving of global interconnects with large capacitive load. When implemented on 0.13μm CMOS technology, *mj–driver* performs 16% faster, reduces the power consumption by 3%, and energy delay product by 19% when compared with a counterpart driver in diode–connected configuration. On the other hand, *mj–driver* has 47% lower active area and only requires one set of sizing for optimum performance at 1 and 0.8V. Furthermore, unlike its counter part which exhibits 30% variation in output swing voltage with variation in the load, the output voltage swing for the proposed driver remains unchanged with the output load. Comparisons of the proposed driver with conventional full swing CMOS driver are presented as well, indicating a significant saving in energy, due to the reduced swing voltage. The proposed driver has the ability to switch from a low swing to high swing mode, through a line monitoring mechanism.**

I. Introduction

Long global wires (busses, clock, and timing signals) constitute the major source of delay and on–chip power consumption in the state of the art digital circuits. The nature of delay with the global interconnet is such that they do not scale with technology generations. Driving large capacitive loads associated with the global interconnects limits the performance and power dissipation of CMOS circuits at low voltages. Several fast drivers for large capacitive load have been reported (see, e.g. [1]–[6]).

Most effective technique for global interconnects to achieve power reduction and energy–delay efficiency is to reduce the voltage swing of the signal on the wire. However, reducing the voltage swing reduces the noise margin. Most low voltage techniques to–date [6] rely on extra power supply, or reference voltage, multiple threshold process technology, large area penalty, and multiple wire interconnects. They also suffer from lager short-circuit current problem, long propagation delay, and high power dissipation [6].

The drivers for long interconnects are categorized according to the direction of the swing voltage reduction in their output [2], [6]. In Up Low swing voltage Driver (ULD) the output voltage ranges between 0 and (`Vdd-2Vtn`), where `Vtn` is the nMOS transistor threshold voltage. In Down Low swing voltage Driver (DLD) output voltage ranges between `2|Vtp|` and `Vdd`, where `Vtp` is the pMOS transistor threshold voltage. In Up–Down Low swing voltage Driver (UDLD), on the other hand, the output voltage symmetrically ranges between `Vtp` and `Vdd-Vtn`.

Alternative circuits based on differential current–mode schemes have shown to have a distinct advantage [6] over the single–ended ones in terms of noise immunity and signal integrity, which is of prime importance in the Very Deep Submicron (VDSM) designs. However, they double the number of wires in a data bus.

In order to improve the driving capability some driver circuits rely on bootstrapping techniques [4], [5]. However, these circuits require extra bootstrapping capacitors, and generally need access to the well terminals that is not available in most digital CMOS processes.

A diode–connected configuration has been used before [1], [3] as a way of reducting the energy–delay product. Unlike most alternatives, no extra power supply nor a multi–threshold process is required. However, diode–conntected drivers do not provide a sufficient driving capability for the larger loads. Furthermore, their performance is sensitive to variations in power supply, device parameter, and loading condition. They also perform poorly in presence of noise.

This paper presents a UDLD based adaptive low/high swing driver that has significant advantages in terms of delay and power compared to other UDLD drivers [2]. Features of the proposed driver (*mj–driver*) is compared with the circuit in [1] (*ddc–driver*) and a conventional 2-stage CMOS driver (*basic–driver*). The circuit proposed in this paper while using diode connected configuration at the output stage, provides a larger driving current during the logic transitions. This results in faster, lower power, and better energy efficiency. It also, improves robustness and sensitivity to power supply variation and device sizing. Furthermore, being adaptive it can conditionally switch from low swing to high swing by monitoring the noise condition on a high sensitivity line.

II. Driver Circuit Structure

Fig. 1 presents the circuit structure for *mj–driver*. It is a UDLD based low swing driver, where the output stage achieves symmetrical low swing through the use of diode connected transistors pairs (`MD10`–`MD11`) and (`MU10`–`MU11`).

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In addition to the output stage the circuit provides high current driving capability through the use of multi–path technique [7], where two separate paths are provided for assisting low–to–high and high–to–low transitions at the output (upper and lower half of the circuit in Fig. 1, respectively). The combination of these two paths and the feedback path through XIF1 provides for large output currents and fast switching of the output during the transitions, as will be described in the next section.

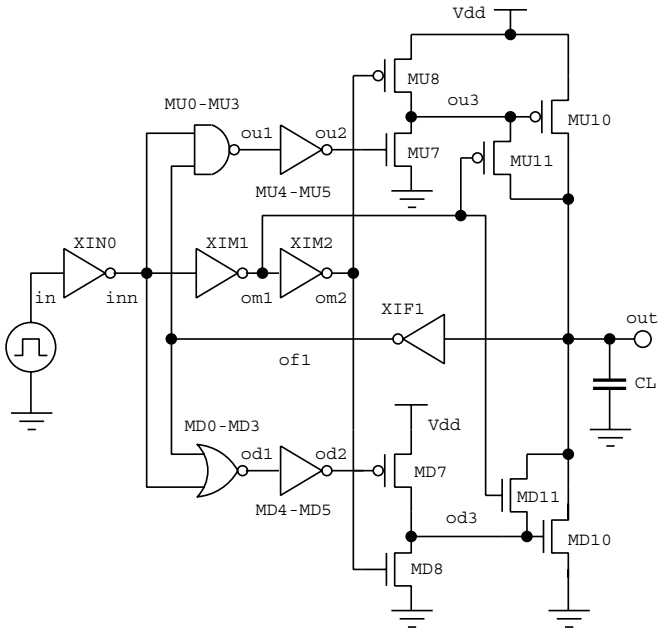

Fig. 1. Proposed low swing CMOS driver.

To provide a good comparison the *ddc–driver* and *mj–driver* circuits have been optimised for the propagation delay under the identical loading conditions, power supply and operating frequency. Both circuits are implemented in 0.13μm technology from UMC. The channel length of all transistors is 0.13μm. Table I shows the transistors sizing for two circuits, for 1V power supply.

Circuit optimisation for 0.8V power supply, does not require resizing of the proposed *mj–driver*. However, *ddc–driver* requires a different transistor sizing for the best performance for 0.8V power supply (see Table II), a clear disadvantage.

For operation at 500MHz frequency, the corresponding voltage swings for 1 and 0.8V power supplies are 0.49 and 0.42V, respectively, for the proposed *mj–driver*. For power supply of 1V, the voltage swing for *ddc–driver* varies from 0.69 to 0.49V, with the capacitive load in the range of 1 to 5pF. Similar voltage swing variation for *ddc–driver* for 0.8V power supply is from 0.62 to 0.42V. The variation in the voltage swing with the load condition is an undesirable feature that reduces the reliability and requires lowering the frequency of operation. Our simulations show that for the voltage swing for *ddc–driver* to remain constant at 0.69V for a load 5pF, an operating frequency as low as 500KHz (an order of magnitude reduction) is required.

TABLE I

CHANNEL WIDTHS FOR TRANSISTORS IN *mj–driver* AND *ddc–driver*.

ddc–driver for 1V			*mj–driver*		
Transistor	Type	Width (μm)	Transistor(s)	Type	Width (μm)
M1	N	59.5	PXIM1, MU2, MU3	P	4.0
M2	N	35.0	NXIM1	N	2.0
M3	N	82.0	PXIM2, PXIF1	P	2.0
M4	N	40.5	NXIM2, NXIF1	N	1.0
M5	P	37.5	MU0, MU1	N	5.0
M6	P	45.5	MU4	P	8.0
M7	P	9.8	MU5, MD8	N	0.28
M8	P	49.5	MU7	N	7.0
M9	P	4.1	MU8, MD0, MD1	P	5.0
M10	P	21.5	MU10	P	75.0
M11	P	0.28	MU11	P	34.0
M12	N	30.0	MD2, MD3	N	4.0
M13	N	8.0	MD4	N	8.0
M14	N	1.8	MD5	P	0.28
—	—	—	MD7	P	4.0
—	—	—	MD10	N	28.0
—	—	—	MD11	N	4.3

Triple well 0.13μm 1.2/3.3V process technology from UMC.

TABLE II

CHANNEL WIDTHS FOR TRANSISTORS OF *ddc–driver* WITH 0.8V SUPPLY VOLTAGE.

ddc–driver for 0.8V		
Transistor	Type	Width (μm)
M1	N	80.0
M2	N	6.0
M3	N	80.0
M4	N	40.0
M5	P	9.8
M6	P	44.5
M7	P	9.8
M8	P	85.0
M9	P	3.1
M10	P	29.5
M11	P	0.28
M12	N	30.0
M13	N	4.5
M14	N	1.8

Triple well 0.13μm 1.2/3.3V process technology from UMC.

III. CIRCUIT OPERATION

This section describes the operation of *mj–driver* in Fig. 1.

Low output: For output in low state we have inn=out=low, ou1=high, and ou2=low, MU7, MU10, and MU11 off, and MU8 on. In this state, the output is driven low through the diode connected pair MD10–MD11.

Low–to–high transition at the output: After a low–to–high transition at inn, due to delay in the feedback loop (XIF1), ou1, and ou3 will go low, and ou2 will go high briefly. This causes MU7, and consequently MU10 to turn on and pull the output node out to high, strongly, to charge up the output load. The feedback loop eventually turns ou3 and ou2 to either steady state values of high and low, respectively, turning MU7 off, disabling it from driving the gate of MU10. However,

transistor MU11 which was turned on when out went low will remain on, providing a diode connected configuration (pair MU10–MU11) to maintain the output voltage at ≈ (Vdd–|Vtp|).

High output: For output in high state we have inn=out=high, od1=low, and ou2=high, MD7, MD10, and MD11 off, and MD8 on. In this state, the output is driven high through the diode connected pair MU10–MU11.

High–to–low transition at the output: After a high–to–low transition at inn, due to delay in the feedback loop (XIF1), od1, and od3 will go high, and od2 will go low briefly. This causes MD7, and consequently MD10 to turn on and pull the output node out to low, strongly, to discharge the output load. The feedback loop eventually turns od3 and od2 to their steady state values of low and high, respectively, turning MD7 off, disabling it from driving the gate of MD10. However, transistor MD11 which was turned on when out went high will remain on, providing a diode connected configuration (pair MD10–MD11) to maintain the output voltage at ≈ Vtn.

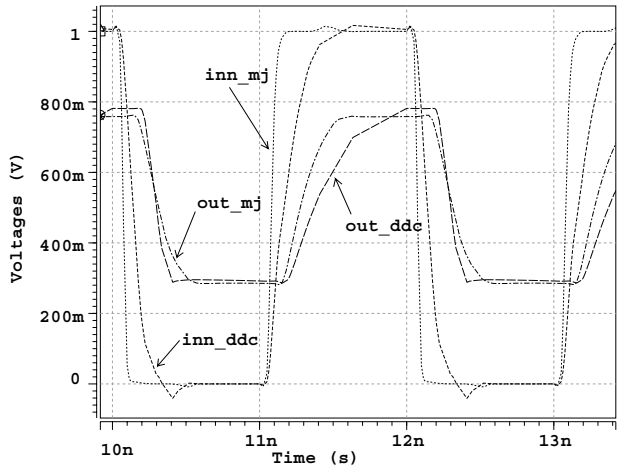

Fig. 2. Comparison of voltage waveforms of inn and out nodes for *mj–driver* and *ddc–driver* with a capacitive load of 5pF and 1V supply voltage.

Fig. 2 is the plot of voltage waveforms of inn and out nodes for *mj–driver* and *ddc–driver* with a capacitive load of 5pF and 1V supply voltage. To drive the circuits through an input source (vin), we have used an inverter (XIN0) with Wp=10.0μ m and Wn=5.0μ m.

IV. Comparative Evaluation

Three driver circuits were implemented using UMC triple well 0.13μm 1.2/3.3V CMOS process. Active areas for the proposed *mj–driver* circuit and *ddc–driver* circuit [1] are 28.87μm^2 and 55.28μm^2, respectively. We implemented two inverters connected in cascade (*basic–driver*) with an active area of 24.96μm^2 for comparison.

The circuits were simulated at 500MHz input frequency with 100ps rise and fall times, at supply voltages of 1 and 0.8V, and output capacitive load in the range of 1 to 5pF. Simulation results show that with the power supply of 1V our *mj–driver* is 16% faster (217ps delay at 5pF load) than the *ddc–driver*. From simulation the power dissipation of *mj–driver* is 1.71mW; 3% and 44% lower than *ddc–driver* and *basic–driver*, respectively. Fig. 3 presents propagation delay time for the 3 drivers at 1 and 0.18V.

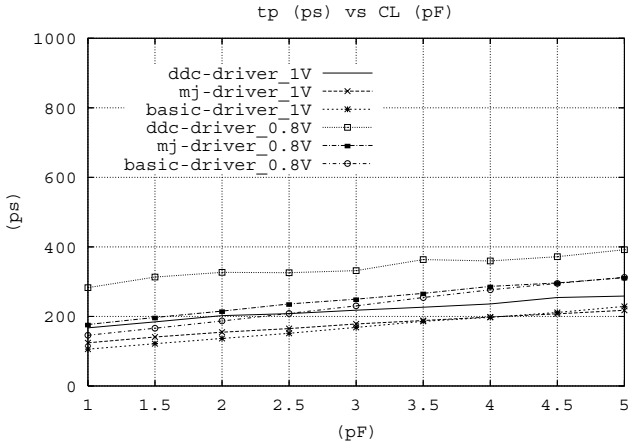

Fig. 3. Propagation delay time versus output load capacitance for UMC 0.13μm process.

In terms of energy consumption, our proposed *mj–driver* driver has 3% lower total energy than *ddc–driver* at 1V power supply. The total energy consists of the energy consumption in the driver circuit plus the dynamic switching energy in the load (E_{load} = CL · Vdd · Vout).

Fig. 4 illustrates Figures of energy efficiency (in energy–delay product) versus load capacitance for the three drivers. As seen energy–delay product for *mj–driver* is 1.36–1.23 times smaller than *ddc–driver*.

V. Adaptive Driver

We have designed an adaptive low/high swing version of *mj–driver* through the addition of 4 extra transistors (MU9,

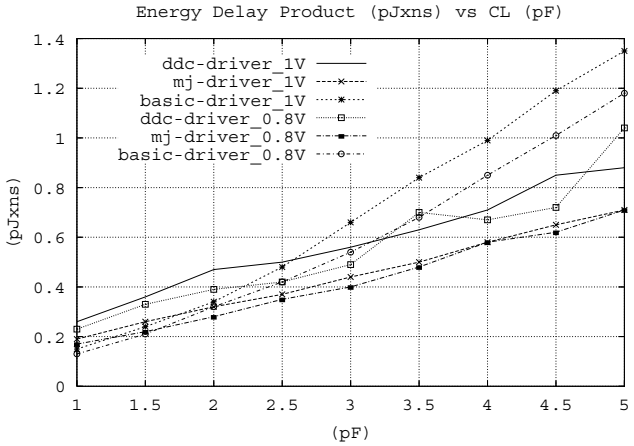

Fig. 4. Energy–delay product versus loading for UMC 0.13μm process.

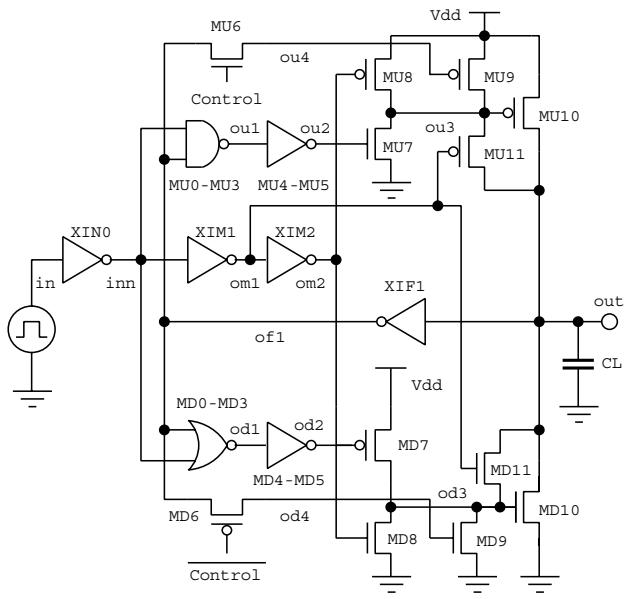

Fig. 5. Adaptive low/high swing *mj–driver*

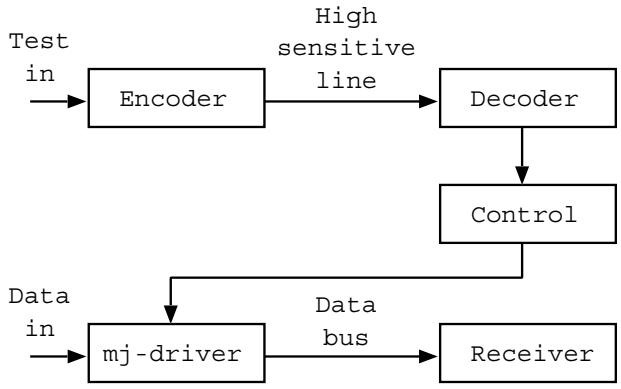

Fig. 6. Bus monitoring system

MD9, MU6 and MD6) as shown in Fig. 5. Use of transistors MU9 and MD9 allows the output of the driver to make full swing transitions to VDD and GND. Transistors MU6 and MD6 provide a mechanism for conditional enabling of MU9 and MD9, to improve the noise immunity. Setting the Control signal (gate of MU6) and its complement (gate of MD6) to high and low values, respectively, allows for direct connection from the of1 node to the gates of MU9 and MD9. This will allow for the full swing at the output to the power rails. The Control signal is driven through the line monitoring circuit of Fig. 6. The encoder circuit generates a known test pattern which is replicated at the receiver side. The two test patterns are compared with each other of the receiver side. If the number errors for a predetermine number of clock cycles exceeds a threshold the Control signal is asserted, switching the *mj–driver* to full swing mode. The high sensitive line is implemented using a low swing driver. The sensitivity of the line connecting the encoder and decoder can be altered by changing the test pattern. The test patterns with a greater transition rates are more sensitive to noise.

VI. Conclusions

This paper presented a new high speed adaptive low/high swing CMOS driver design (*mj–driver*) for driving global interconnet lines. Under a condition of 1V voltage power supply, 0.47V output swing voltage and a capacitive loading of 5pF, the delay and the power consumption associated with *mj–driver* were 217ps and 1.71mW, respectively.

The proposed driver achieved a stable voltage swing at 500MHz for the output load in the range of 1 to 5pF, and obtained a maximum energy $\times$ delay saving of 19%, at 1V 5pF when compared with *dcc–driver*.

Active area was 47% lower than *ddc–driver*.

The key advantage of *mj–driver* was its robustness with respect to the variation in the load (CL) and supply voltage (Vdd).

Our *mj–driver* adapts itself to noise conditions by configuring itself in low and high swing modes of operation through the use of a high sensitive line monitoring system.

Acknowledgement

This research was supported by the Ministry of Information and Communications (MIC), Republic of Korea, under the IT Foreign Specialist Inviting Program (ITFSIP) by the Institute of Information Technology Assessment (IITA).

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