

See discussions, stats, and author profiles for this publication at: <https://www.researchgate.net/publication/221376110>

Analysis and Comparison of High Performance CMOS Adiabatic Drivers.

Conference Paper · May 2009

DOI: 10.1109/ISCAS.2009.5118470 · Source: DBLP

CITATIONS

2

READS

54

3 authors, including:



J.C. Garcia

Universidad de Las Palmas de Gran Canaria

55 PUBLICATIONS 193 CITATIONS

[SEE PROFILE](#)



Juan A Montiel-Nelson

Universidad de Las Palmas de Gran Canaria

178 PUBLICATIONS 463 CITATIONS

[SEE PROFILE](#)

Some of the authors of this publication are also working on these related projects:



I am working about level shifters using 65nm CMOS technology. [View project](#)

Analysis and Comparison of High Performance CMOS Adiabatic Drivers

José C. García, and Juan A. Montiel–Nelson

Institute for Applied Microelectronics
University of Las Palmas de Gran Canaria
Las Palmas de Gran Canaria, Spain
Email: {jcgarcia, montiel}@iuma.ulpgc.es

Saeid Nooshabadi

Department of Information and Communication
Gwangju Inst. of Science and Technology (GIST)
Republic of Korea
Email: saeid@gist.ac.kr

Abstract—This paper presents the design and comparative evaluation of four low energy CMOS adiabatic drivers; ib–driver using a dual-rail structure with complementary input and output; scal–driver using a single input stage based on a single transistor driving a pair of cross-coupled CMOS inverters; ob–driver using an output stage with two inverters driven by a pre–driver circuit consisting of two differential cascode voltage switch (DCVS) logic cells; ee–driver using an output stage with two bootstrap capacitors driven by a pre–driver circuit consisting of two differential cascode voltage switch (DCVS) logic cells. When implemented on a $0.13\mu\text{m}$ CMOS 1.0V technology, ib–driver performs better than the other adiabatic circuits, in terms of the energy–delay product by up to 68%.

I. INTRODUCTION

As feature size in integrated circuits reduces, their performance in terms of energy dissipation and speed is increasingly limited by the interconnects. In order to improve the speed performance of the interconnects with large capacitive loads fast drivers have been reported [?]-[?]. On the other hand, to improve energy efficiency low supply voltage signalling interconnect has been employed [?]-[?]. However, inevitably this results in performance loss. To regain the performance loss in the low-voltage driver circuits, bootstrap techniques have been employed [?]-[?]. Further, to improve the energy efficiency of driver circuits with large capacitive loads, adiabatic technique has been used [?], [?]. Combination of bootstrap and adiabatic techniques has been reported in [?]-[?].

Adiabatic switching is a low-power circuit design approach where the signal energy stored on a capacitor on a circuit node may be recycled instead of dissipated as heat [?]. Power dissipation can be avoided if the capacitor is slowly charged with a voltage ramp. It is possible to recover this charge back into the power source by discharging the capacitor to a down-ramping supply. Adiabatic principles, together with charge reuse by redistribution, can be utilized for power saving in the interconnect lines.

In this paper we present the design of four low supply voltage, adiabatic CMOS driver circuits (*ib–driver*, *scal–driver*, *ob–driver*, and *ee–driver*) suitable for use in clocked circuitry with high capacitive load.

II. THE FOUR DRIVER CIRCUIT STRUCTURES

A. The *scal–driver* Circuit Structure

The circuit in [?], is made of two parts; an input stage and an output stage. The input stage is responsible for the generation of two differential outputs. The output stage is configured as a cross–coupled CMOS inverter driver. The pair of inverters uses a single–phase (PC) clocking scheme. PC signal replaces the power supply connection for the inverter pair. This facilitates energy recovery, due to adiabatic technique. The driver in [?] performs better and consumes less power than the conventional drivers. However, its performance degrades in the presence of high capacitive loads greater than 10pF^1 . We propose a modification in the input stage of circuit in [?] to reduce its energy consumption in the presence of large loads.

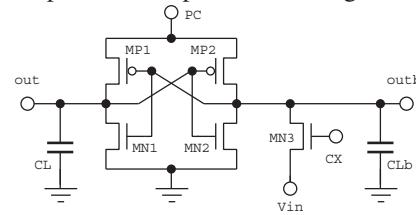


Fig. 1. Circuit structure of *scal–driver*.

The proposed driver of Fig. 1, (termed *scal–driver*), improves the input stage. The input V_{in} drives a cross coupled inverter pair through a pass transistor MN_3 . The gate of pass transistor is connected to an auxiliary timing control clock signal (CX). Use of only one pass transistor allows for quick transitions in both directions at the output.

The *scal–driver* operates in two phases for achieving the adiabatic function. During the initial phase, PC and CX are set high and the output load is driven by *scal–driver*. The adiabatic recycle of the energy takes place in the final phase when the PC goes low.

When PC , and CX , both go low nodes out or $outb$ are discharged to the power supply node through MP_1 or MP_2 . This enables the circuit to efficiently recover the energy trapped in the output node in CL or CL_b .

¹For illustration purposes a 10pF load corresponds to a wire–length of 5mm on a metal–3 layer, with $2\mu\text{m}$ width, for $0.13\mu\text{m}$ technology process from UMC, a common wire–length on modern integrated circuits chips.

If the auxiliary clock CX is low when PC is high the previously stored logic state is held at the outputs out and $outb$. This enables the logic evaluation by the next stage in the pipeline. As in other memory-based adiabatic schemes, *scal-driver*, has an inherent pipelining built into it. Power and clock distribution in *scal-driver* are simpler and more efficient than in multi-phase power clock adiabatic logic families.

B. The *ob-driver* Circuit Structure

Fig. 2, shows the circuit diagram of the the proposed *ob-driver*. Owing to the adiabatic technique, the driver in [?] performs better and consumes less power than the conventional bootstrapped drivers. It also performs better than the adiabatic circuit in [?]. However, it does not perform well in the presence of high capacitive loads greater than 10pF. The proposed circuit modifies the output stage of the bootstrapped adiabatic DCVS circuit in [?] to improve its driving capability in the presence of large loads.

The circuit is made of three parts; two *n-stage* and *p-stage*, pre-drivers and an output stage. The pre-driver stages are responsible for the generation of two differential outputs, through the operation of the n-type and p-type differential cascode voltage switch (DCVS) logic cells. Two complementary p-n DCVS logic cells use a single phase (PC) power supply clocking scheme. PC signal forms the ground connection of the p-type DCVS logic cell, and PCb signal (complement of PC) forms the power supply connection of the n-type DCVS logic cell. This facilitates energy recovery, due to adiabatic switching. The output stage is another n-type DCVS logic cell. The output stage is a bootstrapped configured driver.

The proposed improved output stage is presented at the bottom of Fig. 2. We use two inverters ($MP3n-MN7$) and ($MP4n-MN8$), and two pass transistors $MTN3$, and $MTN4$. Use of pass transistors and inverter pairs at the output stage allows for quick transitions in both directions in the output. Two NMOS device pairs ($MTN1$ and $MTN2$), and ($MTN3$ and $MTN4$), and PMOS device pair ($MTP1$ and $MTP2$) are used to pass the signals to the output stage. Transistors $MN5$ and $MN6$ controls the switching of v_{out} and v_{outb} nodes, respectively. The output stage contains the cross-coupled bootstrap transistors $MN3$ and $MN4$, and two NMOS devices $MN5$ and $MN6$, to provide isolation from the input stages.

The operation of the driver is divided into two phases for achieving the adiabatic function. During the initial phase, PC is high (PCb low) the *ob-driver* drives the output. The adiabatic recycle of the energy takes place in the final phase when the PC goes low.

In the n-type DCVS cell, for Vin high ($Vinb$ low), transistors $MN11$, $MN12$, $MN18$, and $MP11n$ turn off, whereas $MN13$, $MN14$, $MN15$, $MN16$, $MN17$, and $MP12n$ turn on causing nodes $Xn11$ and $Xn12$ to go low and high, respectively. On the other hand, for Vin low, transistors $MN11$, $MN12$, $MP17$, and $MP12n$ turn off while all other transistors turn on, causing nodes $Xn11$ and $Xn12$ to go on high and low, respectively. With PC high, transistors ($MTN1$, and $MTN2$) pass the logic

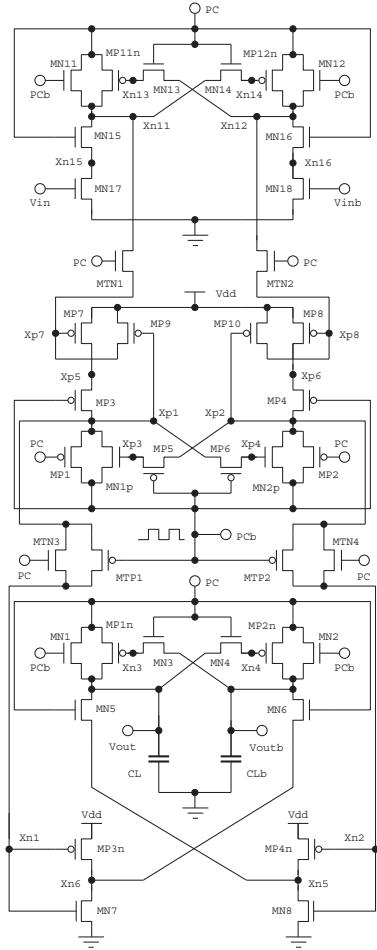


Fig. 2. Circuit structure of *ob-driver*.

levels on nodes $Xn11$ and $Xn12$ to nodes $Xp7$ and $Xp8$, respectively.

In the p-type DCVS cell, when PC is high and nodes $Xp7$ and $Xp8$ are low and high, respectively, transistors $MP1$, $MP2$, $MP8$, $MP9$, and $MN1p$ are turned off and all other transistors are turned on causing $Xp1$ and $Xp2$ nodes to go high and low, respectively. On the other hand, with nodes $Xp7$ and $Xp8$ in high and low, respectively, transistors $MP1$, $MP2$, $MP7$, $MP10$, and $MN2p$ are turned off and all other transistors are turned off, causing $Xp1$ and $Xp2$ to go low and high, respectively.

With PC high and nodes $Xp1$ and $Xp2$ low and high, respectively, the output stage has transistors $MN1$, $MN2$, $MN7$, $MP1n$, and $MP4n$ switching off, and nodes $Xn5$ and $Xn6$ pulling low and high, respectively, facilitating transistors $MN5$, and $MN6$ to discharge and charge the output load capacitors, CL and CLb , respectively. Note that the node out is pulled-down through devices $MN5$, and $MN8$, and other hand, capacitor CLb , is charged via $MN6$ and $MP3n$ up to Vdd pulling up v_{outb} . The complementary condition when PC is high and nodes $Xp1$ and $Xp2$ are high and low, respectively, can be explained in a similar fashion.

Energy is recovered in the final clocking phase, when PC is low. Independent of Vin (and $Vinb$), if PC is low, nodes $Xn11$ and $Xn12$ will be pulled low and the pass transistors

are turned off blocking their paths to nodes X_{p7} and X_{p8} . Therefore, transistors MP3 to MN10, and MN1p and MN2p, will be turned off. This will force both nodes X_{p1} and X_{p2} to go high. In that case the C_{gd} capacitances in the bootstrap transistors, MN3 and MN4, bootstrap the outputs quickly to V_{dd} and ground. At this stage MN5, MN6 are turned off to isolate the output from the inputs stages. This enables the circuit to efficiently recover the energy trapped in the output nodes, CL and CLb. Transistors MN1, and MN2 are used for the full energy recovery.

C. The ee-driver Circuit Structure

The adiabatic driver circuit in [?] is made of two parts; a pre-driver stage and an output stage. The pre-driver stage is responsible for the generation of two differential outputs, through the operation of the p-type and n-type differential cascode voltage switch (DCVS) logic cells with the adiabatic/bootstrap techniques [?]. Two complementary p-n DCVS logic cells use a single phase (PC) clocking scheme. PC signal forms the ground connection of the p-type DCVS logic cell, and PCb signal (complement of PC) forms the power supply connection of the n-type DCVS logic cell. This facilitates energy recovery, due to adiabatic switching. The output stage is a bootstrapped configured driver. Owing to the adiabatic/bootstrap techniques, the driver in [?] performs better and consumes less power than the conventional bootstrapped drivers. However, it does not perform well in the presence of high capacitive loads greater than 10pF.

We propose a modification to the bootstrapped circuit in the output stage of [?] to improve its driving capability in the presence of large loads. The modified circuit (termed *ee-driver*) is shown in Fig. 3. We use two bootstrap capacitors C_{pu} and C_{pd} , and four transistors P1, P2, P4, and P5. Use of two bootstrap capacitors allows for quick transitions in both directions at the output. Two PMOS device pairs (P1 and P2), and (P4 and P5) have their body terminals tied to the node B, and C, respectively, instead of being connected to V_{dd} . Transistors P1 and P4 are used to charge the bootstrap capacitors C_{pu} and C_{pd} , respectively. Transistor pairs N3 and N4 form a split pull-down configuration to reduce the resistance of the output node out without increasing the load on the node D. In addition, P3 and P6 are connected in parallel to, effectively, build a wide transistor.

To achieve the adiabatic function the operation of the driver is divided into two. During the initial phase, PC is low (PC_b high) and the *ee-driver* drives the output load. The adiabatic recycle of the energy takes place in the final phase when the PC goes high. The operation of the *ee-driver* can be explained in a similar fashion to that of *ob-driver*.

D. The ib-driver Circuit Structure

The adiabatic circuit in [?], is made of four parts; a N-logic function block (MN5, MN6), charge recovery path (MN3, MN4), cross-coupled latch (MP1, MP2, MN1, MN2) and output to ground path control block (MN7, MN8).

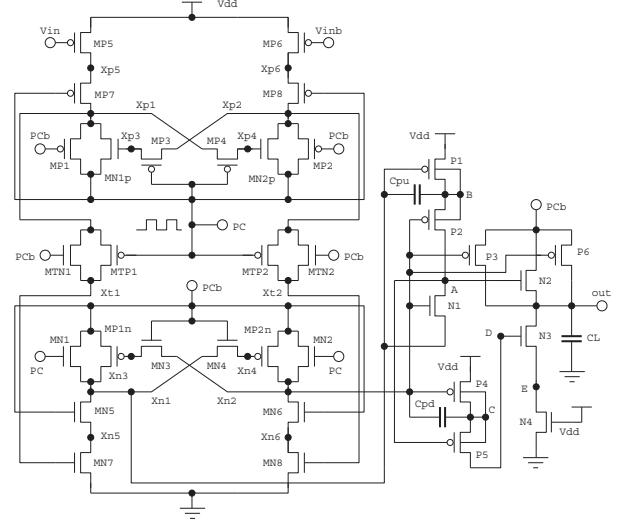


Fig. 3. Circuit structure of *ee-driver*.

The driver in [?] performs better and consumes less power than the adiabatic dynamic logic (ADL) [?], efficient charge recovery logic (ECRL) [?], and high efficient energy recovery logic (HEERL) [?] approaches. However, it does not perform well in the presence of high capacitive loads greater than 10pF.

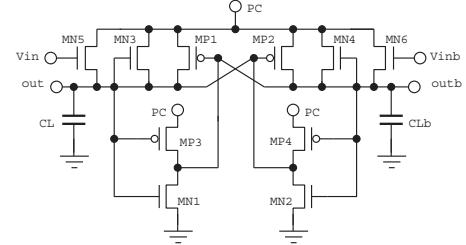


Fig. 4. Circuit structure of *ib-driver*.

We propose a modification to the adiabatic inverter circuit in the cross-coupled path, and output feedback path of [?] to improve its driving capability in the presence of large loads.

The proposed improved output stage (latch and output to ground path) is presented in Fig. 4. In the proposed inverter (termed *ib-driver*), we use two inverters MP3-MN1 and MP4-MN2. This structure allows for quick transitions in both directions at the output.

Two NMOS device pairs (MN5 and MN3), and (MTN4 and MTN6), two PMOS devices (MP1 and MP2), and two inverters (MP3-MN1) and (MP4-MN2) are used to pass the signals to the output stage. There is a sharing of transistors for the pull-up and pull-down blocks for the complementary output nodes out and out_b .

The operation of the driver is divided into two phases for achieving the adiabatic function. During the initial phase, PC is high and the inverter drives the output load. The adiabatic recycle of the energy takes place in the final phase when the PC goes low. The operation of the *ee-driver* can be explained in a similar fashion to that of *ob-driver*.

III. COMPARATIVE EVALUATION

The four proposed driver circuits were implemented using UMC triple well 0.13 μ m 1.2/3.3V CMOS process. Active

areas, when optimized for the lowest energy delay product, for *scal-driver*, *ob-driver*, *ee-driver* and *ib-driver* circuits are $29.90\mu\text{m}^2$, $119.15\mu\text{m}^2$, $31.84\mu\text{m}^2$, and $81.97\mu\text{m}^2$, respectively.

The circuits were simulated at 80MHz clock frequency with 100ps rise and fall times, and the output load in the range of 10 to 20pF. Simulation results show that with an square pulse v_{in} of 1V the *ib-driver* with 0.37ns delay at 20pF load, is faster than the other three drivers. Fig. 5 presents propagation delay time versus the capacitive load for all circuits considered in this paper.

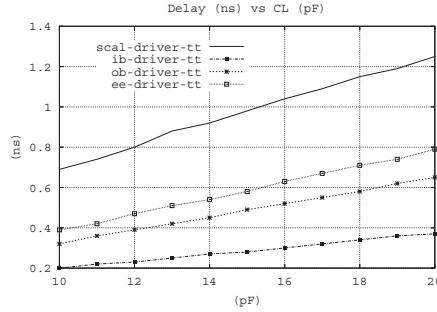


Fig. 5. Propagation delay time versus output load capacitance for UMC $0.13\mu\text{m}$ process.

The energy dissipation of *ib-driver* at 15.52pJ is the lowest among the four drivers. The energy dissipation of *scal-driver* is only 6.5% more.

Fig. 6 illustrates the energy efficiency (in energy-delay product) versus load capacitance for all the proposed drivers. As seen energy-delay product for *ib-driver* is 3.56–3.14 times smaller than its closer competitor *scal-driver* for the loads ranging from 10pF up to 20pF.

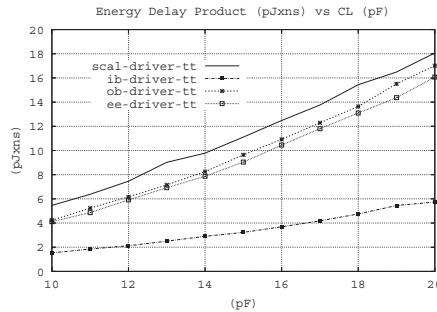


Fig. 6. Energy-delay product versus loading for UMC $0.13\mu\text{m}$ process for typical-typical corner.

IV. CONCLUSIONS

This paper presented four new low energy adiabatic CMOS circuits (*ib-driver*, *scal-driver*, *ob-driver*, and *ee-driver*) for driving high capacitive loads such as global interconnect lines.

Under the condition of v_{in} 1V, at 80MHz and a loading of 20pF, the delay and the energy consumption associated with *ib-driver* were 0.37ns and 15.52pJ for typical-typical corner, respectively. It achieves a maximum energy \times delay saving of 68%, 66%, and 64% when compared with *scal-driver*, *ob-driver*, and *ee-driver*, respectively. Its active area is 63.52% higher than *scal-driver* (the circuit with the lowest active area.)

Evaluations of the test circuits indicate that the proposed *ib-driver* exhibits lower energy-delay product than the other three driver circuits and is suitable for the energy-limited applications.