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# Bootstrapped Adiabatic Complementary Pass–Transistor Logic Driver Circuit for Large Capacitive Load and Low–Energy Applications

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***Abstract*—This paper presents the design of an adiabatic/bootstrapped CMOS driver (xb–ad) using complementary pass–transistor logic (CPL) and a four–phase power clock. The proposed xb–ad uses a bootstrapped load driven circuit with PMOS and NMOS transistors driven by an NMOS evaluation logic block. When implemented on a 65nm CMOS 1V technology, under the large capacitive loading condition (16pF), xb–ad performs better than the reference adiabatic circuit (cpl–ad) in terms of active area (64%), and energy–delay product (39%). Moreover, xb–ad supports 10 times higher output capacitive load without any additional circuit sizing than cpl–ad.**

***Keywords*-adiabatic circuit; bootstrap capacitor; energy–recovery; high capacitive load; low–voltage**

## I. Introduction

Driving large capacitive loads in an energy efficient fashion is a major challenge in the design of high speed integrated circuits. Several fast drivers for large capacitive loads have been reported [1]–[15]. One way to improve energy efficiency is the use of low supply voltage [1]–[3]. However, inevitably this results in performance loss. To regain the performance loss in the low–voltage driver circuits, bootstrap technique has been employed [4]–[9]. Further, to improve energy efficiency of driver circuits with large capacitive loads, adiabatic technique has been used [10], [11]. Combination of bootstrap and adiabatic techniques has been reported in [12]–[14].

Adiabatic switching is a low–power circuit design approach where the signal energy stored on a capacitor on a circuit node may be recycled instead of dissipated as heat [10]. Power dissipation can be avoided if the capacitor is slowly charged with a voltage ramp. It is possible to recover this charge back into the power source by discharging the capacitor to a down–ramping supply. Adiabatic principles, together with charge reuse by redistribution, can be utilized for power saving in interconnects. Adiabatic and energy–recovery techniques offer new possibilities to trade dynamic power consumption for delay in switching circuits.

In this paper we present the design of a low supply voltage, adiabatic CMOS driver circuit suitable for use four–phase power–clock with high capacitive load. The proposed driver requires an inverting and non–inverting input signals, and recovers energy from the output in order to reduce both energy consumption, and delay.

The paper is organized as follows. Section II presents the circuit structure for the proposed adiabatic CMOS driver *xb–ad*. Simulation results are presented and compared in Section III. Section IV presents the conclusions.

## II. The Driver Circuit Structure

It can be seen in the Fig. 1 adiabatic CPL driver for four–phase power–clocks termed *cpl–ad*, and Fig. 2, shows the circuit diagram of the proposed *xb–ad*. The proposed circuit modifies the output stage of the bootstrapped adiabatic CPL circuit in [16] to improve its driving capability in the presence of large loads. The criteria chosen for comparison are delay, energy consumption, energy–delay product and active area.

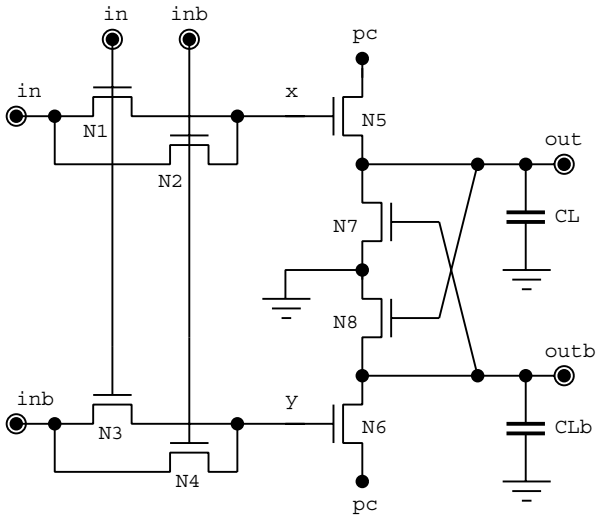


Figure 1. Circuit structure of *cpl–ad*.

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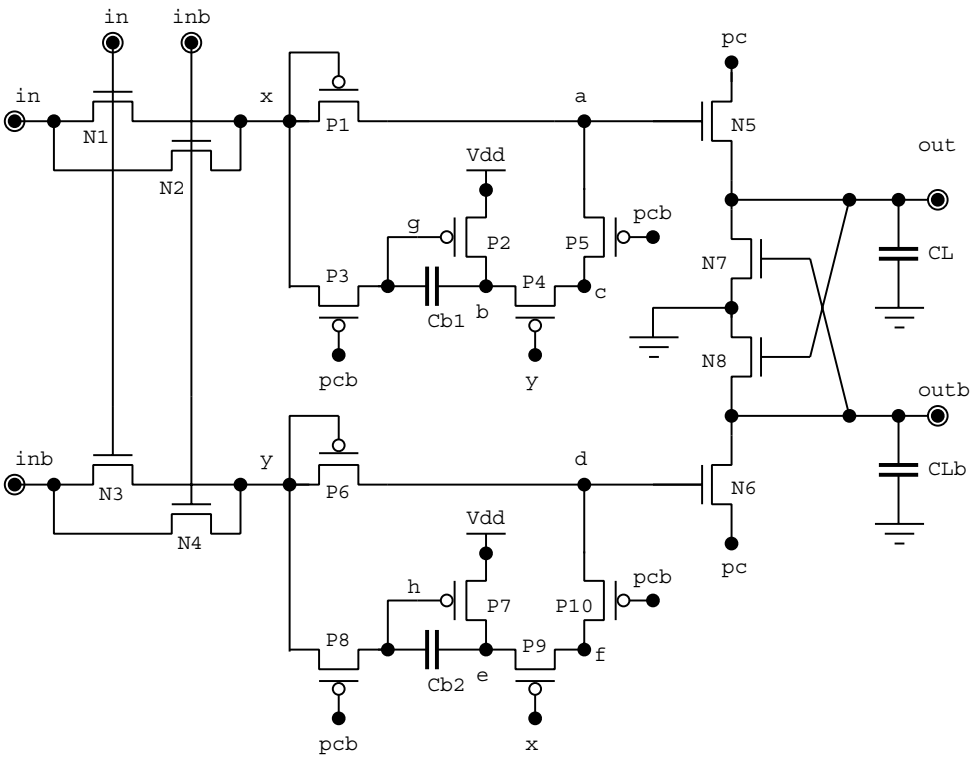


Figure 2. Circuit structure of *xb–ad*.

The operation of the adiabatic CPL driver can be summarized as follows. During the time interval pc is to low logic level, the input in goes high (inb is low). Therefore, N1, and N3 transistors are turned on. Node x is charged to high logic level (P1 and P3 are turned off), while nodes y and d are clamped to ground (P6 is turned on, and P8 is turned off).

During the time interval pc goes up, node a can be bootstrapped due to Cb1 and P2–P5 devices. Therefore, as the clock pc rises, node out is charged through the bootstrapped NMOS switch (N5) and fully–swing is obtained. At the same time, when node out rises above the threshold voltage of the NMOS transistor, N8 will be turned on and node outb is clamped to ground. P8 is turned on and Cb2 is charged through P7 (P9 and P10 are turned off).

During the time interval pc is high, node out is the same as the clock (pc), while node outb is still at ground. At the same time, node x will keep its state because it is isolated.

During the time interval as the voltage of the clock pc falls from Vdd to ground, the charge on node out is recovered through transistor N5 in the adiabatic manner.

From the above analyses and simulation Fig. 3 shows the various waveforms for the major nodes of *xb–ad* and *cpl–ad*.

## III. Comparative Evaluation

The driver circuits were implemented using STM 65nm 1V CMOS process. Active areas for *cpl–ad* [16] and the proposed *xb–ad* circuits are $119.60\mu m^2$, and $43.10\mu m^2$, respectively, (64% increase for *cpl–ad*). Both circuits were optimized for the lowest energy delay product. The optimized parameters for both designs are presented in Table I.

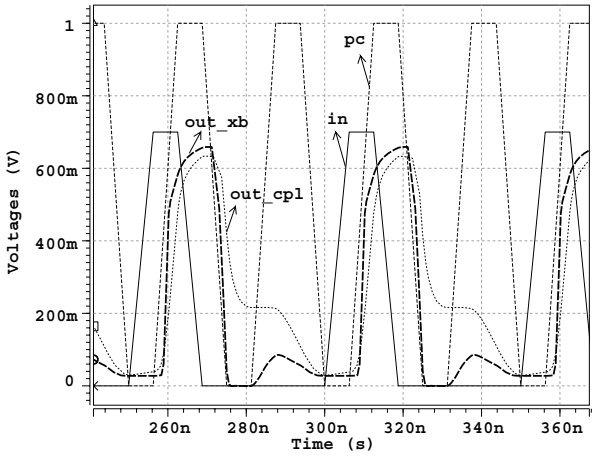


Figure 3. Waveforms for *xb–ad* and *cpl–ad* with a capacitive load of 16pF.

NCb1, and NCb2 are NMOS transistors used to implement bootstrapping capacitors Cb1, and Cb2, respectively.

The circuits were simulated at 40MHz clock frequency

Table I
CHANNEL WIDTHS FOR TRANSISTORS IN *cpl–ad* AND *xb–ad*, (THE CHANNEL LENGTH FOR ALL TRANSISTORS IS 65NM.)

| *cpl–ad* (Active area=119.60$\mu$m$^2$) | | | *xb–ad* (Active area=43.10$\mu$m$^2$) | | |
|---|---|---|---|---|---|
| Transistor | Type | Width ($\mu$m) | Transistor(s) | Type | Width ($\mu$m) |
| N1 | N | 5.0 | N1–N4 | N | 10.0 |
| N2 | N | 5.0 | N5, N6 | N | $10.0 \times 23$ |
| N3 | N | 5.0 | N7, N8 | N | 6.0 |
| N4 | N | 5.0 | P1, P6 | P | $10.0 \times 3$ |
| N5 | N | $10.0 \times 90$ | P2, P7 | P | 10.0 |
| N6 | N | $10.0 \times 90$ | P3, P8 | P | 0.3 |
| N7 | N | 10.0 | P4, P9 | P | 10.0 |
| N8 | N | 10.0 | P5, P10 | P | $10.0 \times 4$ |
| – | – | – | NCb1, NCb2 | N | 0.3 |

65nm 1V CMOS process technology from STM.

with 6.25ns rise and fall times, and the output load in the range of 1 to 16pF. Input signal (in) has a voltage level of 0.7V with 6.25ns rise and fall times, and as well a pulse width of 6.25ns.

Fig. 4 presents propagation delay time versus the capacitive load for both circuits. It is seen that with the power supply of 1V our *xb–ad* is faster than *cpl–driver* for the load condition between 1 to 16pF.

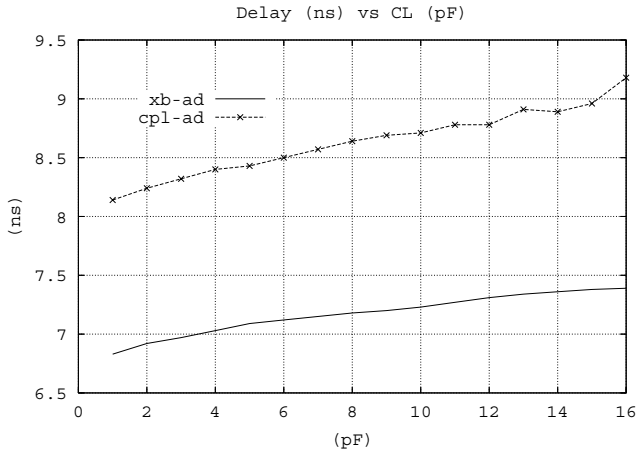


Figure 4. Propagation delay time versus output load capacitance for STM 65nm process.

The plots of energy consumption versus the loading for the two drivers are presented in Fig. 5. The energy dissipation of *xb–ad* is 5.83pJ; 39% lower than the *cpl–ad* at 16pF load.

Fig. 6 illustrates the energy efficiency (in energy–delay product) versus load capacitance for the two drivers. As seen energy–delay product for *xb–ad* is 1.64 times smaller than *cpl–ad* for the load of 16pF.

For comaparison, *xb–ad* has been tested for a capacitive load of 160pF and simulation results show that *xb–ad* supports this load without any additional circuit sizing with

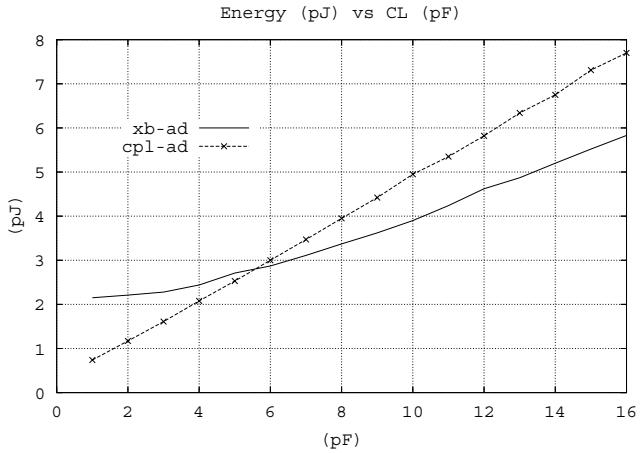


Figure 5. Energy versus loading for STM 65nm process.

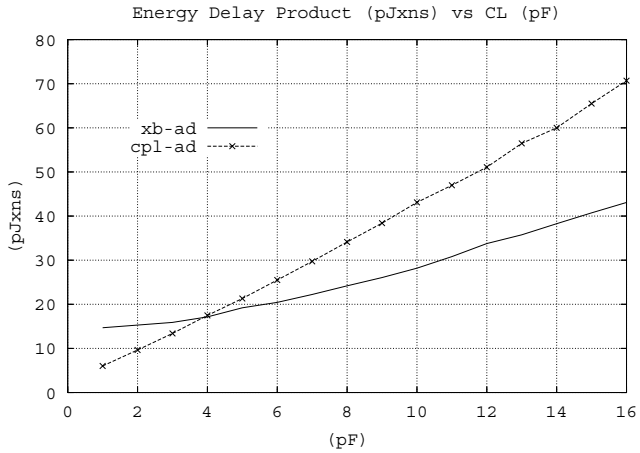


Figure 6. Energy–delay product versus loading for STM 65nm process.

only a decrease of 17% over output voltage in relation to input voltage. However, *cpl–ad* does not work with a load higher than 16pF.

## IV. CONCLUSIONS

This paper presented a new high speed adiabatic CMOS driver (*xb–ad*) for driving high capacitive loads such as global interconnect lines. Under a condition of 1V power supply, four–phase power–clock and a loading of 16pF, the delay and the energy consumption associated with *xb–ad* were 7.39ns and 5.83pJ, respectively.

The proposed *xb–ad* supports 160pF output capacitive load, and its active area is 64% lower when compared with *cpl–ad*.

## REFERENCES

[1] J. C. García, J. A. Montiel–Nelson, and S. Nooshabadi, "Efficient CMOS driver–receiver pair with low–swing signalling for on–chip interconnects," *IEEE 18th Eur. Conf. on Cir. Theo. and Des.*, (ECCTD07), Sevilla Spain, Aug. 2007.

[2] J. C. García, J. A. Montiel–Nelson, and S. Nooshabadi, "Adaptive low/high voltage swing CMOS driver for on–chip interconnects," *IEEE Int. Sym. on Cir. and Sys.*, (ISCAS07), New-Orleans US, May 2007.

[3] J. C. García, J. A. Montiel–Nelson, and S. Nooshabadi, "DB–Driver: A low power CMOS bootstrapped differential cross coupled driver," *Int. Jor. of Elect.*, vol. 94, no. 9, pp. 809–819, Sept. 2002.

[4] J. C. García, J. A. Montiel–Nelson, J. Sosa and H. Navarro, "A direct bootstrapped CMOS large capacitive–load driver circuit," *Design, Automation and Test in Europe Conference and Exhibition*, vol. 1, pp. 680–681, Paris, France, Feb. 2004.

[5] J. B. Kuo, "Evolution of bootstrap techniques in low–voltage CMOS digital VLSI circuits for SOC applications," *Workshop on System–on–Chip for Real–Time Applications*, pp. 143–148, Jul. 2005.

[6] K. S. Yeo, J. G. Ma, M. A. Do, "Ultra–low–voltage bootstrapped CMOS driver for high performance applications," *Electron.Lett.*, vol. 36, no. 8, pp. 706–708, Apr. 2002.

[7] B. S. Kong, D. 0. Kang, and Y. H. Jun, "A bootstrapped CMOS circuit technique for low–voltage application," *Int. Conf. on VLSl and CAD*, (ICVC), pp. 289–292, Oct. 1999.

[8] J. C. García, J. A. Montiel–Nelson, and S. Nooshabadi, "A single capacitor bootstrapped power efficient CMOS driver," *IEEE Trans. Cir, and Syst. II*, vol. 53, no. 9, pp. 877–881, Sept. 2006.

[9] J. C. García, J. A. Montiel–Nelson, and S. Nooshabadi, "Bootstrapped full–swing CMOS driver for low supply voltage operation," *Design, Automation and Test in Europe Conference and Exhibition*, vol. 1, pp. 1–2, Munich, Germany, Mar. 2006.

[10] W. C. Athas, L. J. Svensson, J. G. Koller, N. Tzartzanis, and E. Y.–C Chou, "Low–power digital systems based on adiabatic–switching principles," *IEEE Trans. VLSI Syst.*, vol. 2, no. 4, pp. 398–407, Dec. 1994.

[11] W. Baohua and P. Mazumder, "On optimality of adiabatic switching in MOS energy–recovery circuit," *IEEE Int. Sym. on Low Power Elec. Design*, (ISLPED), pp. 236–239, Aug. 2004.

[12] Y. Zhang, H. H. Chen, and J. B. Kuo, "0.8V CMOS adiabatic differential switch logic circuit using bootstrap techniques for low–voltage low–power VLSI," *Electron. Lett.*, vol. 38, no. 24, pp. 1497–1499, Nov. 2002.

[13] H. P. Chen, and J. B. Kuo, "A low–voltage CMOS load driver with the adiabatic and bootstrap techniques for low–power system applications," *IEEE Int. Midwest Sym. on Cir. and Sys.*, (MWSCAS), vol. 2, pp. II-193–II-196, Jul. 2004.

[14] H. P. Chen, and J. B. Kuo, "A 0.8V CMOS TSPC adiabatic DCVS logic circuit with the bootstrap technique for low–power VLSI," *IEEE Int. Conf. on Electron. Cir. and Sys.*, (ICECS), pp. 175–178, Dec. 2004.

[15] B. Kheradmand–Boroujeni, A. Seyyedi, and A. Afzali–Kusha, "High speed low gate leakage large capacitive–load driver circuits for low–voltage CMOS," *IEEE Int. Conf. on Microelectron.*, pp. 30–35, Dec. 2005.

[16] L. Wang, J. Hu, and J. Dai, "A low–power multiplier using adiabatic CPL circuits," *IEEE Int. Sym. on Integ. Cir.*, (ISIC), pp. 21–24, Sept. 2007.