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High Performance CMOS 2–Input NAND Based on Low–Race Split–Level Charge–Recycling Pass–Transistor Logic

José C. García, and Juan A. Montiel–Nelson
Institute for Applied Microelectronics
University of Las Palmas de Gran Canaria
Las Palmas de Gran Canaria, Spain
Email: {jcgarcia, montiel}@iuma.ulpgc.es

Saeid Nooshabadi
Department of Information and Communication
Gwangju Inst. of Science and Technology (GIST)
Republic of Korea
Email: saeid@gist.ac.kr

***Abstract*—This paper presents the design of a highly efficient CMOS 2–input NAND (gcr–nand). When implemented on a 65nm CMOS technology, under 1pF capacitive loading condition, gcr–nand has a lower active area (3.4 times lower), and energy–delay product (56%) than the reference 2–input NAND (lscpl–nand). Furthermore, gcr–nand is able to operate under a high output load.**

***Keywords*-low–voltage; low–energy; high capacitive load; charge–recycling**

I. Introduction

Energy–delay product has become one of the most important design metrics for energy efficiency in the current deep submicron technologies for the System–on–chip (SoC) solutions and multi–core computing architectures for many common applications.

Further, one common design criterion for a logic gate is its ability to drive large capacitive loads in an energy efficient fashion. To this end, several charge recycling logic techniques, have been proposed [1].

Another common method to improve energy efficiency is the use of low supply voltage [2]. However, inevitably this results in the performance loss. To regain the performance loss in the low–voltage circuits, bootstrap technique has been employed [3]–[8].

In this paper we present the design of a low power 2–input NAND gate suitable for use with high capacitive load. The proposed NAND gate reduces both energy–delay product, and the active area. The advantage of the proposed NAND gate is verified through simulation.

The paper is organized as follows. Section II proposes the appropriate circuit structure for the CMOS NAND gate *gcr–nand*. Section III discusses the principle of operation of *gcr–nand*. Simulation results are briefly described and compared in Section IV. Finally Section V presents the conclusions.

II. The 2–Input NAND Circuit Structure

Fig. 1, shows the circuit diagram of the *lscpl–nand* in [1]. This 2–input NAND gate uses a logic style called Low–race Split–level Charge–recycling Pass–transistor Logic (LSCPL) to minimise the power, delay and sensitivity to signal skew compared to previous logic families such as Split–level Pre–charge Differential Logic (SPDL) [9], Charge Recycling Differential Logic (CRDL) [10], Half–Rail Differential Logic (HRDL) [11], CMOS Pass–gate No–race Charge–recycling Logic (CPNCL) [12], Modular Charge Recycling Pass–transistor Logic (MCRPL) [13], and No–race Charge–recycling Complementary Pass Transistor Logic (NCR-CPL) [14].

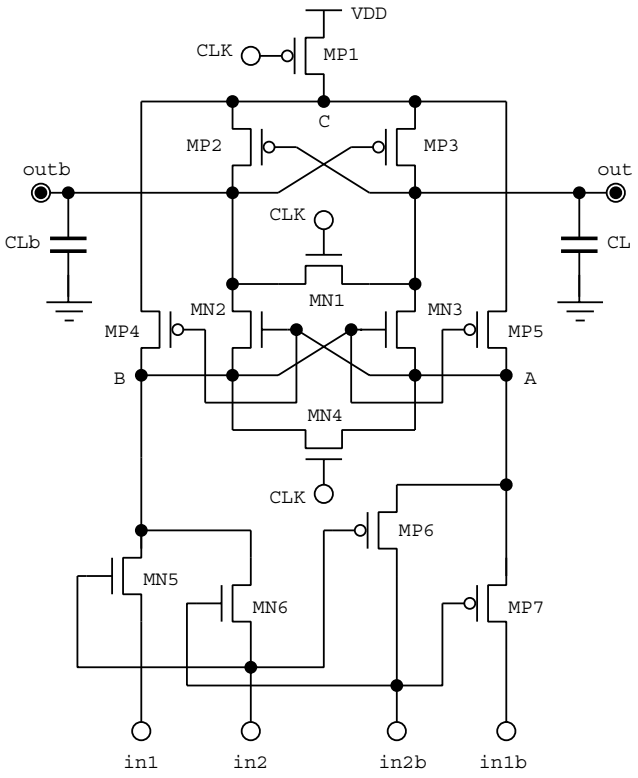

Figure 1. Circuit structure of *lscpl–nand*.

LSCPL family uses an output driver that separates load from pass–transistor logic and hence has better driving capability compared to previous logics. However, even LSCPL is not able to drive large capacitive loads that are associated

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with the typical interconnects in current deep submicron technologies.

The *lscpl–nand* gate is a split–level logic where the complementary outputs are initially set to Vdd/2 during the high phase of CLK signal (pre–charge phase), and settle to the their appropriate logic values of Vdd and GND, during the low phase of CLK signal (evaluation phase). However, since pass–transistor logic passes logic high poorly, the outputs of *lscpl–nand* are not pulled strongly to low GND potential as will be evidenced in the simulations results presented in the next section, when both inputs in1, and in2 are high. This results in loss of noise margin, static power dissipation, and loss of driving capability. To overcome this problem and improve the driving capability in presence of large output capacitive loads when both inputs are high we propose the structure shown in Fig. 2 (*gcr–nand*). Two inverters, (MP4, MN8) and (MP5, MN7) reinforce and improve the performance when both inputs assume high logic values. This will ensure that split-levels swing between GND=0 and ≈ 0.4V (VDD/2) for the pull–down and ≈ 0.4V and 0.8V (VDD), for the pull–up.

We propose *gcr–nand* as an alternative to *lscpl–nand* to reduce its energy consumption in the presence of large loads. The criteria chosen for comparison are delay, energy consumption, energy–delay product and active area.

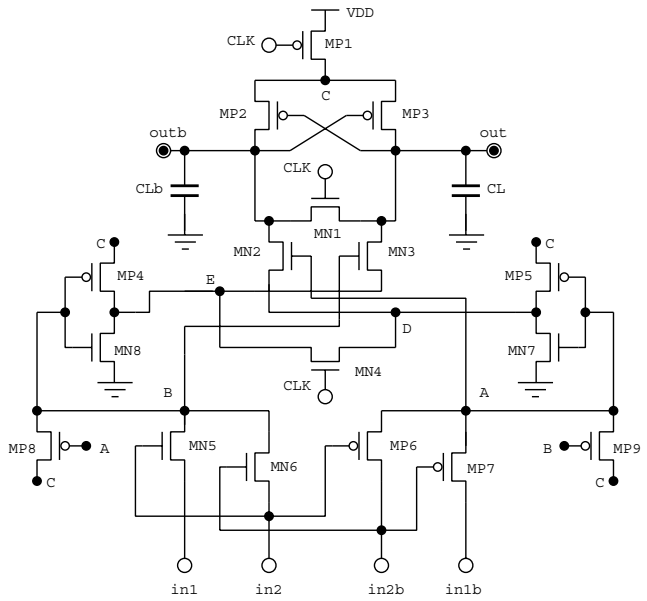

Figure 2. Circuit structure of *gcr–nand*.

III. Principle of Operation

The circuit of the 2–input NAND gate (*gcr–nand*) is made of three parts; pass–transistor logic (initial stage), pre–charge circuit (middle stage), and output driver (final stage). The initial stage (MN5, MN6, MP6, and MP7) is responsible for the generation of voltages for node B and A, respectively. The middle stage (MN7, MN8, MP4, MP5, MP8, and MP9) forces the nodes D and E to assume their respective logic states (complementary to voltage value for nodes A and B, respectively). The final stage (MN1, MN2, MN3, MP1, MP2, and MP3) uses PMOS and NMOS transistors, respectively, for the pull–up and pul–down transition of the nodes out, and outb.

The circuit *gcr–nand* has two phases of operation, namely, pre–charge and evaluation phase. During the pre–charge phase CLK is high and MN1, and MN4 are turned on. This leads to direct connection of node D to E, and node out to outb. In the evaluation phase CLK is low.

The working principle is as follows: assume that the inputs (node in1, and in2), and CLK are low. Transistors MN5, and MP7 are turned off, and MN6, and MP6 are turned on and nodes A, and B are set to high, and low, respectively. Moreover, transistors MP8, and MP9 are turned off, and on, respectively, to reinforce those logic values and improve the speed of the 2–input NAND gate. Inverter (MP5/MN7) switches node D to low, and inverter (MP4/MN8) sets node E to high. Under these conditions, MN1, and MN4 are turned off, but MP1 is turned on and node C is set to high. Transistors MN2, and MN3 are switched on and off, respectively. As a consequence, transistor MP2 is turned off, and transistor MP3 is driven and the output node out is pulled–up to Vdd (0.8V). Also, node outb is pulled–down to GND.

However, when nodes in1, and in2 are high, and CLK is low, nodes A and B are fixed at GND, and C, respectively. As a consequence, node D is set to high, and node E goes to low. This situation leads to nodes out, and outb assuming low and high logic levels, respectively.

Fig. 3 and 4 show the various waveforms for the major nodes of *gcr–nand*, and *lscpl–nand* for a capacitive load CL of 1pF, for, respectively, low–low and high–high input states, when node CLK goes to low (evaluation) phase.

IV. Comparative Evaluation

The 2–input NAND gates were implemented using STM 65nm 1.2V CMOS process. Active areas for *lscpl–nand* [1], and the proposed *gcr–nand* circuits are 219.37μm^2, and 62.85μm^2, respectively, (a 3.4 times saving in favor of *gcr–nand*). All circuits were optimized for the lowest energy–delay product. The optimized parameters for designs are presented in Table I. The circuits were simulated at 100MHz clock frequency (for in1, in2, and CLK) with 100ps rise and fall times, and the output load in the range of 0.1 to 1pF. Simulation results show that with the power supply of Vdd= 0.8V our *gcr–nand* with 1.04ns delay at 1pF load has a performance which is marginally better than the *lscpl–nand*. Fig. 5 presents propagation delay time versus the capacitive load for both circuits considered in this paper.

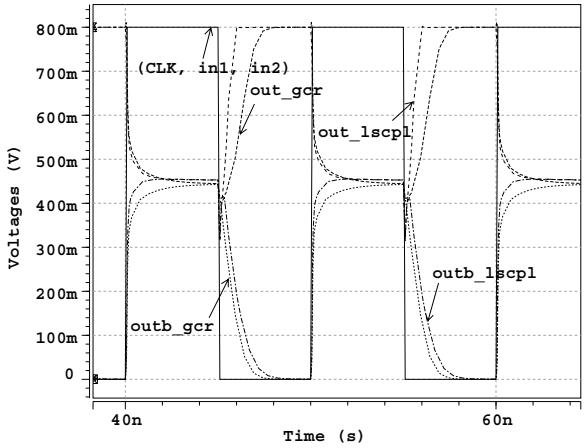

Figure 3. Waveforms for *gcr–nand* and *lscpl–nand* with a capacitive load of 1pF when both inputs are set low during the evaluation phase.

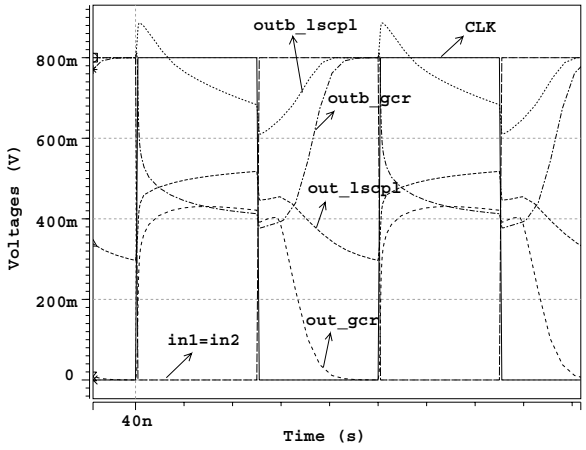

Figure 4. Waveforms for *gcr–nand* and *lscpl–nand* with a capacitive load of 1pF when both inputs are set high during the evaluation phase.

Table I
CHANNEL WIDTHS FOR TRANSISTORS IN *lscpl–nand*, AND *gcr–nand*, (THE CHANNEL LENGTH FOR ALL TRANSISTORS IS 65NM.)

lscpl–nand (Active area=219.37μm^2)			*gcr–nand* (Active area=62.85μm^2)		
Transistor(s)	Type	Width (μm)	Transistor(s)	Type	Width (μm)
MP1	P	19 × 10	MP1	P	18 × 10
MP2, MP3	P	12 × 10	MP2, MP3	P	6
MP4, MP5	P	27 × 10	MP4, MP5	P	5 × 10
MP6, MP7	P	80 × 10	MP6, MP7	P	11 × 10
MN1	N	38 × 10	MP8, MP9	P	8
MN2, MN3	N	5 × 10	MN1	N	15 × 9
MN4	N	32 × 10	MN2, MN3	N	5
MN5, MN6	N	2.5	MN4	N	30 × 9
—	—	—	MN5, MN6	N	8
—	—	—	MN7, MN8	N	4

CMOS065–LP–HVT process technology from STM.

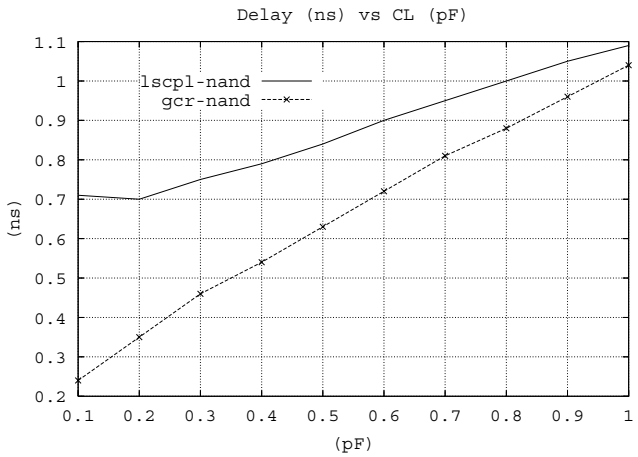

Figure 5. Propagation delay time versus output load capacitance for STM 65nm process.

The plots of energy consumption versus the loading for the two NAND gates are presented in Fig. 6. The energy dissipation of *gcr–nand* is 0.73pJ; 54% lower than the *lscpl–nand* at 1pF load.

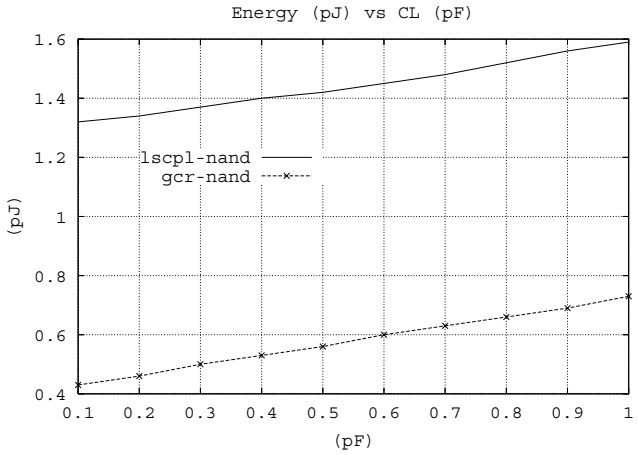

Figure 6. Energy versus loading for STM 65nm process.

Fig. 7 illustrates the energy efficiency (in energy–delay product) versus load capacitance for the two NAND gates. As seen energy–delay product for *gcr–nand* ranges between 89.2% and 56.6% lower than energy–delay product for *lscpl–nand* for the loads ranging from 0.1pF up to 1pF, respectively.

V. CONCLUSIONS

NAND gates are widely used as interfacing logic and functional logic circuits. This paper presented a new high performance CMOS 2–input NAND gate (*gcr–nand*) for driving high capacitive loads (0.1–1pF).

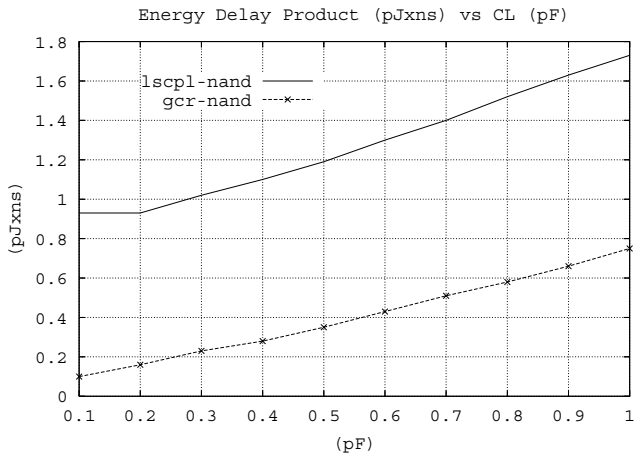

Figure 7. Energy–delay product versus loading for STM 65nm process.

Under a condition of Vdd= 0.8V power supply, and a loading of 1pF, the delay and the energy consumption associated with *gcr–nand* were 1.04ns and 0.73pJ, respectively.

The proposed *gcr–nand* was analyzed in at 100MHz (input, and CLK nodes) and for the output load in the range of 0.1 to 1pF. For a 0.8V input and 1pF output loading it achieves a maximum energy × delay saving of 56.6%, when compared with *lscpl–nand*. However, its active area saving is 3.4 times lower. This gain in the active area results in a higher energy efficiency for driving larger capacitive loads.

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