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High Performance CMOS Dual Supply Level Shifter for a 0.5V Input and 1V Output in Standard 1.2V 65nm Technology Process

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Abstract

*This paper presents the design of a highly efficient CMOS level shifter qc–level shifter. Unlike many recent level shifters, the proposed qc–level shifter does not use bootstrap capacitors to minimize active area. When implemented on a 65nm CMOS technology, under the large capacitive loading condition (2pF), qc–level shifter has a lower active area (94%), and energy–delay product (21.4%) than the reference bootstrap level shifter circuit (ts–level shifter). In comparison to a conventional shifter (*c–level shifter*)the corresponding reductions are 9.5% and 55%, respectively. Also qc–level shifter has very small effective input capacitance in comparison with ts–level shifter as it does not need a bootstrap capacitor connected to its input.*

1. Introduction

Energy and Energy–delay product have become two of the most important design metrics in the current deep submicron technologies for the System–on–chip (SoC) solutions and multi–core computing architectures for many common applications. Therefore, it is a common practice to use separate supply voltages, in different parts of SoCs and multi–core processors, in order to reduce the energy consumption. It is necessary that the core processor that executes the time critical algorithm to run at a higher voltage (`Vddh`), thus maximizing the performance, while all other non–critical subsystems operate at a lower voltage (`Vddl`) to improve the energy efficiency. Level shifters are also suitable for block–level dynamic voltage scaling (DVS) environment [1]. Therefore, a level shifter to translate from low to high–swing, to drive large capacitive loads, in an energy efficient fashion, is a key circuit component for SoC environment.

The requirement for a level shifter is to fully turn–off the PMOS of the gate that it drives and, in same cases, to ensure that no gate oxide voltage exceeds the reliability limits set by the technology node. The conventional level shifters, [2], [3], using cross–coupled PMOS load have large delay as they suffer from contention between the pull–down and pull–up transistors, respectively.

In [4] a variety of existing level shifters were compared in the context of up–converting subthreshold signals to superthreshold levels. Since a level shifter circuit consumes power and has a considerable delay, its optimization for delay performance, low power and low area is important. One way to improve energy efficiency is the use of low supply voltage [5], [6]. However, inevitably this results in the performance loss. To regain the performance loss in the low–voltage circuits, bootstrap technique has been employed [7]–[12].

The work in [2] uses bootstrapped gate drive to minimize voltage swing. This helps in reducing the switching power consumption in the conventional level shifter and also helps to increase the speed of the level shifter.

In this paper we present the design of a low power level shifter circuit suitable for use with high capacitive load. This voltage level shifter acts as interface between different voltage domains and is able to efficiently convert a low voltage level to a higher desired voltage level. The proposed level shifter while reduce both energy–delay product, and active area does not require bootstrap capacitors. The advantage of the proposed level shifter is verified by simulation results.

The paper is organized as follows. Section 2 proposes the appropriate circuit structure for the CMOS level shifter *qc–level shifter*. Simulation results are briefly described and compared in Section 3. Finally, Section 4 presents the conclusions.

2. The Level Shifter Circuit Structure

Figure 1, shows the circuit diagram of the *ts–level shifter* in [2]. This level shifter circuit uses bootstrapped gate driver

to minimize the voltage swing. Two capacitors maintain the voltage difference between the gates of pull–up PMOS and pull–down NMOS transistors. The idea in the design of *ts–level shifter* is to drive the pull–up PMOS and pull–down NMOS with two separate low swing signals to reduce the power dissipation. The pull–down NMOS is driven between 0 and Vddl, while the PMOS is driven from (Vddh−Vddl) to Vddh.

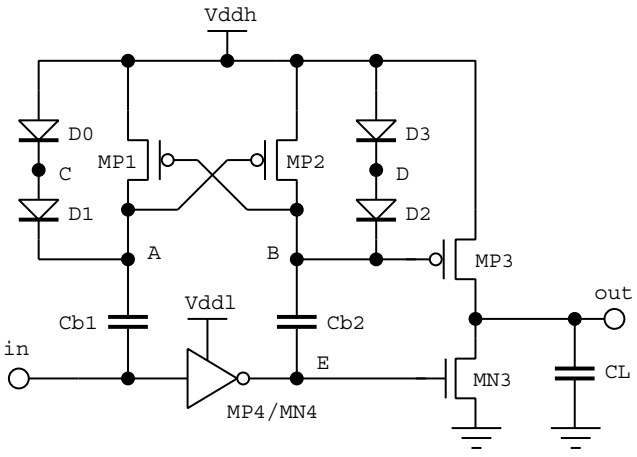

Figure 1. Circuit structure of *ts–level shifter*.

The level shifter in [2] performs better and consumes less power than the conventional one shown in Figure 2. However, it does not have a good performance in the presence of high capacitive loads greater than 2pF.

We propose a new structure (termed *qc–level shifter*) to reduce the energy consumption in the presence of large loads. The criteria chosen for comparison are delay, energy consumption, energy–delay product and active area.

Figure 3 presents the circuit for *qc–level shifter*. In the proposed level shifter the bootstrap capacitor is eliminated, resulting in a reduction in the input capacitance of the level shifter circuit and an increase in the driving capability of the previous stage.

The circuit is made of two parts; an input stage and an output stage. The input stage is responsible for the generation of voltages for node 1 and 2 through the operation of the inverter (MP1/MN1), transistors MN2 and MP2, and diodes D1 and D2. The output stage uses a PMOS (MP3) and NMOS (MN3) transistors for the pull–up and pull–down transitions of the output node out, respectively.

The working principle is as follow: For the case where the input (node in) is low, inverter (MP1/MN1) switches node 1 to high–Vddl, transistor MN2 is turned off due to V3-V1 is lower than its threshold voltage (Vtn=0.48V), transistor MP2 turns on and node 2 is set to high–V4≈0.65V. As a consequence, inverter (MP3/MN3) is driven high and the output node out is pulled–down to

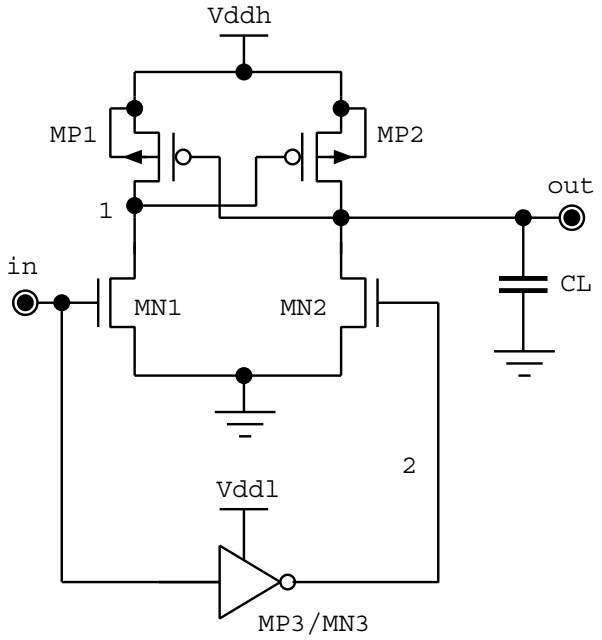

Figure 2. Circuit structure of *c–level shifter*.

GND.

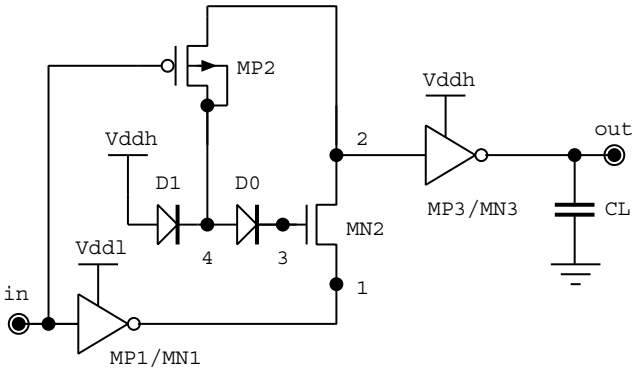

Figure 3. Circuit structure of *qc–level shifter*.

On the other hand, when node in is high–Vddl node 1 pulled to GND, transistor MP2 is turned off, and MN2 is switched on, and node 2 is set to GND. In this state, inverter (MP3/MN3) is driven low and pulls–up node out to the maximum voltage of Vddh. Note that in this state for the MP2 transistor, ($|VGS| < |Vtp|$=0.36V), and is, therefore, fully turned off.

Figure 4 shows the various waveforms for the major nodes of *ts–level shifter*, *c–level shifter* and *qc–level shifter* for a capacitive load CL of 2pF.

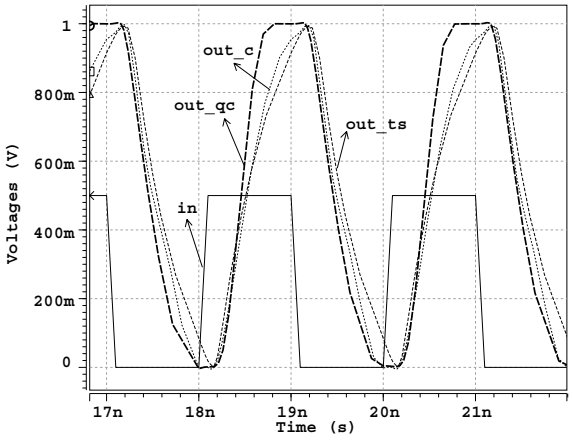

Figure 4. Waveforms for *ts–level shifter* and *qc–level shifter* with a capacitive load of 2pF.

3. Comparative Evaluation

The level shifter circuits were implemented using STM 65nm 1.2V CMOS process. Active areas for *ts–level shifter* [2], *c–level shifter*, and the proposed *qc–level shifter* circuits are 886μm^2, 63μm^2, and 57μm^2, respectively; 15 and 1.1 fold reduction in favor of *qc–level shifter* when compared with *ts–level shifter* and *c–level shifter*. All circuits were optimized for the lowest energ–delay product. The optimized design parameters are presented in Table 1.

`MNCB` is used to implement bootstrap capacitors of 1.2pF. The circuits were simulated with the power supplies `Vddl`= 0.5V, and `Vddh`= 1V, 500MHz clock frequency with 100ps rise and fall times, and the output load in the range of 0.2 to 2pF. Simulation results show that our *qc–level shifter* is faster than the *ts–level shifter* and *c–level shifter* by 0.39ns at 2pF load condition. Figure 5 presents propagation delay time versus the capacitive load for the circuits considered in this paper.

The plots of energy consumption versus the loading for the three level shifters are presented in Figure 6. The energy dissipation of *qc–level shifter* at 2pF load is 2.54pJ; 5.5%, and 48% lower than *ts–level shifter*, and *c–level shifter*, respectively.

Figure 7 illustrates the energy efficiency (in energy–delay product) versus load capacitance for the three level shifters. As seen energy–delay product reduction for *qc–level shifter* with respect *ts–level shifter* ranges between 20% and 21% for the loads ranging from 0.2pF up to 2pF, respectively. The corresponding figures with respect to *c–level shifter* are 150% and 200%

Table 1. Channel widths for transistors in *ts–level shifter*, *qc–level shifter*, and *c–level shifter*, (the channel length for all transistors is 65nm.)

ts–level shifter (Active area=885.53μm^2)			*qc–level shifter* (Active area=56.55μm^2)		
Transistor(s)	Type	Width (μm)	Transistor	Type	Width (μm)
`MP1`	P	0.2	`MP1`	P	3 × 10.0
`MP2`	P	0.2	`MP2`	P	5 × 10.0
`MP3`	P	21 × 10.0	`MP3`	P	6 × 10.0
`MP4`	P	31 × 10.0	`MN1`	N	6 × 10.0
`MN3`	N	19 × 10.0	`MN2`	N	10 × 10.0
`MN4`	N	51 × 10.0	`MN3`	N	6 × 10.0
`MND0`–`MND3`	N	0.8	`MND0`	N	10.0
`MNCB`	N	620 × 10.0	`MND1`	N	50 × 10.0
c–level shifter (Active area=62.53μm^2)					
Transistor	Type	Width (μm)	Transistor	Type	Width (μm)
`MP1`	P	2.0	`MP2`	P	2.0 × 10.0
`MP3`	P	19 × 10.0	`MN1`	N	6.0 × 10.0
`MN2`	N	56 × 10.0	`MN3`	N	13.0 × 10.0

CMOS065–LP–HVT process technology from STM.

4. Conclusions

Level shifters are widely used as output drivers for interfacing logic and functional blocks or circuits on a SoC. This paper presented a new high performance CMOS level shifter (*qc–level shifters*) for driving high capacitive loads (0.2–2pF).

Under a condition of `Vddl`= 0.5V, and `Vddh`= 1V power supplies, and a loading of 2pF, the delay and the energy consumption associated with *qc–level shifter* were 0.39ns and 2.54pJ, respectively.

The proposed *qc–level shifter* was analyzed in at 500MHz for the output load in the range of 0.2 to 2pF. For the 2pF output loading it achieves a maximum energy–delay product saving of 21%, when compared with *ts–level shifter*. However, its active area saving is 15 times.

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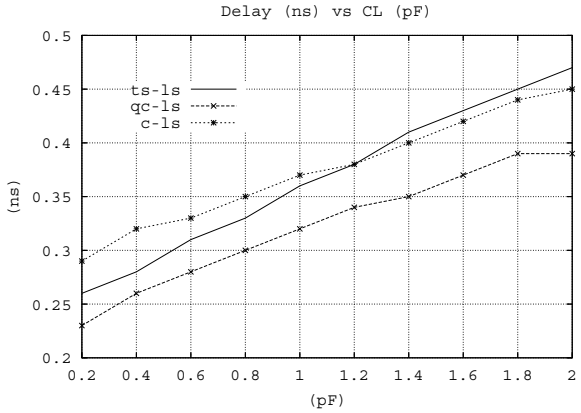

Figure 5. Propagation delay time versus output load capacitance for STM 65nm process.

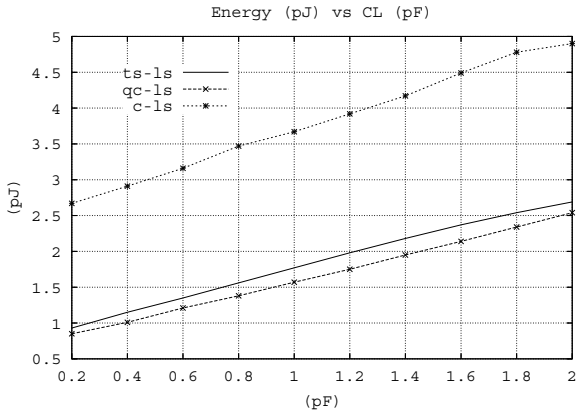

Figure 6. Energy versus loading for STM 65nm process.

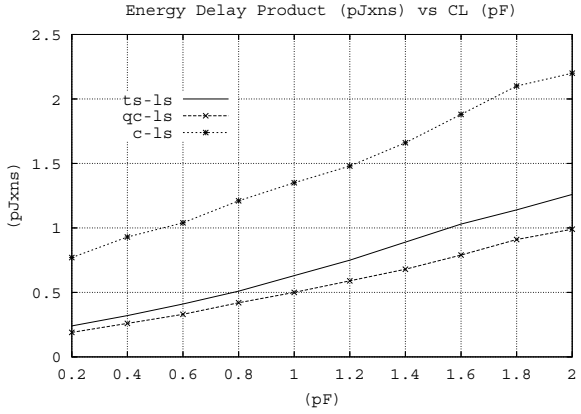

Figure 7. Energy–delay product versus loading for STM 65nm process.

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