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AN ENHANCED GaAs MONOLITHIC TRANSIMPEDANCE AMPLIFIER FOR LOW NOISE AND HIGH SPEED OPTICAL COMMUNICATIONS

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ABSTRACT

The design, implementation and test results of a simple GaAs Monolithic Transimpedance Amplifier with enhanced performance for high speed optical communications is described. A cascode configuration, improved in terms of bandwidth and noise is used. On-wafer and on-carrier measurements show close agreement with simulated behavior. Excellent performance with high transimpedance gain, a bandwidth from DC to 1.6 GHz, low noise and low power consumption is obtained. The temperature and bias point sensitivity are negligible. This last fact turns out to be a major commercial achievement.

INTRODUCTION

The optical signal is transformed both at the receiver and the repeater stations of most fiber-optic communication systems to an electrical signal by means of a photodiode and then amplified before passing through an equalizer for regeneration. Optical preamplifiers may be either a high impedance voltage amplifier or a transimpedance amplifier. The last one has shown to be the most suitable configuration in high bit rate systems, offering high current to voltage conversion, good noise performance, wide bandwidth and large dynamic signal range. It may be constructed in hybrid or in MMIC form. For reproducibility, reliability and cost reasons the last one is commercially preferable [1].

This paper presents the design, construction and test results of a GaAs MMIC transimpedance amplifier with excellent performances although based in a very simple structure. The design is DC coupled to avoid the construction of high value capacitors that should be needed otherwise to achieve the required low frequency cutoff in the KHz range. The basic configuration is a simple cascode one, optimized in terms of the gain and the bandwidth of the voltage amplifier. The configuration has been also improved in terms of transimpedance bandwidth and noise by means of the introduction of two peaking inductors, one in series with the input FET and the other one as a series feedback. A shunt feedback loop gives the transimpedance behavior. A final buffer stage is included for matching purposes. The device has been constructed employing the GaAs half-micron F20 process of GEC Marconi Materials and Technology Limited

(GMMTL). The chips were tested on-wafer and on-carrier, and in different temperature conditions, in the facilities of the SSR Department of the ETSI Telecomunicación of the University of Madrid. Measured results show good agreement with the simulated behavior and excellent performances for speeds up to 1.7-1.8 Gb/s, high transimpedance gain (63.5 dB Ω), wide bandwidth (from DC to 1.6-1.7 GHz), low power consumption (about 0.5 W), low equivalent noise current (4-5 pA/ $\sqrt{\text{Hz}}$) and negligible dependence of the behavior with the temperature and the bias point variations.

Further simulations of the structure in order to establish its low-frequency transimpedance gain and bandwidth limiting values show that the highest value for the transimpedance gain would be of the order of 64-65 dB Ω for a maximum transimpedance bandwidth of the order of 1.8 GHz. Thus if the desired performances are greater than those limiting values, a different configuration must be employed.

DESIGN OF THE TRANSIMPEDANCE AMPLIFIER

Figure 1 shows the transimpedance amplifier design.

The cascode configuration was selected as the basic one in order to obtain a high gain-bandwidth product [2]. It consists of a common source FET (F1) initial stage, followed by a common gate one (F3). In order to have a maximum value for the bandwidth of the voltage amplifier the relation between the gate widths of F1 and F3, w_1/w_3 , must be as high as possible. In the other hand the high value desired for the transimpedance bandwidth will fix an upper limit for the width w_1 . As a compromise between both requirements F1 has been selected as a 4 fingers, 150 μm width FET, while F3 is a 2 fingers, 50 μm width FET; this represents an optimization of the basic structure given in [2].

The bias network has been designed by means of active loads, consisting of several FETs with $V_{gs}=0$. It must be pointed out that the width of these FETs must be as small as possible, in order to give the highest low-frequency gain [3]. Due to that reason the FETs for the active loads are 2 fingers, 50 μm width. The DC voltage at the gate of F3 has been fixed by means of an active load (2x50 μm FET) followed by two shifting level diodes.

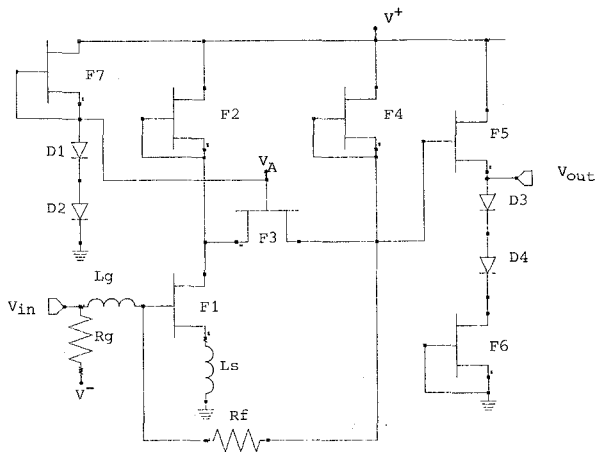


Figure 1. Transimpedance Amplifier Design

The effect of the L_g inductor in series with the gate of the input FET is to produce a high frequency peak in order to increase the bandwidth. An inductor, L_s , has been also included between the F1 source and ground. The principal effect of this feedback loop is to produce a high frequency minimum of the equivalent noise current at the amplifier input in order to compensate the noise increment (due to the f^2 dependence) in the upper part of the frequency band [4].

A resistor shunt-shunt feedback loop has been employed in order to obtain a transimpedance amplifier from the original voltage amplifier. It is easily seen that the low frequency transimpedance gain value is determined by the value of the R_f resistor [5].

Finally, a common drain FET has been employed as output stage, with a two fold objective: to obtain low value loads for the previous stages, and to achieve a matched output. For those reasons a FET with gate width sufficiently high ($2 \times 100 \mu\text{m}$) has been chosen.

FABRICATION OF THE DEVICE

Figure 2 shows the device layout. The sensitivity of the main performance parameters to process variations (from wafer to wafer) and to parameter dispersion (across wafer) was checked before delivering it to the foundry. The chips were fabricated at the GMMTL foundry employing their half-micron F20 process.

TEST RESULTS

The chips were tested at the facilities of the SSR Department of the Polytechnic University of Madrid.

On-wafer DC and RF (S parameters and transimpedance gain) measurements were done by means of a Cascade

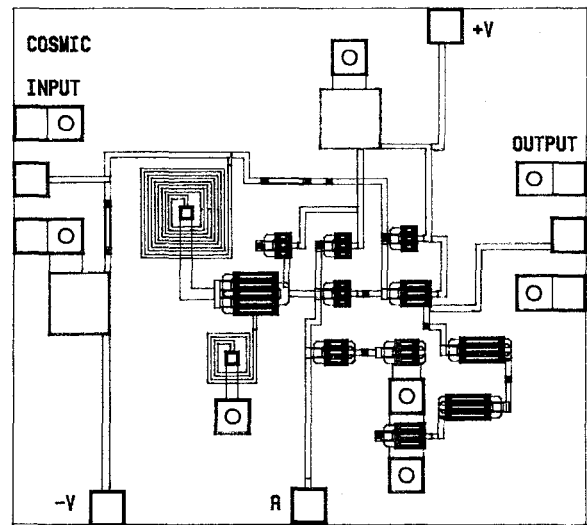


Figure 2. Layout

Microtech Summit 9000 probe station. Table I shows the DC results; it may be pointed out the low power consumption obtained. Figure 3 shows the S_{11} and $|S_{21}|$ parameters for 18 samples of the same wafer. Figure 4 shows the comparison of the simulated and the measured transimpedance gain values for those samples. It can be seen that the parameter dispersion is negligible. The agreement between simulated and measured values is excellent as well as the performance, giving a transimpedance gain of about 63.5 dB Ω with a bandwidth from DC to 1.6-1.7 GHz.

The on-carrier measurements agree well with the on-wafer ones. Figure 5 plots the dependence of the main parameters (transimpedance gain and bandwidth) with the variations in the bias point. It may be seen that an excellent behavior is obtained, being almost negligible the sensitivity to the bias point. This achievement represents a major commercial one.

Table I. DC Behavior		
$V^+ = 7(\text{v})$,	$V^- = -6(\text{v})$,	$P_{\text{cons}} = 590(\text{mW})$
$\bar{I}^+ = 83.43(\text{mA})$,	$\sigma_{I^+} = 3.02(\text{mA})$	
$\bar{I}^- = 1.8(\text{mA})$,	$\sigma_{I^-} = 0.01(\text{mA})$	
$\bar{V}_A = 1.69(\text{v})$,	$\sigma_{V_A} = 0.01(\text{v})$	
$V^+ = 7(\text{v})$,	$V^- = -5.5(\text{v})$,	$P_{\text{cons}} = 550(\text{mW})$
$\bar{I}^+ = 77(\text{mA})$,	$\bar{I}^- = 1.8(\text{mA})$	
$V^+ = 6(\text{v})$,	$V^- = -5(\text{v})$,	$P_{\text{cons}} = 500(\text{mW})$
$\bar{I}^+ = 83(\text{mA})$,	$\bar{I}^- = 1.8(\text{mA})$	
$V^+ = 5.5(\text{v})$,	$V^- = -5(\text{v})$,	$P_{\text{cons}} = 460(\text{mW})$
$\bar{I}^+ = 82(\text{mA})$,	$\bar{I}^- = 1.8(\text{mA})$	

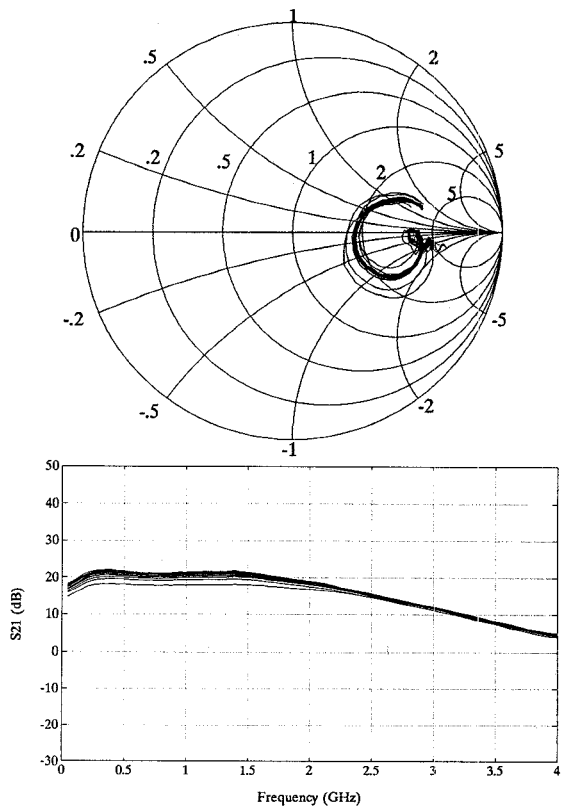


Figure 3. S_{11} and $|S_{21}|$ Measured Parameters for $V^+ = 6(v)$ and $V^- = 5(v)$

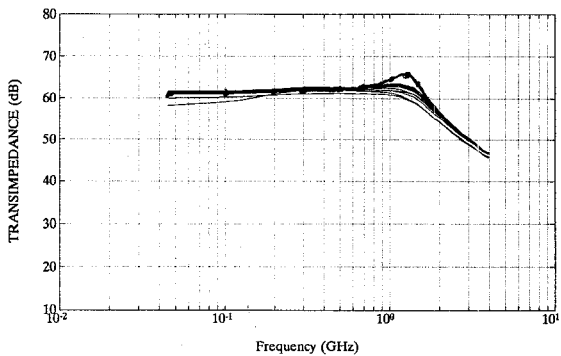


Figure 4. Transimpedance Gain for $V^+ = 6(v)$ and $V^- = 5(v)$
 • Simulated result

On-carrier temperature and noise measurements were done. Figures 6 and 7 show S_{11} , S_{22} , $|S_{12}|$, $|S_{21}|$ and the transimpedance gain for six different values (-20° , -10° , 0° , 10° , 25° and 50° C) of the temperature; it may be concluded that the temperature dependence is also negligible. Figure 8 plots the results for the input equivalent noise current spectral density for the same temperature values showing in one hand an equivalent noise current of about $4-5 \text{ pA}/\sqrt{\text{Hz}}$ (which represents a sensitivity of the receiver of the order of

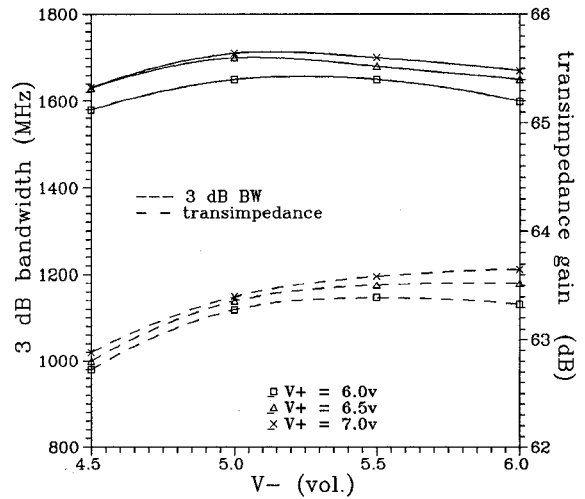


Figure 5. Bias Point Dependence of the Transimpedance Gain and Bandwidth

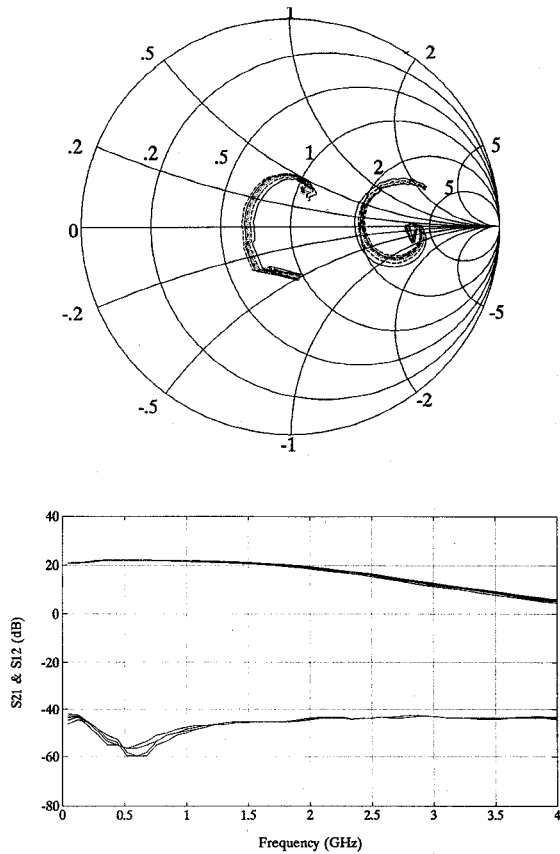


Figure 6. S_{11} , S_{22} , $|S_{21}|$ and $|S_{12}|$ for Six Different Values of the Temperature, for $V^+ = 7(v)$, $V^- = 5.5(v)$, $I^+ = 77(mA)$, $I^- = 1.8(mA)$

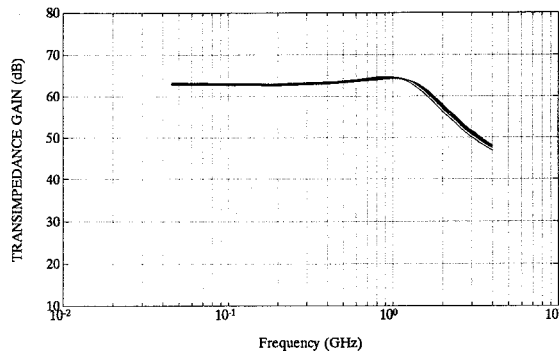


Figure 7. Transimpedance Gain for Six Different Values of the Temperature, for $V^+ = 7(v)$, $V^- = 5.5(v)$, $I^+ = 77(mA)$, $I^- = 1.8(mA)$

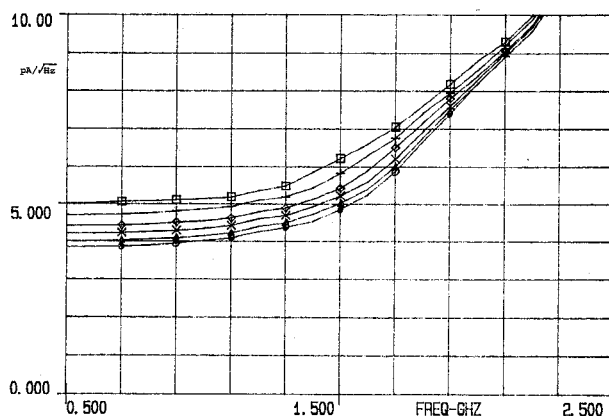


Figure 8. Equivalent Noise Current for Six Different Values of the Temperature, for $V^+ = 7(v)$, $V^- = 5.5(v)$, $I^+ = 77(mA)$, $I^- = 1.8(mA)$
 $\square: 50^\circ C$, $+: 25^\circ C$, $\diamond: 10^\circ C$, $\times: 0^\circ C$, $\Delta: -10^\circ C$, $\circ: -20^\circ C$

-28 to -33 dBm, depending on the photodetector employed), and in the other hand that the noise dependence with the temperature is also negligible.

Comparing those results with those presented in [1]-[5] it may be concluded that excellent performances have been obtained mostly from a commercial point of view.

Preliminary results of optical/electrical measurements show that a decrement of about 15% or greater is to be expected in the transimpedance bandwidth, depending on the photodetector employed. Thus the device will allow speed rates up to 1.7-1.8 Gb/s for direct detection and digital transmission systems employing a PIN diode of 0.1 pF and considering a roll-off-factor of 0.8.

FURTHER IMPROVEMENTS OF THE PERFORMANCES OBTAINED

Further simulations of the structure have been performed in which several parameters have been optimized in order to establish the limiting values for the transimpedance gain and bandwidth. It has been demonstrated that a maximum value of 64-65 dB Ω of transimpedance gain with a maximum bandwidth of 1.8 GHz are the limiting performances of the structure under study, with an increment of the power consumption. Thus, the results measured are very close to those limits.

It may be concluded that in order to improve those performances a different structure must be implemented. With the scope of obtaining a higher transimpedance gain and a lower power consumption a novel structure based in a three inverter chain has been implemented and is being tested.

CONCLUSIONS

A GaAs MMIC transimpedance amplifier for low noise and high speed optical communication systems has been designed, constructed and tested, showing excellent performances in terms of reproducibility, reliability, and electrical behavior (high transimpedance gain and bandwidth, low noise, low power consumption). The device shows very low sensitivity to the temperature and bias point variations, and low parameter dispersion across the wafer. The electrical results are very close to the theoretical limits of the structure. Further improvements of those performances must consider a different configuration.

ACKNOWLEDGEMENTS

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