Analog Integrated Circuits and Signal Processing, 35, 121–132, 2003

Integrated Inductors Modeling for Library Development and Layout Generation

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Abstract. In this work we propose a modification to the conventional lumped equivalent circuit model for integrated inductors. Also the widely used parametric model is modified. The proposed models expand the frequency range where the integrated inductor behavior is accurately predicted. They are useful in developing automatic tools to assist the designers in selecting and automatically laying-out integrated inductors [1]. This work is based on measurements from integrated inductors fabricated in a standard silicon process.

Key Words: RFIC, integrated inductor, CAD tools

1. Introduction

Standard Silicon CMOS technologies offer reduced costs and high production levels. Besides, the cut-off frequencies of the transistors are as high as to make these technologies the choice when a radio frequency (RF) system—conceived to operate in the range of a few GHz (GSM, GPS, DCS-1800, DECT, UMTS, Bluetooth, etc.), [2–4]—goes to production.

Further reduction of the final cost may be achieved by integrating the inductors, avoiding in this manner placing external inductors in extra steps in the fabrication process. But the quality factor of integrated inductors on standard Silicon processes is poor due to the low resistivity of the substrate [5,6]. Nevertheless, the capabilities of the technology can be stretched if optimized structures are used because of the reduction of the associated losses. So the designers should have a deep knowledge of the physics involved in order to perform the optimization task. Alternatively, a good integrated inductors library, together with automatic tools, linked with the library, may find optimal integrated inductors for them. Unfortunately, the foundries hardly ever offer good libraries or automatic tools to assist the designers. Therefore, the development of these libraries and tools is a major concern for the RF design community.

All these aspects rely on lumped equivalent circuit models for the integrated inductors, required to simulate the circuit. The widely used equivalent model [7,8], that we call here conventional model, accurately fits the integrated inductor behavior at the frequencies we have already mentioned.

Besides, as frequency increases the error introduced in the characterization phase may be significant, therefore the parameter extraction methodology [1] is critical in order to get adequate model predictions.

This paper is focused in modeling the integrated inductor behavior; in addition the automatic tools already presented in [1] will be extended with a revised parametric model. We report in Section 2 the conventional model showing its drawbacks at high frequencies (up to 10 GHz). Also a classification of the models is given: narrow and wide band models. The frequency intervals where they are useful, and their limitations are also stated. Sections 3 and 4 are devoted to present our proposed modified models for integrated inductors. In both cases the models are demonstrated to be valid up to 10 GHz. Section 5 presents a set of equations that constitute the parametric model. This model

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permits the designers to predict the structure that better fits a particular integrated inductor not previously fabricated and characterized (not included in a particular library). In Section 6 we are presenting an automatic tool, embedded into Cadence [8], which manages the parametric model and help the circuit designer. This tool is linked with another one [1] that automatically layout any integrated inductor given its geometry. Finally some conclusions are presented.

2. Conventional Model

The conventional two ports lumped equivalent model for an integrated spiral inductor is shown in Fig. 1 [7,8]. The magnetic field caused by the ac current flowing in the metal traces is responsible for the device inductive behavior. Serially connected to the inductor L_S, there is a resistor R_S that models the ohmic losses in the metal traces. The capacitor C_P takes into account the capacitive coupling due to the electrical field between the spiral tracks and the electric field between the spiral and the cross-under. The remaining elements in the circuit incorporate the substrate effects. Thus, capacitors C_{OX1} and C_{OX2} model the oxide capacitance between the coil and the substrate, while C_{SUB1} and C_{SUB2} are the substrate capacitance, and R_{SUB1} and R_{SUB2} take into account its ohmic loses.

The values of the equivalent circuit elements are extracted through a fitting procedure based on the analysis of the experimental data [1].

The equivalent circuit in Fig. 1 is not symmetrical because the capacitive coupling to the substrate is different in both ports: an underpass is needed to connect the inner port to the rest of the circuit. Therefore, the extracted values C_{OX1}, C_{SUB1}, and R_{SUB1} are slightly different from C_{OX2}, C_{SUB2}, and R_{SUB2}.

The measurements and the fitting examples of the following figures are taken from a two metal layer inductor (metal 1 is 0.6 μm thick, metal 2 is 1μm thick; with an oxide separation of 1 μm) with 150 μm external radius, 12 μm metal width, 1.8 μm separation between metals and 3.5 turns. The lower metal is separated from the substrate only 1 μm.

Figure 2 shows the measured and modeled real and imaginary parts of the admittance between the input port and ground. It can be seen that the network C_{OX1}, C_{SUB1}, and R_{SUB1} correctly predict the ground branch behavior for the entire frequency range. Similar results are obtained for the admittance between port 2 and ground.

However, the same does not occur for the main branch (modeled by the elements L_S, R_S, and C_P). Figure 3 shows the measured real and imaginary parts of the main branch admittance so as the predictions from the conventional model against frequency. The model fits well at low frequencies but at high frequencies there is a deviation between the modeled and measured real part of the main branch admittance; the last one begins to grow.

The lumped model presented in Fig. 1 agrees with the measurements at low frequencies (around 1 GHz)

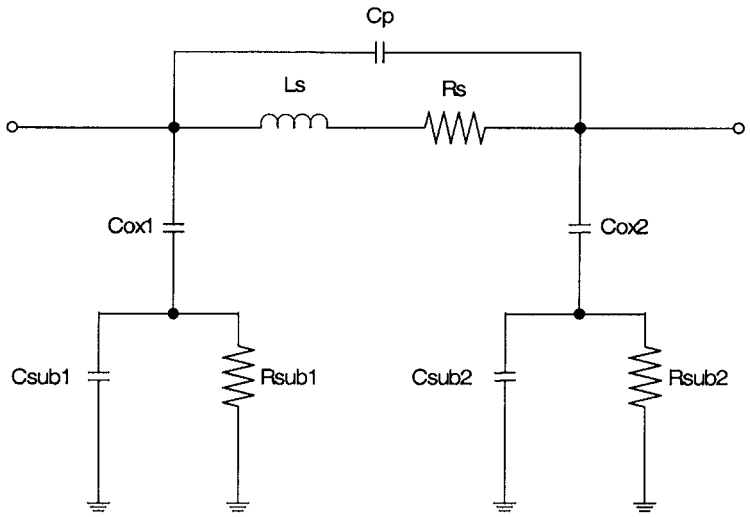

Fig. 1. Two ports conventional equivalent integrated inductor circuit model.

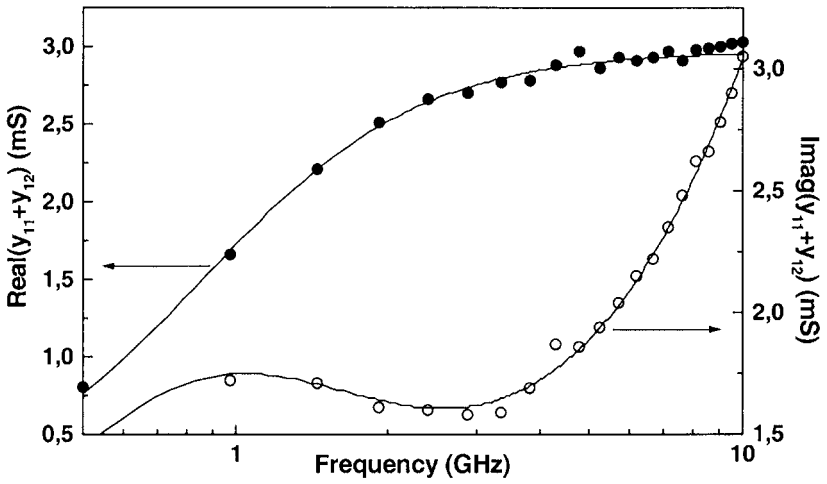

Fig. 2. Measured (circles) and computed (lines) real (solid circles) and imaginary (open circles) parts of the input-to-ground branch admittance against frequency.

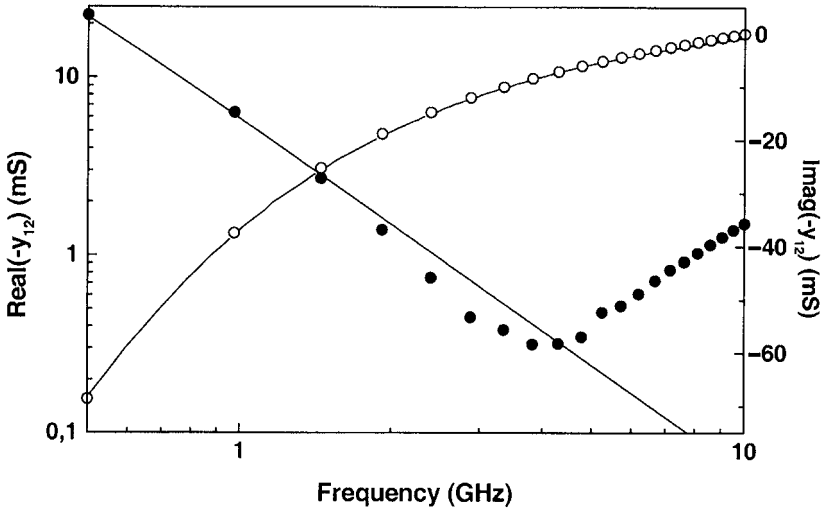

Fig. 3. Real (solid circles) and imaginary (open circles) parts of the main branch admittance vs. frequency and the result obtained with the conventional model. Lines are modeled values.

[3,4,7]. However, at higher frequencies the error increases. We call it a narrow band model. A narrow band model is a lumped equivalent circuit model, with frequency independent parameter values, which correctly predicts the integrated inductor behavior in a small frequency interval. Considering Fig. 1, the inductance and the resistance seen from any of the ports will have the measured values only at the central frequency of the interval. The error is significant at frequencies far from that in which the integrated inductor was characterized.

Conversely, we call wide band model to an equivalent circuit model that correctly predicts the integrated inductor behavior in a wide frequency range.

Narrow band model development requires the characterization of all the measured integrated inductors at every possible operating frequency. For example, if we have five operating frequencies and 10 structures for every frequency, we will then need to build-up 250 different narrow band models for the complete characterization of the integrated inductors. This figure shows

that the parameter extraction for narrow band modeling can be very slow. Besides, the great number of available narrow band models (one for each operating frequency) makes difficult the selection of the best possible integrated inductor for a particular design. Moreover, an integrated inductor operating at a frequency not previously considered will not be adequately modeled. However, the error is very small for those integrated inductors included in the library, and this modeling strategy usually satisfies the designer's requirements.

Wide band models would allow the exploitation of integrated inductors to the limit of the technology. This is because they allow us to implement optimization routines, and the selection of optimal structures. Thus, an integrated inductor, conceived to operate at a particular frequency, could be useful at a different frequency; but this only can be guaranteed if the wide band model is available. Otherwise, the simulation at the second frequency will not be reliable. Having the wide band models for the complete set of fabricated and measured integrated inductors would enlarge the number of structures to be selected by the designers.

A possible methodology to make wide band models is simply to adequately merge narrow band models. But not necessarily all the narrow band models present the same circuit topology (in some cases a circuit element can be imposed to be zero) and this introduces additional complexity in model development and characterization. Another possibility is to force the equivalent circuit elements to depend on frequency. In this case the problem is that typical electrical simulators cannot manage frequency dependent model parameters. In the following sections we present new models to improve the wide band modeling of integrated spiral inductors.

3. Modified Model

As the operating frequency increases, above 4 or 5 GHz for our technology (see Fig. 2 and Fig. 3), the substrate losses are dominant. Therefore, it is needed a better substrate (for example Silicon On Insulator, SOI), or the introduction of pre- or post-processing steps in the fabrication process on silicon (non-standard technologies). In those cases it should be necessary to improve the equivalent circuit model making emphasis in the integrated inductor behavior at higher frequencies. The models proposed here would be necessary when the substrate losses are reduced.

The modified model presented here is shown in Fig. 4. There is a new resistor R_P [9] in series with the capacitor C_P. R_P accounts for the under-pass oxide leakage and high frequency effects (eddy currents) that constrains the use of only a capacitor at certain frequencies. These elements must be taken into account in modeling the integrated inductor response in the complete working frequency range.

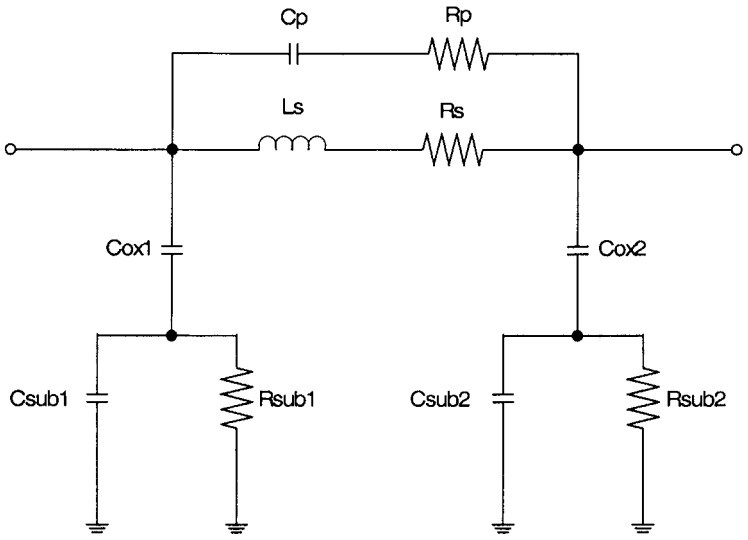

Fig. 4. Modified two ports integrated inductor model.

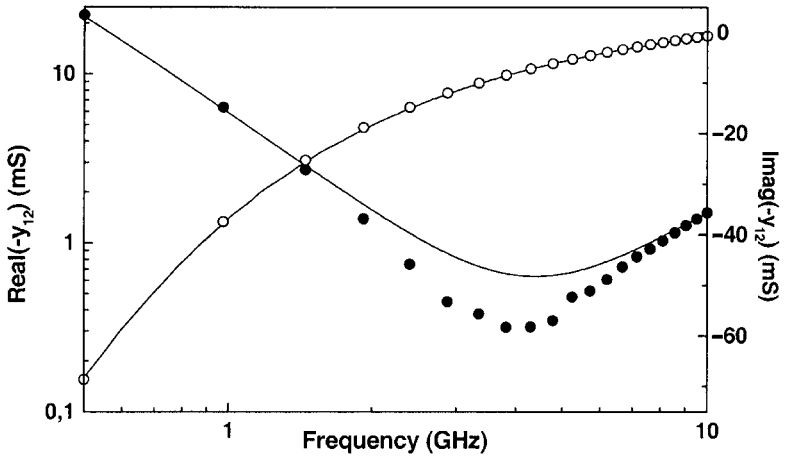

Fig. 5. Real (solid circles) and imaginary (open circles) parts of the main branch admittance vs. frequency and the result obtained with the modified model. Lines are modeled values.

As in Fig. 3, Fig. 5 shows the measured real and imaginary parts of the main branch admittance and the result obtained with the modified model against frequency. R_P in conjunction with C_P makes the overall model to fit better to the measurements, especially at high frequencies. In some cases the error is appreciable near the valley.

4. Improving the Modified Model

The modified model increase the precision reached with the conventional model but the fitting is not precise at some frequencies. In order to improve the accuracy we have analyzed two possibilities.

The first one is to introduce more fitting components adding two new circuit elements to the modified model, an inductor L_P in parallel with R_P, and a capacitor C_S in parallel with R_S (the names for these new elements do not have any special meaning, see Fig. 6). Figure 7 shows how the accuracy has been improved, especially around the valley. However, the same does not occur for inductor with metal traces wider than around 20 μm.

The second one has already been mentioned: force the equivalent circuit elements (L_S, R_S, C_P, and R_P) to

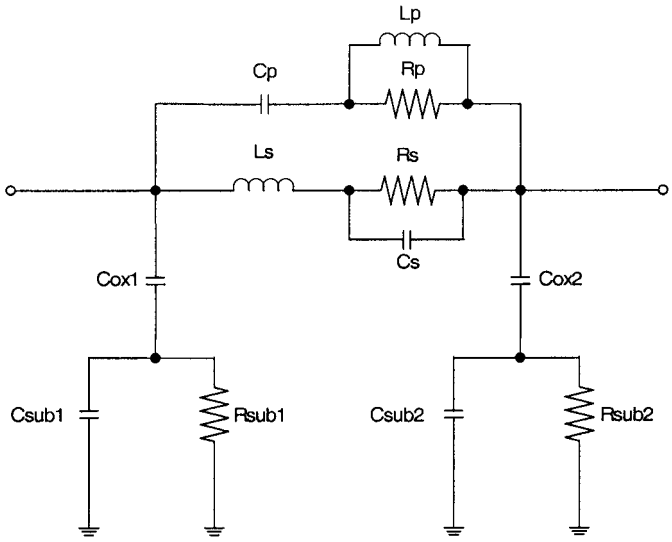

Fig. 6. Modified two ports integrated inductor model with more components (non-physically based).

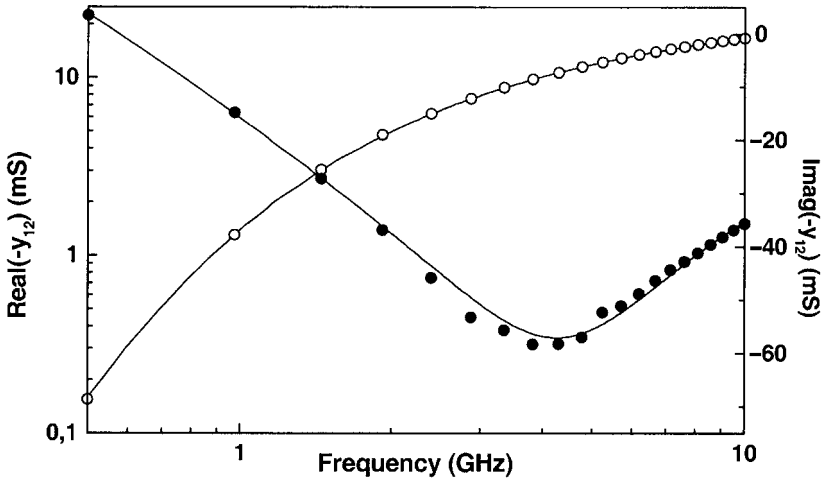

Fig. 7. Results for the modified model with more components.

depend on frequency. With these results we can give the narrow band model for every frequency. The problem is that the usual electrical simulators do not permit us to introduce frequency dependent model parameters. As a result, we need a tool to generate the narrow band model for every application in order to simplify the selection.

5. Parametric Model

The presented models contain model parameters extracted from measurements. Therefore, the integrated inductors must be fabricated before modeled. This is a good methodology for the development of a library of integrated inductor to be used in circuit design. Sometimes there is a need for an element not included in the library, and we should be able to calculate the lumped equivalent circuit of the integrated inductor. Thus, analytical expressions for the lumped elements are needed; these expressions constitute a parametric model. They will enhance the resulting tools to automate the design tasks. A widely accepted parametric model is reported in [8]. Here we propose modified expressions for some parameters together with a new formula for the resistor R_P.

An expression to calculate the inductance is reported in [8]. There the influence of the metal strips needed to assemble the device terminals is neglected, but it can be important in some cases. We have found that this additional inductance is proportional to the total terminal length. That is the reason why we introduce the second addend in the following equation

$$L_S \approx \frac{K_e \cdot \mu_o \cdot n^2 \cdot a^2}{22 \cdot r - 14 \cdot a} + K_t \cdot l_t \tag{1}$$

where K_e and K_t are technology dependent empirical constants; μ_o is the vacuum permeability, n is the number of turns, a is the average radius, r is the maximum radius, and l_t represents the total terminal length (see Fig. 8). In our standard CMOS technology $K_e \approx 30$, and $K_t \approx 3\ \mu$H/m.

Series resistance, R_S, should be computed from electromagnetic (EM) simulation [10], because an analytical solution for the problem is not available. But simulation requires large CPU times and not always converges to a solution. We have solved a simplified one-dimensional EM problem for an isolated squared metal strip [11], which is the basis for the following semi-empirical equation

$$\frac{R_S}{l} = \frac{1}{2\sigma w \delta_{1D}} \frac{sh\frac{t}{\delta_{1D}} + \sin\frac{t}{\delta_{1D}}}{ch\frac{t}{\delta_{1D}} - \cos\frac{t}{\delta_{1D}}} \tag{2}$$

where l represents the total spiral length, σ is the metal conductivity, w is the metal width, and δ_{1D} is the following empirical skin depth

$$\delta_{1D} = \sqrt[3]{\frac{t}{w}}\,\delta; \quad \delta = \sqrt{\frac{1}{\pi f \mu \sigma}} \tag{3}$$

where f is the frequency of operation.

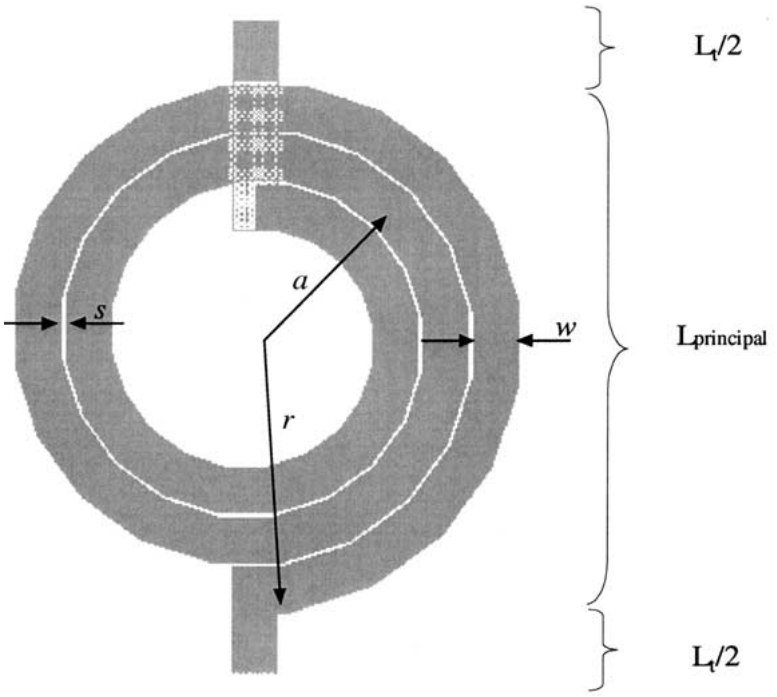

Fig. 8. Integrated inductor layout showing the terminals.

Figure 9 plots the ratio R_S/R_{DC} (R_{DC} represents the series resistance in direct current) predicted by equation (3) (solid line) against simulation results (hollow circles) from [10] for a strip exhibiting a $w/t = 6$. Note how our expression underestimates the series resistance as frequency increases and it should not be used, but at low or moderate frequencies it offers a good approximation. This R_S model gives a better approximation than DC resistance up to 10 GHz. It is easily computed, in higher resistive substrates than silicon its use is recommended.

As proposed in [8] C_P models capacitive couplings between the spiral strips and the underpass and between strips in different turns. The last contribution is usually neglected, but we have observed that it may be important. Therefore, the expression for this capacitance is

$$C_P = \frac{n_u \cdot w^2 \cdot s + l_t \cdot t_m \cdot t_{ox\,M1-M2}}{t_{ox\,M1-M2} \cdot s} \cdot \varepsilon \qquad (4)$$

n_u represents the number of crossings between the spiral strips and the underpass, l_t is the length of the region along which the strips are capacitively coupled, t_m represents the metal thickness, and s the spacing of the metal strips, $t_{oxM1-M2}$ is the oxide thickness separating the under-pass and the spiral, ε is the oxide permittivity.

Resistor R_P becomes important as the substrate losses decrease (SOI or non-standard processes). It is related to high frequency effects (eddy losses) and with losses in the metal-oxide contacts. At our range of frequencies this resistance is nearly constant, for a given the topology. It can be calculated from the following heuristic equation [11]

$$R_P = \frac{1}{l_t \cdot t_m + n_u \cdot w^2} \cdot \rho_C \qquad (5)$$

where ρ_C is a technology dependent parameter. Its value is approximately 0.2 Ωmm^2.

Expressions for the remaining model parameters are the following [8]

$$C_{OX} = w \cdot l \cdot \frac{\varepsilon}{t_{ox}}, \quad R_{SUB} \approx \frac{2}{w \cdot l \cdot G_{SUB0}}, \quad C_{SUB} \approx \frac{w \cdot l \cdot C_{SUB0}}{2} \qquad (6)$$

where t_{OX} represents the separation between the spiral and the substrate, G_{SUB0}, and C_{SUB0} are both technology dependent parameters. A typical value for G_{SUB0}

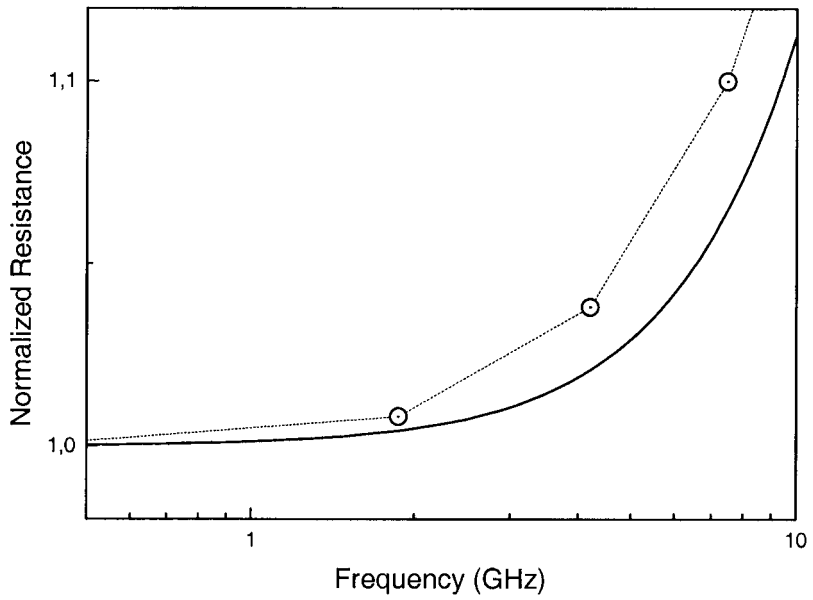

Fig. 9. Normalized resistance (R_S/R_{DC}) against frequency for an integrated inductor with $w/t = 6$. Hollow circles represent simulation results; solid line represents the proposed model. $\sigma = 3.54 \cdot 10^7$ S/m.

is 10^{-7} S/μm^2 while C_{SUB0} ranges in the interval from 10^{-3} to 10^{-2} fF/μm^2.

Expressions for the quality factor can be derived from the set of equations (1)–(6).

Our equations are coded in a set of tools that requests the desired inductance value at a determined frequency and gives back the geometry of the better inductors available in a particular technology.

6. Automatic Selector and Design Tool

In addition to the automatic selector that uses the models with extracted parameters (reported in [1]), we have coded the parametric model in SKILL language. The resulting integrated inductor design program is now embedded into Cadence [9]. In this manner, if a particular element is not included in the library of integrated inductors the designer may easily find the structure that fulfills the constraints, provided that exists.

The Component Description Format (CDF) of our tool is shown in Fig. 10. The user must introduce the frequency of operation and the required inductance values ($\pm$0.2 nH). The program evaluates wether or not the required inductor can be produced by the technology used, and computes its geometry. The output is a list of integrated inductors ordered by the estimated value of the quality factor. In this manner the designer has an additional degree of freedom to select, for example, a small structure with a quality factor slightly smaller than the quality factor of the larger inductor.

The tools can also be used together with circuit optimizers without limitation in the inductance values because the lumped equivalent circuit is known from the parametric model.

Making by hand the layout of a spiral integrated inductor is slow and error prone. We have developed a user-friendly tool, an Automatic Layout Generator, which automatically generates the layout. The program is almost independent of the technology (except for a technology file) and has different options. Figure 11 shows the CDF for the developed Automatic Layout Generator. As we have written in Section 5, it can be linked to the Automatic Selector or used independently. It is a parametric cell with the following main parameters: number of turns (restricted to multiples of 0.25), outer radius, metal width, metal strips separation, the metals that will implement the spiral and the output. These parameters cannot have arbitrary values; the tool will correct any non-permitted values if introduced erroneously.

The other parameters are the number of sides per turn (allows squared, octagonal or any other integer

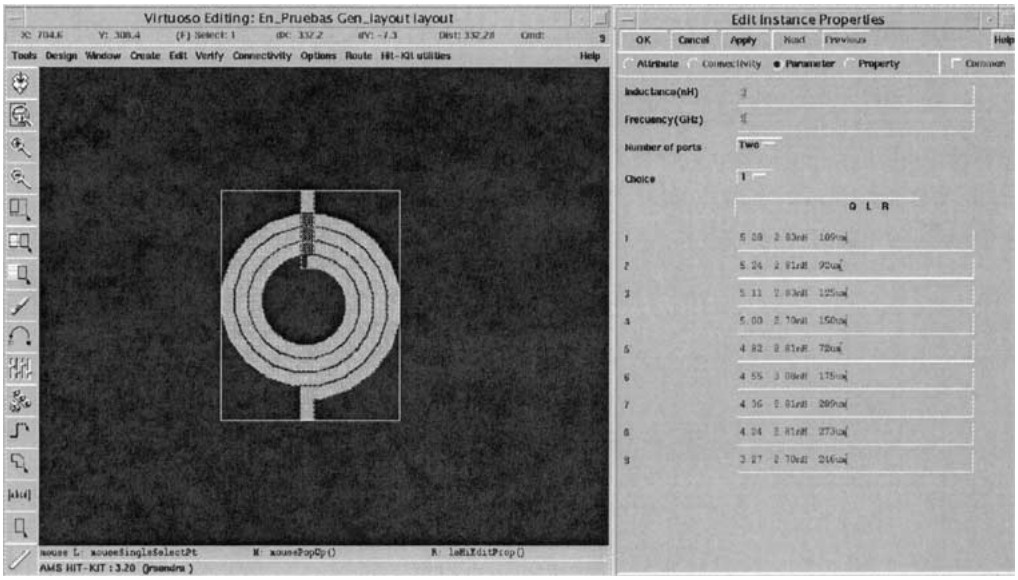

Fig. 10. Automatic integrated inductor generator based on the parametric model.

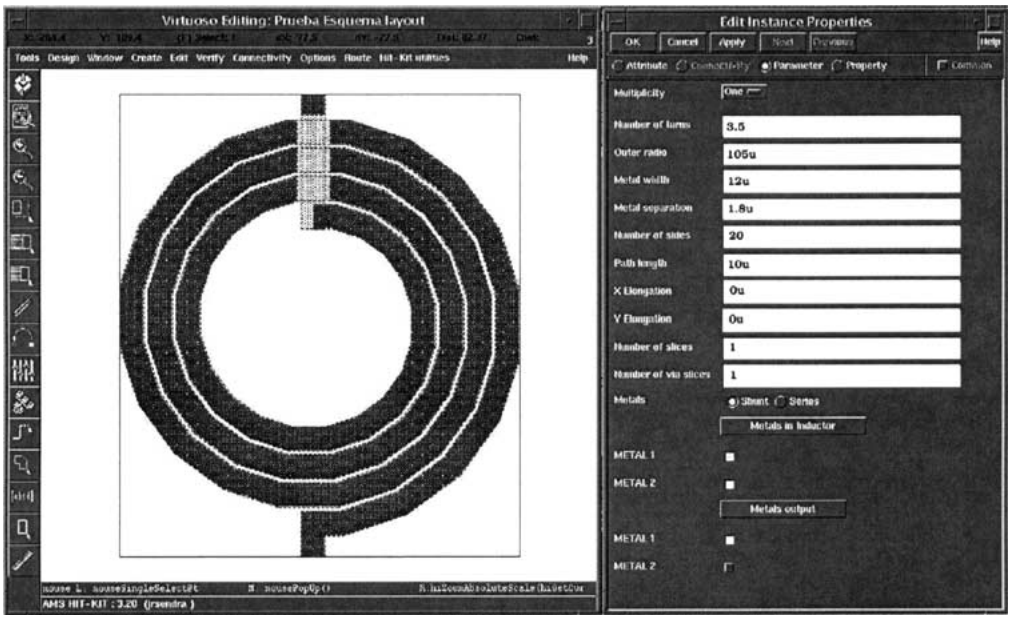

Fig. 11. Automatic layout generator.

number), and the length of the terminals. It permits to elongate the spiral in the horizontal or vertical direction. Also, the tool allows placing multilevel spiral inductors and associations of multiple spirals in the same metal level. The program has some other features.

7. Conclusions

In this paper we report our work in modeling spiral-integrated inductors based on measurements taken from integrated inductors on a standard silicon

technology. These models extend the application of the conventional model being wide band models: inductor behavior is represented in a wide frequency range. Also a parametric model based on the existing literature is reported.

The extracted models are valid up to 10 GHz with a maximum error in the quality factor estimation smaller than 10% in all studied cases, while the parametric model may introduce greater errors (we have measured up to a 15–20%).

Different CAD tools to assist the designers in designing and automatically laying-out integrated inductors are also reported. The desired inductance and the operating frequency are given to the tool as inputs and the result is the integrated inductors fitting the requirements, the lumped equivalent model so as the layout. These programs reduce the design time needed to meet RF circuit constraints.

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Antonio Nunez was born in Madrid, Spain, in 1951. He received the Engineering degree in 1974 from the School of Telecommunication Engineering at the Technical University of Madrid, and received the Ph.D. degree in 1981 from the same university. From 1974 to 1976 he worked as a consultant for Telefonica. He was a research scientist with the Electrical Engineering Department of EPFL Lausanne in 1981, and a visiting scientist (1986–1987) and visiting professor (1987–1988) at the School of Electrical Engineering of Purdue University, USA. He was appointed titular professor at the

University of Las Palmas GC, in 1982, and professor in 1989. He is currently director of the Research Institute for Applied Microelectronics. He has published five books, over 40 journal papers, and 80 conference papers. His current research fields include GaAs and Compound Semiconductor IC Design, RFIC and High Speed IC Design, and optimization of integrated circuits (including routing and layout techniques, power estimation, timing and interconnect analysis).