Temperature in HFETs when operating in DC

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ABSTRACT

This work analyses the DC response of InGaAs channel Modulation Doped Field-Effect Transistors, when varying temperature from 300 to 400 K. An analytic model for the intrinsic drain current is derived from previous work, done for a similar AlGaAs channel device, in order to explicitly show the temperature dependence. The extrinsic resistances are numerically evaluated and added in a straightway form to the model. Experimental output characteristics at different temperatures of an InGaAs HFET in static operation are compared with those offered by the resulting extrinsic model and numerical simulations. Computed relative errors are around 10%.

Keywords: HFET´s, semiconductor device modeling, temperature, numerical simulations, static operation.

1. INTRODUCTION

InGaAs channel Heterostructure Field-Effect Transistor (HFET), having typical cut-off frequencies of various tens of GHz, exhibits excellent properties for ultra fast operation[1]. As result, a great number of applications in Microwave Monolithic Integrated Circuits (MMICs) are based on this transistor[2,3]. Typical temperatures of operation are moderate, from 300 to 400 K. Nevertheless, device characteristics of HFETs may significantly change in this range[4, 5].

The motivation of this paper is to find a fully physics-based model that predicts the temperature-dependent behaviour of InGaAs HFETs in static operation, but, at the same time, simple enough to be implemented in a circuit simulator such as SPICE.

Several models, including temperature dependence, have been previously published for intrinsic HFETs. However, even when they are physics-based, usually incorporate empirical parameters[6] or, if that is not the case, are applied to the more simple AlGaAs/GaAs system[7]. Anyway, the extrinsic resistances need to be measured and added later as external circuit elements to the overall simulation. Usually the extrinsic resistances are extracted at different temperatures in the linear region, assuming that in saturation their values are preserved[5, 8]. Furthermore, when simulated, the source and drain series resistences are assumed equal[5], without any consideration about the electron transport through the heterojunction that forms the channel[9].

The InGaAs HFET under study is presented in section 2. For this transistor we report in section 3 an analytical study of the intrinsic behaviour, derived from one presented for AlGaAs/GaAs[7]. The model is extended in a straightway form to incorporate the extrinsic resistances in section 4. Section 5 is devoted to emphasize the temperature dependences of the model parameters. To extract the extrinsic resistances at any operating biases, the HFET is numerically simulated in section 6, where results for the output characteristics derived from the model and simulations at different temperatures are compared with measurements. Finally, some conclusions are given in section 7.

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2. THE InGaAs HFET

The HFET layer arrangement, shown in Fig. 1, correponds to a transistor reported[5] with a Schottky gate 3 μm long and 55 μm wide. The operation is based on the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As/GaAs$ heterostructure. The n^+ GaAs cap layers, that form the source and drain ohmic contacts, are uniformly doped with a $4\cdot10^{18}$ cm^{-3} donor concentration. To avoid an abrupt transition between the caps and the barrier, $Al_xGa_{1-x}As$ is added with the material composition, x, varying linearly from 0 to 0.28, and the donor concentration from $4\cdot10^{18}$ to 10^{18} cm^{-3}. Two $Al_{0.28}Ga_{0.72}As$ supply layers are followed by intrinsic $Al_{0.28}Ga_{0.72}As$ (spacer). It follows an undoped $In_{0.15}Ga_{0.85}As$ region (the channel), and an undoped $Al_{0.5}Ga_{0.5}As$ layer is placed at the bottom (substrate). Then, a double conduction level discontinuity is located at the borders of the high mobility $In_{0.15}Ga_{0.85}As$ channel. For all layers the material composition, geometrical paremeters and doping, when used, are shown in Fig. 1.

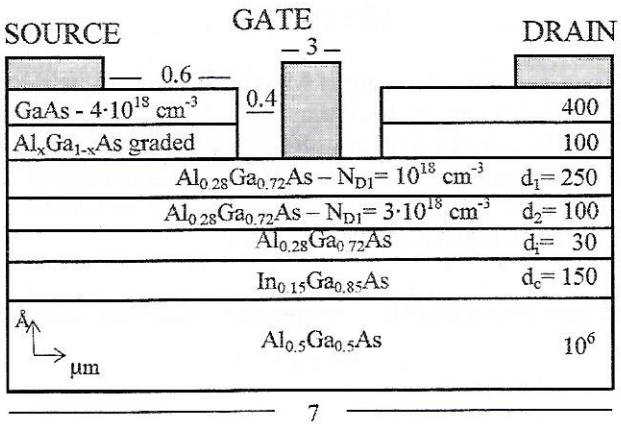

Figure 1. PHFET structure

3. INTRINSIC MODEL

3.1 Charge control model for static operation

A charge control model for AlGaAs/GaAs heterostructures has been presented[7]. There are several differences between these heterostructures and the AlGaAs/InGaAs/GaAs system investigated:

a) no uniform doping
b) double conduction band discontinuity in the channel
c) the channel material itself

These three differences are going to be incorporated in the analysis reported[7] with the following restriction: the gate voltage is low enough so that the depletion region is extended through the whole AlGaAs barrier. In this manner the undesired parasitic MESFET is avoided.

At medium/high temperatures all impurity donors are ionized. Then, solving the Poisson equation under the gate electrode, the pinch-off barrier energy, ΔE_{PO}, is given by

$$\Delta E_{PO} = \frac{q^2}{\varepsilon_b}\cdot\left(\frac{N_{D1}d_1^2}{2}+\frac{N_{D2}d_2^2}{2}+N_{D2}d_1d_2\right) \quad (1)$$

where N_{D1} and N_{D2} are the donor doping concentrations of the $Al_{0.28}Ga_{0.72}As$ supply layers, d_1 and d_2 represent their respective depths (see Fig. 1), ε_b is the $Al_{0.28}Ga_{0.72}As$ permitivity, and q is the absolute electron charge.

The electron concentration in the channel, n, depends on the Fermi energy level. This dependence should been obtained solving auto-consistently the Schrödinger and Poisson equations. However, for simplicity, we use a linear approximation as for the AlGaAs/GaAs system, but replacing the Drummond factor[10] by the channel depth, d_c. Then,

$$E_F \approx E_{FO} + \frac{q^2 \cdot d_c}{\varepsilon_b} \cdot n \tag{2}$$

being E_{FO} the Femi energy level when the channel is depleted ($n = 0$). From Gauss theorem and the continuity of the normal component of the displacement vector at the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$ heterojunction, the electron concentration in the channel can be expressed as:

$$n = \frac{\varepsilon_b}{q(d + d_c)} \cdot (V_g - V_T) \tag{3}$$

d is the distance between the metal-semiconductor interface and the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$ heterojunction ($d=d_1+d_2+d_i$; see Fig. 1), V_g is the intrinsic gate-to-source voltage, and V_T the threshold voltage,

$$V_T = \phi - \frac{1}{q}\Delta E_C - \frac{1}{q}\Delta E_{PO} + \frac{1}{q}E_{FO} \tag{4}$$

where ϕ is the metal-semiconductor barrier height, and ΔE_C the conduction band discontinuity at the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$ heterojunction.

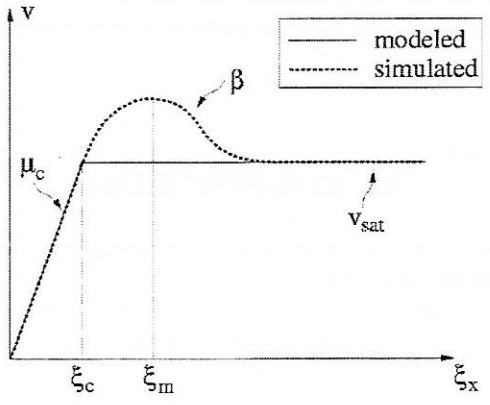

Figure 2. Electron mobility: two piecewise approximation

3.2 Current-voltage charasteristics in static operation

The electron velocity versus the longitudinal electric field, v-ξ_x, in an $In_xGa_{1-x}As$ channel is charaterized by a constant mobility region at low electric fields, μ_c, the electric field for which the velocity is maximum, ξ_m, some negative mobility at intermediate electric fields, modeled with β, and the saturation velocity in the channel, v_{sst} (see Fig. 2).

The intrinsic current in the channel is calculated in a simple way, assuming that v-ξ_x is expressed by the following two piecewise function:

$$v = \begin{cases} \mu_c \xi_x & for\ \xi_x \le \xi_c \\ v_{sat} = \mu_c \xi_c & for\ \xi_x > \xi_c \end{cases} \tag{5}$$

being ξ_c the electric field for which electrons would reach the saturation velocity. Thus, integrating along the channel, neglecting the diffusion current, and considering the gradual channel approximation, the current-voltage characteristic in the linear region can be expressed by

$$I_d = \frac{W \varepsilon_b \mu_c}{(d + d_c)L} \cdot (V_g - V_T - \frac{1}{2} V_d) \cdot V_d, \quad V_d \le V_{dsat} \tag{6}$$

where V_d is the intrinsic drain-to-source voltage, W is the transistor width, L the channel length, and V_{dsat} is the saturation intrinsic drain voltage, which is given by

$$V_{dsat} = V_c + (V_g - V_T) - \sqrt{V_c^2 + (V_g - V_T)^2} \tag{7}$$

with $V_c = L\xi_c$. In saturation region,

$$I_d = \frac{W \varepsilon_b \mu_c}{(d + d_c)L} \cdot V_c \cdot \left(\sqrt{V_c^2 + (V_g - V_T)^2} - V_c \right), \quad V_d > V_{dsat} \tag{8}$$

For this region the theoretical output conductance predicted is zero; as the channel length modulation is not being modeled (instead of L, an effective length should be included in case of submicron devices).

Comparisons between the intrinsic model and numerical simulations of the intrinsic structure have been done[11], showing relative errors smaller than 10% for drain currents and transconductances whatever applied biases, and output conductances in linear region.

4. EXTRINSIC MODEL

The extrinsic drain current in static operation is obtained considering the relation between the intrinsic and the external voltages applied to the HFET terminals:

$$\begin{aligned} V_d &= V_D - I_D \cdot (R_S + R_D) \\ V_g &= V_G - I_D \cdot R_S \end{aligned} \tag{9}$$

where V_D and V_G are the external drain and gate voltages respectively, R_S and R_D are the source and drain extrinsic resistances, and I_D is the extrinsic drain current. R_S and R_D are series resistances ($I_D = I_d$), substituting V_d and V_g in equations (6) - (8) by expressions (9), and solving for I_D, the extrinsic current-voltage characteristic in linear region, $V_D \le V_{Dsat}$, is found to be:

$$I_D = \frac{\gamma + \left(R_S + R_D\right)\cdot\left(V_G - V_T\right) - R_D V_D}{R_S^2 - R_D^2} - \frac{\sqrt{\left(\gamma + \left(R_S + R_D\right)\cdot\left(V_G - V_T\right) - R_D V_D\right)^2 + \left(R_S^2 - R_D^2\right)\cdot\left[V_D - 2\cdot\left(V_G - V_T\right)\right]\cdot V_D}}{R_S^2 - R_D^2} \tag{10}$$

with $\gamma = \frac{(d + d_c)L}{W \varepsilon_b \mu_c}$. In saturation region, $V_D > V_{Dsat}$:

$$I_{Dsat} = \sqrt{\gamma}\,\frac{\sqrt{\gamma V_c^2 + 2R_S V_c^2\cdot(V_G - V_T) + \gamma(V_G - V_T)^2} - \left[\gamma^2 V_c + \gamma R_S V_c\cdot(V_G - V_T)\right]}{\gamma^2 - R_S^2 V_c} \tag{11}$$

being the saturation drain voltage:

$$V_{Dsat} = V_c + (V_G - V_T) - \sqrt{V_c^2 + (V_G - V_T)^2} + I_{Dsat}\cdot(R_S + R_D) \tag{12}$$

Thus, the drain current in static operation is completely characterized once the extrinsic resistances of the transistor are known.

5. EXPLICIT TEMPERATURE FORMULATION

The temperature range considered in this paper is $T(\mathrm{K}) \in [300, 400]$[5]. In this range the relative permittivity, ε_b, Schottky barrier height, ϕ, and conduction band discontinuity, ΔE_C, are nearly constant, with values 12.2, 0.61 V and 0.34 eV respectively[5, 7]. The pinch-off barrier energy, ΔE_{PO}, given by expression (1), is 2.03 eV. Therefore, from equation (4), the threshold voltage depends on temperature as E_{FO} does. It is known that for AlGaAs/GaAs heterojunctions E_{FO} only diminishes 11 meV as temperature increases between 300 and 400 K[7]. In our case, E_{FO} is expected to vary in the same order of magnitude. Thus, we assume that the threshold voltage is not temperature dependent[6], and according with experimental measurements[5]; E_{FO} is set to that value for AlGaAs/GaAs heterojunctions at 300 K, and the resulting threshold voltage is negative: –1.20 *V*.

On the other hand, the low field electron mobility and the saturation velocity do depend on temperature. These dependences are obtained fitting the theoretical mobility reported[5], that considers the more relevant scattering mechanisms involved in transport, with some models reported[12]. Thus, μ_c and v_{sat} are given by

$$\mu_c = 6400\cdot\left(\frac{T}{300}\right)^{-2.2} \quad (cm^2/Vs) \tag{13}$$

$$v_{sat} = \frac{13\cdot 10^6}{0.7 + 0.3\cdot\left(\frac{T}{300}\right)} \quad (cm/s) \tag{14}$$

The electric field for which electrons reach the saturation velocity is also temperature dependent. From equations (5),

considering (14) and (15), the resulting expression can be adjusted linearly:

$$\xi_c = \frac{v_{sat}}{\mu_c} \approx -2334 + 14.5 \cdot T \quad (V/cm) \tag{15}$$

The only relevant temperature dependence still unknown is that for the extrinsic resistances. Usually the extrinisic resistances are measured at very low drain voltages[13], and assumed equal when simulated[5]. Nevertheless, in order to evaluate properly the extrinsic model their values must be known at different temperatures and biases. For this purpose the HFET is numerically simulated as reported in the following section.

6. NUMERICAL SIMULATION

6.1 The simulation: relevant considerations

The HFET gate length, 3 μm, is long enough, so that the simulation can be performed using the drift-difussion approximation[12]. For the electron mobility in the channel, μ, a velocity-field dependence that includes the negative region is used[12] (see Fig. 2):

$$\mu = \frac{\mu_c + v_{sat} \cdot \dfrac{\xi_x^{\beta-1}}{\xi_m^{\beta}}}{1 + \left(\dfrac{\xi_x}{\xi_m}\right)^{\beta}} \tag{16}$$

where μ_c and v_{sat} are temperature dependent and given by equations (13) and (14). Fitting the mobility reported[5], the electric field for which the electron velocity is maximum, ξ_m, is set to $4 \cdot 10^3$ Vcm^{-1}, and the negative mobility region is included doing $\beta = 4$.

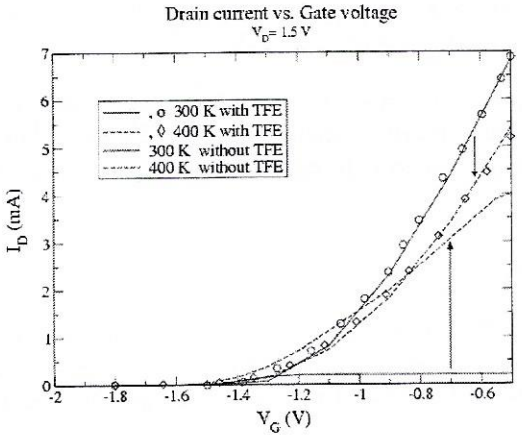

Figure 3. Impact of the tfe model on the transfer characteristics

Previous works[14, 15] have mentioned the necessity of including some heterojunction model at the upper border of the channel to predict the transistor performance, specially when the temperature dependece is considered[16]. In our case, a termionic-field-emission (TFE) model[17] is used to simulate the electron transport through the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$ heterojunction (the effective length of the TFE model is set to 7 nm [16]).

As far as we know, any influence of the TFE model on the extrinsic resistances has not been already established. In HFETs, the intrinsic drain current, transconductance and output conductance show an inverse temperature dependence. When considering the extrinsic resistances these dependences are preserved[5]. In order to show the impact of the TFE model in simulations, Fig. 3 plots the input characteristics of our HFET at 300 and 400 K in saturation region (V_D= 1.5 V). The measurements are presented with open symbols. The simulated values at 300 and 400 K are plotted with solid and dashed lines respectively; those closer to the measurements are considering the TFE model. Notice that without TFE not only the drain current is underestimated, mainly at 300 K, but also the temperature dependence predicted is opposite to the actual (similar results are obtained for the transconductance). This behaviour is attributed to the electron transport through the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$ heterojunction and conditions the extrinsic resistances.

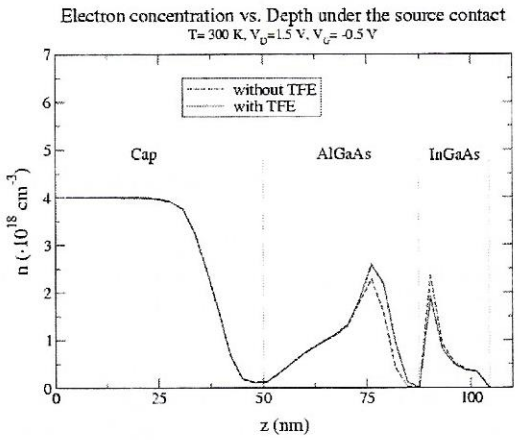

Figure 4-a. Electron concentration profile under the source contact: influence of the tfe model

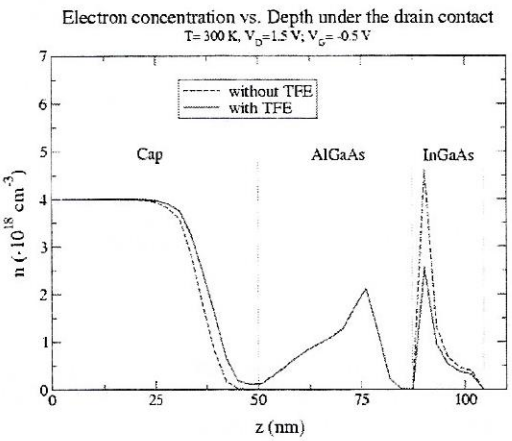

Figure 4-b. Electron concentration profile under the drain contact: influence of the tfe model

6.2 Extrinsic resistances

When the gate voltage is low enough to avoid the undesired MESFET parasitic (our case) and current flows, the electrons have to cross the depletion region beside the spacer layer (depletion region in the $Al_{0.28}Ga_{0.72}As$ barrier caused by emigration of electrons into the channel) twice, once under the drain contact and another one under the source contact. The resistivity of these regions and its temperature dependence are crucial to determine the overall transistor performance, specially when the gate length is reduced. The probability for an electron to cross the energy barrier at the upper interface of the channel under the ohmic contacts, either by thermionic emission or tunneling, can not be neglected[17]. In this way, the electron profile under the ohmic contacts can be modified, and so the extrinsic resistances.

The TFE model implemented in the simulator[17] considers the tunnel current across the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$ heterojunction only when electrons flow from the semiconductor with the lowest energy gap to that with the highest (when electrons leave the channel). However, the thermionic emission is considered in both directions. Therefore, different extrinsic resistances at the source and drain contacts should be expected. Figures 4 represent the simulated electron profile under the source (4-a) and drain (4-b) contacts respectively, when the transistor operates in saturation region (V_G=-0.5 V, V_D= 1.5 V), with and without considering the TFE model at the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$

heterojunction; z represents the depth from the gate electrode. For both contacts, the TFE model predicts a greater electron concentration in the barrier, and a lower one in the channel. Under the source contact, because only the thermionic effect is involved, the electron profile is practically not modified by the TFE model. Nevertheless, under the drain contact the impact of the tunnel current can not be ignored. Without considering the TFE model the AlGaAs barrier is totally deplected, and the electron concentration in the channel is overestimated. When the model is considered, a non-negligible electron concentration in the barrier appears, coming from the channel by tunneling. Hence, the extrinsic resistance for the drain contact is expected to depend not only on temperature, but also on the drain voltage. Figure 5 represents the simulated results for the extrinsic resistances under the source (dashed line) and drain (solid lines with symbols) contacts, at different temperatures and drain-to-source voltages.

The extrinsic source resistence is nearly constant. Whatever operating biases applied, the intrinsic source voltage is not high enough to turn-on the source-cap/barrier/channel equivalent diodes between the source and Schottky gate[9]. Thus, when temperature increases, the thermically generated electrons must be balanced with a mobility degradation (because of the inverse relation between resistivity, mobility and carrier concentration).

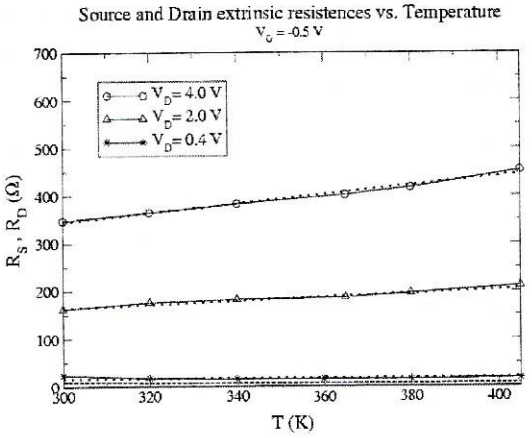

Figure 5. Extrinsic resistances dependence on temperature and operating biases

When electrons leave the channel they must overcome the conduction band discontinuity at the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$ heterojunction. Therefore, a higher value for the extrinsic drain resistence (R_D>R_S) should be expected, as found in Fig. 5. As higher the drain voltage is, as the drain-cap/barrier/channel equivalent diodes between the Schottky gate and drain contact are more inversely biased[9], increasing R_D. On the other hand, the extrinisic drain resistance has a linear and positive temperature dependence, raising as the transistor operates in saturation region. The high electron concentration in the barrier, due to tunneling (see Fig. 4-b), reduces the thermal electron generation. Therefore, the increase of R_D as temperature rises is attributed to degradation of the electron mobility.

Hence, we found that the extrinisic resistances can be approximated by the following expresions:

$$\begin{aligned} R_S &\approx 7.5\,(\Omega) \\ R_D &\approx R_{D,300}(V_D) + m(V_D)\cdot(T-300)\,(\Omega) \end{aligned} \tag{17}$$

$R_{D,300}$ is the voltage dependent extrinsic drain resistance at room temperature; m is also a drain voltage dependent parameter. Both can be expressed by a second order polinomial:

$$R_{D,300} = R_S + V_D \cdot \sum_{i=0}^{2} r_i \cdot V_D^i$$

$$m = V_D \cdot \sum_{i=0}^{2} m_i \cdot V_D^i \qquad (18)$$

where the coefficients m_i and r_i are given in table 1. For comparison, the extrinsic drain resistance modeled with (17) is represented in Fig. 5 with dotted lines. The agreement with numerically simulated values is quite good.

From equations (17) and (18), when the drain voltage diminishes R_D tends to R_S; the influence of the TFE model on the extrinsic resistances vanishes.

r_0 (Ω/V)	1.49	m_0 (Ω/VK)	-0.28
r_1 (Ω/V^2)	55.86	m_1 (Ω/V^{2}K)	0.36
r_2 (Ω/V^3)	-8.79	m_2 (Ω/V^{3}K)	-0.06

Table 1: Parameters for the drain voltage dependence of the extrinsic drain resistance

6.3 Results and comparisons

The drain current predicted by the model can be now evaluated substituting expressions (17) and (18) for the extrinsic resistances in equations (10)-(13). Figure 6 shows the results obtained for the output characteristics in our HFET at 300 and 400 K. The numerically simulated and measured values are plotted with closed and open symbols respectively, and the modeled ones with solid lines. Observe that the inverse temperature dependence of the drain current is adequately predicted, with a good correspondence in the transition from linear to saturation region. At room temperature the agreement is quite good. Only in saturation at very high drain voltage (V_D> 3 V) the experimental kink effect observed (may be due to impact ionization) is obviously not predicted. Nevertheless, this region should be avoided in practice to prevent a linear response. At 400 K, in linear region, the drain current is modeled precisely. However, it is underestimated in saturation because the channel length modulation is not being considered.

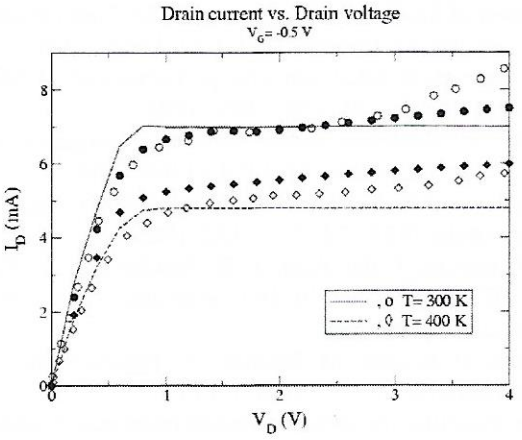

Figure 6. Temperature dependence of the output characteristics: results from measurements, numerical simulations and the proposed extrinsic model

With the proposed model all relevant DC electrical magnitudes, drain current, transdonductance and output conductance (in linear region) exhibit a decreasing temperature dependence, according with experimental

measurements. The relative error between measured and modeled values is smaller than 10% in the operation regimes of interest, and could be more reduced if the channel length modulation and an effective channel depth value for d_c were considered. In fact, it is well known that the electron concentration in the channel is not uniformly distributed in depth, but presents a maximum closer to the $Al_{0.28}Ga_{0.72}As/In_{0.15}Ga_{0.85}As$ heterojunction[18].

7. CONCLUSIONS

We have developed an analytical model to predict the temperature dependence of the drain current in an InGaAs HFET between 300 and 400 K. The extrinsic resistances were numerically evaluated considering a thermionic field emission model at the upper heterojunction in the channel, and were included in the model. We have found that the source extrinsic resistance can be assumed constant. However, the extrinsic drain resistance not only increases with temperature, as well known, but also as the transistor operates more in saturation region. Comparisons between measurements and our model results have been done for ouput characteristics at different temperatures, and demonstrate the ability of our model to predict the transistor behaviour, with maximum errors within typical values from other similar models. General and simple temperature dependent expressions have been also proposed, which can be implemented in circuit simulators.

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