# DC Modeling of PN integrated cross varactors

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## ABSTRACT

In this paper models for the capacitance of cross integrated varactors based in the PN junction are presented. Three different approximations are assumed, in order to reproduce the measured results of the capacitance. The relative error with the measured capacitance is under 10% in all cases.

## INTRODUCTION

Wireless systems demand low cost technologies for radio frequency applications. Radio Frequency Integrated Circuits (RFICs) based on silicon technologies are being working at different standards in the frequency range from 0.9 GHz to 6 GHz, such as GSM, GPS, UMTS, Bluetooth and WLAN. This development has been possible by the design of integrated passive components: inductors [1] and varactors.

Integrated voltage controlled capacitors (varactors) are used in multiple RF applications [2], [3]. The most common architectures for integrated varactors are PN junction [4], MOS [5] and gated varactors [6]. In this work PN varactors with squared cross geometry are analyzed [7].

Integrated varactors based on the PN junction was designed because this structure presents advantages over MOS and gated varactors, such as, a higher quality factor, easy scalability, and better linearity [4].

A PN junction varactor is formed by a $P^+$ diffusion on a N-well zone. The operation of these varactors is based on the junction capacitance associated to the depletion region between the $P^+$ diffusion (anode) and the N-well (cathode). $N^+$ diffusions are placed on the N-well for decreasing the series resistance of the device. The $P^-$ substrate is connected to ground. Being the PN junction under reverse biasing, a capacitance appears due to the depletion zone.

The aim of this papers is to model the capacitance of a PN cross varactor. This modelling process has been validated by fabricating integrated varactors and by comparing experimental results. It is only relatively recently that physical models have begun to find a role in contemporary engineering and there has been an effort to bridge the gap between theoretical principles and practical solutions. A finite-element based three stage solution process was introduced to model a silicon p-n junction varactor; using the initial conditions the semiconductor device equations were solved using the finite-element method [8].

The effect of the corners in the total capacitance is considered in Section 2. Section 3 is devoted to carry out three different models, and their results are compared with measurements in Section 4. Finally some conclusions are given in Section 5.

## 2. THE CORNER CAPACITANCE

In a PN junction, the depletion width varies with the bias voltage, and so does the capacitance. Then, structures with large perimeter per unit area are desirable [9], because they will present longer capacitance values. The square island configuration is normally used when a varactor is implemented with PN junction. These varactors require a huge amount of area in order to offer a typical tuning range from ±10% to ±20% [6] one solution is to increase the perimeter-per-unit-area longer than in a square island configuration, such as, interdigitated varactors [10] and cross varactors can be used: both geometries show an enhanced $P^+$ to N-well lateral contact surface, reducing the area occupied.

To make a cross varactor, $P^+$ and $N^+$ diffusions are inserted in cross shape, with some of the extreme arms removed to give a square form to the layout for better connectivity. The crosses have been designed with the same size of arm. The size of arms in N-cross is 13.6 μm, and 13.8 μm for the P+-cross. Then, cross varactors have been designed and fabricated with different sizes of occupied area: $0.25{\cdot}10^4$ μm$^2$, $1{\cdot}10^4$ μm$^2$ and $2.25{\cdot}10^4$ μm$^2$. In nominal size (i.e. $0.25{\cdot}10^4$ μm$^2$), the total number of crosses is twenty where ten are P+ cross island and other ten N+ cross island. For the other sizes the total number of cross island is 80 and 180. It is looked for to scalable the capacitance with these three sizes. Then, a varactor with $1{\cdot}10^4$ μm$^2$ will be four times higher than the nominal size and the biggest size will be nine times higher. The distance between a P+ cross and a N+ cross is the minimum value permitted by the technology AMS SiGe 0.8 μm standard process. The model will be applied a structure with two metals where to connect all crosses two metal layers have been used in order to minimize the resistance Figure 1 shows the layout of a cross integrated varactor with $0.25{\cdot}10^{-4}$ μm$^2$ occupied area.

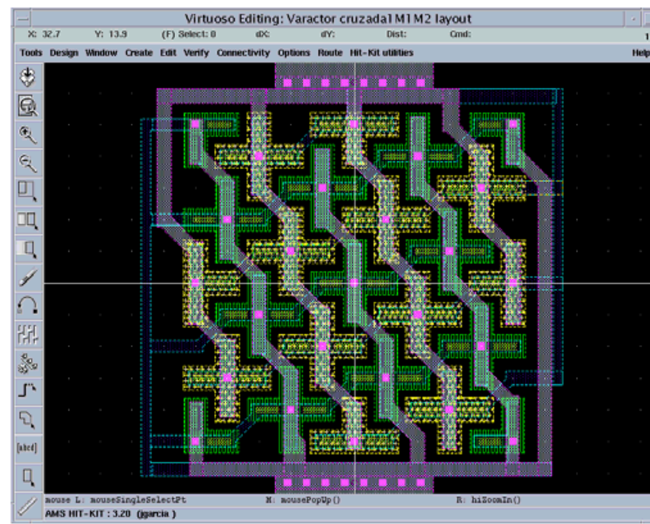


**Fig. 1** PN integrated cross varcator layout

The integrated varactor use the junction capacitance associated with the depletion region between the $P^+$ diffusion and the N-well, when reverse polarization is applied. The $N^+$ diffusions try to distribute in the structure the voltage applied to the cathode ohmic contact. Therefore, in our varactor the capacitance is due to eight complete crosses and four mutilated crosses $P^+$ type:

$$C = 4 \cdot C_{cm} + 8 \cdot C_c \tag{1}$$

with $C_m$ as the capacitance of a mutilated cross (without an arm) and $C_c$ is the capacitance of a complete cross.

Two contributions for the capacitance must be considered in every $P^+$ cross: the lateral capacitance and the capacitance under the cross (the area capacitance). For both, abrupt junction is assumed in the depletion capacitance. Capacitance under the crosses is similar to a typical PN junction, but the effect of the corners must be included when the lateral capacitance is studied.

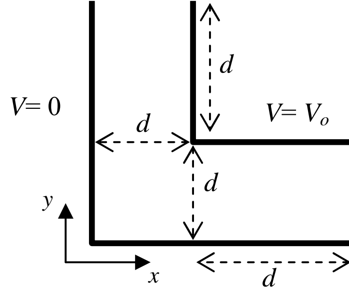


**Fig. 2** Capacitor in L

To model the effect of the corner in the lateral capacitances, we study an L formed capacitor, as figure 2 shows. Where $d$ is the square corner side and $L$ the arms length. We assume a capacitor Z width. For this varactor the capacitance, $C_L$, can be approximated by,

$$C_L = 2 \cdot C_{\|} + C_{\llcorner} \quad (2)$$

being $C_{\|}$ the capacitance of an ideal parallel-plate capacitor with the dimensions of the arms,

$$C_{\|} = \varepsilon \frac{ZL}{d} \quad (3)$$

with $\varepsilon$ the dielectric permittivity, and $C_{\llcorner}$ is the capacitance associated to the corner between the two flat capacitors. This is obtained solving the two dimensional Laplace equation,

$$\vec{\nabla}^2 V = 0 \quad (4)$$

with the following boundary conditions:

$$V = \begin{cases} 0 & if\ x = 0\ or\ y = 0 \\ V_o & if\ x = d\ or\ y = d \end{cases} \quad (5)$$

with $V_o$ as the applied voltage. Applying the separate variables method, the potential in the corner is given by,

$$V(x, y) = \frac{V_0}{d^2} xy \quad (6)$$

From the electric field ( $\vec{E} = -\vec{\nabla} V$ ) at the lateral contour of the corner, and considering its relation with the electron charge density ( $\rho_s = E \cdot \varepsilon$ ), the capacitance of the corner can be approximated by,

$$C_{\llcorner} = \varepsilon Z \quad (7)$$

Therefore, the total capacitance in the L formed capacitor is:

$$C_L = 2\varepsilon \frac{ZL}{d} + \varepsilon Z \qquad (8)$$

In order to validate this expression, the L form capacitor was numerically simulated with SAP [11]. The results for the electric field are shown in figure 3.

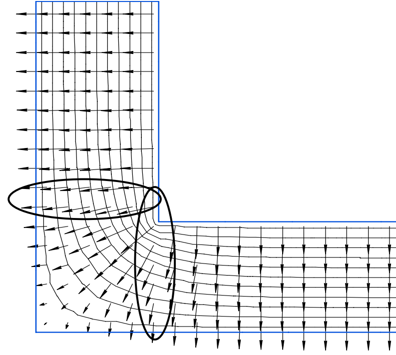

**Fig. 3** Electric field into the corner

It is shown that the electric field around the boundary between the corner and the arms has a normal component, due to the border effect of the capacitance of the arms. This effect reduces the corner capacitance, and it is considered using a fitting parameter, *K*, in equation (8),

$$C_L \approx 2\varepsilon \frac{ZL}{d} + K\varepsilon Z \qquad (9)$$

From simulations, $K = 0.5$: the capacitance of the corner is half the theoretically expected.

## 3. MODEL DEVELOPMENT

In order to determine the $P^+$-N well capacitance, three alternatives have been studied: the approximate, rectangular and spherical-cylindrical model.

### 3.1. Approximate model

In the approximate model the complete arms of the crosses are considered as parallel-plate capacitors (*i.e.* the effect of the corner is neglected). Thus, the cross capacitance $C_c$ is approximated by,

$$C_c = 12\varepsilon \frac{L \cdot X_{jp}}{W} + 5\varepsilon \frac{L^2}{W} \qquad (10)$$

And the mutilated cross capacitance $C_m$ by,

$$C_c = 10\varepsilon \frac{L \cdot X_{jp}}{W} + 4\varepsilon \frac{L^2}{W} \qquad (11)$$

where the first terms correspond to the area capacitance, and the second ones to the lateral capacitance; $X_{jp}$ is the depth of the diffusion and $W$ is the depletion region width.

### 3.2. *Rectangular* model

In this model the effect of the corner in the lateral capacitance is taking into account through equation (9), where the region arms do not perform as parallel-plate capacitors any more. Therefore, for the cross varactors:

$$C_c = 4\varepsilon\left(X_{jp} - x_p\right)\left[\frac{L_M}{W} + 3K + 2\frac{L_m}{W}\right] + \varepsilon\left[\frac{4L_M L + L_M^2}{W} + 8KL_m + 4KL_M + 12\frac{3}{4}KW\right] \quad (12)$$

And for the mutilated cross varactors,

$$C_c = 4\varepsilon\left(X_{jp} - x_p\right)\left[\frac{L_M}{W} + 4K + \frac{3}{2}\frac{L_m}{W}\right] + \varepsilon\left[\frac{3L_M L + L_M^2}{W} + 6KL_m + 4KL_M + 8\frac{3}{4}KW\right] \quad (13)$$

where the first terms correspond to the area capacitance, and the second ones to the lateral capacitance; $L_m$= *L-W; $L_M$* = *L*-2$X_p$ and $X_p$ is the depletion region width in the $P^+$ semiconductor.

### 3.3. *Spherical*-cylindrical *model*

In the spherical-cylindrical model the shape of the $P^+$ diffusions is treated in a more realistic way. When a $P^+$-N well junction is formed by diffusion into a bulk semiconductor, through a window in an insulating layer, the impurities will diffuse downward and also sideways. Hence the junction consists of flat region with approximately cylindrical edges, as shown in figure 4.

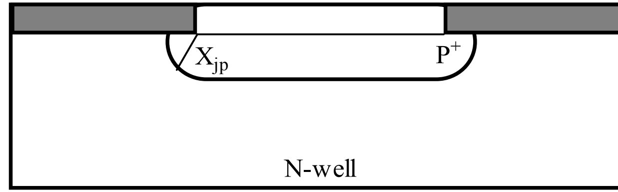


**Fig. 4** P+ diffusion cross-section

In addition, if the diffusion mask contains sharp corners, the junction near the corner will be roughly spherical in the shape. In this way, cross capacitance for spherical-cylindrical model is

$$C_c = 2\pi\varepsilon\frac{3L - 4X_{jp}}{\ln\frac{X_{jp} + W/2}{X_{jp} - W/2}} + 6\pi\varepsilon\frac{X_{jp}^2 - \left(\frac{W}{2}\right)^2}{W} + 5\varepsilon\frac{L^2}{W} \quad (14)$$

And the mutilated cross capacitance is

$$C_m = \pi\varepsilon\frac{5L - 4X_{jp}}{\ln\frac{X_{jp} + W/2}{X_{jp} - W/2}} + 4\pi\varepsilon\frac{X_{jp}^2 - \left(\frac{W}{2}\right)^2}{W} + 4\varepsilon\frac{L^2}{W} \quad (15)$$

being the first terms the cylindrical lateral capacitance, the second ones the spherical capacitances at the corners, and the third ones the area capacitance.

## 4. RESULTS AND COMPARISON

The varactor with cross geometry have been designed and fabricated in the AMS SiGe 0.8 μm standard process. In Fig. 5, a microphotography of a 0.25 $10^{-4}$ μm integrated cross varactor is shown. These varactors were measured with a Vector Network Analyzer HP8719ES. To calibrate the measurement system, the short-open-load-through (SOLT) was used. The varactors have been fabricated together with a measurement structure in order to use the Cascade ACP40 GSG microprobes. The de-embedding process is used to move the measurement reference plane from the calibration point (probe tips) to the DUT (Device Under Test) [12].

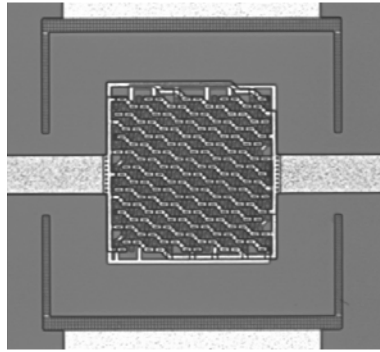

**Fig. 5** Integrated varcator microphotography

Firstly the varactor capacitance for zero bias voltage was obtained (the maximum capacitance because the varactor is reverse polarized). Table 1 shows the results for the varactor with the three models operating at 0.9 GHz. All of them show relative errors lower than 10%.

| Area (μm$^2$ ) | $C_{max}$ (pF) | Approximate | Rectangular | Spherical-cylindrical |
|---|---|---|---|---|
| 0,25·$10^4$ | 0,73 | 11,3% | 7,4% | 3,7% |
| 1·$10^4$ | 2,53 | 3,3% | 1,4% | 4,9% |
| 2,25·$10^4$ | 5,53 | 2,3% | 2,5% | 5,6% |

**Table 1** Relative error versus measured capacitance in cross varactor with double metallization al 0.9 GHz

Then, the effect of the reverse applied voltage, $V_A$, was included in the model as,

$$C = \frac{C_0}{\left(1 - \frac{V_A}{V_{bi}}\right)^s} \tag{16}$$

being $C_0$ the capacitance without polarization, and $V_{bi}$ and s fitting parameters technologically dependent.
In figure 6 and figure 7, the capacitance measured (squares) and modelled are shown for the approximate model (circles), the rectangular model (solid triangles), and spherical-cylindrical model (inverter triangles).

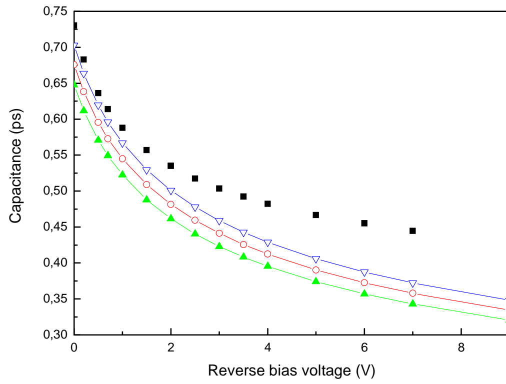


**Fig. 6** Capacitance vs. Reverse bias voltage for a varactor with $0.25 \cdot 10^{-4}$ µm$^2$ at 0.9 GHz

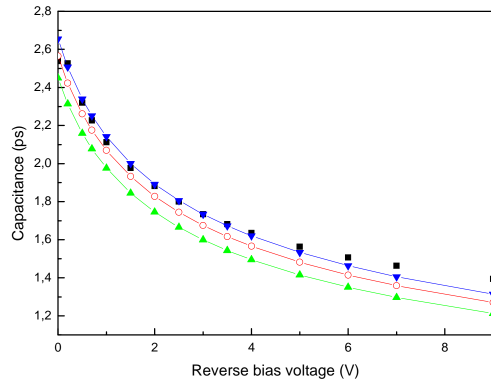


**Fig. 7** Capacitance vs. Reverse bias voltage for a varactor with $1 \cdot 10^{-4}$ µm$^2$ at 0.9 GHz

In figure 8, the capacitance modelled vs. capacitance measured is shown. The models predict the dependency of the capacitance with the reverse bias voltage with relative error under 10%. As higher is the voltage the error increases.

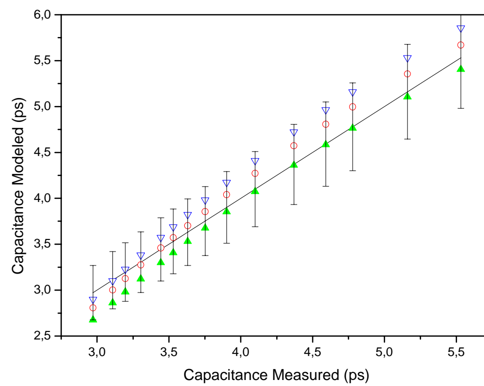


**Fig. 8** Capacitance for a varactor with 2.25·10-4 µm2 at 0.9 GHz: modelled vs. measurements

Other important parameters, such as the tuning range, can be predicted by the model with a relative error under 5%.

## 5. CONCLUSIONS

In this paper, three different alternatives to model the capacitance of a cross integrated varactor for RF applications have been presented. The results have been compared with capacitance measurements at different frequencies and voltages. The spherical-cylindrical model presents the best results, with the lowest relative error, 3.7%.


## ACKNOWLEDGMENT

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