Design and modelling of an on silicon spiral inductor library using improved EM simulations

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ABSTRACT

This paper deals with the design and modeling of integrated spiral inductors for RF applications by means of a general purpose Electromagnetic (EM) simulator. These tools allow optimizing flexibly the inductor layout structure. The inductor performance can be obtained by using a three-dimensional design tool or a two-dimensional one. Planar 2-D or so called 2.5-Ds simulators are faster and accept complex coil geometries. We have used one of these simulators, the Advanced Design System planar EM simulator, Momentum, from Agilent©.

The inductor quality factor (*Q*) is limited, among other phenomena, by the series resistance of the metal traces and the substrate losses. Therefore the simulator requires an accurate set up of the process and simulator parameters and a correct algorithm to model metal thickness to rely on simulation results. In this paper we analyze and compare these different approaches.

A high-quality factor inductor library on a 0.35 μm SiGe technology at 5 GHz is also designed in this work using the proper simulator set up. Nine of the inductors have been fabricated and measured to test the simulator reliability. Measurements taken over a frequency range from 500 MHz to 10GHz show a good agreement with 2.5-EM simulations.

Keywords: Electromagnetic simulations, inductance, on-chip spiral inductor, quality factor.

1. INTRODUCTION

Recently, silicon-based technologies have become increasingly attractive for use in RF circuit applications because they satisfy the new personal communication equipment requirements: low-cost, small size, low power consumption and low noise level systems, among others. However, silicon is a low resistive substrate, and high performance integrated passive components are difficult to achieve. The performance of voltage controlled oscillators (VCOs), low noise amplifiers (LNAs) and matching networks depends strongly on the inductor quality; therefore the high-*Q* inductor is a critical component in RF circuit design.

Standard integrated inductors in RF ICs suffer from their poor quality factors (*Q*) due to the substrate loss of the conductive substrate and the ohmnic loss of the thin metal strips. Several phenomena degrades the performance at high frequencies including skin effect, proximity effect, electric field penetration into substrate, and substrate eddy current losses [1][2]. Several studies have sought to improve the *Q* value, mainly by introducing advances in processing technology or suggesting post-processing techniques. Published examples include a patterned ground shield layer to protect from substrate losses [3], etching substrates [4], suspended spiral inductors [5] or toroidal inductors that confines flux [6]. It is worth noting that all these approaches increase the cost of the final product.

Not long ago the inductor design process was longer and more expensive than now. Some inaccurate simulations were run to prove the new structure behaviour, and without having reliable results, a big number of them were fabricated. Once the inductors were measured, its real performance was known, and the designer could select those required for the different applications. The most important drawback of this process is the waste of money because of the big amount of non-used fabricated coils. However, nowadays the design flow has changed considerably. Designers have powerful electromagnetic simulators that take into account most of parasitic effects. For that reason simulation results are reliable and only those coils the designer is interested in are fabricated. These tools involve saving money and time in the first step of the design process.

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As said before, designing optimal inductors for the required frequency is the key in the design of high-quality receiver front-ends. In this work a set of high Q inductors will be designed, simulated, fabricated and measured using a 0.35 μm SiGe technology for the IEEE 802.11a standard, which makes use of the 5 GHz band.

This paper is organized as follows. Section 2 is devoted to describe the guidelines followed in the inductors design. In Section 3 we describe the EM simulations, including a brief explanation about Momentum, and the improvements in meshing and modelling thick conductors. In Section 4 we show the results and finally some conclusions are given in section 5.

2. OPTIMUM INDUCTOR DESIGN

The receiver front-end in our application, the standard 802.11a, needs a number of high quality inductors with inductance values up to 10 nH at 5 GHz. Usually, the set of inductors offered by the foundries are not designed for a specific application. For that reason, sometimes the quality factor is not as high as the designer needs, or is not centered at the required frequency. Therefore designing new coils satisfying our requirements is an essential and a rather complex task, even though the structure looks simple.

The most common way to design an integrated inductor on silicon is to layout a simple metallic spiral directly on the substrate. At least two metal levels must be available, because an underpass is required to give access to one of the inductor's port. The challenge is to choose, for a given technology with a fixed metal layer thickness, the optimum combination of the number of turns (n), the metal width (w), the spacing between tracks (s) and the external radio (r) to arrive at a specific inductance and optimum Q for the desired frequency. This task is disturbed by the eddy current effects in the metal turns, current crowding and skin effect in the metal conductor. Furthermore, the inductor occupied area should be minimum for cost reasons.

Spiral inductors with different geometry were simulated. In order to improve its behavior all the designed inductors share some common characteristics. First of all, the spacing between the metal lines should be as small as possible. Increasing the spacing decreases the total inductance because of the decreasing of the mutual inductance. It also increases the series resistance and the total area. Therefore the spacing s was fixed in 2 μm, the minimum allowed by the foundry.

It is well known that circular shape is the optimum for spiral coils and could bring Q at least 10% higher than square ones [7]. However, octagonal shapes were used, since the technology allows 45º routing. The rest of geometrical parameters were varied as follows: r from 60 to 170 μm, n from 1.5 to 6.5 and w from 6 to 22 μm.

The used technology, Austrian Mikro Systems (AMS) SiGe 0.35 μm, provides four metal levels. Three of them are similar, with equal thickness and conductivity, and the top metal level is thicker and more conductive. Some simulations were run to decide the best metal combination in the inductors. Results showed that the quality factor is higher for inductors designed with the top metal level. So, inductors were designed with this top metal level, thick and conductive enough to present a low coil resistance, and far from substrate enough to work at high frequencies.

3. EM SIMULATIONS

Around 200 inductors were designed following the guidelines described in the previous section. Each spiral layout was previously generated by the Automatic Layout Generator Tool presented in [8], and then exported to the electromagnetic simulator in a gds file. As said in the introduction, EM simulations are essential in the inductors design flow, because these results determine the inductor set that will be fabricated.

3.1. Momentum simulator

EM simulators allow optimising flexibly the inductor layout structure. Inductors can be simulated using a three-dimensional design tool or a two-dimensional one. The former is very time-consuming, although it simulates fully all the inductor parasitic effects [1]. In order to collect a large number of inductors in the 5 GHz frequency range, simulations must be done as fast as possible. For that reason we have used one of the planar 2-D (or 2.5-D) simulators, which also admit complex coil geometry, the Advanced Design System planar EM simulator, Momentum, from Agilent© [9].

In the present study we show the results obtained using the previous version, ADS 2003A and the new one, ADS 2004A. This one employs a new approach to model thick metal and an updated simulation engine. We will test these improvements, and compare results with on wafer measurements.

3.2. Meshing and convergence

Since Momentum is a simulator based on the method of moments [10], a mesh is required in order to simulate the design effectively. A mesh is a pattern of triangles and rectangles applied to a design in order to break it down into small cells. Momentum computes the current within each cell and identifies any coupling effects in the circuit during simulation. From these calculations, S-parameters are then derived for the circuit, an inductor in this case.

As far as inductors are concerned, the two important mesh parameters are the *Edge Mesh* and the *Number of Cells per Wavelength*. The former must be enabled to take into account the proper currents distribution at high frequencies and the latter is used to determine the density of the mesh. Versions 2003A and 2004A suggest 20 cells/λ as a default number. In order to ensure accurate results this number could be increased, since the more cells, the better the current sinusoid is represented. Logically, there should be a limit, and results should not change when the number of cells rises above that value. Furthermore, there is no point in using a number higher than that limit because it would increase the simulation time with no improvement in the results.

However, the old version results converged only for the inductance value. For the case of the quality factor, the more cells per wavelength we set, the higher simulated *Q* became.

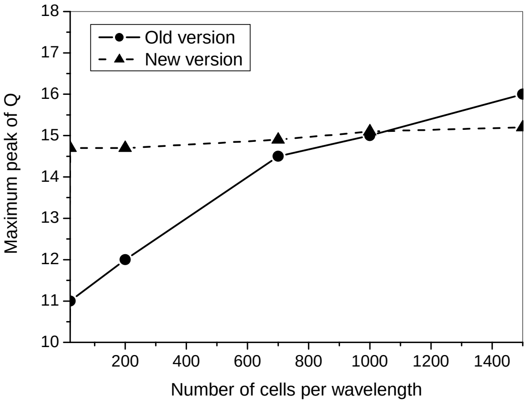


Figure 1: Comparison between both versions convergence for one of the designed inductors.

Figure 1 illustrates this behaviour for an inductor characterized by r=130 µm, n=1.5 and w=18 µm. We can see that the maximum value of *Q* with the old version grows significantly when the number of cells/λ is increased. However the default value, 20 cells/λ, is enough to assure accurate results using the new version.

Results of quality factor and inductance for the coil described above are drawn in Figure 2 for three different mesh densities: 20 cells/λ (solid line), 200 cells/λ (dashed line), and 1000 cells/λ (dotted line). Inductance value changes slightly using both ADS 2003A (higher graphs) and ADS 2004A (lower graphs), but *Q* varies considerably with the previous version. On the other hand it is interesting to note that simulated *Q* presents the maximum peak at different frequencies: 6.5 GHz using the current edition and around 8.2 GHz with the old one, which changed the result depending on the mesh.

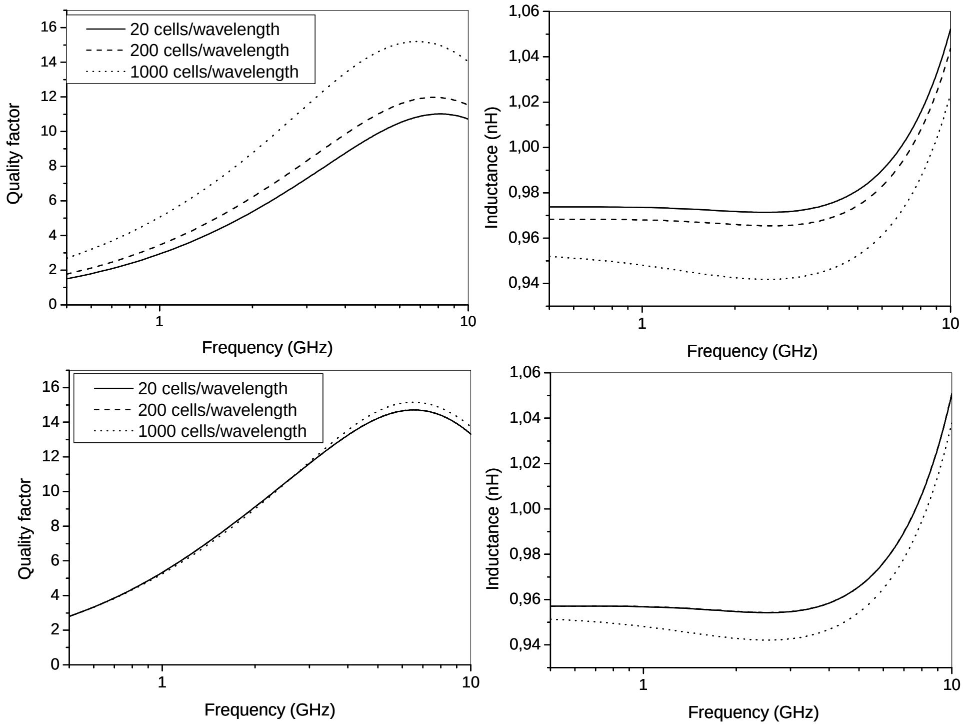


Figure 2: Performance of one of the coils designed for different mesh densities, using old (upper) and new (lower) versions.

3.3. Thick conductor modelling

As said before, the inductor quality factor will be limited by the series resistance of the metal traces and the substrate losses. Our simulator requires an accurate set-up of the process parameters and the substrate and metallization characteristics [11].

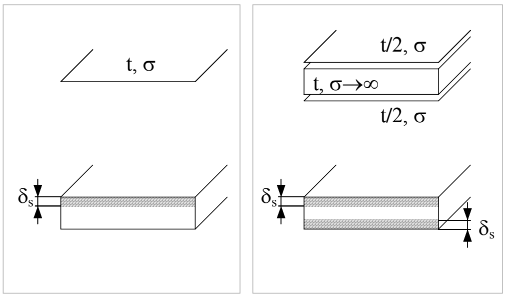
Thick conductor can be simulated with Momentum in two different ways: zero thickness or finite thickness approach [9]. With the former a 3D conductor is modelled like a sheet conductor using the Surface Impedance Model $Zs(t,\sigma,\omega)$, where t is the real metal thickness, σ is the metal conductivity and ω is the angular frequency. Zs takes thickness and frequency dependency (skin effect) of the conductor loss into account. With this approach low-frequency currents will run in entire cross section of the metallization, while high-frequency currents will run in simple skin depth (δ_S) surface layer and will be concentrated on one side of the finite thickness conductor (see Figure 3.a). δ_S is given by

$$\delta_S = \sqrt{\frac{2}{\omega \cdot \mu \cdot \sigma}} \qquad (1)$$

where μ is the metal permeability.

However, with the finite thickness approach we consider thick conductors as two metallization layers, each one characterized by $Zs(t/2,\sigma,\omega)$. Top and bottom layers will be separated by a t-thickness via. This way low-frequency currents will run in entire cross section of the metallization, and high-frequency currents will run in double skin depth surface layer, with equal distribution on both sides of the conductor (see Figure 3.b).

Typically, when the width/height aspect ratio is bigger than a factor of 5, the effect of accounting for the finite thickness of the conductors will need to be allowed for in Momentum simulations [9].



a) Zero thickness **b) Finite thickness**

Figure 3: Layer modelling and high frequency currents distribution.

Apart from the currents distribution, if we model conductors as a zero thickness layer, we do not define the substrate distances correctly. All metal conductors are simulated as infinite thin sheets of metal because of the method of moments [10]. Although we set up the thickness of each strip, this is only used for loss calculations, not during the actual EM simulations [9]. So, the finite thickness approach will take into account the correct distances from the substrate, and parasitic capacitance between coil and substrate and between metal tracks will be correctly simulated. As a consequence, quality factor will be centred at the right frequency.

Preceding Momentum edition only modelled zero thickness conductors. If the user wanted to define a finite thickness metal, he had to include manually the two different $t/2$-thickness layers separated by a t-thickness via in the substrate definition. Current version includes a 3D metal expansion feature that develops the process automatically (see figure 4). This expansion can be done *up* or *down*. In the former the extra dielectric layer inserted has the dielectric properties of the layer above the metal layer, and in the latter, this new layer has the material properties of the layer below it.

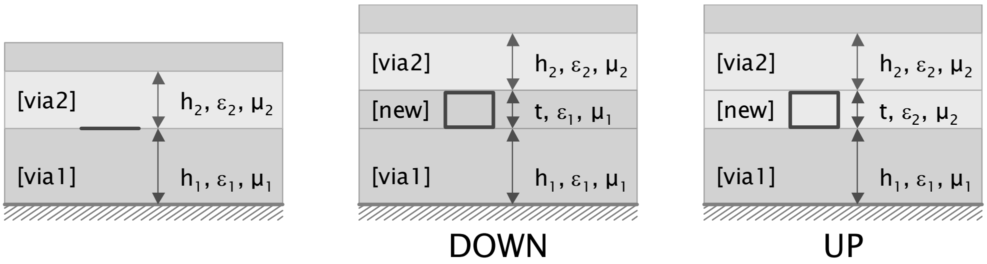


Figure 4: Automatic 3-D expansion for thick conductors.

4. RESULTS

Sixteen inductors of the designed and simulated library were fabricated in an AMS SiGe 0.35 μm standard process. Nine of them were standard spiral inductors, chosen taking into account different geometrical parameters and inductance range up to 10 nH. The layout of the rest of the coils was specially modified to test different structures, and these results are not included in this work.

The measurement system used for the characterization of the inductors consists of the HP8720ES Vector Network Analyzer and the Summit 9001 Probe Station. To calibrate the measurement system, the short-open-load-through (SOLT) method was used. Finally, the four-steps de-embedding method [12] was followed to remove the parasitic effects introduced by the measurement structures.

Figure 5 shows the final layout of the fabricated chip, which occupies a total area of 12.34 mm^2. Apart from the inductors and the measurement structures (upper area of the chip), it is composed of other devices such as VCOs, LNAs and mixers. For each coil, the inductance and *Q* for the frequency range between 0.5-10 GHz was measured. Table I shows the geometrical parameters and the measured results at 5 GHz.

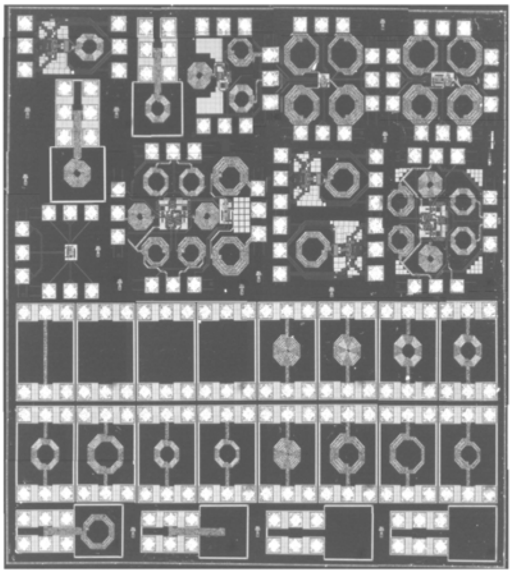


Figure 5: Fabricated chip final layout.

TABLE I
Geometrical Parameters For High *Q* Inductors

	n	*r* (μm)	*w* (μm)	L (nH)	*Q*
L1	1.5	100	20	0.6	9
L2	1.5	130	18	1	9.6
L3	2.5	130	18	2	8.2
L4	5.5	100	13	2.6	5.5
L5	3.5	90	6	3.3	8.2
L6	4.5	90	6	4.7	6.9
L7	4.5	100	6	5.5	6
L8	5.5	100	6	8.3	4.2
L9	6.5	100	6	10.5	3.2

Figure 6 illustrates the comparison between measurements (scatter) and simulated results using the different approaches explained before to model thick conductors: zero thickness or sheet (solid line), finite thickness manually set (dashed line), finite thickness automatic *up* expansion (dotted line), and finite thickness automatic *down* expansion (dashed-dotted line). Results show that the inductance value varies slightly using the different approaches. The quality factor is similar for the three finite thickness ways of modelling, because the substrate is hardly changed when the expansion is automatically set and vias between metals share the same properties. However the *Q* value differs substantially from the zero thickness approach.

Two of the four inductors showed in the figure present a width/height aspect ratio bigger than 5 (see L1 and L3 in Table I). According to the Momentum user's manual, finite thickness approach in these cases should agree better with measurements than the zero thickness one. Nevertheless, the quality factor error is considerable. On the other hand, sheet modelling simulations of inductors with aspect ratio less than 5 (see L4 and L7 in Table I) show better agreement with *Q* measurements, although the error grows at high frequencies.

Simulated inductance results show good agreement with measurements using both approaches. However the error is lower with the finite thickness conductor modelling without depending on the aspect ratio, as it is shown in Figure 6.

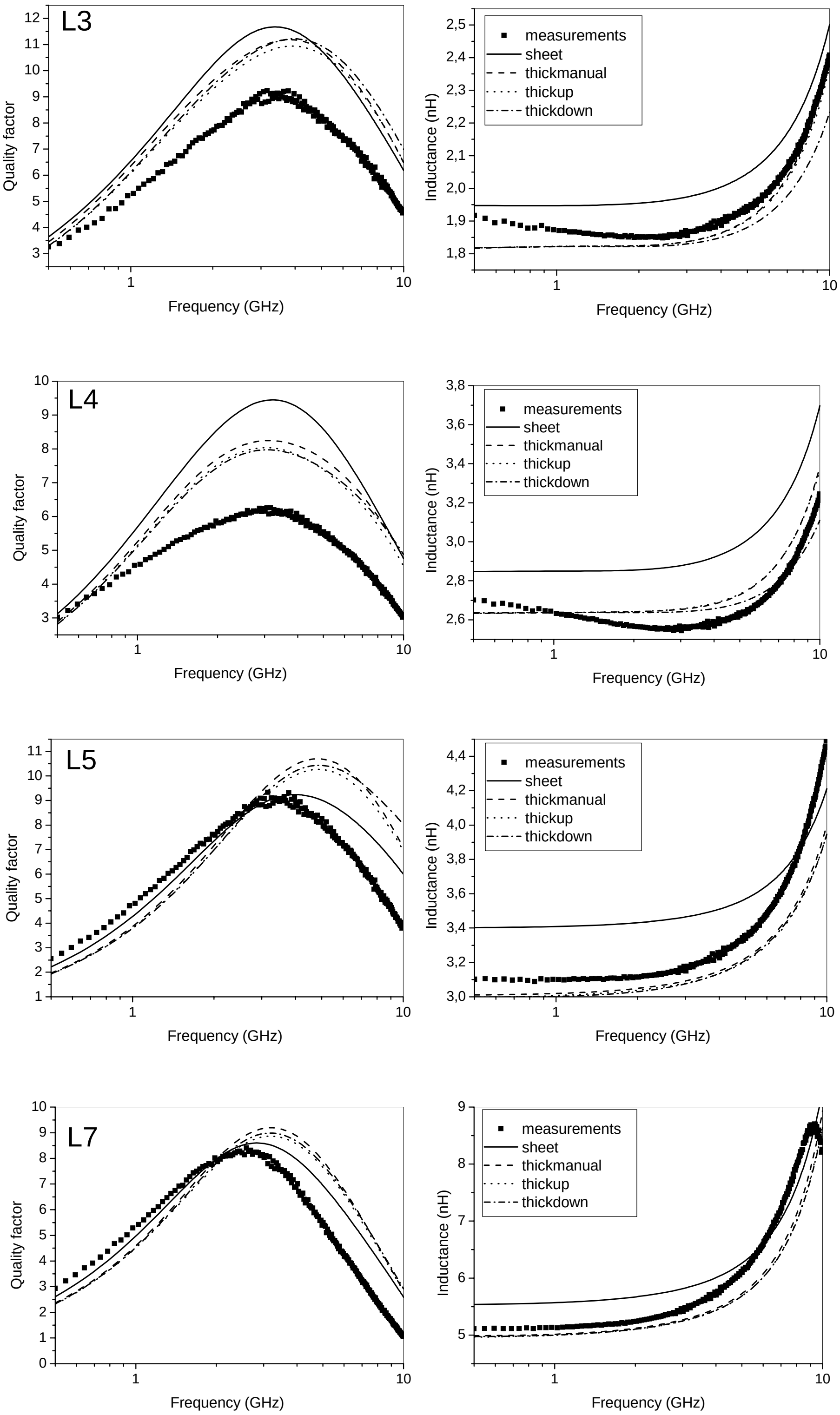


Figure 6: Simulated (lines) and measured (scatter) *L* and *Q* for some of the fabricated inductors (see Table I).

5. CONCLUSSIONS

In this work we have reported an analysis of on silicon spiral inductors for RF applications using Momentum. We have compared EM simulations against measured results taken from octagonal inductors fabricated in a low-cost four metal SiGe 0.35μm process. Using the top metal level and choosing the correct combination of the geometrical parameters, inductors from 0.6 to 10 nH range to work in the 5GHz band with high quality factor have been designed.

Nine standard inductors of the designed library have been fabricated and measured. As far as inductance is concerned, simulated and measured values show a very good agreement in a wide frequency range (0.5 to 10 GHz). In general inductance results show that finite thickness approach simulations fit better with measurements than those obtained by sheet approach, although results hardly vary.

However, Momentum overestimates the quality factor. Results of inductors with narrow metal traces (aspect ratio lower than 5) show good agreement with measurements using the zero thickness approach to model conductors, though the higher the frequency is, the more the error grows. On the other hand, inductors with aspect ratio higher than 5 show worse agreement. Modelling conductors with finite thickness is recommended with these coils, but the error continues to be high. The fact that the skin effect is not properly modelled in these wide traces inductors could possibly explain the difference from measured data. It seems that further research is needed in order to redefine somehow the substrate and achieve a better agreement.

These results suggest that Momentum is a very useful tool to the RF designer, who can rely on the simulations, provided that the quality factor is overestimated in some cases. As a consequence, we have now a wide high-Q inductor library (around 200) designed on a low-cost technology. RF designer can use this library to design VCOs, LNAs or mixers, and achieve this way a high-quality receiver front-end for the 802.11a standard.

REFERENCES

1. J. Craninckx, M. S. J. Steyaert, “A 1.8 GHz low-phase-noise CMOS VCO using optimized hollow spiral inductors,” *IEEE Journal of Solid-State Circuits*, vol. 32, no. 5, pp. 736-744, May. 1997.
2. J. N. Burghartz and B. Rejaei, “On the design of RF spiral inductors on silicon,” *IEEE Trans. On Electron Devices*, vol. 50, no. 3, March 2003.
3. C. P. Yue and S. S. Wong, “On-chip spiral inductors with patterned ground shields for Si-based RF ICs,” *IEEE J. Solid-State Circuits*, vol. 33, pp 743-752, May 1998.
4. J. M. Villegas, J. Samitier, C. Cane, P. Losantos, and L. Bausells, “Improvement of the quality factor of RF integrated inductors by layout optimization,” *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 76-83, Jan. 2000.
5. Xi-Ning Wang, Xiao-Lin Zhao, Yong Zhou, Xu-Han Dai, and Bing-Chu Cai, “Fabrication and performance of a novel suspended RF spiral inductor,” *IEEE Trans. On Electron Devices*, 2004.
6. W. Y. Liu, J. Suryanarayanan, J. Nath, S. Mohammadi, L. P. B. Katehi, and M. B. Steer, “Toroidal inductors for radio-frequency integrated circuits,” *IEEE Trans. Microwave Theory Tech.,* vol. 52, no. 2, February 2004.
7. F. Ling, J. Song, T. Kamgaing, Y. Yang, W. Blood,, M. Petras, and T. Myers, “Systematic analysis of inductors on silicon using EM simulations,” *Electronic Components and Technology Conference*, 2002.
8. J. del Pino, J. R. Sendra, A. Hernández, S.L. Khemchandani, J. Aguilera, B. González, J. García, and A. Nunez “Models and Tools for CMOS Integrated Inductors”, *Analog Integrated Circuits and Signal Processing*, vol.33, pp. 171–178, Kluwer Academic Publishers, 2002.
9. http://eesof.tm.agilent.com.
10. R.F. Harrington, *Field Computation by Moment Methods*, New York, IEEE Press, 1993.
11. Jan Van Hese, “Design and simulation of spiral inductors on silicon substrates,” *Agilent Technologies.*
12. T.E. Kolding “On wafer calibration techniques for giga-Hertz CMOS measurements,” *Proceedings IEEE International Conf. on Microelectronics Test Structures* (ICMTS), March 1999.