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Improved tolerance to operation temperature in δ-doped inverted HFETs

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Abstract
Inverted delta doping in HFETs offers the possibility of enhanced performance. It makes possible the development of very high frequency/speed and power transistor circuits. The operating temperature range and δ-doping concentration are critical, because they strongly affect the device ability to confine the current flow into the fast quantum well channel. In this study, the effect of temperature and δ-doping concentration on the performance of inverted HFETs is analysed by means of numerical simulations. The results are analytically and qualitatively discussed, showing how to fine-tune the δ-doping concentration from medium to high temperatures. Comparisons with a similar conventional HFET demonstrate a better tolerance to temperature variations in the inverted ones.

1. Introduction

Most of work on heterostructure field effect transistors (HFETs) has concentrated on metal–AlGaAs–InGaAs–GaAs structures (conventional HFETs). However, mobility enhancement in the quantum well is also found in metal–GaAs–InGaAs–AlGaAs layers (i.e. inverted HFETs) [1, 2].

Inverted HFETs (I-HFETs) exhibit superior electrical properties with significant higher sheet concentrations than those corresponding to conventional HFETs (six times higher, 5.35×10^{12} cm^{-2}, in [3]). This may be the result of a better confinement provided by band-bending near the surface due to Fermi level pinning of the thin GaAs gate barrier.

The utilization of an undoped GaAs gate barrier may reduce the distance between the gate and the two-dimensional electron gas (2DEG) at the heterointerface. Furthermore, small gate leakage current is also achieved, indicating potential for use in high speed applications [4, 5].

With the δ-doping technique I-HFETs have been demonstrated to exhibit a reduction in short channel effects, increased gate to drain breakdown voltage, up to a figure as high as 40 V in [6–8], and enhanced transconductance with kink-free characteristics at room temperature [9]. They also exhibit a better noise performance than conventional HFETs [10], and high unity current gain cut-off frequency and maximum oscillation frequency [8, 9]. However, few studies about binary on top of ternary semiconductors have been reported, mainly due to difficulties in the crystal growth of the inverted type structure [11].

As GaAs surfaces are more stable than the AlGaAs surface, GaAs barriers in I-HFETs may lead to a higher yield and reproducibility in device fabrication, which is especially relevant for the development of circuits with HFETs. Another advantage of the I-HFETs is related to the fact that its transconductance is nearly independent of doping [2]. Furthermore, it is easier to fabricate ohmic contacts on GaAs than on AlGaAs.

These aspects have motivated the study of δ-doping influence in I-HFETs when temperature, T, and its concentration, N_δ, vary. In section 2, the charge control model of δ-doped I-HFETs is briefly explained. Section 3 presents the adopted criteria to characterize the δ-doping. The basic I-HFET under study is reported in section 4, together with aspects related with the numerical simulator used, Taurus-Medici [12], and modelling. In section 5 the simulation results of the δ-doping concentration and temperature influence are shown for several inverted structures, and compared with those previously obtained for a similar conventional HFET. Finally, section 6 summarizes the main conclusions.

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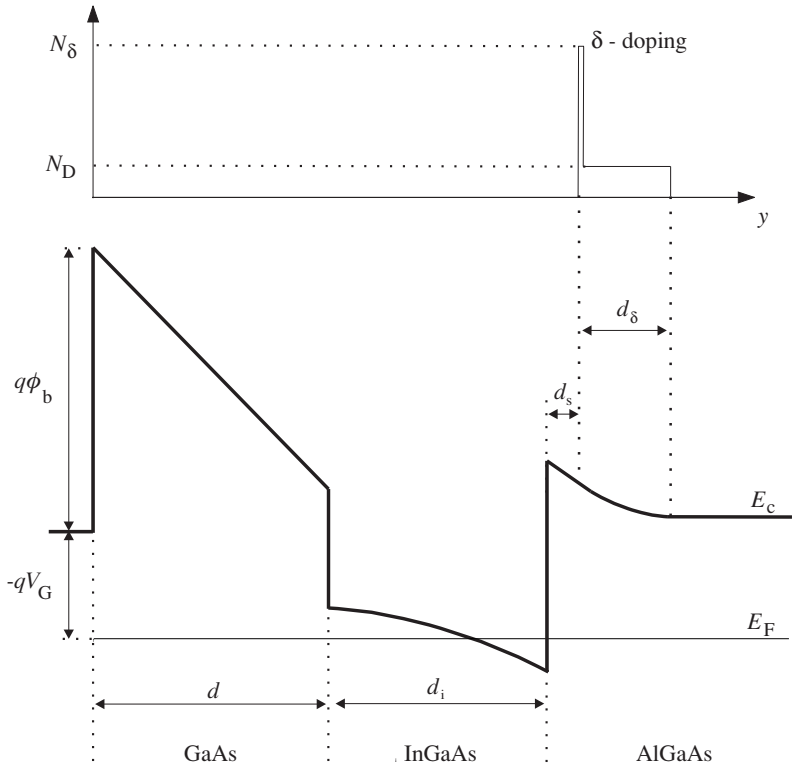

Figure 1. Doping and energy conduction level under the gate in common I-HFETs.

2. Charge control model of δ-doped I-HFETs

Optimum performance in HFETs is obtained when the only available electron concentration is in the device channel. For that purpose the layers surrounding the channel must be depleted. Thus, the current can flow through the channel, avoiding any other parallel contribution (parasitic MESFET) with lower electron mobility.

A channel of double heterojunction (trapezoidal quantum well) is frequently found in HFETs. This makes the channel wider than in a simple heterojunction. Then, more electrons are confined in the quantum well, avoiding scattering into the substrate.

Thus, double pseudomorphic I-HFETs are commonly used. An upper Schottky gate is formed on undoped GaAs, which is on the InGaAs channel where the 2DEG is formed. A δ-doped layer is placed between the AlGaAs spacer and supply layers, below the InGaAs channel, and above the GaAs substrate. The corresponding doping profile and energy conduction level under the gate is shown in figure 1, where y represents the depth from the gate contact. The AlGaAs supply layer, which provides some electrons to the 2DEG, must be thin enough to be depleted avoiding parasitic parallel conduction. The main contribution to the high electron concentration of the 2DEG is the δ-doped layer, which must be depleted too, and the spacer layer is introduced to reduce the ionized impurity scattering on the 2DEG.

The influence of surface traps in HFETs can be minimized by reducing gate-recess extension and inter-electrode spacing. Furthermore, sulfur passivation has been developed to diminish the effects of problematic surface chemistry on the transistor behaviour, improving thermal stability. The $(NH_4)_2S_x$ treatment can effectively passivate the semiconductor surface [9, 13], and when silicon nitride (Si_xN_y) deposition on GaAs is used, the density of electronic states is reduced even more (a minimum of $3 \times 10^{11}\,\mathrm{cm}^{-2}\,\mathrm{eV}^{-1}$ was achieved in [14]). Therefore, for simplicity, charge on the GaAs surface is neglected in our study.

At moderate temperatures all donor atoms are ionized. Hence, when only impurity donors in volume exist (without δ-doping), the electron concentration in the channel of I-HFETs is approximated by the following expression [2]:

$$n \approx N_D d_\delta + \frac{\varepsilon(V_G - \phi_b)}{qd} \tag{1}$$

where ε is the dielectric permittivity of the GaAs barrier d deep, q is the elementary charge, V_G the gate voltage, ϕ_b is the Schottky barrier at the gate contact and N_D is the donor concentration in the AlGaAs supply layer, d_δ deep; d is normally fitted up to $d + d_i$, d_i being the width of the trapezoidal quantum well, to model the non-planar electron concentration of the 2DEG (i.e. the depth of the channel) [2].

If an AlGaAs δ-doped layer with N_δ impurity concentration is included on the AlGaAs supply layer, equation (1) can be extended as follows:

$$n \approx N_\delta + N_D d_\delta + \frac{\varepsilon(V_G - \phi_b)}{qd}. \tag{2}$$

Rearranging equation (2) the electron concentration in the channel with δ-doping can be written as

$$n = \frac{\varepsilon}{qd}(V_G - V_T) \tag{3}$$

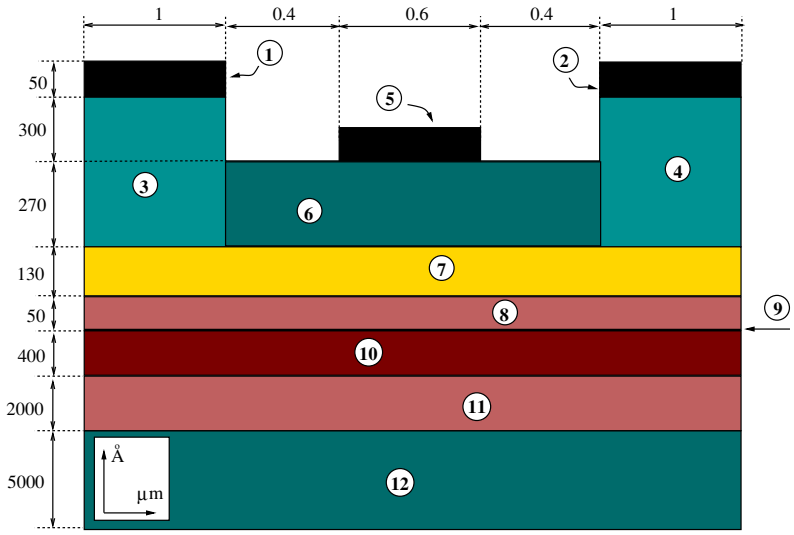

Figure 2. Basic I-HFET structure: (1) and (2) represent the source and drain contacts, (3) and (4) are 10^{19} cm^{-3} n-type doped GaAs, (5) is the Schottky gate, (6) undoped GaAs, (7) $In_{0.2}Ga_{0.8}As$ quantum well, (8) undoped $Al_{0.28}Ga_{0.72}As$, (9) location of the δ-doped layer, (10) represents 10^{18} cm^{-3} n-type doped $Al_{0.28}Ga_{0.72}As$, (11) is the undoped $Al_{0.28}Ga_{0.72}As$ and (12) is the GaAs substrate.
(This figure is in colour only in the electronic version)

with V_T being the resulting I-HFET threshold voltage, which is given by

$$V_T \approx \phi_b - \frac{qdN_D d_\delta}{2\varepsilon} - \frac{qdN_\delta}{\varepsilon}. \quad (4)$$

3. Optimization criteria of δ-doped HFETs

The charge control model of I-HFETs, equation (3), is valid for conventional HFETs [2]. Therefore, similar expressions for the current–voltage characteristics are derived. On the other hand, inverted and conventional HFETs differ in the expression for the threshold voltage, but in both cases it preserves a linear dependence on N_δ. Thus, the optimization criteria established for the δ-doping concentration in conventional HFETs [15] can be applied in inverted ones. Then, setting specified external dc operating conditions of the I-HFET in an optimized circuital configuration, the impact of the δ-doped layer can be studied from the I–N_δ characteristic curve, with I being the source to drain current.

The ideal, degraded and low efficiency behaviours are established with suitable δ-doping concentrations [15]:$N_{\delta-\mathrm{id}}$ is the optimum concentration for which the current is ideal, I_{id} (maximum current provided the relation I–N_δ is linear and the transconductance is maximum, $g_{m_{max}}$). $N_{\delta-\mathrm{db}}$ represents the δ-doping concentration for which the transconductance is $0.8 \cdot g_{m_{max}}$. It is a doping concentration limit for the degraded behaviour, which is defined as the operating region where the transconductance is lower than $0.8 \cdot g_{m_{max}}$. Finally, $N_{\delta-\mathrm{le}}$ is the δ-doping concentration for which the current is $0.9 \cdot I_{\mathrm{id}}$. This current is a limit for the region of low efficiency behaviour, which is defined as the transistor operation region where the current is smaller than 90% of the ideal value. In this case no current flows through the δ-doped layer, but the channel current is not efficiently exploited.

The three δ-doping concentrations, $N_{\delta-\mathrm{id}}$, $N_{\delta-\mathrm{db}}$ and $N_{\delta-\mathrm{le}}$, can depend on temperature as section 5 will show. They allow us to find δ-doping concentrations for which the I-HFET performance is improved, that is, the device will operate between the degraded and low efficiency regions.

4. Simulation

4.1. The basic I-HFET under study

The basic inverted transistor under research is a double pseudomorphic HFET 50 μm wide. Figure 2 shows its structure. An undoped $In_{0.2}Ga_{0.8}As$ trapezoidal quantum well (7) is formed between the undoped $Al_{0.28}Ga_{0.72}As$ spacer layer (8) and the upper intrinsic GaAs barrier (6). The δ-doped layer is indicated with (9), and the supply layer (10) is 10^{18} cm^{-3} n-type doped $Al_{0.28}Ga_{0.72}As$. Undoped $Al_{0.28}Ga_{0.72}As$ (11) is placed between the supply layer and the GaAs substrate (12).

The caps (3, 4) are made of GaAs with a donor concentration of 10^{19} cm^{-3}, which is extended in depth up to the InGaAs channel in order to reduce the extrinsic parasitic resistances. Finally, regions (1), (2) and (5) represent the source, drain and gate contacts, respectively.

4.2. Simulation tool and modelling

The analysis of the I-HFET has been carried out through numerical simulations performed with the electronic device simulator Taurus-Medici [12]. The Poisson and continuity equations are numerically solved. No energy balance equation has been considered.

In the case of HFETs the simulation is extremely sensitive to the model used at the heterointerfaces [16]. In the proposed transistor the current crosses over the heterointerface between the $In_{0.2}Ga_{0.8}As$ channel and the GaAs barrier twice, once under the drain and once under the source regions. In order to reproduce experimental results, a thermionic field

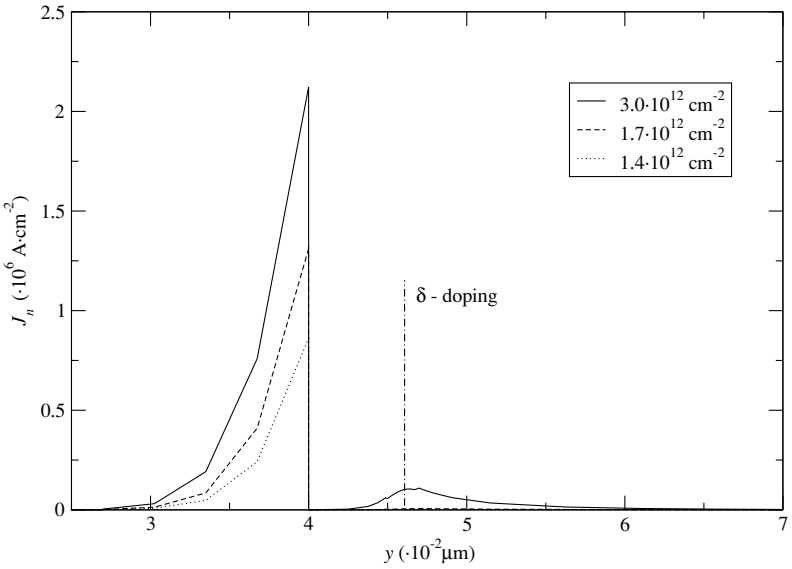

Figure 3. Basic I-HFET density current versus depth from the gate, for different δ-doping concentrations; $T = 300$ K, $V_G = 0$ V, $V_D = 0.1$ V.

emission model with tunnel effect [17] has been included at this heterointerface. Our study is limited to temperatures between 300 K and 500 K. For lower temperatures the thermionic field emission model does not predict the temperature dependence of the current correctly. At higher temperatures the gate leakage current increases degrading the transistor behaviour.

Taurus-Medici includes proper models for GaAs, $Al_{1-x}Ga_xAs$ and $In_{1-x}Ga_xAs$, taking into account the material composition dependence, x [12]. A critical parameter in the simulation is the electron mobility in the quantum well. For low electric fields an electron mobility model depending on temperature is precise enough (there are no impurity atoms in the channel) [18], and for high electric fields the Caughey–Thomas model is used [19].

No trap effects are considered due to the relatively high temperatures involved in simulations. Finally, a Schottky barrier height of 0.63 eV is assumed for the gate contact [18].

5. Simulation results

In order to bias the basic I-HFET in the linear region, the drain and gate voltages were set to 0.1 V and 0 V, respectively.

The influence of the δ-doping concentration on the transistor performance is first analysed at room temperature. Two layers contribute to the electron concentration in the quantum well: the AlGaAs supply layer and the δ-doped layer. Figure 3 shows the resulting electron density current profile, under the middle of the gate for three different δ-doping concentrations. For N_δ equal to 3×10^{12} cm^{-2} (solid line) the transistor operates in the degraded behaviour region. The practical region corresponds to 1.7×10^{12} cm^{-2} (dashed line), and the low efficiency region is obtained with 1.4×10^{12} cm^{-2} (dotted line). Note that in all cases the peak of the electron density current appears in the InGaAs/AlGaAs heterojunction, by the substrate side, and increases significantly with N_δ, even in the degraded behaviour region.

In I-HFETs the electron concentration in the channel does not tend to saturate when the behaviour is degraded. This response is opposite to that observed in conventional HFETs. Therefore, in the degraded behaviour region of I-HFETs a non-negligible parasitic MESFET appears in the δ-doped layer, before the electron current in the quantum well is maximized.

In the practical behaviour region, when a parasitic MESFET appears in the δ-doped layer (the transconductance decreases), its associated current is negligible as compared with the channel current; therefore, it can be ignored. And in the low efficiency region N_δ could be increased with current only flowing through the channel (the transconductance increases) but not high enough.

Figure 4 shows the drain to source current as a function of the δ-doping concentration at 300 K (solid line), 400 K (dashed line) and 500 K (dotted line). The results of the optimization criteria are represented by circles and squares. The black circle delimits the upper value for the current in the low efficiency region. The black square is the lower current with degraded behaviour. And the white circle represents the ideal operating condition. For δ-doping concentrations of interest, when temperature increases the current and the variation of the current with N_δ decrease.

The derived regions are obtained and represented in figure 5. The shaded regions, degraded and low efficiency regions, must be avoided in order to obtain a proper device performance.

In the conventional HFET of [15] $N_{\delta-\mathrm{db}}$, $N_{\delta-\mathrm{id}}$ and $N_{\delta-\mathrm{le}}$ decrease significantly as temperature rises, showing a parabolic dependence. At 500 K their values have been reduced respectively to 25%, 42% and 43% of their maximum values at room temperature. On the contrary, the maximum variations in the basic I-HFET with respect to their values at room temperature are only 1%, 1% and 0.5%, respectively. That is, the δ-doping concentrations for which the ideal and the limits of the behaviour regions are defined, are nearly independent of temperature; $N_{\delta-\mathrm{db}}$, $N_{\delta-\mathrm{id}}$ and $N_{\delta-\mathrm{le}}$ can be approximated to 1.93×10^{12}, 1.71×10^{12} and 1.62×10^{12} cm^{-2}, respectively.

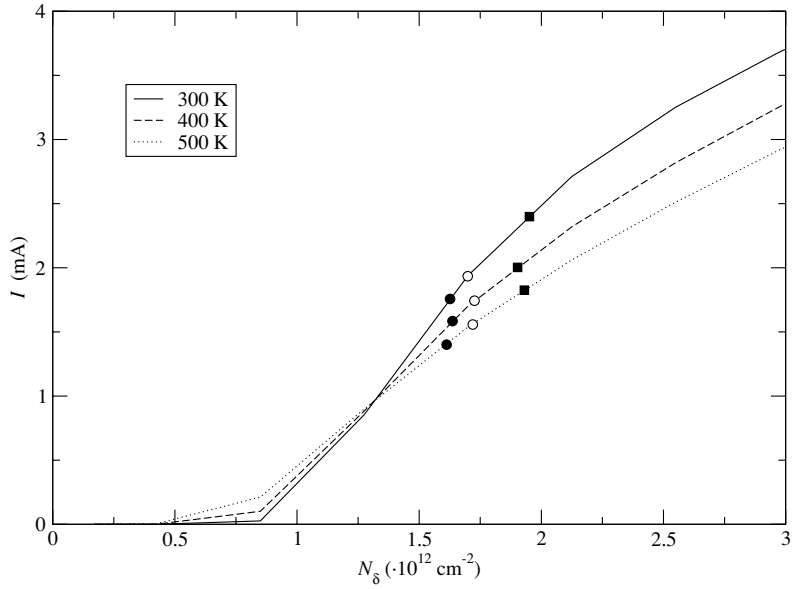

Figure 4. Basic I-HFET drain to source current versus δ-doping concentration, for different temperatures, and optimization criteria; $V_G = 0$ V, $V_D = 0.1$ V.

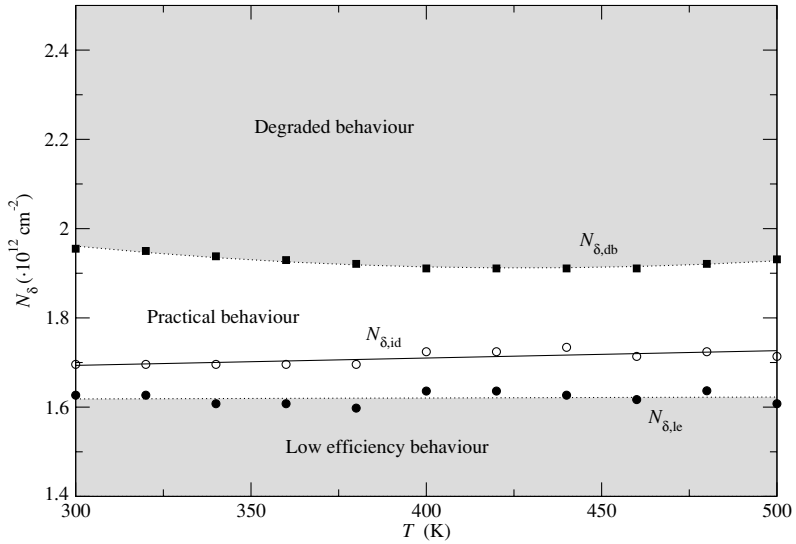

Figure 5. Basic I-HFET δ-doping concentration versus temperature and behaviour regions; $V_G = 0$ V, $V_D = 0.1$ V.

This result is attributed to the fact that the 2DEG is located at the InGaAs heterojuntion by the substrate side, increasing the electron concentration in the quantum well with temperature (in conventional HFETs it decreases). Then, the current through the quantum well is reduced when temperature increases due to mobility degradation, but not so intensively as for the conventional HFET, and similar to that through the δ-doped layer. Thus, the current through the channel and the δ-doped layer decrease with temperature in the I-HFET, but the behaviour is not degraded.

For a given temperature, additional δ-doping increases the current in the δ-doped layer more than in the quantum well, degrading the transconductance and thus the overall behaviour.

Similar results are obtained for other inverted structures and/or bias conditions. Our charge control model, equations (3) and (4), predicts that variations on the bias condition, V_G, and the geometric and physical parameters d, d_δ, N_D and ϕ_b, will move the I–N_δ characteristic curves along the N_δ axe, resulting in the same type of variation in $N_{\delta-db}$, $N_{\delta-id}$ and $N_{\delta-le}$ with temperature. Therefore, the shape of the behaviour regions remains the same.

However, the quantum well geometry and spacer layer depth are not considered in the model. For that purpose several simulations have been performed varying the spacer layer depth to $d_s = 20$ Å, the channel layer depth to $d_i = 80$ Å, and $In_{1-x}Ga_xAs$ material composition to $x = 0.3$ (see figure 1) in the basic I-HFET. Table 1 shows, for temperatures between 300 and 500 K, the corresponding average values and maximum variations of $N_{\delta-db}$, $N_{\delta-id}$ and $N_{\delta-le}$ relative to their values at room temperature. Insignificant variations of the δ-doping concentrations are found, except for $N_{\delta-db}$ when $d_i = 80$ Å. But even in this case, the maximum relative

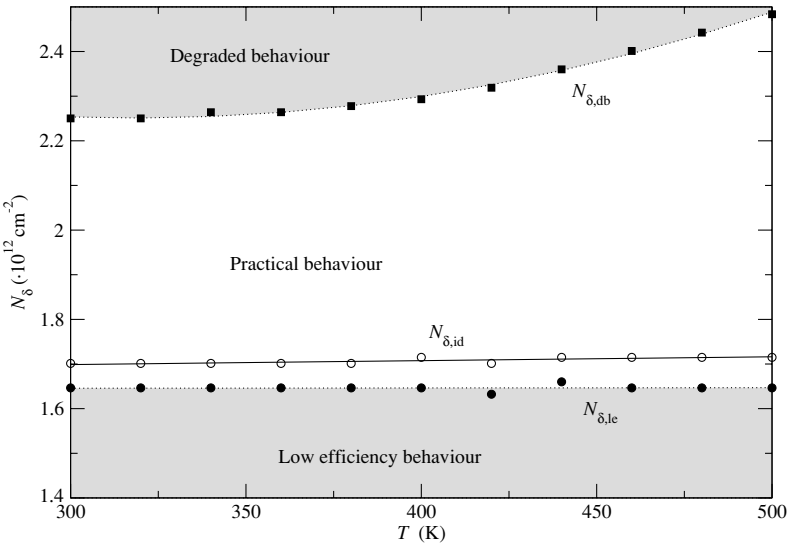

Figure 6. δ-doping concentration versus temperature and behaviour regions for the I-HFET with 80 Å channel layer; $V_G = 0$, V, $V_D = 0.1$ V.

Table 1. From 300 to 500 K, average values and maximum variations of $N_{\delta-db}$, $N_{\delta-id}$ and $N_{\delta-le}$, with respect to their values at 300 K, for I-HFETs with different d_s, d_i and material composition.

	$\langle N_{\delta-db}\rangle$ (cm^{-2})	$\langle N_{\delta-id}\rangle$ (cm^{-2})	$\langle N_{\delta-le}\rangle$ (cm^{-2})	$\Delta N_{\delta-db}$ (%)	$\Delta N_{\delta-id}$ (%)	$\Delta N_{\delta-le}$ (%)
$d_s = 20$ Å	2.44×10^{12}	1.70×10^{12}	1.63×10^{12}	2.2	0.8	2.5
$d_i = 80$ Å	2.33×10^{12}	1.71×10^{12}	1.64×10^{12}	10.4	0.8	1.6
$In_{0.3}Ga_{0.7}As$	1.86×10^{12}	1.28×10^{12}	1.22×10^{12}	0.7	1.1	1.2

variation obtained ($\Delta N_{\delta-db} = 10.4\,\%$) is less than half of that for the conventional HFET and positive with temperature (the behaviour is not degraded when temperature increases, as figure 6 shows).

When $d_s = 20$ Å and $d_i = 80$ Å both layers decrease. $N_{\delta-id}$ and $N_{\delta-le}$ are the same as in the basic I-HFET, but a higher $N_{\delta-db}$ is necessary to degrade the behaviour. On the other hand, when the indium material composition increases, $x = 0.3$, $N_{\delta-db}$, $N_{\delta-id}$ and $N_{\delta-le}$ diminish. As a higher conduction band discontinuity is formed at both sides of the trapezoidal quantum well, more electrons are confined in it, and the practical behaviour region is extended. Nevertheless, the difference between $N_{\delta-id}$ and $N_{\delta-le}$ remains the same than for the rest of I-HFETs ($\approx 7 \times 10^{10}$ cm^{-2}).

In summary, when temperature changes, the I-HFETs exhibit a more stable response with the δ-doping concentration than the conventional HFET.

6. Conclusions

Once the device voltage conditions are established in I-HFETs for a circuit configuration, the methodology to characterize the transistor performance at different temperatures and δ-doping concentrations is similar to that for conventional HFETs. For every temperature, if the δ-doping concentration is higher than the optimum value, a parasitic MESFET appears in the δ-doped layer, which can be ignored in the practical behaviour region. And if it is lower, the current flows through the quantum well, being insufficient in the low efficiency behaviour region. The δ-doping concentrations which limit the behaviour regions are defined.

Simulation results show a better behaviour of different I-HFETs, for any bias conditions, compared to conventional ones with temperatures between 300 K and 500 K. In I-HFETs the optimum δ-doping concentration does not show significative temperature dependence. Therefore, they are preferable in a circuit to similar conventional HFETs when the operating temperature varies in a wide range.

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