In-depth analysis and modelling of self-heating effects in nanometric DGMOSFETs

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Abstract: Self-heating effects (SHEs) in nanometric symmetrical double-gate MOSFETs (DGMOSFETs) have been analysed. An equivalent thermal circuit for the transistors has been developed to characterise thermal effects, where the temperature and thickness dependency of the thermal conductivity of the silicon and oxide layers within the devices has been included. The equivalent thermal circuit is consistent with simulations using a commercial technology computer-aided design (TCAD) tool (Sentaurus by Synopsys).
In addition, a model for DGMOSFETs has been developed where SHEs have been considered in detail, taking into account the temperature dependence of the low-field mobility, saturation velocity, and inversion charge. The model correctly reproduces Sentaurus simulation data for the typical bias range used in integrated circuits. Lattice temperatures predicted by simulation are coherently reproduced by the model for varying silicon layer geometry.

Keywords: DGMOSFET; self-heating effects; compact modelling; thermal resistance.

1. Introduction

Double-gate MOSFETs (DGMOSFETs), among other multigate devices, are serious alternatives to fulfil the future scaling needs of the integrated circuit industry [1]. The use of two gates reduces short channel effects in comparison to conventional bulk devices. In addition, random-dopant-induced variability and junction parasitic capacitances are diminished. These devices are also characterised by high mobilities and I_{on} / I_{off} ratios. These latter features are linked to the use of undoped substrates, allowed

by greatly reduced short channel effects, and volume inversion operation connected with a strong geometrical quantum confinement.

Self-heating effects (SHEs) may be extremely important in the operation of future transistors, due to the complexity and high level of integration of current integrated circuits. The scaling race in the electronics industry is forcing an overall reduction of the dimensions of the devices, which implies a reduction of their capacity as body heat sinks. This trend also affects the source and drain contacts, whose role played both from the electric and thermal point of view, resembles a bottle neck, particularly in silicon on insulator (SOI) technology. Furthermore, SHEs are expected to increase because of the lower thermal conductivities, with respect to bulk silicon, of the new materials used in prototypes for future nodes described by the International Technology Roadmap for Semiconductors (ITRS) [2].

Among the new structures under scrutiny are different kinds of SOI devices as well as multi-gate bulk devices. In both types of structure, due to their specific geometric configuration, heat removal is much more difficult than in conventional bulk devices, where heat dissipation typically occurs through the silicon bulk towards the backside of the die. For SOI transistors most of the thermal energy flux comes out of the device through interconnect metals, whereas the back side of the die has a negligible contribution [3, 4]. The facts outlined above make DGMOSFET thermal characterisation an essential issue both for characterisation and modelling.

Accurate modelling of multi-gate devices will surely be a key factor in making this technology the choice of design houses, among the offerings from different foundries. That is why we are witnessing a remarkable effort from the microelectronics community to fabricate, characterise, and model these devices [5]. In the case of DGMOSFETs, a high number of papers devoted to modelling activities can be found in the recent literature [6–10]. Furthermore, taking into account their $I_{DS} - V_{DS}$ characteristics in the saturation region, where the output conductance is nearly constant, SHEs are particularly important since they can lead to negative output resistances, especially in DC and AC low-frequency regimes [11, 12]. At high frequencies, the thermal response of these devices could render dynamic SHEs negligible [11].

In this context we present our study. The DGMOSFETs under consideration are described in section 2. Their thermal resistances are evaluated in section 3. Section 4 is devoted to modelling of SHEs and its numerical validation. Finally, the conclusions are presented in section 5.

2. DGMOSFETs under study

According to the present ITRS technology roadmap [2], we have considered horizontal DGMOSFETs with epitaxially deposited source and drain [13], with the layer stack sketched in figure 1. For this structure, the silicon channel is up-down surrounded by two oxide layers, silicon and hafnium dioxides, whose depths are $t_{SiO_2} = 0.7\,\text{nm}$ and $t_{HfO_2} = 2.4\,\text{nm}$, respectively, with an equivalent oxide thickness (EOT) of $t_{ox} = 0.9\,\text{nm}$.

Metal gate technology is particularly attractive because it eliminates the poly-Si gate depletion effect and, consequently, the associated degradation in the transistor performance; the doping concentration in the silicon body can be reduced, increasing the electron mobility. Thus, a near mid-gap metal gate, $CoSi_2$, is assumed (G) with a 4.6 eV work function [14] and a depth of $t_{CoSi_2} = 50\,\text{nm}$.

Different device sizes are used in the study. For a gate width, W, of 100 nm, the channel lengths have been L = 22, 44, and 66 nm [15], and the thicknesses of the silicon layer chosen have been $t_{Si} = 10$, 20, and 30 nm [16]. The DGMOSFET with L = 22 nm (L_{nom}) and $t_{Si} = 10$ nm ($t_{Si,nom}$) is named nominal, because its performance will be reference for the rest of transistors.

Epitaxially regrown contacts (S and D, respectively), and source and drain extensions are selected to ensure heat is more easily transferred out the nominal DGMOSFET. Thus, according [17], the source and drain height is 50 nm ($\approx 5t_{Si,nom}$), and extensions are 9 nm long ($\approx L_{nom}/2$), from the borders of the gate.

Concerning the doping profile, an unintentionally p-type $1.2\text{x}10^{15}$ cm^{-3} doping is supposed. In the case of source and drain contacts, constant n-type $5.2\text{x}10^{19}$ cm^{-3} doping is set up to 3 nm into the extensions, which is the peak value of the next Gaussian profile with 2.83 nm variance.

3. Thermal analysis

3.1 Thermal conductivity of thin films

It is known that the thermal conductivity of ultra-thin films is strongly reduced with respect to the bulk material value by approximately one order of magnitude. In our DGMOSFET, the thin films introduced are the gate oxides and the silicon channel, whose thermal conductivities can be expressed as follows [4],

$$k_{\text{thin film}} \approx a + bT_l + cT_l^2, \tag{1}$$

where T_l stands for the lattice temperature and a, b, and c are fitting parameters for the corresponding layer thickness (see table 1). Figure 2 shows the resulting thermal conductivities (including that of the silicon layers chosen), for the temperature range of interest for the DGMOSFET operation regimes. As for bulk samples, the thermal conductivity in silicon thin films remains two orders of magnitude higher than in oxide ones. The Si and HfO_2 thermal conductivities diminish linearly as temperature increases, and that of the SiO_2 films shows an opposite quadratic behaviour. In addition, the Si thermal conductivity rises linearly as the layer thickness increases.

For the source and drain regrown contacts the thermal conductivity (1) is still valid, with silicon fitting parameters replacing t_{Si} by 50 nm [4] (see S/D values in figure 2).

3.2 Thermal characterisation

3.2.1 Numerical evaluation of the thermal resistance of the device

SHEs can be properly simulated (a drift-diffusion scheme coupled with the heat flow equation is employed here, with the room temperature, 300 K, set in all contacts) when all thermal conductivities of the materials involved in the DGMOSFET configuration are considered. For the nominal DGMOSFET the resulting output characteristics are shown as lines in figure 3. The corresponding data solving the heat flow equation are plotted with solid lines. Notice that in this case a negative output conductance appears in the saturation region. However, as expected, if SHEs are ignored (dotted lines) this behaviour vanishes.

Making use of the numerically simulated output characteristics, the total thermal resistance, R_{th}, is estimated as reported in [11, 12],

$$R_{th} \approx \frac{\Delta g_D}{I_{DS} \cdot \partial I_{DS}/\partial T_l|_{T_o}}, \quad (2)$$

where Δg_D stands for the difference between output conductances (calculated with and without SHEs), and T_o is the room temperature. As the electric power (and consequently the thermal power) rises, SHEs acquires relevance and R_{th} can be more precisely evaluated (the magnitude of the different terms in equation (2) changes). According for this, R_{th} results in 749450 KW^{-1} for $V_{DS} = V_{GS} = 1\,V$, when the lattice temperature increment in the nominal DGMOSFET is maximum.

3.2.2 Equivalent thermal circuit

Alternatively, the DGMOSFET thermal resistance can be evaluated from an equivalent thermal circuit [18–20]. Figure 4 sketches a thermal circuit with the main contributions, which are linked to the different areas of the DGMOSFET.

The thermal resistance components are estimated accounting for the geometry (see figure 1), the thermal conductivity of the materials employed [21–25], and the heat flow orientation. In general, for the usual bias conditions, the heat flows from drain to source and from the channel region to the gates, through the different areas of the device.

Thus, regarding the silicon channel, the associated thermal resistance, R_{ch}, is written as

$$R_{ch} = \frac{L}{k_{Si} W t_{Si}}, \quad (3)$$

where k_{Si} is the silicon thermal conductivity given by (1).

On the other hand, $R_{ox,h}$ accounts for the thermal resistance of both oxide layers in parallel, where the heat flows from drain to source. Then,

$$R_{ox,h} = \frac{L}{W\left(k_{SiO_2} t_{SiO_2} + k_{HfO_2} t_{HfO_2}\right)}, \quad (4)$$

where k_{HfO_2} and k_{SiO_2} are the thermal conductivities of hafnium and silicon dioxide, respectively, according to (1).

The heat flux from the silicon channel to the gates, through the oxide layers, is considered by means of $R_{ox,v}$. With oxide layers in series, $R_{ox,v}$ is given by

$$R_{ox,v} = \frac{t_{HfO_2}}{k_{HfO_2} LW} + \frac{t_{SiO_2}}{k_{SiO_2} LW}. \quad (5)$$

The heat flux through the $CoSi_2$ gates has also been taken into account. The flux from drain to source is modelled using R_g,

$$R_g = \frac{L}{k_{CoSi_2} W t_{CoSi_2}}, \tag{6}$$

where k_{CoSi_2} stands for the thermal conductivity of $CoSi_2$. Whereas the heat exchange at the external gate pads is characterised by the thermal resistance $R_{g,t}$, evaluated as follows,

$$R_{g,t} = \frac{W}{k_{CoSi_2} L t_{CoSi_2}}. \tag{7}$$

The contribution of the thermal resistance components linked to the gate to the total thermal resistance is low, because the thermal conductivity of $CoSi_2$ is much higher than that of the rest of the materials employed.

Furthermore, R_{gd} must be added for a convenient characterisation of the device heat dissipation. It accounts for the heat flux spreading from the drain extension towards the gates [17, 26], crossing the SiO_2 field oxide volume, and is conveniently evaluated using Sentaurus [27].

Finally, the source and drain extrinsic thermal resistances, R_s and R_d, have been also numerically evaluated with Sentaurus, considering the channel extension and regrown silicon region.

Fractions of thermal resistance in the equivalent thermal circuit (see figure 4) are due to the symmetries of the DGMOSFET geometrical structure. Table 2 summarises the resulting thermal resistances reported above for the nominal DGMOSFET at room temperature, for which, from numerical simulations, it is noted that 23% of the generated heat is escaping from the body through the gates, and 56% through the drain contact; the rest through the source terminal. Therefore, 77% of the heat dissipated in the device is spread out through the source and drain fan-out regions, which must be carefully designed, especially in the case of the drain contact, in order to reduce the associated thermal resistance.

Therefore, the key element in figure 4 is R_d, which should be reduced as much as possible. For that proposal flare extensions are commonly used [26]; this technique can also be applied to R_s, maintaining the symmetry of the transistor geometry. Self-heating could be alleviated even more by increasing the body thickness, t_{Si}, to reduce the channel thermal resistance, R_{ch}. However, in order to ensure a good electrostatic behaviour, t_{Si} is limited to be lower than $L/2$ [17]. Finally, by using metal gates with superior thermal conductivity (*e.g.* molybdenum in [4]) a better heat dissipation is expected (*i.e.* a lower thermal resistance through the gates, R_g and $R_{g,t}$).

3.2.3 Modelling scheme to account for SHEs

From the modelling perspective, SHEs are taken into account following the approach described in [18]: the lattice temperature in the channel, T_l, is related to the power dissipated in the device as follows,

$$T_l = T_o + R_{th} I_{DS}(V_{ds}, V_{gs}) \cdot V_{ds} \tag{8}$$

where $V_{ds} = V_{DS} - I_{DS}(R_{s,ohm} + R_{d,ohm})$ and $V_{gs} = V_{GS} + I_{DS}R_{s,ohm}$ are the intrinsic drain to source and gate to source voltages, respectively, being $R_{s,ohm}$ and $R_{d,ohm}$ the source and drain extrinsic ohmic resistances, numerically evaluated with Sentaurus.
However, in equation (8) the channel temperature is assumed uniform, which means that T_l represents its average value. When solving iteratively equation (8) making use of the analytical expression of the modelled drain current, I_{DS}, to be described in the following section, we have noticed that SHEs are better reproduced if an average value for the R_{th} along the channel is used, instead of the one derived from the hottest spot only (this latter approach was suggested by Pop et al. [17]).
In line with this idea, the DGMOSFET thermal resistance that we propose to enhance the model should be calculated as shown below,

$$R_{th} = (R_{th,1} + R_{th,2} + R_{th,3})/3, \tag{9}$$

where $R_{th,i}$ (i = 1, 2, 3) stands for the thermal resistances from the initial, middle, and end points of the silicon channel in the thermal circuit (see figure 4). Using this approach, we calculated a value of 445360 KW^{-1} for the total nominal thermal resistance, at room temperature, which is reasonable compared with that obtained in the subsection 3.2.1.
In the previous calculation, the temperature dependence of the thermal resistance can be incorporated. Assuming the lattice temperature is linearly distributed in the thermal circuit through $R_{ox,h}$, $R_{ox,v}$, R_{gd}, and R_d, from T_l to T_o, and considering a uniform distribution in every region, the thermal resistance is found to be proportional to the increment of the average lattice temperature:

$$R_{th} = R_{th_o}[1 + \alpha(T_l - T_o)], \tag{10}$$

where R_{th_o} is the nominal thermal resistance at zero injected power. Thus, the parameters R_{th_o} and α are found for all the geometries studied (see table 3). The resulting thermal resistances for possible expected temperature increments, $\Delta T_l = T_l - T_o$, are shown in figure 5. Notice that in all cases the thermal resistance is superior at higher temperatures, according with [28]. Their values are reasonable if compared with experimental results for single-gate MOSFETs of similar size [29].
Furthermore, R_{th} theoretically rises as the gate length, L, increases or the silicon layer thickness, t_{Si}, is reduced. However, as L increases the rise in thermal resistance relaxes significantly, which could be caused by a predominant heat flow through the drain thermal contact (not much affected by the channel length change), losing relevance the source terminal as heat exchanger.

4. Drain current modelling

The drain current model used here is based on a charge control model presented in [30].

The inversion charge (11) and drain current (12) are calculated as in [30, 31] for all the important operation regimes,

$$Q = 2C_{ox}\left(-\frac{2C_{ox}\beta^2}{Q_o}+\sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o}\right)^2+4\beta^2\ln^2\left[1+\exp\left(\frac{V_{gs}-V_{th}+\Delta V_{th}-V}{2\beta}\right)\right]}\right) \quad (11)$$

$$I_{DS} = \beta^2 W\mu_{eff}\left(L+\delta_o\frac{\mu_{eff}V_{ds}}{v_{sat}}\right)^{-1}\left[\frac{2(Q_s-Q_d)}{\beta}+\frac{Q_s^2-Q_d^2}{4\beta^2C_{ox}}+8C_{Si}\ln\left(\frac{Q_d+2Q_o}{Q_s+2Q_o}\right)\right], \quad (12)$$

where β is the thermal voltage, $Q_o = 4\beta C_{Si}$ ($C_{Si}=\varepsilon_{Si}/t_{Si}$), $C_{ox}=\varepsilon_{SiO_2}/t_{ox}$, δ_o is a parameter introduced in [31] to account for velocity saturation effects, $Q_s = Q(V=0)$ and $Q_d = Q(V=V_{ds})$, and V_{th} and ΔV_{th} are given in [30]. The effective mobility model introduced, μ_{eff}, is based on the one presented in [32]. Finally, a scheme like in [33] is used for the calculation of the saturation current, inclusive of the pinch-off region length.

The accuracy of the model, in relation to the temperature dependence of the different magnitudes, was previously checked in the nominal DGMOSFET by comparison with simulation results at different constant lattice temperatures (neglecting SHEs). In connection with this fact, the low-field mobility dependence used, $\mu_{eff} = \mu_{eff_o}(T_o/T_l)$, is close to the one described in [34] for ultra-thin-body SOI devices, and the velocity saturation dependence is $v_{sat} = 2.4\times10^7/[1+0.8\exp(T_l/600)]$ cms^{-1}. The result at room temperature is shown with squares in figure 3, where a good fit is achieved (compare with dotted lines).

With this model we are also able to reproduce accurately the simulation results for DGMOSFETs of different sizes. From the modelling perspective, SHEs are taken into consideration by means of (8), with the thermal resistance given by (10) and the corresponding data of table 3. Thus, for each iteration the new T_l is obtained with (8), wherein both terms, I_{DS} and R_{th}, are evaluated with the lattice temperature of the previous iteration. The process is repeated until convergence is achieved (notice that the mobility, saturation velocity and inversion charge are temperature dependent).

As can be seen in figure 3 for the nominal DGMOSFET, in triangles, and in figure 6 for all transistors, in symbols ($V_{GS}=1$ V was chosen to enhance SHEs), the simulated output characteristics with SHEs (in solid lines) are correctly reproduced. We have found that the negative output conductance in the saturation region completely vanishes when the silicon layer thickness, t_{Si}, is higher than 14 nm.

We have also compared, for the sake of coherence, the simulated temperature from source to drain in the intrinsic channel (see figure 7, where circles represent the location of the borders of the gates, which are solid by the drain side, and $V_{GS}=V_{DS}=1$ V to maximize SHEs), with the T_l obtained when the model iterative calculation converges, which is plotted with hollow triangles (an horizontal line has been added in this case to ease the comparison with the local temperature). We found similar values for all geometries, within a relative error lower than 7.3%. In all cases the peak temperature takes place at the end of the channel, by the drain side, according to [17, 26].

As described in [4], the average channel temperature decreases when the gate length and silicon layer thickness increase. In the former case, this is because the electrical

dissipated power is reduced (the drain current decreases), in spite of a higher thermal resistance. In the latter case the thermal resistance diminishes drastically and, consequently, so does the thermal dissipated power.

5. Conclusions

An in-depth simulation and modelling study of SHEs in DGMOSFETs has been performed. Making use of temperature-dependent thermal resistances, accounting for the thermal conductivity reduction with the layer thickness, DC thermal effects in DGMOSFETs have been successfully modelled, when varying the silicon layer geometry, by using an equivalent thermal circuit. The equivalent thermal resistances obtained with the thermal circuit are consistent with simulation results using Sentaurus. An analytical model for the drain current of these devices is proposed, accounting for SHEs, velocity saturation, and short channel effects. The average lattice temperatures derived with the model calculations are consistent with those obtained from numerical simulations, thereby validating the proposed model. Furthermore, the lattice temperature variation, as the gate length and silicon layer thickness are increased, is correctly predicted. On the other hand, in our analysis, negative conductance values cannot be seen for silicon layer thicknesses above 14 nm. Finally, the modelling approach we present here to account for SHEs can be easily incorporated in circuit simulators as an add-on to other well-established models.

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FIGURES

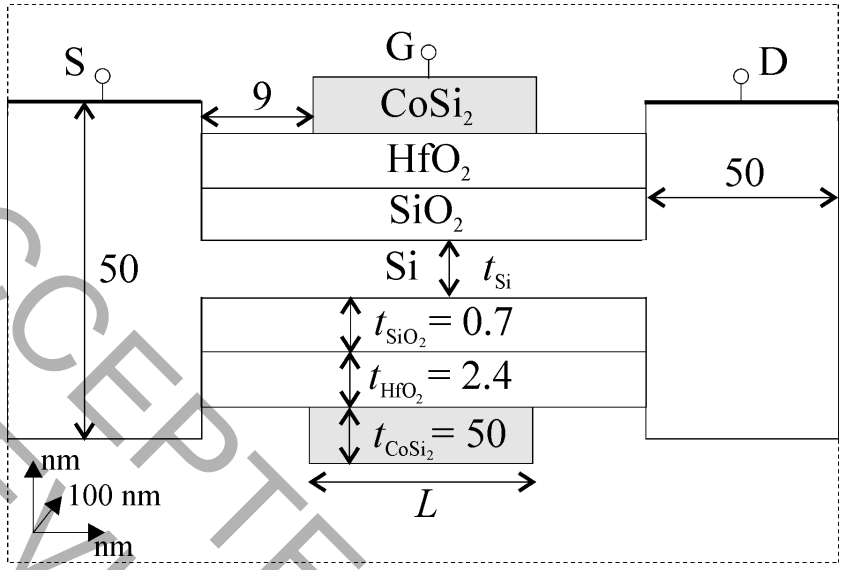

Figure 1. Cross-sectional view of the DGMOSFETs under study (not drawn to scale).

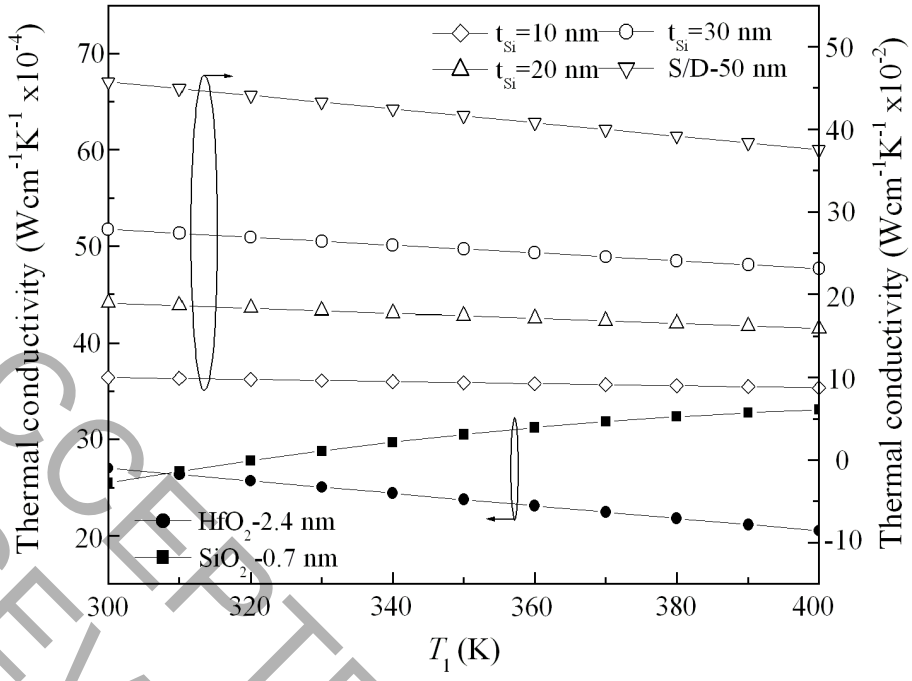

Figure 2. Temperature dependence of the thermal conductivity of thin films, and source and drain (S/D) regrown contacts. Open symbols represent the thermal conductivity of Si. Closed circles and squares are thermal conductivities of HfO_2 and SiO_2, respectively.

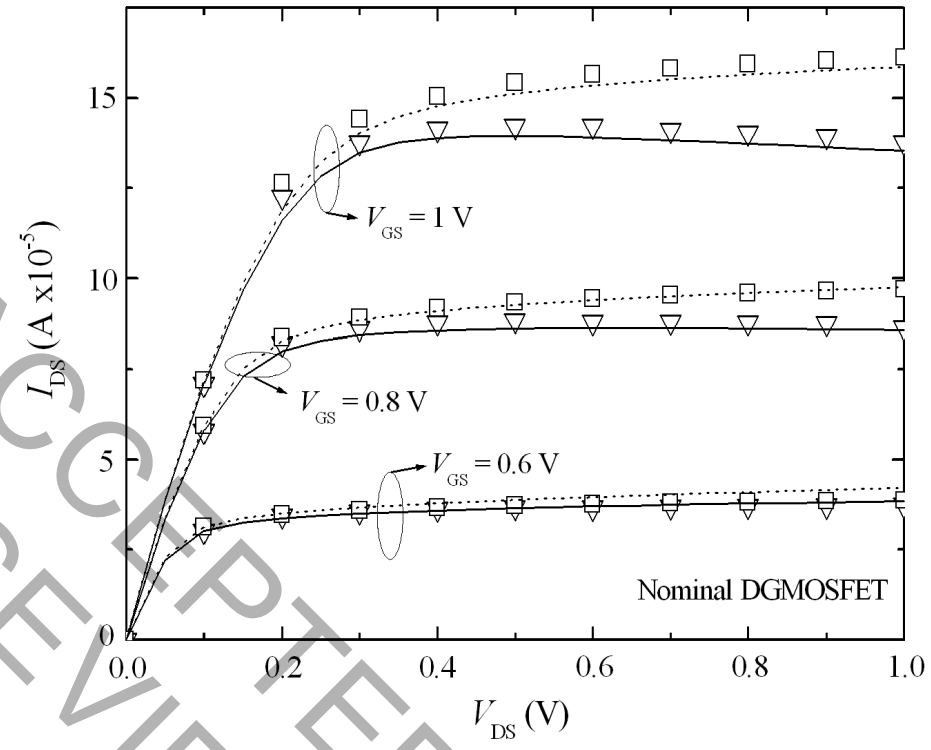

Figure 3. Output characteristics for the nominal DGMOSFET and V_{GS} = 0.6, 0.8, and 1 V. Simulations are shown in lines (room temperature results in dotted lines and data including SHEs in solid ones), and modelled data in symbols (room temperature results in squares and data including SHEs in triangles).

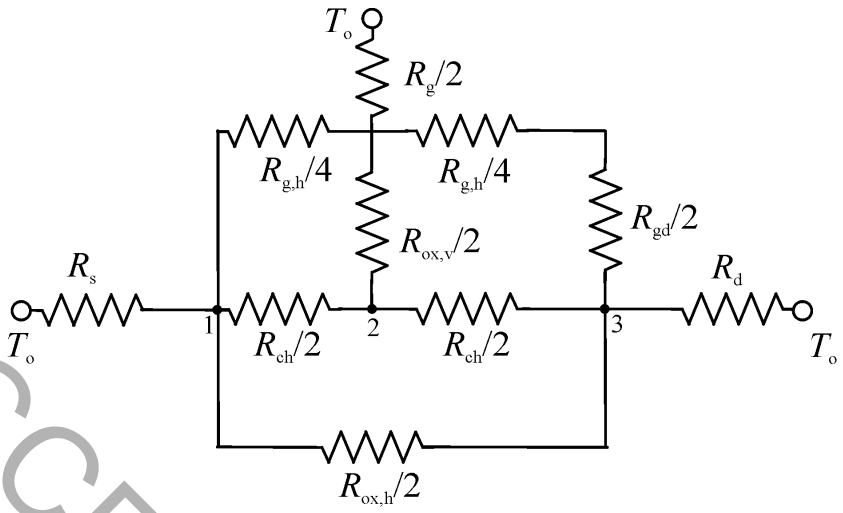

Figure 4. Equivalent thermal circuit for DGMOSFETs.

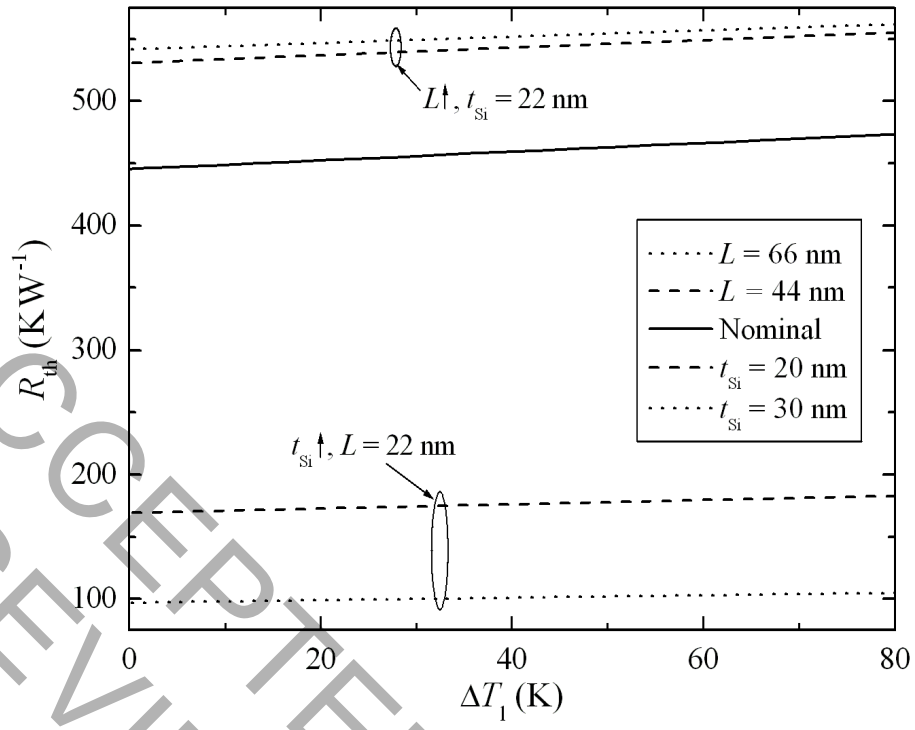

Figure 5. Temperature dependence of the DGMOSFET thermal resistance for different geometrical configurations.

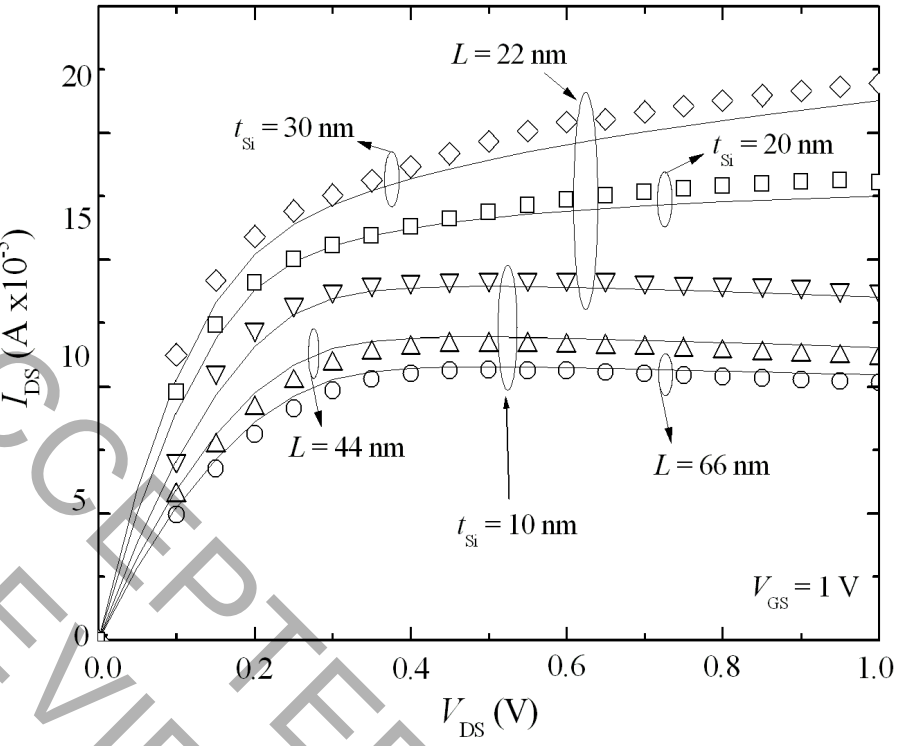

Figure 6. Output characteristics with SHEs for DGMOSFETs with L = 44 and 66 nm (for t_{Si} = 10 nm), t_{Si} = 20 and 30 nm (for L = 22 nm), and the nominal DGMOSFET (L = L_{nom} = 22 nm and t_{Si} = $t_{Si,nom}$ = 10 nm). Simulations are shown in lines and modelled data in symbols; V_{GS} = 1V.

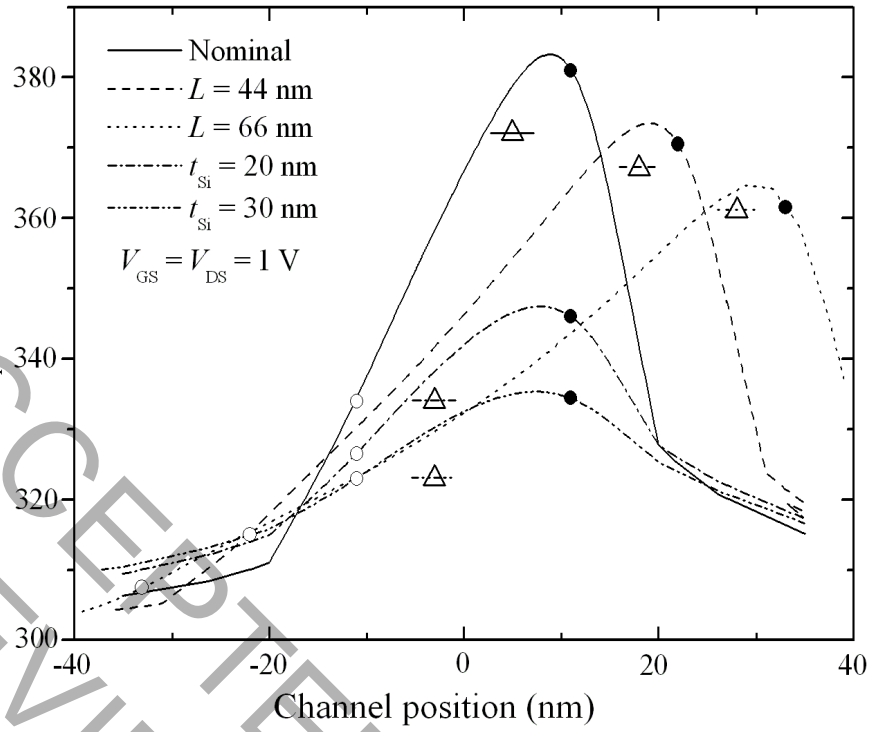

Figure 7. Simulated local channel temperature versus channel position along the longitudinal direction, for DGMOSFETs with different geometries, is shown in lines. Circles represent the location of the borders of the gates, being solid at the drain side. The average channel temperature obtained with the model, accounting for SHEs, is shown in hollow triangles (an horizontal line has been added in this case to ease the comparison with the local temperature); $V_{GS} = V_{DS} = 1$ V.

TABLES

	Si t_{Si} (cm)	**SiO_2** 0.7 nm	**HfO_2** 2.4 nm
$\boldsymbol{a}$ ($Wcm^{-1}K^{-1}$)	$141575t_{Si}$ -3.9x10^{-3}	-5.6x10^{-3}	-4.6x10^{-3}
$\boldsymbol{b}$ ($Wcm^{-1}K^{-2}$)	-174t_{Si} +4.8x10^{-5}	4.2x10^{-5}	-6.5x10^{-6}
$\boldsymbol{c}$ ($Wcm^{-1}K^{-3}$)	–	-4.9x10^{-8}	–

Table 1. Thermal conductivity parameters

Thermal resistances at 300 K (KW^{-1} x10^5)						
$\boldsymbol{R_{ch}}$	$\boldsymbol{R_{s/d}}$	$\boldsymbol{R_{ox,h}}$	$\boldsymbol{R_{ox,v}}$	$\boldsymbol{R_{g,h}}$	$\boldsymbol{R_{g,t}}$	$\boldsymbol{R_{gd}}$
11	12.9	1330	59.6	1.3	27.5	171

Table 2. Thermal resistances for the equivalent thermal circuit of the nominal DGMOSFET at room temperature

	Nominal DGMOSFET	$\boldsymbol{L}$ (nm)		$\boldsymbol{t_{Si}}$ (nm)	
		44	66	20	30
$\boldsymbol{R_{th_o}}$ (KW^{-1})	445360	530659	541669	169244	96991
$\boldsymbol{\alpha}$ (K^{-1} x10^{-4})	7.9	5.8	4.7	10.0	10.1

Table 3. Thermal resistance parameters