DC self-heating effects modelling in SOI and bulk FinFETs

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ABSTRACT

DC thermal effects modelling for nanometric silicon-on-insulator (SOI) and bulk fin-shaped field-effect transistors (FinFETs) is presented. Among other features, the model incorporates self-heating effects (SHEs), velocity saturation and short-channel effects. SHEs are analysed in depth by means of thermal resistances, which are determined through an equivalent thermal circuit, accounting for the degraded thermal conductivity of the ultrathin films within the device. Once the thermal resistance for single-fin devices has been validated for different gate lengths and biases, comparing the modelled output characteristics and device temperatures with numerical simulations obtained using Sentaurus Device, the thermal model is extended by circuital analysis to multi-fin devices with multiple fingers.

Keywords: Fin-shaped field-effect transistor (FinFET), self-heating effects (SSE), thermal resistance, compact modelling.

1. Introduction

Multi-gate MOSFETs are one of the most competitive alternatives for the future scaling scenario described by Moore's law (which considers channel lengths below 20 nm), as predicted by the International Technology Roadmap for Semiconductors (ITRS) [1]. They show excellent gate controllability over the channel, leading to strong immunity to short-channel effects and an ideal sub-threshold slope [2]. In addition, random-dopant-induced variability and junction parasitic capacitances are reduced. Multi-gate devices also present high mobilities and I_{on}/I_{off} ratios, which are linked to the use of undoped silicon, and the volume inversion operation connected with geometrical quantum confinement [3].

Within the multi-gate device environment, fin-shaped field-effect transistors (FinFETs, see Fig. 1(a)) show a tremendous potential for scaling, while maintaining CMOS compatibility. Both, silicon-on-insulator (SOI) and bulk based devices can be found in FinFET technology. However, a great deal of progress is still needed to effectively describe and model their thermal characteristics, due to the low thermal coupling that takes place in devices with nano-scale dimensions [4–6], which is expected to increase because of the lower thermal conductivities of the films used in prototypes for future nodes described by the ITRS.

The microelectronics community is working hard towards the development of compact models for multigate MOSFETs, particularly FinFET models [7, 8]. In this context, it is important to account for self-heating effects (SHEs) in DC and AC low-frequency regimes [9, 10], when they can even lead to negative output conductance.

Although some authors have shown a detailed thermal model accounting for the different regions of a device [5], we have chosen a local simplified scheme, accurate enough to reproduce SHEs on FinFETs [4]. In this respect, we have not deepen on non-stationary transport [11, 12] since here we are mainly focused on the thermal facet of the model (although velocity overshoot effects could have

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been incorporated in the electrical section of the model). Thus, the model we are proposing characterizes the physics of thermal conduction within the device accurately, keeping at the same time a reasonable degree of simplicity, which is an essential feature from the compact modelling viewpoint.

The structure of the SOI and bulk FinFETs under study is described in Section 2. The necessary numerical details to evaluate the proposed thermal and electric models with Sentaurus Device [13], by Synopsys, are given in Section 3, including the thermal conductivities of the ultrathin films involved in the structure. The resulting output characteristics and local channel temperatures for 3D single-fin devices are also exposed in this section. Afterwards, the single-fin FinFETs' thermal resistance is evaluated in Section 4, with the help of an equivalent thermal circuit; DC electrical and thermal modelling is also presented, as well as its numerical validation. In Section 5 the thermal model is extended by circuit analysis to multi-fin devices with multiple fins, incorporating the components associated with each element. Finally, Section 6 presents the main conclusions.

2. FinFETs under study

According to the guidelines suggested in [1], we have studied and modelled FinFETs for which the single-fin structure is shown in Fig. 1(a). Its vertical cross-section (through the gate) has been sketched in Fig. 1(b), and the corresponding geometrical parameters, taken from [1, 5] and [14–16], are listed in Table 1.

We have considered a TiN gate, whose work-function can be adjusted to 4.5 eV, showing an electrical resistivity of 270 μΩcm [17]. The material chosen for the high-k gate insulator is HfO_2, which is supposed to be 3 nm thick below the lateral gates, and 20 nm deep under the top gate [18]. The silicon fin is surrounded by a SiO_2 layer, 0.8 nm thick. The two insulator films (HfO_2 and SiO_2) result in a lateral equivalent oxide thickness (EOT) of 1.3 nm. In addition, the fin height chosen is 60 nm. The fin width is set to 20 nm; for this thickness the quantum effects (of very high computational cost [19]) are known to have a lesser influence. Moreover, the source and drain extensions, 30 nm long, are covered with silicon nitride spacer dielectric [20].

An unintentional p-type 10^{15} cm^{-3} basic doping is assumed in silicon. In relation to the overlap source and drain contacts, constant n-type 5.2×10^{19} cm^{-3} doping is present up to 24 nm into the extensions (from the border of the pads), which is the peak value of a Gaussian profile with 2.83 nm variance [16].

A typical buried oxide (BOX) layer thickness of 100 nm is chosen for SOI FinFETs. In bulk FinFETs the fin body extends down through the silicon dioxide, with the p-type 10^{15} cm^{-3} substrate doping. The resulting inactive fin (in between the active fin and the substrate) is indicated with a dotted contour in Figs. 1(a) and 1(b). Finally, a 700-μm-thick substrate is assumed [5].

3. Numerical simulation of single-fin devices

3.1. General considerations

Neither drift-diffusion nor energy transport can describe the DC *I-V* characteristics of transistors at nano-scale regimes, as they do not obey the thermal velocity limit on the diffusive transport of carriers across thin low-field regions [21]. However, in silicon the saturated velocity is almost the same as the thermal velocity, and therefore the drift-diffusion transport works well, particularly if accurate mobility models for this approach are employed [21–23]. In addition, this simulation scheme is more reasonable from a time-computing view, if it has to be solved self-consistently with the heat equation in 3D geometrical structures.

The impact of SHEs on the transistor performance has been analysed in depth by auto-consistently solving the heat flow equation with the Poisson and drift-diffusion equations, using Sentaurus Device [13]. The mobility model includes the degradation of the transport properties at the SiO_2–Si interface by means of surface-roughness scattering, phonon scattering, and saturation velocity effects, through Canali and Lombardi based models; in addition, Coulomb scattering is included considering the concentration of ionized impurities (see Section 2) through the Masetti model [13]. Furthermore, the

mobility model parameters have been modified for (110) wafer orientation, by reducing the low-field mobility as in [24].
For the heat equation solution the substrate is substituted by a boundary condition, consisting of a room-temperature thermal contact located at the bottom of the structure, incorporating an equivalent surface thermal resistance, 0.023 Kcm^2/W, numerically evaluated to account for a thermal resistance that represent the thermal coupling of the bottom of the FinFET structure to the underlying substrate (normalized to the FinFET cross section area). Finally, the room temperature, T_o = 300 K, is set as the temperature for all metallic contacts of the devices.

3.2. Thin films thermal conductivity calculation

For a proper thermo-electrical simulation in the DC operating regime, the temperature-dependent thermal conductivity of the different layers constituting the device needs to be incorporated in the heat flow equation [23]. Furthermore, it is necessary to consider the reduction in the thermal conductivity in thin films with respect to the bulk value (by approximately one order of magnitude in the case of ultrathin films) [6, 25].
In the FinFETs under study, the gate insulators, the silicon fin, and pads are ultrathin films, therefore we have accounted for the thermal conductivity reduction explained above. For the purpose of numerical simulation within the temperature range of interest found in the usual operating regimes (between 300 K and 400 K), with data taken from [18, 20, 22] and [25–27], a general quadratic temperature dependence for all thermal conductivities (including that of thicker films), $k_{film} \approx a + bT_l + cT_l^2$, can be used by the TCAD tool, where T_l stands for the lattice temperature, and a, b, and c are fitting parameters for the corresponding film (see Table 2).

3.3. Output characteristics and local channel temperature

For SOI and bulk single-fin devices, the simulated output characteristics at room temperature are represented with squares (without SHEs) and triangles (with SHEs) in Figs. 2(a) and 2(b), respectively, for the two channel lengths studied: 25 nm and 50 nm. The current reduction is evident when SHEs are incorporated, due to mobility degradation. Furthermore, bulk FinFETs show a 7% higher current than their SOI counterparts, with and without SHEs. Therefore, it must be attributed to some inversion charge which is found in the oxide-semiconductor surface of the inactive fin.
On the other hand, the simulated local channel temperature, from source to drain in the intrinsic channel, has been represented in Fig. 3 with solid and dashed-dotted lines for SOI and bulk single-fin devices, respectively, where the bias chosen is $V_{GS} = V_{DS} = 1$ V to enhance SHEs. For both types of FinFET and for the two channel lengths under consideration, the peak temperature takes place at the end of the channel by the drain side (since the drift-diffusion scheme is being used, instead of a non-local transport approach, the peak temperature is placed less inside the drain, around 6 nm [4, 6]. This displacement does not cause a drastic variation of the thermal performance, since this characteristic is more closely linked to the resistance of the thermal paths, technologically dependent, through which the heat generated in the device operation is evacuated).
In both types of single-fin device the lattice temperature reduces, in a similar way, as the channel length increases (at around 12 K the peak values). And in bulk FinFETs, for which the current is superior, the simulated peak temperature is only 3 K lower than in their SOI counterparts, demonstrating that for single-fin devices the inactive fin role in alleviating SHEs is not decisive.

4. Single-fin thermal characterization

Several expressions for DC and AC regimes have been proposed in the literature to evaluate the thermal resistance of field-effect transistors [9]. However the *I-V* characteristics must be previously known, with the resulting value depending on the bias selected, or heat is assumed to flow towards the substrate. These disadvantages can be overcome when a proper equivalent thermal circuit is used [4]. The thermal circuit should correctly describe the heat flow orientation, mainly from drain to source and from the channel region to the gate, as well as maintaining a reasonable degree of simplicity, to be useful in the context of compact model development for circuit simulators.

4.1. Equivalent thermal circuit

The single-fin thermal resistance is evaluated with the equivalent thermal circuit shown in Fig. 4, where nodes 1, 2, and 3 represent the initial, middle, and end points of the silicon channel, respectively. The contributions linked to the main device regions (from the thermal perspective) have been included by their related thermal resistances (different fractions of these thermal resistances are employed due to the symmetries found in the transistor geometrical structure), which are evaluated at room temperature.

Thus, for the silicon channel the associated longitudinal thermal resistance is R_{ch}. The extrinsic source and drain thermal resistances are R_s and R_d, respectively. The heat flux from the silicon fin to the metal gate, through both gate oxides (including top and side layers), is considered by means of R_{ox}. Different heat fluxes in the TiN gate are taken into account with R_{gt} and R_{gl}: R_{gt} models the thermal flux that spreads out laterally through the gate, and R_{gl} the heat flux contribution from the drain and source regions, through the top and side gate metals.

Inside the FinFETs, the heat is mainly produced in the channel region. In particular, the hottest spot is found at the gate-drain border, where the carriers reach the peak temperature (see Fig. 3). The high temperature difference expected between the drain and metal gate regions makes it necessary to incorporate a component to account for a thermal conduction path, from the drain extension towards the gate, through the nitride spacer [4]; R_{sp} denotes this component in the thermal circuit. Nevertheless, the corresponding gate to source thermal resistance can be ignored, due to the low temperature difference observed in numerical simulations between these two regions. Thus, on the source side R_{gl} /2 is directly connected to the border of the silicon channel (node 1 in Fig. 4).

In the case of SOI FinFETs, the back of the die has a negligible contribution to the thermal energy flow [4], [5]. However, for bulk devices the heat flow through the inactive fin towards the substrate, along the silicon body, must be considered. As Fig. 4 shows with dotted branches, the thermal resistances $R_{ch,b}$, $R_{s,b}$ and $R_{d,b}$ are incorporated in the bulk single-fin thermal circuit to account for this flow from the channel, and from the source and drain extensions. Finally, R_{sub} models the substrate thermal resistance.

The thermal components R_s, R_d, R_{ch}, R_{ox}, R_{gl} and R_{sp} are calculated as in [4]. For R_{gt} approximately the length of the resistive path is the metal gate thickness, w_{TiN}, and the cross-sectional area of the heat flux path is the average of the two areas at the sides of the interconnection, $w_{TiN} \times L$ and $h_{TiN} \times L$ in Fig. 1. Finally, for $R_{ch,b}$ the cross-sectional area of the heat flux path is that corresponding to the inactive fin region, $w_{fin} \times L$, which is $w_{fin} \times (L_{ext} + w_{pad})$ for $R_{s,b}$ and $R_{d,b}$; the length of their resistive path is the inactive fin height (*i.e.* h_{BOX}).

Thus, all thermal components, except R_{sub}, are evaluated with the expressions summarized in the appendix; R_{sub} has been determined with Sentaurus Device, through the thermal coupling of the bottom of the FinFET structure to the underlying substrate.

4.2. Thermal resistance and device temperature modelling

In a general purpose FinFET, SHEs are modelled by evaluating the average lattice temperature in the intrinsic channels, T_l, accounting for the Joule heating produced by the device operation as follows:

$$T_l = T_o + R_{th} N_F N I_{DS} V_{ds}, \qquad (1)$$

where R_{th} is the equivalent thermal resistance; N_F and N denote the number of fingers and fins (per finger), respectively; I_{DS} is the modelled drain current for a single-fin; $V_{ds} = V_{DS} - I_{DS}(R_{s,ohm} + R_{d,ohm})$ is the intrinsic drain to source voltage, with V_{DS} the corresponding extrinsic voltage; and $R_{s,ohm}$ and $R_{d,ohm}$ the source and drain extrinsic ohmic resistances, respectively, which are evaluated like the thermal ones, R_s and R_d, by substituting the electrical for thermal conductivities [23] (equipotential inter-finger source/drain contacts are assumed).

According to the modelled lattice temperature (1), the thermal resistance must be evaluated on average along the channels. Thus, for single-fin devices ($N_F = N = 1$) the thermal resistance, $R_{th} = R_{1,1}$, is obtained as in [22]: the average of the thermal resistances from nodes 1, 2, and 3 in the corresponding single-fin thermal circuit, to room-temperature nodes (see Fig. 4). Its value is shown

in Table 3 for both types of FinFET and the two gate lengths studied. In general, $R_{1,1}$ rises as the gate length increases, and is lower for bulk FinFETs than for their SOI counterparts, but still superior to those for the double-gate MOSFETs (DGMOSFETs) in [22], with similar channel lengths and silicon thicknesses (according to [10]). This lower thermal coupling in FinFETs between the silicon body and the outer device areas is linked to the enhanced heating confinement, with channels more surrounded by oxide layers.

On the other hand, the drain current model used in (1) is based on a previous DGMOSFET charge control model presented in [28]. This model works well for the FinFETs under study here, since the contribution of the inversion charge under the top gate is low in comparison with the charge associated with the side gates. Thus, the current is calculated as in [22], for all significant operating regimes, with a scheme similar to [29] for the calculation of the saturation current, inclusive of the velocity saturation and pinch-off region length. The effective mobility model is based on the model presented in [30], whose parameters are fitted with simulation data, and the result is the same for the two channel lengths studied. Then, the low-field mobility dependence used, $\mu_{\text{eff}} = \mu_{\text{eff}_o}(T_o/T_l)^{0.8}$, is close to the one described in [6] (the exponent, 0.8, is lower) and in [31] (in this case the exponent is higher) for ultrathin body SOI devices, and the velocity saturation dependence is $v_{\text{sat}} = 2.4\times10^7/[1+0.8\exp(T_l/600)]$ cm/s.

The extension of the active oxide-semiconductor surface in bulk FinFETs, observed in numerical simulations, is modelled using a correction in the silicon fin height ($h_{\text{fin}}\times1.07$), which proved to work correctly in the operating regimes considered (it is not the case for the sub-threshold region, when volume inversion dominates over surface inversion and SHEs are negligible).

The device temperature and current are modelled through an iterative procedure; for each iteration T_l is recalculated using (1), where I_{DS} is evaluated with the lattice temperature of the previous iteration, until convergence is achieved. **The details of the real MOSFET model employed to calculate I_{DS} are given in Ref. [22]; although, for the sake of clarity, we have not included them here, since we were mainly focusing on the thermal facet of the model. Once convergence is achieved we assumed that the device average temperature and current are determined.**

In the case of SOI and bulk single-fin devices, the resulting modelled output characteristics at room temperature are shown with solid lines (without SHEs) and dashed lines (with SHEs) in Figs. 2(a) and 2(b), respectively. A good fit of the simulation results is achieved for the two channel lengths studied. The bulk FinFETs' fit works better for the longer device, which is expected since the uniformity of the charge in the inactive fin is altered less by short-channel effects.

Finally, the simulated local temperature along the intrinsic channel of the single-fin devices has also been successfully compared with the T_l obtained when the model converges (hollow triangles in Fig. 3). Simulated and modelled temperatures for the same biases show similar behaviour in both types of device (as Subsection 3.3 describes), with a relative error between them lower than 3.8%.

5. Thermal characterization of multi-fin devices with multiple fingers

Once the thermal characterization of the single-fin devices has been validated, the thermal model is extended to multi-fin devices, with multiple fingers, appropriately connecting the constituting fin thermal circuits through the inter-fin gate and the inter-finger source/drain resistances. Then, applying the iterative procedure described for single-fin devices, with thermal resistances obtained by circuital analysis as follows, the device temperature of the general purpose FinFETs can be predicted.

The following scalable model for the FinFETs' thermal resistance with the number of fins, N, and fingers, N_F, can be extracted from experimental measurements in [10]:

$$\frac{1}{R_{\text{th}}} = \frac{N_F^2}{R_{1,1} + R_{\infty,1}(N_F - 1)} + \frac{N_F^2(N-1)}{R_{1,\infty} + R_{\infty,\infty}(N_F - 1)}, \qquad (2)$$

where $R_{1,\infty}$ represents the thermal resistance per fin for multi-fin devices with single finger ($R_{th} \approx R_{1,\infty}/N$); $R_{\infty,1}$ corresponds to single-fin devices with multiple fingers ($R_{th} \approx R_{\infty,1}/N_F$); and $R_{\infty,\infty}$ stands for that of multi-fin devices with multiple fingers ($R_{th} \approx R_{\infty,\infty}/N_F N$). They can be extracted by analysis of their respective equivalent thermal circuits, as Figs. 5(a), 5(b) and 5(c) show, with R_i and R_m being the inter-fin gate and inter-finger source/drain thermal resistances, respectively.

In every case, the number of fins and/or fingers is risen (fifteen is enough) until the pads are far away from the inner fins, in this case, adding more components to the device will no longer increase the peak temperature. Then, the thermal resistance of the inner fins stops rising and its value, evaluated on average along the corresponding channel, represents the required thermal resistance per fin. Table 3 shows the resulting parameters for general purpose FinFETs, assuming a fin spacing 225 nm long [4] (*i.e.* $R_i = 2.3\times10^6$ K/W and 1.2×10^6 K/W for L = 25 nm and 50 nm, respectively), and copper inter-finger source/drain contacts [5] (*i.e.* $R_m = 5.0\times10^5$ K/W and 5.8×10^5 K/W for L = 25 nm and 50 nm, respectively).

As far as we know, very few experimental data of FinFETs' thermal resistances (strongly technologically dependant) have been published in the literature, and those found are for SOI devices. Thus, for a single-finger-40-nm SOI FinFET, with ten fins, a thermal resistance of 50×10^3 K/W has been measured in [32], meanwhile our model predicts 67×10^3 K/W with 50 nm long gates. Additionally, for a 14-nm SOI FinFET with 120 fingers, and two fins per finger, 13×10^3 K/W was obtained in [10], meanwhile our model predicts 8×10^3 K/W with the gate which length is 25 nm. Finally, for 47-nm UTB MOSFETs, $R_{1,\infty} = 638\times10^3$ K/W is extracted from experimental measurements in [33], close to our modeled parameter with 50 nm long gates, 508×10^3 K/W. These comparisons confirm the goodness of fit of our model in describing the thermal resistance dependence on the number of fins and fingers.

Notice that $R_{1,\infty}$ and $R_{\infty,\infty}$ do not increase with gate length as $R_{1,1}$ and $R_{\infty,1}$ do, because the heat removal path through inter-fin gate contacts is less resistive. Furthermore, all of them are lower for bulk FinFETs than for their SOI counterparts, evidencing a reduced impact of SHEs in bulk devices. In Figs. 6(a) and 6(b), the left axis represents the resulting modelled thermal resistance reduction with the number of fins (for N_F = 1) and fingers (for N = 30) respectively, with solid and dashed lines for SOI and bulk devices, and the two gate lengths studied here (25 nm and 50 nm, with triangles and squares, respectively). In the former figure, as in single-fin devices, R_{th} rises as the gate length increases; however, this dependence vanishes with the number of fins, in agreement with [33]. Thus, as expected, no influence of the gate length is observed in the last figure: data for L = 50 nm overlap those for L = 25 nm. In any case, the bulk FinFETs' thermal resistance keeps being lower than in the SOI case.

In Figs. 6(a) and 6(b), the right axis shows the corresponding modelled temperature rise (average temperature rise in channel) for $V_{GS} = V_{DS}$ = 1 V (this bias was chosen to enhance SHEs). For both types of transistor, the modelled temperature rise diminishes as the gate length increases. This reduction enhances as the number of fins rises, and keeps a constant behaviour with the number of fingers. Furthermore, the modelled temperature rise increases with the number of fins and fingers, although a saturation value shows up (for bulk devices the impact of the number of fingers is not as significant). In any case, lower temperatures are obtained for bulk devices in comparison with their SOI counterparts. In the worst SHE case considered here (*i.e.* for N = 30 and N_F = 30) the modelled temperature tends to 410 (390) K for SOI devices with L = 25 (50) nm, respectively, and 380 (363) K for their bulk counterparts. Thus, ~30 K lower temperatures are obtained in bulk devices, with a 12.3% higher current (for both gate lengths).

Finally, it can be pointed out that the thermal response of bulk FinFETs would tend to that of SOI FinFETs if thinner fins were used. Nevertheless, considering the Si thermal conductivity in thin films, for an identical thermal response in both technologies (*i.e.* when $k_{Si\text{-}fin} = k_{SiO_2}$) a fin body thinner than 1 nm would be required (with BOX thicknesses superior to 100 nm) [23].

6. Conclusions

Accounting for SHEs in compact models is essential to accurately describe the DC current decrement, due to the rise in device temperature, in nanometric SOI and bulk FinFETs, mainly when multi-fin devices with multiple fingers are used. For this purpose an equivalent thermal resistance was obtained by circuital analysis, representing the temperature distribution and main heat flow paths in the device, and considering the degraded thermal conductivity of the internal thin layers. The thermal resistances, lower for bulk devices, reduce with the number of fins and fingers, and are consistent with those previously reported for other SOI technologies. Furthermore, their superior values for higher gate lengths vanish with the number of fins. On the other hand, a DC current model including SHEs, through the thermal resistances, is used to predict the average device temperatures for the different gate lengths and biases analysed. For the same bias, it is shown that the device temperature diminishes as the gate length increases, and saturates with the number of fins and fingers. With the highest electric power, the device temperature of bulk FinFETs can be 30 K lower than in the SOI case, when multiple fins and fingers are involved, keeping the current 12.3% superior. The thermal model we present could be implemented into other well-established models to be included in circuit simulators.

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Appendix

$$R_{\mathrm{ch}} = \frac{L}{k_{\mathrm{Si\text{-}fin}} h_{\mathrm{fin}} w_{\mathrm{fin}}},$$

$$R_{\mathrm{s}}\big|_{h_{\mathrm{fin}}=h_{\mathrm{pad}}} = R_{\mathrm{d}}\big|_{h_{\mathrm{fin}}=h_{\mathrm{pad}}} \approx \frac{L_{\mathrm{ext}}}{k_{\mathrm{Si\text{-}fin}} h_{\mathrm{fin}} w_{\mathrm{fin}}} + \frac{w_{\mathrm{pad}}}{k_{\mathrm{Si\text{-}pad}} h_{\mathrm{fin}} (w_{\mathrm{pad}} + w_{\mathrm{fin}})},$$

$$R_{\mathrm{ox}} = \frac{w_{\mathrm{SiO_2}}}{k_{\mathrm{SiO_2\text{-}0.8\,nm}} L(w_{\mathrm{fin}} + 2h_{\mathrm{fin}})} + \\ + \frac{h_{\mathrm{HfO_2}} w_{\mathrm{HfO_2}}}{L(k_{\mathrm{HfO_2\text{-}3\,nm}} 2h_{\mathrm{fin}} h_{\mathrm{HfO_2}} + k_{\mathrm{HfO_2\text{-}20\,nm}} w_{\mathrm{fin}} w_{\mathrm{HfO_2}})},$$

$$R_{\mathrm{gt}} \approx \frac{2w_{\mathrm{TiN}}}{k_{\mathrm{TiN}}(h_{\mathrm{TiN}} + w_{\mathrm{TiN}})L} = \frac{2w_{\mathrm{TiN}}}{k_{\mathrm{TiN}}(h_{\mathrm{fin}} + w_{\mathrm{SiO_2}} + h_{\mathrm{HfO_2}} + 2w_{\mathrm{TiN}})L},$$

$$R_{\mathrm{sp}} \approx \frac{10^{-6}}{k_{\mathrm{SiO_2}} w_{\mathrm{fin}} (h_{\mathrm{fin}} + w_{\mathrm{SiO_2}} + h_{\mathrm{HfO_2}} + w_{\mathrm{TiN}})},$$

$$R_{\mathrm{gl}} = \frac{L}{k_{\mathrm{TiN}} w_{\mathrm{TiN}} [2(h_{\mathrm{TiN}} + w_{\mathrm{SiO_2}} + w_{\mathrm{HfO_2}}) + w_{\mathrm{fin}}]},$$

$$R_{\mathrm{ch,b}} = \frac{h_{\mathrm{BOX}}}{L w_{\mathrm{fin}} k_{\mathrm{Si\text{-}fin}}},$$

$$R_{\mathrm{s,b}} = R_{\mathrm{d,b}} = \frac{h_{\mathrm{BOX}}}{(L_{\mathrm{ext}} + w_{\mathrm{pad}}) w_{\mathrm{fin}} k_{\mathrm{Si\text{-}fin}}}.$$

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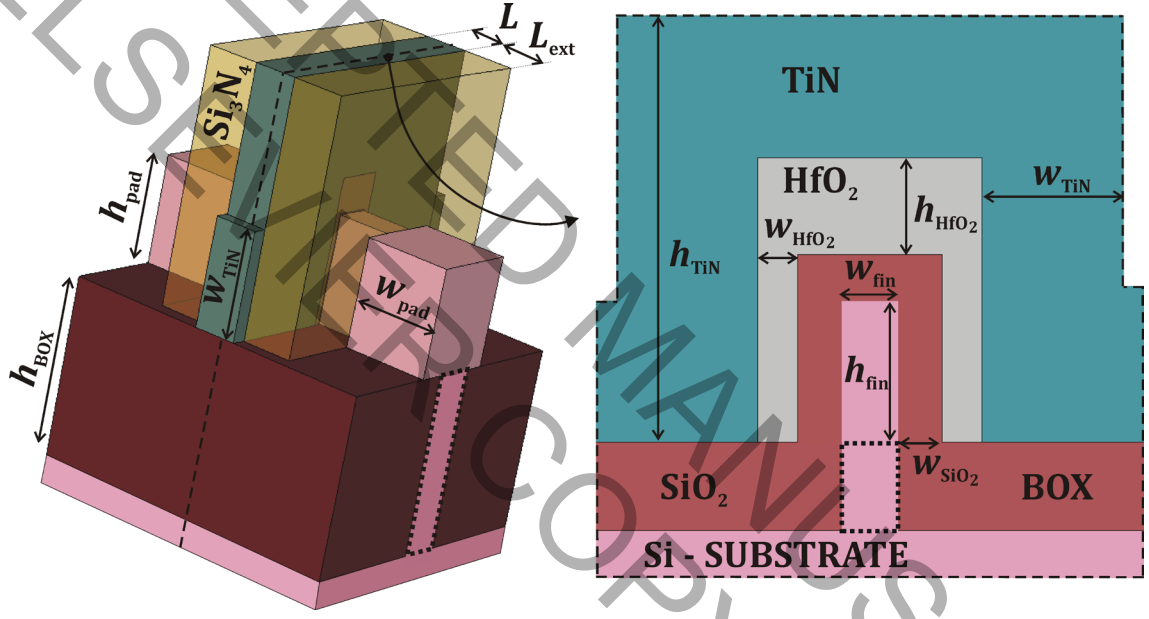
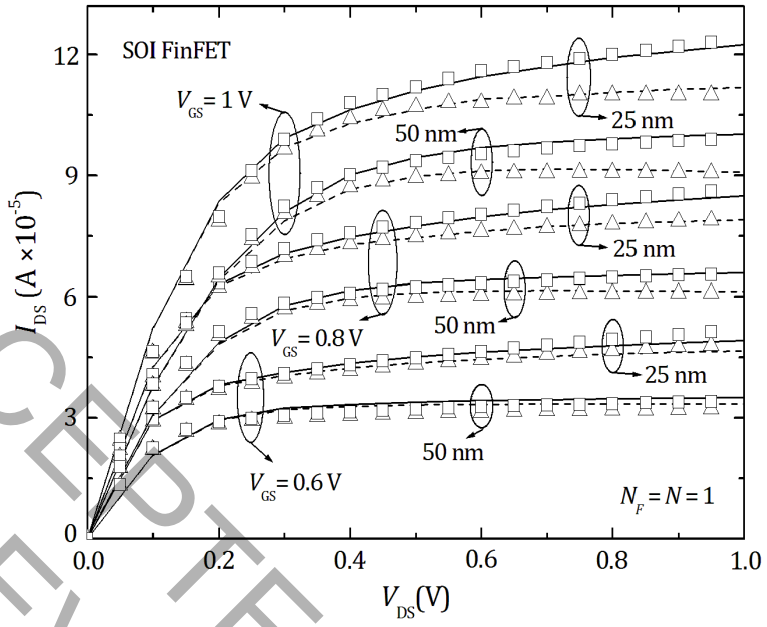
FIGURES

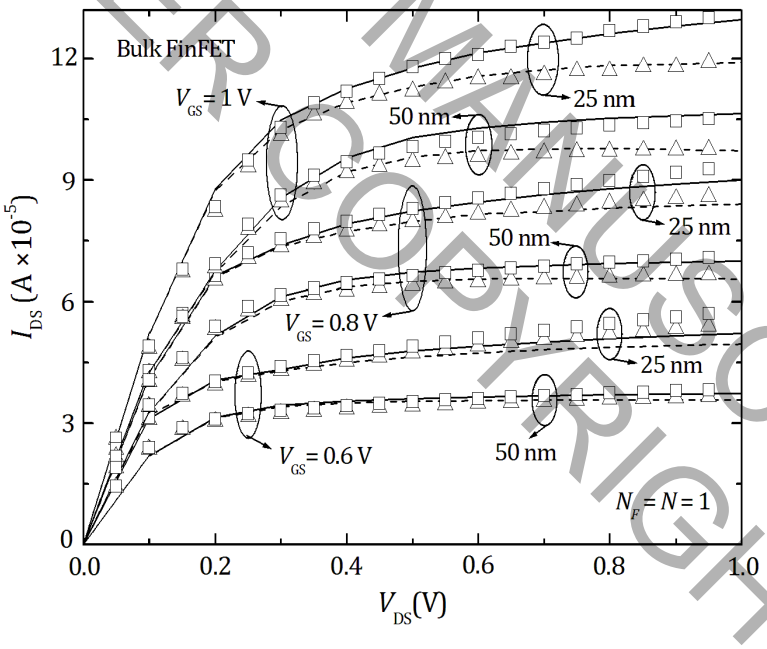


(a) (b)

Fig. 1. (a) FinFET under study: single-fin. (b) Cross-sectional view through the gate (not drawn to scale). The inactive fin added for bulk FinFETs is indicated with a dotted contour.



(a)



(b)

Fig. 2. Output characteristics for single-fin devices with L = 25 nm and 50 nm, and V_{GS} = 0.6, 0.8, and 1 V. Simulation results are shown as symbols (room-temperature results as squares and data including SHEs as triangles), and modelled data as lines (room-temperature results as solid lines and data including SHEs as dashed lines). (a) SOI FinFETs. (b) Bulk FinFETs.

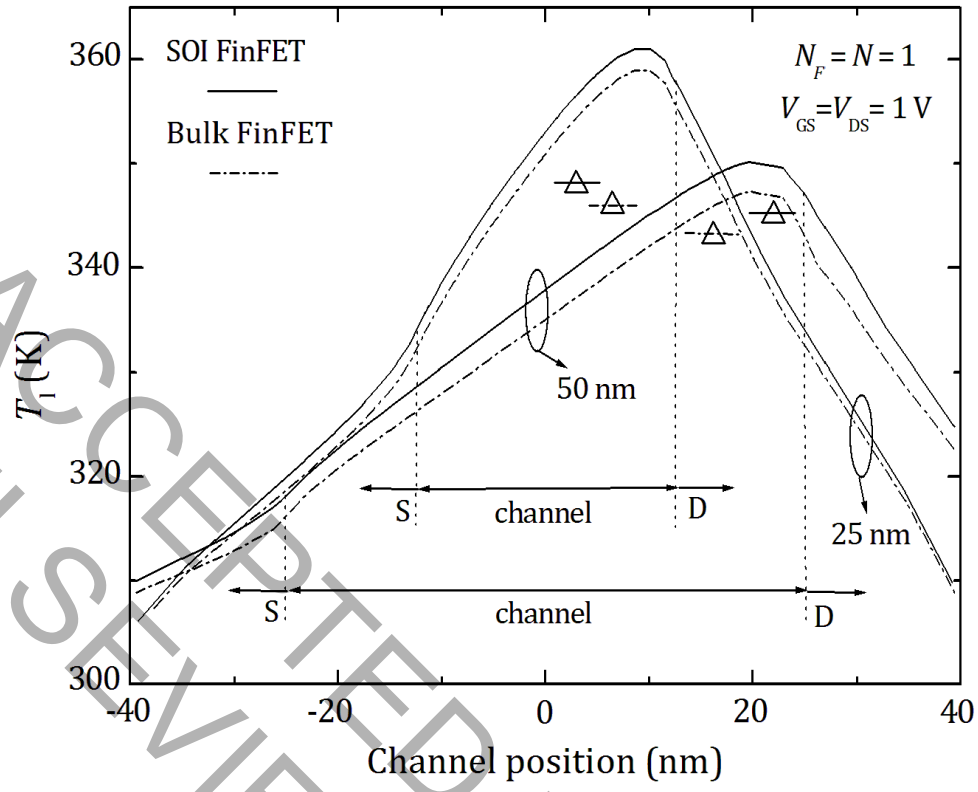


Fig. 3. Simulated local channel temperature at the top of the fin vs. position along the channel (0 nm corresponds to center of the device), for the SOI and bulk single-fin devices, is shown as solid and dashed-dotted lines, respectively, with L = 25 nm and 50 nm, and $V_{GS} = V_{DS} = 1$ V. The average channel temperature obtained using the model, accounting for SHEs, is shown as hollow triangles (the corresponding horizontal line has been added to ease the comparison with the local temperature).

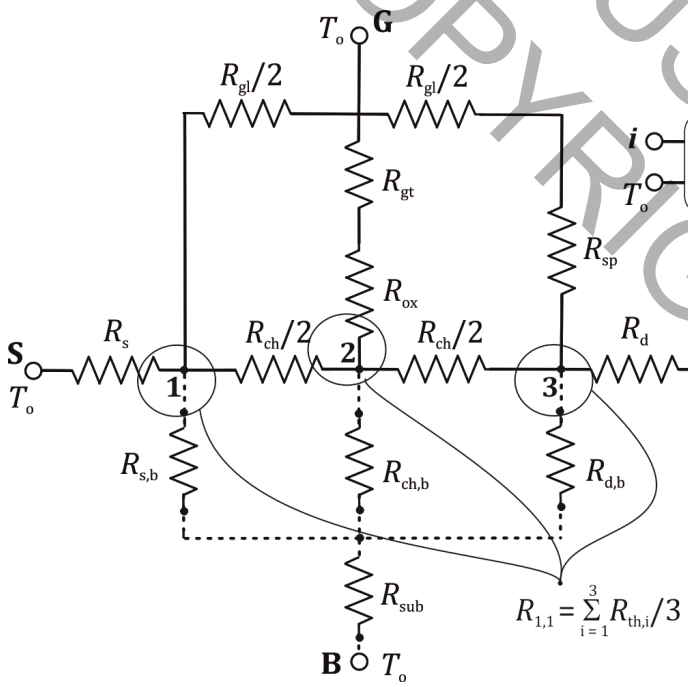


Fig. 4. Single-fin thermal circuit; dotted branches are for bulk FinFETs.

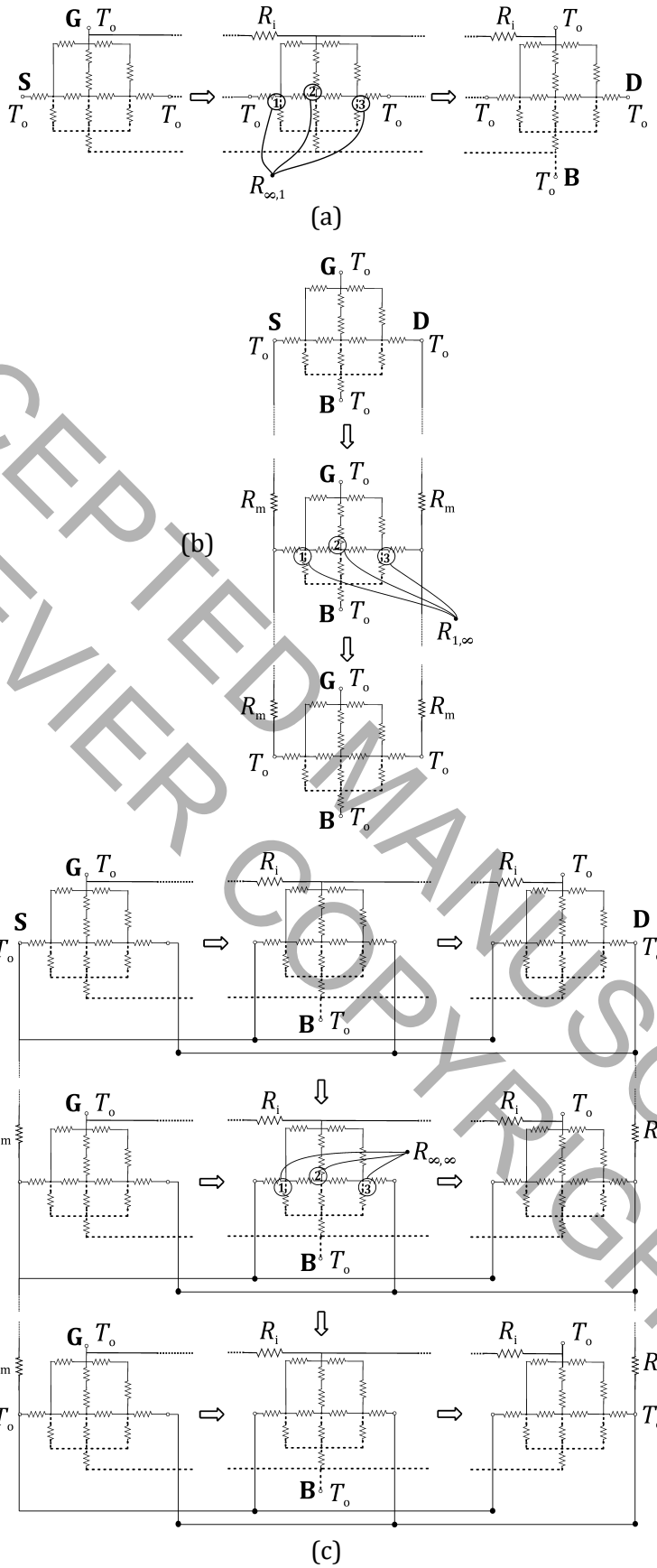


Fig. 5. Thermal circuits for: (a) Multi-fin devices with single finger (N_F = 1, N » 1). (b) Single-fin devices with multiple fingers (N_F » 1, N = 1). (c) Multi-fin devices with multiple fingers (N_F » 1, N » 1); dotted branches are for bulk FinFETs.

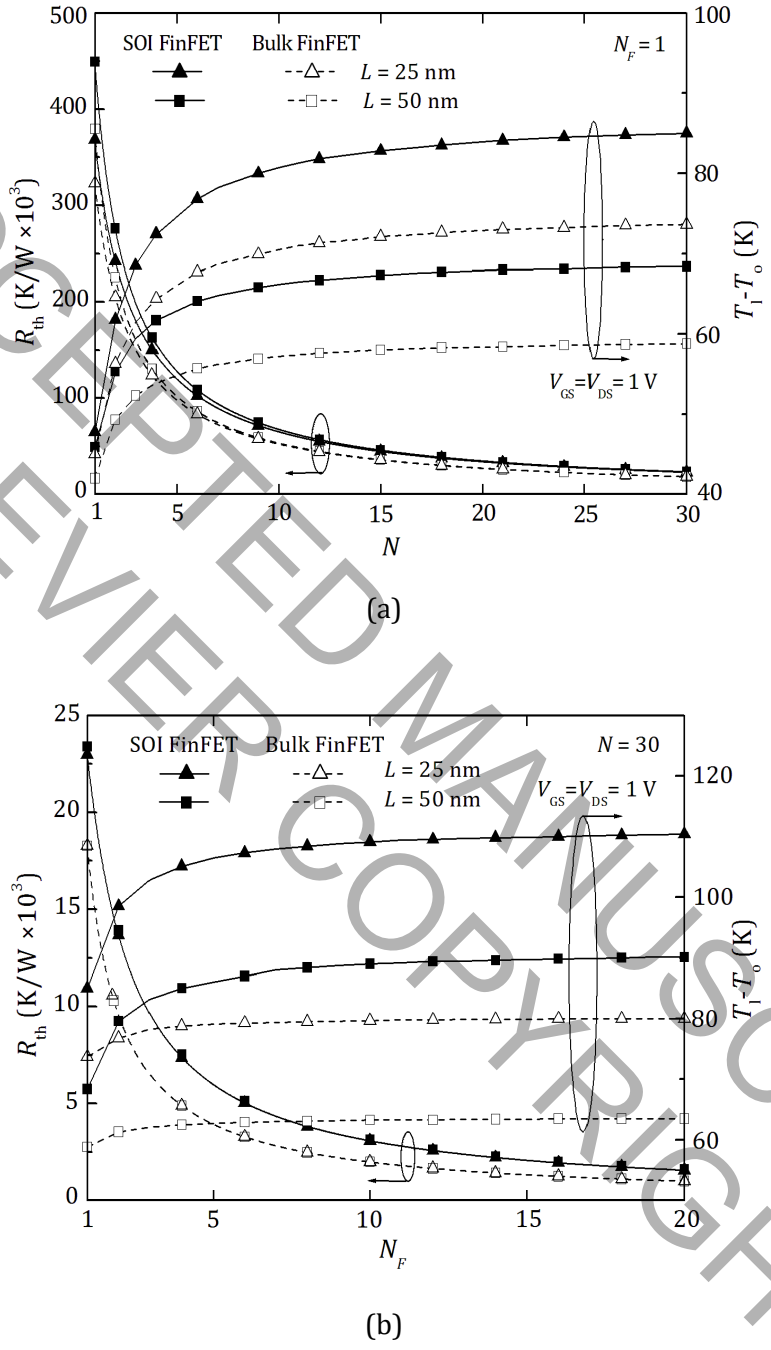


Fig. 6. Thermal resistance (left axis) and modelled temperature rise with V_{GS} = V_{DS} = 1 V (right axis) for SOI and bulk multi-fin devices are shown as solid and dashed lines, respectively, for L = 25 nm (triangles) and L = 50 nm (squares). (a) Versus number of fins for N_F = 1. (b) Versus number of fingers for N = 30 (in this case, R_{th} for L = 25 nm and 50 nm are very similar); T_o = 300 K.

TABLES

Table 1
FinFET geometrical parameters (nm).

L = 25, 50									
w_{fin}	h_{fin}	L_{ext}	w_{pad}	h_{pad}	w_{SiO_2}	w_{HfO_2}	h_{HfO_2}	w_{TiN}	h_{BOX}
20	60	30	50	60	0.8	3	20	60	100

Table 2
Thermal conductivity fitting parameters for films constituting the FinFETs.

Film	a (W/K-cm×10^{-3})	b (W/K^2-cm×10^{-5})	c (W/K^3-cm×10^{-8})
Si-fin-20 nm	279	−30	–
Si-pad-50 nm	704	−82	–
SiO_2-0.8 nm	−5.6	4.2	−4.9
SiO_2	14	–	–
HfO_2-3 nm	−2.7	2.5	−2.4
HfO_2-20 nm	8.1	–	–
Si_3N_4	4.1	9.3	−11
TiN	106	143	−276

Table 3
FinFETs' thermal resistance parameters (K/W×10^3).

	SOI		Bulk	
L (nm)	25	50	25	50
$R_{1,1}$	368	449	323	379
$R_{1,\infty}$	711	715	562	556
$R_{\infty,1}$	410	508	351	415
$R_{\infty,\infty}$	910	917	608	593