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Numerical simulation and compact modelling of AlGaN/GaN HEMTs with mitigation of self-heating effects by substrate materials

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In this paper, DC characteristics of an AlGaN/GaN on sapphire high-electron mobility transistor (HEMT) are measured, numerically simulated, and modelled accounting for self-heating effects (SHEs), with the main electrical parameters being extracted. Decomposing the transistor thermal resistance into the buffer and substrate components, our study can be easily extended to other substrate materials. Thus, sapphire is substituted with silicon, molybdenum, and SiC, which reduce current-collapse due to SHEs thanks to their considerably higher thermal conductivity, which improves transistor performance. Furthermore, we implement a compact model available for AlGaN/GaN HEMTs, incorporating the temperature dependence of extrinsic source/drain ohmic resistances, which are numerically evaluated for the different substrates.

1 Introduction The well-known advantages of GaN-based heterostructures allow electronic and optical devices to work in high temperature/frequency/power applications under saturated radiation environments [1]. However, self-heating effects (SHEs) due to the temperature rise in the 2-DEG channel heavily degrade the operation efficiency of these devices [2, 3].

Substrates with a high thermal conductivity are desirable in high-electron mobility transistors (HEMTs) [4], because most of the internal heat is spread out through the substrate [5]. Sapphire has been the main substrate used in optical GaN-based devices. However, advancements in technological manufacturing processes have allowed alternative materials, with better thermal conductivity, to be employed in the high power electrical application [6, 7]. That is why an increasing effort from the microelectronics community to model AlGaN/GaN-based HEMTs is being witnessed, paying attention to heating effects [8–12]. Proper handling of heat is a key issue in device development and in device modelling for design and manufacture. Moreover several questions on behaviour and reliability need still to be answered.

In this paper, AlGaN/GaN HEMT samples grown on sapphire are firstly considered, and their structure is described in Section 2, where the measurement methodology is also exposed, as well as the different data extracted from measurements. Furthermore, DC characteristics of the HEMTs are numerically reproduced with ATLAS (from Silvaco) and modelled in the circuit simulator ADS (from Keysight), through the industry standard modelling language for analog circuits Verilog-A, with the compact model developed in [8], incorporating the temperature dependence of source/drain ohmic contacts. The impact of the use of substrate materials–sapphire, silicon (Si), molybdenum (Mo), and SiC-on SHEs is numerically investigated and modelled in Section 3. Finally, we present our conclusions in Section 4.

2 AlGaN/GaN on sapphire HEMTs In this section we characterise, experimentally and numerically, the DC performance of AlGaN/GaN on sapphire HEMTs. Furthermore, the drain current is modelled incorporating the temperature dependence of extrinsic source/drain ohmic resistances, which are numerically evaluated.

2.1 Structure The AlGaN/GaN HEMTs structure used in this study, the layer stack which is shown in Fig. 1(a), was grown through the [0001] direction (wurtzite) on 330 μm thick sapphire. It consists of a 3 μm thick GaN buffer and a 19 nm thick $Al_{0.3}Ga_{0.7}N$ barrier, unintentionally doped. The 2-DEG concentration in the channel is modulated by a Schottky gate, which is 2 μm long and 150 μm wide.

The HEMTs layout (typical for microwave design, also valid for DC performance) is shown in Fig. 1(a). Source and drain terminals are 4 μm and 10 μm distanced, respectively, from the gate borders, with a donor concentration of $10^{20}\,cm^{-3}$ extended down to the GaN channel.

2.2 Measurements All measurements have been performed at the ISOM-UPM lab. For the *C–V* characteristics, previously to metallization processing, a mercury microprobe with an area of $4.24\times10^{-3}\,cm^2$ and the HP41992A-LF multi-frequency capacitance measurement unit were used. Measured capacitances at 50 kHz for gate biases, V_{gs}, ranging from –6 V to 0 V, are shown with crosses in Fig. 2. The corresponding electron concentration profile, n, evaluated as $n=(C^3/q)\cdot dV/dC$ [13], is also represented in Fig. 2 with crosses; when n is integrated over depth, a $1.2\times10^{13}\,cm^{-2}$ 2-DEG concentration results.

DC characteristics have been measured within a KARL-SUSS probe station, with DC parametric probes and the HP4145B semiconductor device analyser. Output characteristics, with the drain to source voltage, V_{ds}, up to 15 V, are shown in Fig. 3 for –2 V, –1 V, and 0 V gate biases. Notice

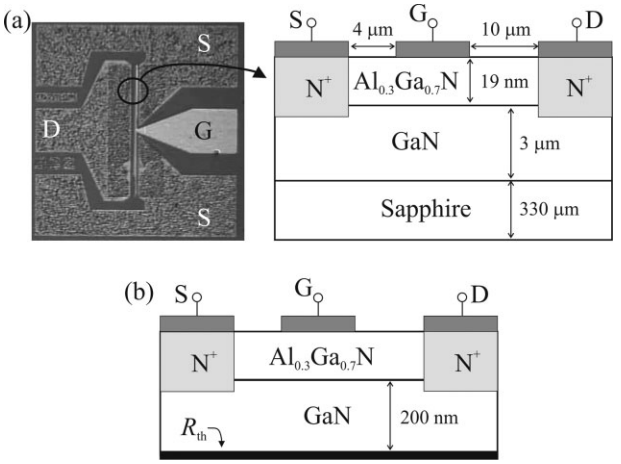

Figure 1 (a) AlGaN/GaN on sapphire HEMTs structure (not to scale). (b) Equivalent thermal resistance, R_{th}, at the bottom of the structure.

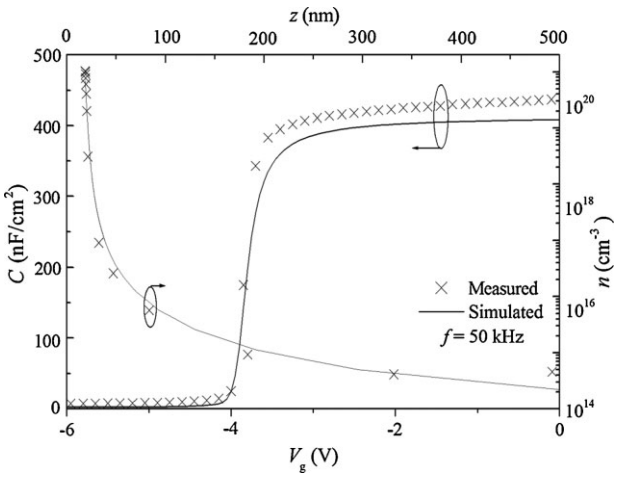

Figure 2 *C–V* characteristics (left axis) and electron profile against the depth from the AlGaN top surface (right axis). Measured and simulated data are represented with crosses and solid lines, respectively.

the current-collapse due to SHEs for high current levels and that the knee voltage is less than 4.0 V, which shows the excellent nature of the ohmic contacts.

Furthermore, pinch-off characteristics are appropriate with a threshold voltage of –3 V, obtained from the measured transfer characteristics in linear region as the gate bias intercept of the extrapolation of drain current, at the point of the maximum transconductance (8.3 mS/mm for $V_{ds}=0.1$ V) [14].

2.3 Numerical simulation Numerical simulations have been performed with ATLAS [15]. First, in order to reproduce the DC HEMTs response, the electron profile

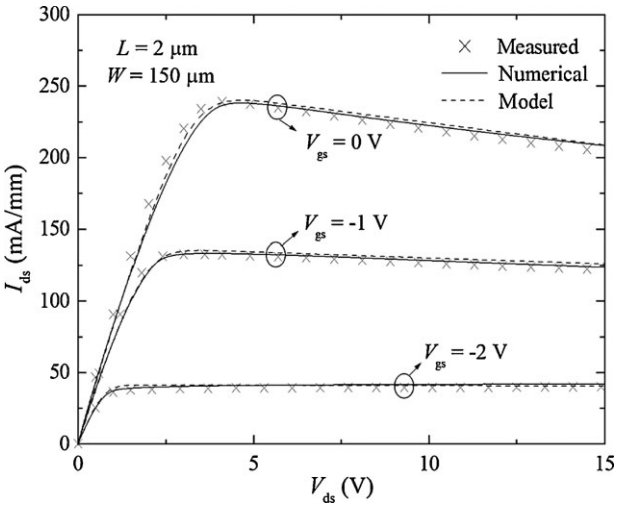

Figure 3 Sapphire HEMTs output characteristics. Measured, simulated and modelled data are represented with crosses, solid lines and dashed lines, respectively; $V_{gs}=-2$, –1 and 0 V.

through heterojunctions must be established. For that purpose, accounting for the piezoelectric and spontaneous polarizations, as in [16], the measured *C–V* characteristics are fitted as shown in Fig. 2 with a solid line, incorporating $10^{18}\,\mathrm{cm}^{-3}$ and $10^{14}\,\mathrm{cm}^{-3}$ N-type doping concentration in the barrier and buffer layers, respectively, and establishing a work function of 5.7 eV for the Schottky gate.

From the different trapping effects, dislocations, or surface states which could alter the transistor DC response, the most relevant are the ones located at the free AlGaN surface [17]. Thus, we found that assuming an 86% of the ideal polarisation charge at the free AlGaN surface, the total polarisation charge at the AlGaN/GaN heterojunction can be incorporated and a proper electron concentration profile in buffer under the gate, represented in Fig. 2 with a solid line, results.

The resulting simulated electron concentration profile after integration, predicts a $10^{13}\,\mathrm{cm}^{-2}$ 2-DEG concentration, which is slightly inferior to that obtained from measurements, but high enough for numerical simulation purposes [18]. The electron concentration deviation observed deep in the buffer (see Fig. 2), can then be attributed to AlN interlayers and/or traps not incorporated in this work [17], which have a little or even negligible impact on DC characteristics. Fully quantifying all these contributions is still an open problem in the literature.

Thus, DC characteristics are considered next as in GaAs-based HEMTs [19–22], excluding thermionic field emission modelling at the interface between the barrier and buffer layers, to avoid numerical divergence.

In our AlGaN/GaN HEMTs, the gate length (2 μm) is long enough for using a drift–diffusion scheme [19]. Furthermore, we select the following nitride specific field dependent mobility model [15, 20], with appropriate negative differential mobility due inter-valley transfer at high electric fields [21]

$$\mu = \frac{\mu_0 + v_{\mathrm{sat}} \dfrac{\varepsilon^{n_1-1}}{\varepsilon_{\mathrm{c}}^{n_1}}}{1 + \xi\left(\dfrac{\varepsilon}{\varepsilon_{\mathrm{c}}}\right)^{n_2} + \left(\dfrac{\varepsilon}{\varepsilon_{\mathrm{c}}}\right)^{n_1}}, \tag{1}$$

where ε represents the electric field (ε_{c} being the critical field [11], which is nearly the electric field of the peak of the velocity after the fitting procedure [23]), v_{sat} is the saturation velocity, n_1, n_2 and ξ are extracted parameters from Monte Carlo data in [20], and μ_0 stands for the low-field electron mobility, which is temperature dependent as follows:

$$\mu_{\mathrm{o}} = \mu_{\max}\left(\frac{T_{\mathrm{l}}}{300}\right)^{-\alpha}, \tag{2}$$

with T_{l} representing the lattice temperature, and $\mu_{\max}$ the low-field electron mobility at room temperature, $T_{\mathrm{l}} = 300\,\mathrm{K}$; α models the lattice temperature degradation of μ_0.

The mobility parameters (with the exception of $\mu_{\max}$) are the ones used by default in ATLAS [15], being material composition dependent in the case of $Al_{0.3}Ga_{0.7}N$; values for $\mu_{\max}$ reported in [17], where our measured HEMTs were also investigated, are consistent with the nature of the barrier and the 2-DEG channel. It has been possible to incorporate these values in numerical simulations by making use of the 86% assumption of the ideal polarisation charge at the free AlGaN surface. All mobility parameters, for the $Al_{0.3}Ga_{0.7}N$ barrier and GaN buffer, are summarised in Table 1.

Self-heating is well known to affect device performance in high power conditions (i.e., our case). As mentioned previously, in the case of HEMTs most of the heat is spread down from the channel towards the substrate [24, 25]. Therefore, for numerical simulation purposes, the substrate and nearly the entire GaN buffer (except a necessary region to establish the 2-DEG channel) can be substituted by an equivalent thermal resistance, R_{th}, as Fig. 1(b) shows, at the bottom of the simulated structure.

An 18×10^3 K/W μm normalised thermal resistance is derived for the sapphire HEMTs, from the temperature rise per watt measured in [26] with similar devices. As our HEMT is 150 μm wide, its thermal resistance, $R_{\text{th-sapphire}}$, equals 120 K/W.

Figure 3 shows the resulting simulated output characteristics (with solid lines) obtained for our HEMTs, with the gate biases considered, showing a 9.1% maximum relative error with respect to measured data (for $V_{\mathrm{gs}} = 0\,\mathrm{V}$); on average, the global relative error is only 3%.

2.4 Compact modelling The drain current of the AlGaN/GaN on sapphire HEMTs is modelled using the simple compact analytical model presented in [8], based on semiconductor physics. This compact model is developed from a unified charge control model, obtained from the band structure in the potential well, by considering the contribution of only the first energy level (assuming a triangular potential well), where a considerable part of the 2-DEG is located. This assumption allows the establishment of a simple relationship between the applied voltage and the charge carrier concentration, which in turn results in a simple analytical model for the drain current, while maintaining a good level of accuracy.

The contribution of the first energy level in the triangular quantum well, at the AlGaN/GaN interface, results in the following accurate and simple unified charge control model for the electron density, n, in the 2-DEG:

Table 1 Mobility parameters for the GaN buffer and $Al_{0.3}Ga_{0.7}N$ barrier.

	GaN	$Al_{0.3}Ga_{0.7}N$
v_{sat} (10^7 cm/s K)	1.91	1.12
ε_{c} (kV/cm)	221	365
n_1	7.20	5.32
n_2	0.79	1.04
ξ	6.20	3.23
$\mu_{\max}$ (cm^2/V s)	950	100
α	1.5	1.5

$$n = DV_{\mathrm{th}} \ln\left[\exp\left(\frac{E_{\mathrm{F}} - E_0}{V_{\mathrm{th}}}\right) + 1\right], \tag{3}$$

where D stands for the density of states, V_{th} is the thermal voltage, E_{F} represents the Fermi level and E_0 is the position of the first energy level in the quantum well. Based on this, the drain current covering all the different operating regimes is given by

$$I_{\mathrm{ds}} = -\frac{q\mu_0 W}{L}\left[\frac{qd}{2\varepsilon}\left(n_{\mathrm{D}}^2 - n_{\mathrm{S}}^2\right) + \frac{2}{5}\gamma_0\left(n_{\mathrm{D}}^{5/3} - n_{\mathrm{S}}^{5/3}\right) + V_{\mathrm{th}}\left(n_{\mathrm{D}} - n_{\mathrm{S}}\right)\right], \tag{4}$$

with n_{S} and n_{D} being the electron density in the 2-DEG at the source and drain terminals, respectively, W is the transistor width, L the channel length, ε is the dielectric permittivity of the barrier layer, d thickness, q represents the absolute electron charge and γ_0 is a fitting parameter.

The compact model accounts for the 2-DEG channel current, including channel length modulation and short channel effects [8]. Therefore, model parameters for the low-field electron mobility are those used for GaN in numerical simulations.

However, in order to predict the current collapse in the saturation regime, the modelled saturation velocity, $v_{\mathrm{sat}}^{\mathrm{m}}$, which modulates the saturation drain voltage as $V_{\mathrm{sat}} = v_{\mathrm{sat}}^{\mathrm{m}} V_{\mathrm{go}} / (v_{\mathrm{sat}}^{\mathrm{m}} + (\mu_0/2L)V_{\mathrm{go}})$ (see [8] for more details), incorporates the usual lattice temperature linear degradation [15] as follows:

$$v_{\mathrm{sat}}^{\mathrm{m}} = v_{\mathrm{sat,o}} - v_{\mathrm{sat,d}}(T_{\mathrm{l}}/300), \tag{5}$$

with $v_{\mathrm{sat,0}}$ and $v_{\mathrm{sat,d}}$ being fitting parameters (1.19×10^5 cm/s and 4.3×10^4 cm/s, respectively). It can be mentioned, also, the fact that $v_{\mathrm{sat,d}}$ accounts for the probably influence of the parasitic MESFET that appears in the device for $V_{\mathrm{gs}} = 0$ V, which also helps in reducing the current collapse in the saturation regime.

The modelled temperature is being obtained iteratively as $<T_{\mathrm{l}}>_{i+1} = 300 + R_{\mathrm{th}} I_{\mathrm{ds}}(<T_{\mathrm{l}}>_i) \cdot V_{\mathrm{ds}}$ ($i = 1, 2, 3, \ldots$), with R_{th} being the HEMT thermal resistance; for each iteration the new temperature is calculated with Eq. (4), wherein I_{ds} is evaluated with the lattice temperature of the previous iteration. The process is repeated until convergence is achieved, with the mobility Eq. (2), saturation velocity Eq. (5) and (through the thermal voltage) inversion charge Eq. (3) temperature dependences.

Extrinsic source/drain ohmic resistances, R_{s} and R_{d}, are decisive for the DC performance evaluation of HEMTs. If the device temperature is raised, the electron mobility in the channel degrades [6], and a proportional increase in channel resistance, related to the source/drain resistances, is expected. Thus, the voltage drop in R_{s} and R_{d} modifies, respectively, the source-gate and gate-drain potentials, in a way that the conductive path for electrons is being pinched off. Consequently, the saturation drain current is reduced.

We have extracted from numerical data the temperature increment dependence of source/drain ohmic resistances in sapphire HEMTs, which is represented in Fig. 4 with squares. A second-order polynomial is enough to fit this dependence (represented in Fig. 4 with solid lines), that is $R_{\mathrm{s,d}} \cong a + b<\Delta T_{\mathrm{l}}> + c<\Delta T_{\mathrm{l}}>^2$, where $<\Delta T_{\mathrm{l}}>$ stands for the average channel temperature increment for the compact model; fitting parameters, a, b and c, for sapphire HEMTs are indicated in Table 2.

Introducing the temperature dependent source/drain ohmic resistances in the compact model (drain to source voltage is $I_{\mathrm{ds}}(R_{\mathrm{s}} + R_{\mathrm{d}})$ reduced, and gate to source voltage is $I_{\mathrm{ds}}R_{\mathrm{s}}$ risen), we obtain the modelled output characteristics of Fig. 3 (with dashed lines), showing a 5.3% maximum relative error with respect to measured data (for $V_{\mathrm{gs}} = 0$ V); on average, the global relative error is only 3.7%.

3 Mitigation of SHEs varying substrate materials Once numerical simulations and modelling of the sapphire HEMTs DC characteristics have been successfully validated, the impact of SHEs, when the substrate material is varied, is analysed with ATLAS as follows. For that purpose, technological dependent parasitic effects such as trapping, dislocations, or surface states, are assumed to contribute similarly to the measured HEMTs for deriving similar 2-DEG concentration, threshold voltage, and (temperature dependent) electron mobility in buffer and barrier layers. In our case this includes the use of similar passivation layers on top of the barrier, and similar terminal layout.

3.1 Device thermal resistance In relation to the device thermal resistances, two different strategies are usually employed to evaluate them: a thermal circuit

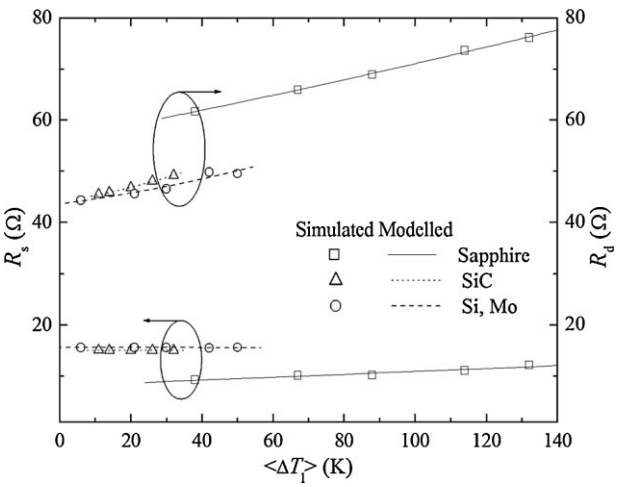

Figure 4 R_{s} (left axis) and R_{d} (right axis) against average channel temperature increment for sapphire, SiC and Si or Mo substrates (Si and Mo data are fully overlapped). Numerical data are represented with squares, triangles and circles, and modelled data with solid, dotted and dashed lines, respectively.

Table 2 Fitting parameters for R_s and R_d with substrates.

	sapphire		Si/Mo		SiC	
	R_s	R_d	R_s	R_d	R_s	R_d
a (Ω)	8.1	56.4	15.6	43.6	15	44
b (Ω/K)	0.03	0.13	0	0.09	0	0.11
c (Ω/K^2)	–	1.4×10^{-4}	–	7.8×10^{-4}	–	1.7×10^{-3}

approach [9, 12], or a simple fitting parameter to reproduce SHEs [8]. We propose a new physics-based but simple methodology to estimate substrate thermal resistance, and its contribution to the global device thermal resistance, as follows.

When sapphire is substituted with Si in the measured HEMTs, with identical thickness, the device thermal resistance, $R_{th\text{-}Si}$, is reduced by a quarter [26], resulting in 30 K/W. Then, accounting for the particular contribution of buffer and substrate layers, $R_{th\text{-}sapphire}$ and $R_{th\text{-}Si}$ can be expressed as

$$\begin{aligned} R_{th-sapphire} &\approx R_{GaN} + R_{sapphire} \\ R_{th-Si} &\approx R_{GaN} + R_{Si} \end{aligned}, \tag{6}$$

with R_{GaN}, $R_{sapphire}$ and R_{Si} standing for the constituting thermal resistance of the GaN buffer, sapphire substrate, and Si substrate, respectively. Then, solving (6) with $R_{sapphire} \approx k_{Si\text{-}300}R_{Si}/k_{sapphire\text{-}300}$ ($k_{sapphire\text{-}300}$ and $k_{Si\text{-}300}$ being the sapphire and Si thermal conductivities at room temperature, 0.24 W/cm K and 1.48 W/cm K, respectively), the following is obtained:

$$\begin{aligned} R_{Si} &\approx \frac{(R_{th-sapphire} - R_{th-Si})k_{sapphire-300}}{k_{Si-300} - k_{sapphire-300}} \\ &= 17.4\,\mathrm{K/W}, \end{aligned} \tag{7}$$

$R_{sapphire} \approx R_{Si}k_{Si\text{-}300}/k_{sapphire\text{-}300} = 107.4$ K/W, and $R_{GaN} \approx 30 - R_{Si} = 12.6$ K/W.

For Mo substrate, with elemental thermal resistance $R_{Mo} \approx R_{Si}k_{Si\text{-}300}/k_{Mo\text{-}300} \approx 18.7$ K/W ($k_{Mo\text{-}300}$ being the Mo thermal conductivity at room temperature, 1.38 W/cm K), the device thermal resistance results $R_{th\text{-}Mo} \approx R_{GaN} + R_{Mo} = 31.3$ K/W, which is nearly $R_{th\text{-}Si}$. Therefore, similar degradation by SHEs is expected with Si and Mo substrates, in both cases much lower than for the sapphire substrate.

In a similar way, for SiC substrate the device thermal resistance is $R_{th\text{-}SiC} \approx 20$ K/W (with a SiC thermal conductivity at room temperature, $k_{SiC\text{-}300}$, of 3.5 W/cm K) [27].

3.2 DC numerical performance By employing the corresponding device thermal resistance, we obtain the numerical output characteristics of Fig. 5 for sapphire (with squares), SiC (with triangles) and Si or Mo (they overlap, with circles) substrates, for null gate bias to enhance SHEs, and the corresponding average channel temperature increment (within closed symbols), $<\Delta T_l>$.

The resulting device peak temperature, $T_{l,max}$, and the maximum average channel temperature, $<T_l>_{max}$, with $V_{ds} = 15$ V, are indicated in Table 3, where the maximum drain current density, $I_{ds,max}/W$, with higher drain biases for higher substrate thermal conductivities, is also exposed.

As expected, for Si, Mo and SiC substrates the current-collapse by self-heating is alleviated, with the maximum drain current density being around 10.9% superior to that for sapphire.

With Si or Mo the peak temperature and the corresponding average channel temperature are, respectively, 24 K and 25 K higher than with SiC, and 86 K and 78 K lower than with sapphire.

On the other hand, from numerical transfer characteristics the transconductance in the saturation region, g_m, with $V_{ds} = 15$ V and $V_{gs} = 0$ V, is also indicated in Table 3. Notice that g_m degrades significantly with sapphire, being around 33 mS/mm lower than with the rest of substrates.

Finally, it can be pointed out that for each substrate material considered self-heating degradation enhances

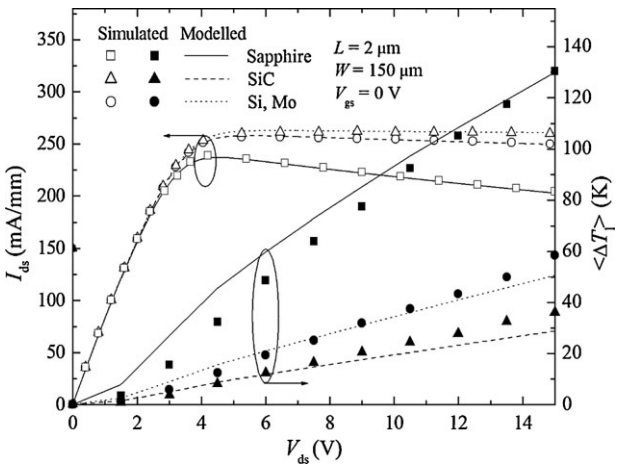

Figure 5 Output characteristics (left axis) and $<\Delta T_l>$ (right axis) vs. drain voltage for sapphire, SiC and Si or Mo substrates (Si and Mo data are fully overlapped). Numerical data are represented with squares, triangles and circles, and modelled data with solid, dotted and dashed lines, respectively; $V_{gs} = 0$ V.

Table 3 DC numerical performance parameters with substrates.

substrate	$T_{l,max}$ (K)	$<T_l>_{max}$ (K)	$I_{ds,max}/W$ (mA/mm)	g_m (mS/mm)
sapphire	467	435	239	86
Si/Mo	381	357	262	118
SiC	357	332	267	120

considerably with multi-finger layout devices aiming at very high power operation. This problem could be alleviated with appropriate metallisation and form of the terminals, trying to enhance additional heat flow paths, mainly through the gate and drain contacts. These topics will be investigated in future studies. Nevertheless they underline the importance of using appropriate substrates and assessing their limits.

3.3 Compact modelling The temperature increment dependency of extrinsic source/drain ohmic resistances with the substrates under study is determined as in Section 2.4, with sapphire. In Fig. 4, numerical data for SiC (with triangles) and Si or Mo (they overlap, with circles) are incorporated with those previously reported for sapphire. For the corresponding quadratic approximation of R_s and R_d (with the parameters of Table 2), dotted and dashed lines are used.

With all substrates the drain resistance is higher than the source resistance, particularly with sapphire, and increases with the average channel temperature (this dependence enhances also with sapphire). However, in comparison, the source resistances are practically constant. Thus, we are accounting for the particular contribution of terminals, source and drain, to the total extrinsic parasitic resistance, which is a more precise strategy than the one employed in [26], where R_s was extrapolated from the functional dependence of the source-drain resistance divided by 2 in a linear regime.

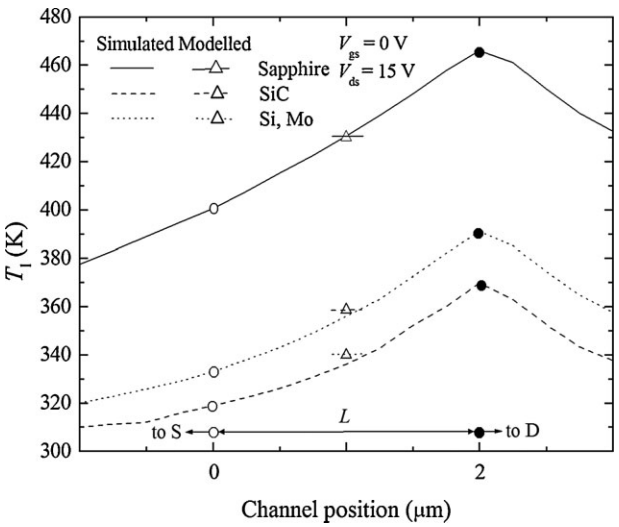

Figure 6 Simulated local channel temperature vs. channel position along the longitudinal direction, for the different substrates, is shown in lines. Circles represent the location of the borders of the gate, being solid at the drain side of the gate. The average channel temperature obtained with the model, accounting for SHEs, is shown by hollow triangles (a horizontal line has been added in this case to ease the comparison with the local temperature); $V_{gs} = 0$ V and $V_{ds} = 15$ V.

Our compact model has a universal application for GaN-based HEMTs (with different geometries, material compositions and substrates), which has been demonstrated in [12, 28, 29], where measured output characteristics for different HEMTs were reproduced. Thus, incorporating the source/drain ohmic resistances with substrates into the compact model, we obtain the modelled output characteristics and the corresponding modelled temperature increment of Fig. 5 for sapphire (with solid line), SiC (with dotted line) and Si or Mo (they overlap with dashed line). The modelled drain current shows a 7.3% maximum relative error (for sapphire) with respect to numerical data; on average, the global relative error is 1.6%. On the other hand, the modelled temperature shows a 4% maximum relative error (for sapphire) with respect to numerical data; on average, the global relative error is 1.3%. Furthermore, the modelled temperature increment shows values according to those experimentally derived in [26] with sapphire and Si, and a similar drain to source voltage linear dependency to the one numerically observed in [30] with sapphire and SiC, with values according to that modelled in [11].

We have also compared, for the sake of coherence, the simulated local temperature from source to drain in the intrinsic channel (see Fig. 6, where the horizontal position at the borders of the gate is shown with circles, which are solid by the drain side, and $V_{gs} = 0$ V and $V_{ds} = 15$ V to maximize SHEs) with the modelled temperature, $<T_l>$, which is plotted with hollow triangles. We found similar values for every substrate, within a relative error lower than 9%. In all cases the peak temperature takes place at the end of the channel, by the drain side, which is in accordance with [24, 25]. Furthermore, as expected, the average channel temperature decreases when the thermal resistance diminishes and, consequently, so does the thermal dissipated power (the drain current rises).

4 Conclusions A simple methodology to evaluate the thermal resistance of GaN-based HEMTs, when varying the substrate material, has been presented. Once DC measured characteristics of GaN-on-sapphire HEMTs are numerically set up, the impact of SHEs on the device performance when sapphire is substituted with Si, Mo or SiC is simulated. The expected degradation on drain current and transconductance as the substrate thermal conductivity diminishes has been confirmed and quantified, recognising the importance of using a suitable substrate for the manufacture of GaN-based HEMTs. In addition to this analysis, the temperature dependence of extrinsic source/drain ohmic contacts has been extracted numerically and implemented in a compact

model with SHEs, reproducing successfully the numerical output characteristics for the substrates under study (within a 7.3% relative error), which is key in making accurate and reliable design kits available. Ongoing work deals with patterned and engineered substrates, using graded buffers and transferred and bonded layers, with multi-finger layout devices.

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