

Research Article

Large-Signal DG-MOSFET Modelling for RFID Rectification

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This paper analyses the undoped DG-MOSFETs capability for the operation of rectifiers for RFIDs and Wireless Power Transmission (WPT) at microwave frequencies. For this purpose, a large-signal compact model has been developed and implemented in Verilog-A. The model has been numerically validated with a device simulator (Sentaurus). It is found that the number of stages to achieve the optimal rectifier performance is inferior to that required with conventional MOSFETs. In addition, the DC output voltage could be incremented with the use of appropriate mid-gap metals for the gate, as TiN. Minor impact of short channel effects (SCEs) on rectification is also pointed out.

1. Introduction

Nowadays, SOI technology offers wafers with thin and uniformly distributed oxide layers, exhibiting excellent electrical insulation and very high quality silicon/oxide interfaces. These properties encourage the design of different multiple-gate devices [1–4] and development of compact models to account for their performance [5–7]. However, there is a lack of papers on applications with this type of transistors. The aim of this work, based on electrical simulations, is to demonstrate the feasibility of using Double Gate MOSFETs (DG-MOSFETs) in rectifier circuits for RFIDs and Wireless Power Transmission (WPT) applications [8, 9] at microwave frequencies. The application of this technology for rectifier circuits has not yet been reported elsewhere, as far as we know.

The topology of the rectifier under consideration is shown in Figure 1, where two n -channel transistors, acting as charge pump, are connected [10]. The rectifier converts RF input to DC output power, as Figure 2 indicates. Gate and drain interconnections force transistors to operate in saturation or cut-off regimes. Thus, when the RF input signal, V_{RF} , is in its negative half cycle, with $|V_{RF}| > V_{th} > 0$ and V_{th} being

the threshold voltage, the drain current of transistor DG-M1, I_{ds1} , flows from ground to the coupling capacitor, with $C_c = 1$ pF, and transistor DG-M2 remains off. Conversely, in the positive half cycle, with $V_{RF} > V_{th}$, DG-M2 turns on, flowing its current, I_{ds2} , from the input terminal to the smoothing capacitor, with $C_s = 1$ pF, with DG-M1 remaining off. In another case, both currents, I_{ds1} and I_{ds2} , are null. This process is repeated until the steady state is reached, when a DC output voltage is generated [10].

When DG-M2 switches off, C_s can be discharged through load resistance, causing output ripples. In our study, we will assume a 10 k Ω output load to compare our results with those reported in [11].

The structure of this paper is as follows. In Section 2, the compact model implemented in the large-signal equivalent circuit is presented, including intrinsic capacitance for DG-MOSFETs. Section 3 is devoted to analyse the rectifier performance, which is validated through numerical simulations with Sentaurus [12]. Technological and design aspects, as the use of different gate metal and number of stages, are also analysed in this section. Finally, some conclusions are exposed in Section 4.

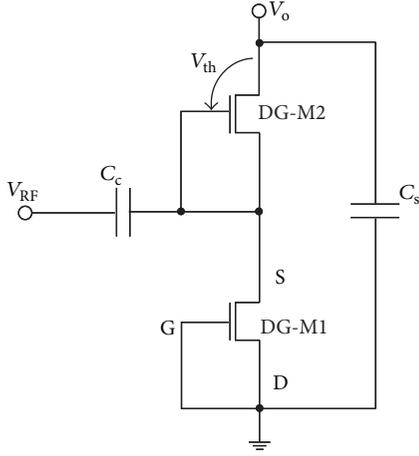


FIGURE 1: Schematic of the rectifier.

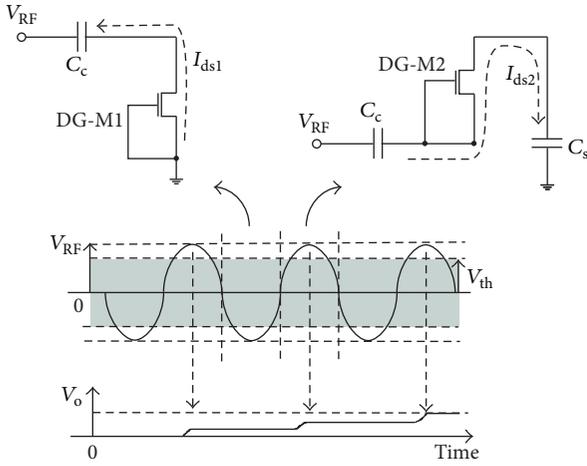


FIGURE 2: Rectification mechanism.

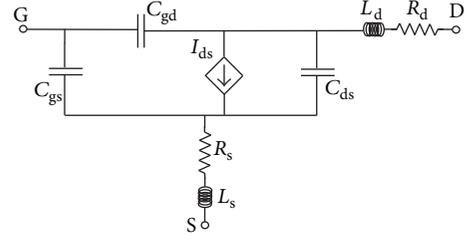


FIGURE 3: DG-MOSFET large-signal equivalent circuit.

2. Large-Signal Equivalent Circuit

The large-signal equivalent circuit proposed for the undoped DG-MOSFETs, with pads, is shown in Figure 3 [13]. It is composed by the intrinsic current, I_{ds} , and capacitance from gate-to-source, C_{gs} , gate-to-drain, C_{gd} , and drain-to-source, C_{ds} , and extrinsic source and drain resistances, $R_s = R_d = 0.32 \Omega$, and the extrinsic inductances, $L_s = L_d = 10^{-13} \text{ H}$.

The intrinsic current, based on the charge control model in [6], is given by

$$I_{ds} = \frac{W\mu}{L} \left[2\beta(Q_s - Q_d) + \frac{Q_s^2 - Q_d^2}{4C_{ox}} + 8\beta^2 C_{Si} \ln \left(\frac{Q_d + 2Q_o}{Q_s + 2Q_o} \right) \right], \quad (1)$$

with the inversion charge, Q , being evaluated as

$$Q = 2C_{ox} \left\{ -\frac{2C_{ox}\beta^2}{Q_o} + \sqrt{\left(\frac{2C_{ox}\beta^2}{Q_o} \right)^2 + 4\beta^2 \ln^2 \left[1 + \exp \left(\frac{V_{gs} - V_{th} + \Delta V_{th} - V}{2\beta} \right) \right]} \right\}, \quad (2)$$

where β is the thermal voltage, $Q_o = 4\beta C_{Si} (C_{Si} = \epsilon_{Si}/t_{Si})$, $C_{ox} = \epsilon_{SiO_2}/t_{ox}$, $Q_s = Q (V = 0)$, and $Q_d = Q (V = V_{ds})$, with V_{th} and ΔV_{th} (to assure the correct behaviour of Q above threshold) as in [5].

For DG-M1 and DG-M2, a constant mobility, $\mu = 300 \text{ cmV}^{-1}\text{s}^{-1}$, is assumed, and the gate length, L , and gate width, W , are set to $0.18 \mu\text{m}$ and $3.6 \mu\text{m}$, respectively, with a gate oxide thickness of $t_{ox} = 2 \text{ nm}$, n^+ polysilicon gate, and $t_{Si} = 20 \text{ nm}$ for the thickness of the nonintentionally doped silicon layer.

Setting the gate-to-drain bias voltage, V_{gd} , the gate-to-source capacitance can be obtained as

$$C_{gs} = \left. \frac{dQ_{Tot}}{dV_{gs}} \right|_{V_{gd}}$$

$$= \left(\frac{dQ_{Tot}}{dQ_s} + \frac{dQ_{Tot}}{dI_{ds}} \cdot \frac{dI_{ds}}{dQ_s} \right) \cdot \left. \frac{dQ_s}{dV_{gs}} \right|_{V_{gd}}, \quad (3)$$

where Q_{Tot} is the total channel charge in [6] and

$$\frac{dQ_{Tot}}{dQ_s} = \frac{W^2\mu}{I_{ds}} \cdot \left(\frac{Q_s^2}{2C_{ox}} + \beta Q_s + \frac{\beta Q_s^2}{Q_s + 2Q_o} \right), \quad (4)$$

$$\frac{dI_{ds}}{dQ_s} = \frac{W\mu}{L} \cdot \left(2\beta + \frac{Q_s}{2C_{ox}} - \frac{8\beta^2 C_{Si}}{Q_s + 2Q_o} \right), \quad (5)$$

$$\frac{dQ_s}{dV_{gs}} = \frac{1}{1/2C_{ox} + \beta(1/Q_s + 1/(Q_s + 2Q_o))}. \quad (6)$$

Substituting (4)–(6) in (3), with $dQ_{\text{Tot}}/dI_{\text{ds}} = -Q_{\text{Tot}}/I_{\text{ds}}$, C_{gs} , finally results in

$$C_{\text{gs}} = \frac{(W^2\mu/I_{\text{ds}}) \left[(Q_s^2/2C_{\text{ox}} + \beta Q_s + \beta Q_s^2/(Q_s + 2Q_o)) - Q_{\text{Tot}}/WL \cdot (2\beta + Q_s/2C_{\text{ox}} - 8\beta^2 C_{\text{Si}}/(Q_s + 2Q_o)) \right]}{1/2C_{\text{ox}} + \beta(1/Q_s + 1/(Q_s + 2Q_o))}. \quad (7)$$

In a similar way, the drain-to-source capacitance can be written as

$$C_{\text{ds}} = - \left. \frac{dQ_{\text{D}}}{dV_{\text{ds}}} \right|_{V_{\text{gd}}} \quad (8)$$

$$= - \left(\frac{dQ_{\text{D}}}{dQ_s} + \frac{dQ_{\text{D}}}{dI_{\text{ds}}} \cdot \frac{dI_{\text{ds}}}{dQ_s} \right) \cdot \left. \frac{dQ_s}{dV_{\text{ds}}} \right|_{V_{\text{gd}}},$$

where Q_{D} is the total drain charge in [6]. Then, by replacing (5) in (8), with $dQ_s/dV_{\text{ds}} = dQ_s/dV_{\text{gs}}$ (see (6)) and $dQ_{\text{D}}/dI_{\text{ds}} = -2Q_{\text{D}}/I_{\text{ds}}$, C_{ds} is given by

$$C_{\text{ds}} = \frac{2W\mu Q_{\text{D}}/LI_{\text{ds}} \cdot (2\beta + Q_s/2C_{\text{ox}} - 8\beta^2 C_{\text{Si}}/(Q_s + 2Q_o)) - dQ_{\text{D}}/dQ_s}{1/2C_{\text{ox}} + \beta(1/Q_s + 1/(Q_s + 2Q_o))}, \quad (9)$$

with

$$\frac{dQ_{\text{D}}}{dQ_s} = \frac{(Q_{\text{d}}^3 - Q_s^3)/\beta C_{\text{ox}} + 6(Q_{\text{d}}^2 - Q_s^2) - 12Q_o(Q_{\text{d}} - Q_s) + 24Q_o^2 \ln((2Q_o + Q_{\text{d}})/(2Q_o + Q_s))}{12C_{\text{ox}}LI_{\text{ds}}^2(2Q_o + Q_s)/\beta W^3\mu^2 [4\beta C_{\text{ox}}(Q_o + Q_s) + 2Q_o Q_s^2]}. \quad (10)$$

Finally, C_{gd} can be obtained by replacing Q_s by Q_{d} in (7), taking into account the DG-MOSFET symmetry. Therefore, C_{gd} is given by

$$C_{\text{gd}} = \frac{(W^2\mu/I_{\text{ds}}) \left[(Q_{\text{d}}^2/2C_{\text{ox}} + \beta Q_{\text{d}} + \beta Q_{\text{d}}^2/(Q_{\text{d}} + 2Q_o)) - Q_{\text{Tot}}/WL \cdot (2\beta + Q_{\text{d}}/2C_{\text{ox}} - 8\beta^2 C_{\text{Si}}/(Q_{\text{d}} + 2Q_o)) \right]}{1/2C_{\text{ox}} + \beta(1/Q_{\text{d}} + 1/(Q_{\text{d}} + 2Q_o))}. \quad (11)$$

Note that all the capacitance and the drain current can be explicitly expressed in terms of the charge density in source and drain, Q_s and Q_{d} .

3. Rectifier Performance

We implement the large-signal equivalent circuit for the DG-MOSFET in Keysight Advanced Design System (ADS), using Verilog-A, which is the industry standard modelling language for analogic circuits [14].

In the rectifier under consideration (see Figure 1), gate and drain terminals in both DG-MOSFETs are short-circuited. Thus, C_{gd} can be ignored, and C_{gs} and C_{ds} depend only on the drain-to-source voltage, V_{ds} . Additionally, as Figure 4 shows, to avoid divergence problems by asymptotical

response for V_{ds} close to zero, C_{gs} modelled capacitance and C_{ds} modelled capacitance (represented with symbols) are approximated by sigmoidal functions (represented with lines) as

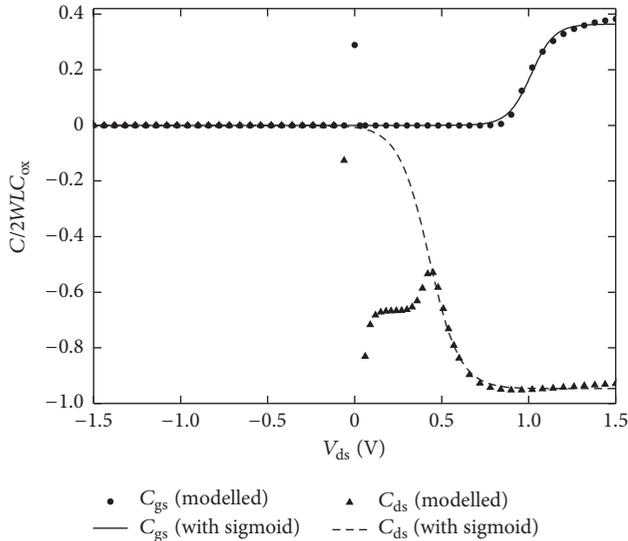
$$C_{\xi\text{d}} \Big|_{V_{\text{gd}}=0} \approx \frac{A_{0\xi}}{1 + e^{(A_{1\xi} + A_{2\xi} V_{\text{ds}})}} + A_{3\xi}, \quad \text{with } \xi \equiv \text{g, d}, \quad (12)$$

with $A_{0\xi}$, $A_{1\xi}$, $A_{2\xi}$, and $A_{3\xi}$ being fitting parameters, summarised in Table 1.

The electrical simulations for the rectifier in ADS are validated through numerical simulations with Sentaurus, accounting for the extrinsic elements of the transistors. Thus, Figures 5(a) and 5(b) show the dynamic drain current for DG-M1 and DG-M2, respectively, with RF input signal of 1 V amplitude at 1 GHz, after 10 ns (i.e., at steady values). It

TABLE I: Fitting parameters for C_{gs} and C_{ds} .

A_{0g}, A_{0d} ($\times 10^{-14} \text{ Fcm}^{-2}$)	A_{1g}, A_{1d}	A_{2g}, A_{2d} (V^{-1})	A_{3g}, A_{3d} ($\times 10^{-14} \text{ Fcm}^{-2}$)
-1.3, 3.3	-15.3, -4.9	15.1, 11.4	1.3, -3.3

FIGURE 4: Modelled C_{gs} and C_{ds} (with symbols) and their sigmoidal approximations (with lines) versus drain-to-source voltage.

can be noticed that the numerical dynamic current (with symbols) is correctly modelled (with line) in both transistors. An unexpected negative modelled current for DG-M2, being off, appears, when ADS artificially adds auxiliary resistance, between gate and source, to facilitate convergence. However, its short duration, inferior to 0.1 ns, makes DC output voltage deviations irrelevant.

Additionally, Figure 6 shows the numerical (with symbols) and modelled (with line) DC output voltage, varying the RF input power, at 5 GHz, from -5 dBm to 10 dBm. A good agreement between both data is achieved, with a maximum relative error of 11.7%. Furthermore, the resulting power conversion efficiency (DC output - RF input power ratio) is similar to that reported in [10], with conventional MOSFETs.

Once the rectifier performance with ADS has been numerically validated, Figure 7 compares the transistor response for the electrical output voltage (with squares), for an input power of 5 dBm at 5 GHz, with that for the rectifier implemented in HSPICE with commercial $0.18 \mu\text{m}$ -NMOS, from Texas Instruments, with identical dimensions (with solid line). Note that a similar DC output voltage of around 0.6 V is obtained, even when the threshold voltage for the NMOS is 0.18 volts lower than that for the DG-MOSFET (0.55 V), which is compensated with its double current capability.

When threshold voltage is reduced, by using alternative gate metals, a higher rectified output voltage is expected. The use of titanium nitride (TiN) films as gate electrode in

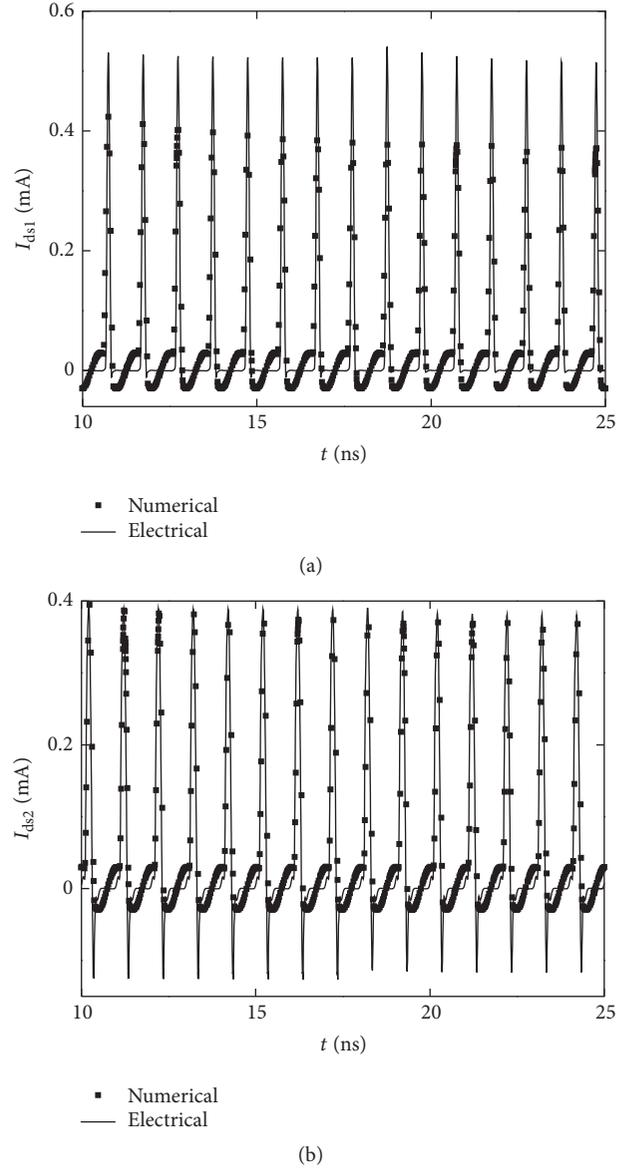


FIGURE 5: Numerical (with symbols) and modelled (with solid line) steady-state dynamic current for (a) DG-M1 and (b) DG-M2, with an input signal of 1 V amplitude at 1 GHz.

MOS capacitors and in Schottky diodes on n-type Si (100) substrates has been reported in [15], having a work function of 4.2 eV and electrical resistivity of $270 \mu\Omega\text{cm}$. Thus, when using TiN as the metal gate in the DG-MOSFETs, as Figure 7 indicates, the DC rectified voltage (with dotted line) grows (0,25 V) up to 0.83 V.

On the other hand, the influence of the number of stages on the rectified output voltage has been analysed. In every stage (single rectifier in Figure 1), the source of DG-M2 must be connected to the drain of DG-M1 in next stage, with all coupling capacitance connected to the common RF input signal. Thus, the output voltage (with an output load of 10 k Ω) is the sum of all voltages between the terminals of the smoothing capacitances, which are connected in series.

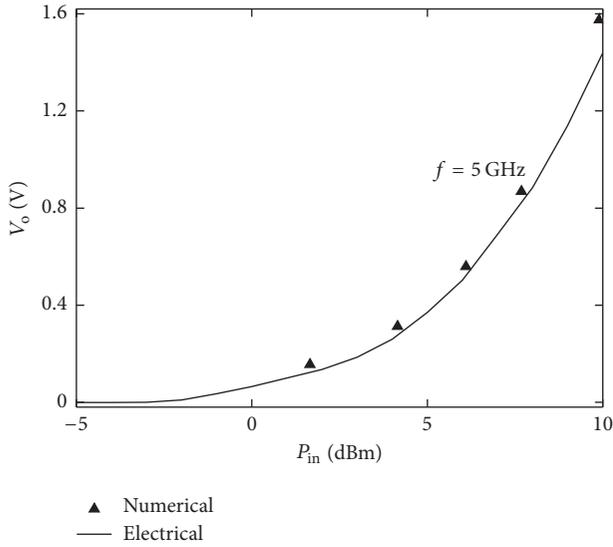


FIGURE 6: Numerical (with symbols) and modelled (with line) rectified output voltage as function of the RF input power at 5 GHz.

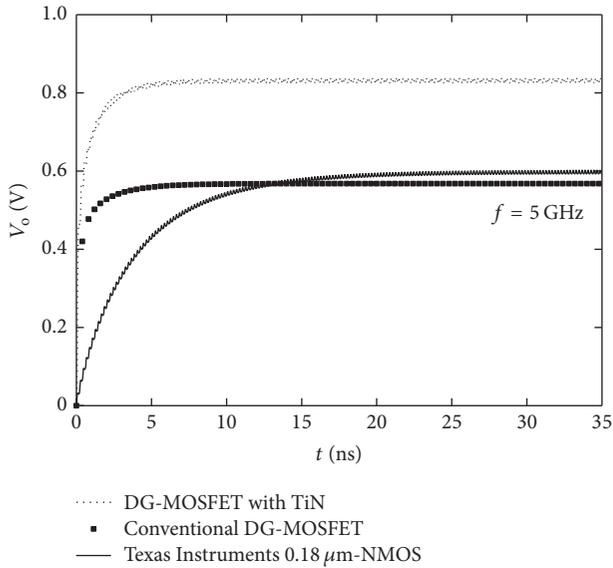


FIGURE 7: Transient response for the rectified output voltage with conventional DG-MOSFETs (squares), Texas Instruments 0.18 μm -NMOS (solid line, with HSPICE), and DG-MOSFETs with TiN (dotted line), for an input power of 5 dBm at 5 GHz.

Figure 8 shows the electrical output voltage when varying the RF input power from -5 dBm to 10 dBm, for different number of stages: from one to five, at 5 GHz with TiN as gate metal. Note that, up to two stages, the output voltage increases, decreasing with additional stages: two is the optimal number of stages in the rectifier with DG-MOSFETs. This result differs from that reported in [10], with conventional N-MOSFETs, where six stages is the optimal configuration. Therefore, smaller number of stages than with conventional MOSFETs is necessary to produce the maximum output voltage with DG-MOSFETs.

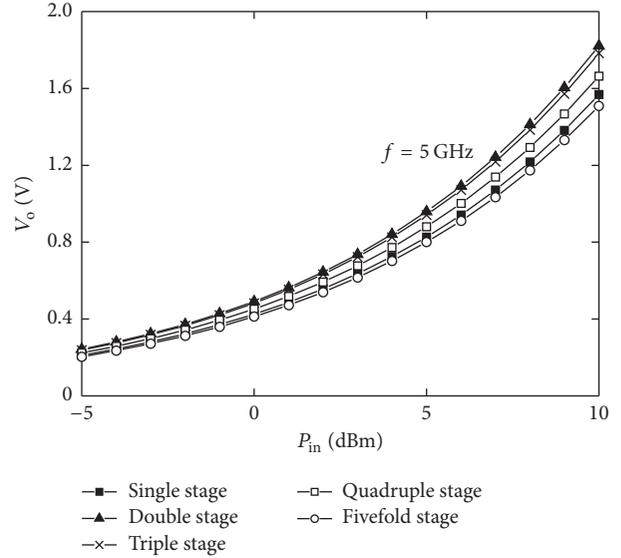


FIGURE 8: Modelled rectified output voltage for multiple stage configurations as function of the RF input power at 5 GHz with TiN.

Finally, it can be pointed out that with short channel effects (SCEs) a superior current and, consequently, a higher DC output voltage would be expected. However, when incorporating the saturation velocity, effective mobility, and channel length modulation effects, as in [5], a minor impact on the DC output voltage is appreciated, which only increases 1.3% for an input power as high as 5 dBm (at 5 GHz, with TiN), evidencing a determinant circuitual topology influence.

4. Conclusions

A compact model for DG-MOSFETs has been developed and implemented in ADS, with Verilog-A, to perform electrical simulations of RFID rectifiers, which have been validated through numerical simulations with Sentaurus.

From transient simulations at microwave frequencies, it has been observed that the proposed rectifier with DG-MOSFETs efficiently produces a DC output voltage. Furthermore, using TiN as metal gate, the DC output voltage increases 0.25 V, compared with that obtained with n^+ polysilicon. We have also demonstrated that just two stages are necessary to achieve the optimal performance of the rectifier, less than with conventional N-MOSFETs, and that SCEs have a minor impact on the DC output voltage.

Competing Interests

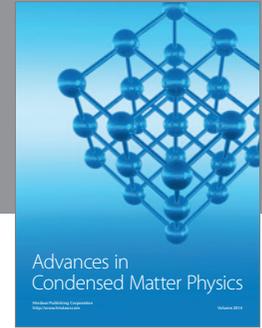
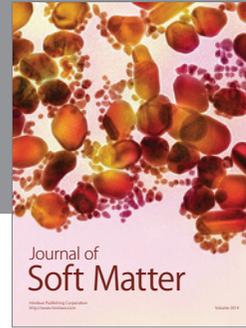
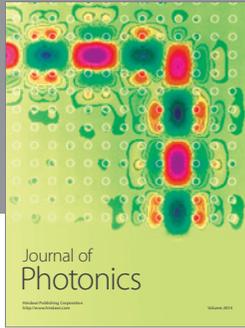
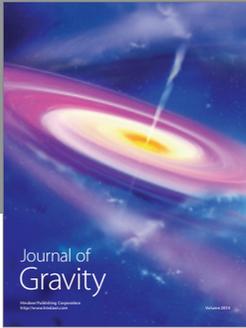
The authors declare that there are no competing interests regarding the publication of this paper.

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