

Experimental characterization of a Synchronous Frequency-Hopping Spread-Spectrum transceiver for Wireless Optical Communications

S. T. Pérez^{*}, J. A. Rabadán, F. A. Delgado, J. R. Velázquez, R. Pérez Jiménez

Universidad de Las Palmas de Gran Canaria,
Departamento de Señales y Comunicaciones,
Grupo de Tecnología Fotónica y Comunicaciones,
Las Palmas de Gran Canaria, Spain

ABSTRACT

In this paper, the design and experimental characterization of a wireless optical transceiver for indoor applications, based on Frequency-Hopping Spread-Spectrum techniques, is presented. Using these techniques reduce the narrowband interference produced by optical sources and the intersymbol interference induced by multipath propagation. It also makes possible using the CDMA capabilities associated with Spread Spectrum, in order to improve the performances when several emitters and receivers are considered. The main drawback of these kind of systems lies on the high complexity of the synchronization system of the receiver, typically consisting on two cascaded structures: acquisition and tracking. We propose using a dual-pilot signal, transmitted by a master emitter, for reducing both complexity and cost of the synchronization stage of the receiver.

Keywords: optical wireless communications, spread spectrum, frequency hopping, synchronism pilot signal, CDMA

1. INTRODUCTION

Wireless networks had become one of the most demanded infrastructures for both office and in-home environments, due to their easy implementation and modification, and because their performances are getting closer to wired ones. In fact, today's trends are conducting to a massive implementation of these networks, leaving wired or fiber optics ones to those applications requiring higher traffic capabilities (as WAN, MAN, backbones). These wireless LANs are mainly based on radiofrequency carriers as transmission method, but infrared radiation is gaining nowadays more and more application scenarios. Wireless optical links are a good alternative to radiofrequency ones in some special environments due to their immunity to electromagnetic interferences and because radiation is confined to the room where it is emitted¹. Furthermore, they are not limited by spectrum regulations (as RF ones). In the other hand, they present some drawbacks as a limited range of application (due to the path loss on the optical channel) and its high vulnerability to obstacles.

The wireless optical indoor channel has some special characteristics that limit the performances of the transmission links, i.e. narrowband interferences produced by optical data sources (as IrDA links or remote control devices), noise sources induced by illumination and intersymbol interference produced by multipath propagation due to reflections over reflecting surfaces or obstacles³. Spread spectrum techniques dramatically improve the performances of these kind of communication links in the presence of colored noise or interferences². We have proposed using these schemes over the optical channel as a way of, not only reducing the above mentioned drawbacks, but allowing the use of new capabilities as CDMA in order to share the channel among multiple simultaneous users. In this work a Synchronous Optical Fast-FHSS transceiver prototype that we have developed and tested is presented. Synchronization is obtained by means of a pilot-signal that permits simplify the structure (and their complexity and cost) of the receivers. This pilot also permits introducing not only a centralized topology (master-slave) but also synchronous communications between terminals.

^{*} sperez@dsc.ulpgc.es; phone: +34928451277; fax: +34928451243

The proposed system presents some significant advantages. They can easily co-exist with other optical pre-existent wireless networks, as it is a carrier-based scheme and optical links are mainly based on IM/DD baseband modulations. It also will improve the joint throughput of the net by using CDMA. The prototype has been designed mainly over logical programmable devices and digital frequency synthesizers. These structures permit easily changing the coding and frequency assignment by re-programming the logical devices.

This submission is organized as follows: section 2 briefly describes the FHSS behavior over the wireless optical channel. In section 3 the synchronization procedure is explained in depth, and then, the prototype design and its block components are described in section 4. Section 5 shows the results and measurements obtained by the operation of this system. Finally some conclusions are given and possible applications are presented.

2. FHSS SYSTEMS IN WIRELESS OPTICAL CHANNEL

FHSS systems are modulation schemes which make use of several carrier frequencies for data transmission. For different time slots of period T , carrier signal changes its frequency accordingly to a code sequence (or pseudo noise sequence). In this way the spectrum spreading process is performed. Modulated signal bandwidth comprises from lowest to highest carrier frequencies.

The carrier change rate, known as chip rate ($1/T$), determinates the type of FHSS system²:

- Slow FHSS (SFHSS) schemes transmit several data bits in the same time slot, so T is bigger than the data bit period.
- Fast FHSS (FFHSS) systems use several carrier frequencies in the transmission of the same data bit.

The use of SFHSS or FFHSS schemes and the code sequence family⁶ used for frequency hopping, determinate the implemented system characteristics.

On the other hand, wireless optical channel depends on several factors as emitter and receiver position or walls and obstacles properties. In general, the wireless optical channels present two main disadvantages as communication media:

- Interferences⁸: illumination sources and other optical links (remote controls, optical networks).
- Multipropagation⁷: reflections in obstacles, which reach the receiver at different time, causing inter symbol interference (ISI).

As we said above, FHSS techniques present some properties that can improve wireless optical links:

- They have narrowband interference rejection capability, ought to the frequency hopping². The interference only affects if transmitted signal lies on interference bandwidth. Besides as in the case of optical channel the main interferences are base band signals, the modulated FHSS signal is not affected.
- They also reduce the effects of multipropagation⁴. Reflections with large delays (bigger than time slot T) are treated as narrowband interferences.

Spread spectrum techniques also provide Code Division Multiple Access (CDMA)⁵, which can be used in the wireless optical channel as access method instead of traditional Time Division Multiple Access (TDMA) or Frequency Division Multiple Access (FDMA).

3. SYNCHRONOUS FHSS SYSTEMS

As we said in introduction, the main disadvantage of SS systems is the synchronization process complexity. They need different stages in order to obtain the complete recuperation of code frequency and phase⁶: acquisition and tracking. Specific circuits have been development for performing these processes as Tau Dither Tracking (TDT)⁶ or Traditional Full-Time Tracking Loop (TFTL)².

In this work we propose a new synchronous scheme which uses a pilot signal. This pilot has information about the frequency and the phase of the code generation clock and it consists on a BPSK signal with the following properties:

- Carrier signal is a synchronized frequency multiple of the code clock signal.
- Data signal is a square signal with a period of twice the code length.

This signal is generated in the transmitter (or central node as explained below). Therefore, the BPSK signal changes its phase 180° each time the transmitter code generator starts a new code sequence. Besides this pilot signal has a carrier frequency which not interferes in the FHSS signal. In figure 1 an example of the pilot signal is shown, we can see the carrier signal, the data signal and the modulated signal with the phase shifts.

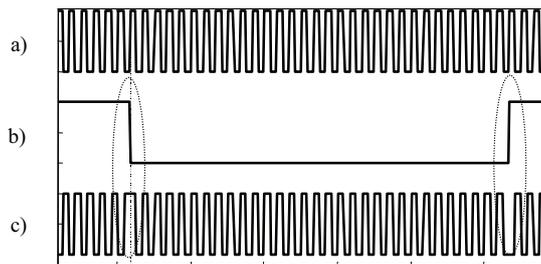


Figure 1: Pilot signal generation: a) carrier; b) data; c) digital pilot.

The synchronization process at reception is reduced to a BPSK demodulation of the pilot signal. In this way, we obtain two different signals from the pilot: the code generation clock, and a preset signal, which sets the code generator at the beginning of the code sequence.

Pilot signal makes possible the implementation of a wireless network topology based on CDMA, where all network nodes are synchronized to the same pilot signal (we can name this topology as synchronous CDMA network). We can see the network configuration in figure 2, a central node generates the synchronization signal and secondary nodes lock to it. There can be communications links between different secondary nodes and between secondary and central node. Besides, central node performs router functions for external cable networks connection.

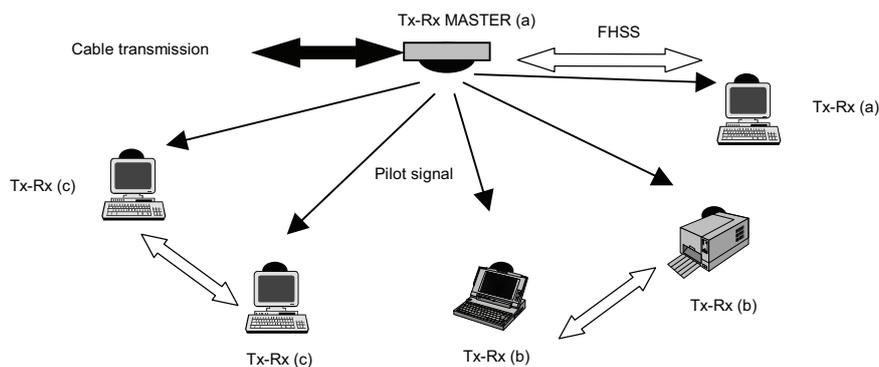


Figure 2: Synchronous CDMA network topology.

As disadvantage, the proposed topology does not work if the pilot signal is interfered. However, for indoor wireless optical communications there is not external interference and we only have to worry about internal emissions in the pilot signal bandwidth.

4. DESIGNED SYSTEM

Figure 3 shows the block diagram of the optical fast frequency hopping (FFHSS) designed system, where the transmitter sends the FHSS signal and the synchronization to the receiver through two separate optical emitters. Binary rate is 512 kbits per second, using three frequencies per bit, resulting a chip rate of 1.536 Mchips per second.

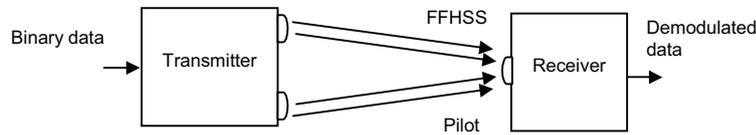


Figure 3: Block diagram of the designed system.

Figure 4 shows the transmitter block diagram. All the digital blocks are implemented through programmable devices, (in this particular prototype is integrated in an ALTERA® EPM7128S). This logical control includes: frequency dividers, a pseudorandom data generator (15 bits length), a data multiplexer (for external data) and a Maximum Length Sequence (MLS) pseudorandom code generator (31 states length). We have also included in this main block all digital synchronization source used for all the net receivers and the control signals for the DDS, as well as the DDS codes used for the FHSS frequency generation. For this prototyping we have used an AD9851 DDS from ANALOG DEVICES®.

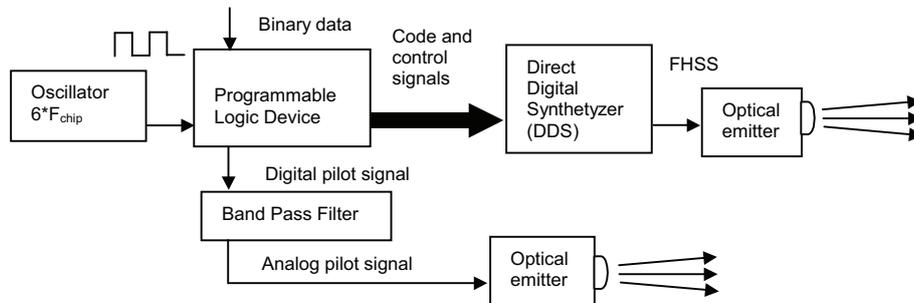


Figure 4: Transmitter block diagram.

The transmitted frequency for the FHSS signal is chosen from a 32 frequencies set, uniformly distributed from 24.382 MHz until 72 MHz and stepped 1.536 MHz. Frequencies are selected by a 5 bits codeword, the less significant bits belongs to the pseudorandom code generator and the data bit is taken as the most significant bit. Table 1 shows code and frequency assignation. Lowest sixteen frequencies are dedicated to transmit the “0” data while the highest sixteen are taken for the “1”. Previous to the electronic design, a simulation stage was extensively taken using SIMULINK®. There, the FHSS was simulated through a VCO (Voltage Controlled Oscillator), sampling-and-hold its output at the same frequency of the DDS clock (180 MHz). Then a low pass filter was used to eliminate the undesired high frequency harmonics. The FHSS estimated bandwidth is 50.688 MHz (figure 5) and the process gain results 15.2 dB.

The pilot used for synchronization is obtained from the programmable logic block. The carrier frequency (9.216 MHz) is six times the chip frequency (1.536 MHz). It is a BPSK signal, inverting the phase when the pseudorandom generator code reach the end of the sequence. In order to have the transmitted sinusoidal pilot (figure 6), it is necessary to band-pass filtering the signal by means of a tuned at 9.216 MHz filter (MINICIRCUITS® PBP-10.7). As we said before, both FHSS and pilot were sent by two separate similar optical emitters (figure 7). They are based on a HAMAMATSU® L7726 LED as optical source. The emitted wavelength for measurements is 650 nanometers.

Code	Frequency number	Frequency (MHZ)	Code	Frequency number	Frequency (MHZ)
00000	0	24.384	10000	16	48.96
00001	1	25.92	10001	17	50.496
00010	2	27.456	10010	18	52.032
00011	3	28.992	10011	19	53.568
00100	4	30.528	10100	20	55.104
00101	5	32.064	10101	21	56.64
00110	6	33.6	10110	22	58.176
00111	7	35.136	10111	23	59.712
01000	8	36.672	11000	24	61.248
01001	9	38.208	11001	25	62.784
01010	10	39.744	11010	26	64.32
01011	11	41.28	11011	27	65.856
01100	12	42.816	11100	28	67.392
01101	13	44.352	11101	29	68.928
01110	14	45.888	11110	30	70.464
01111	15	47.424	11111	31	72

Table 1 : FHSS set frequencies.

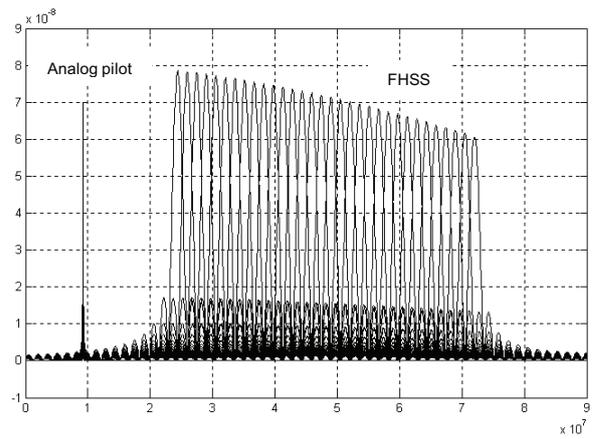


Figure 5: FHSS and analog pilot spectrum modules.

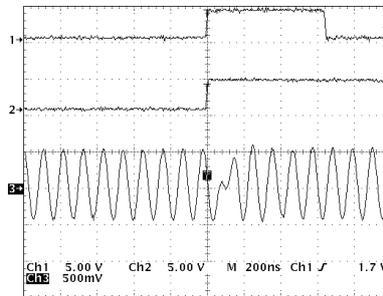


Figure 6: Pseudocode generator initial state (above), pseudocode generator length (middle) and analog pilot (below).

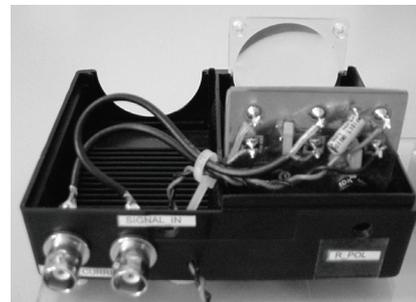


Figure 7: Diferent sights of the optic emitter.

Figure 8 shows the receiver block diagram. As optical receiver for testing we have used a HAMAMATSU® C5331 APD module. This optical receiver allows until 100 MHz signal bandwidth. Figure 9 shows the optical receiver block. The output signal of this module is connected to the splitting filters. Again, a PBP-10.7 band pass filter extracts the analog synchronization signal, and a MINICIRCUITS® SCHF-17 high pass filter permits to obtain the FHSS signal.

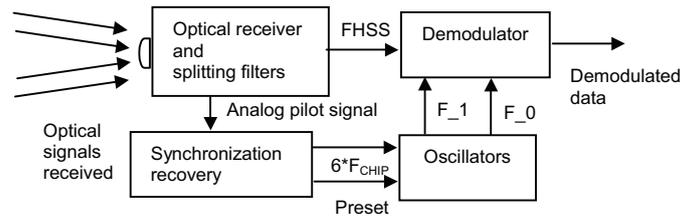


Figure 8: Receiver block diagram.

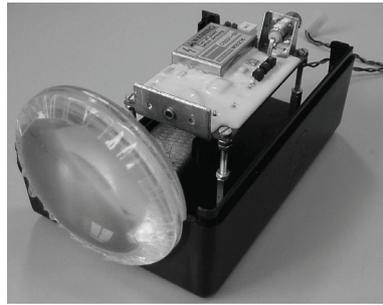


Figure 9: Optical receiver Hamamatsu C5331 module.

Synchronization recovery circuits include a non-linear square-power elevator circuit and a Phase Lock Loop for the pilot carrier recovery. Recovered carrier is then connected to the programmable digital logic device, where the chip frequency (1.536 MHz) is extracted by division. This clock is then used by the pseudorandom code generator. Then the received analog pilot is synchronously demodulated and connected to a comparator. The comparator output is sent to two timer circuits for compensating the circuitry-induced delay. Finally, these two outputs signals are combined in order to obtain the preset signal used to synchronize the initial state of the pseudorandom code generator in the receiver. Demodulator (figure 10) uses a typical double-branch structure, which detects separately zeros and ones. The FHSS signal is split in two by means of a MINICIRCUITS[®] PSC-2-1. Each branch uses a mixer block, based on a MINICIRCUITS[®] SBL-3 and then the mixed signal pass through a band-pass PBP-10.7 filter. Envelope detection is performed by a PHILIPS[®] SA602AN multiplier. In the upper branch (ones detector branch) the output of the envelope detector has the same shape than the data, while in the other the signal is inverted.

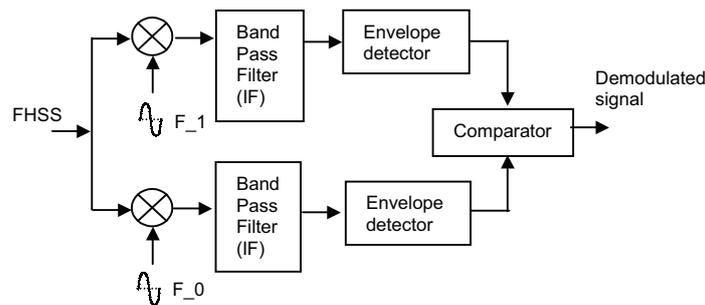


Figure 10: Demodulator.

The local oscillators were designed using two DDS's, controlled by the programmable digital logic device, which receives the signal from the synchronization recovery circuit. The programmable logic block also includes an initialization block, frequency dividers, a pseudorandom code generator, and the control and code signals used for programming the DDS's. The output of the code generator is used to synchronize the DDS's. Two local oscillators (F_1 and F_0) generate the frequencies of the FHSS signal minus the intermediate frequency value (10.7 MHz). Finally, figure 11 shows the designed transceiver.

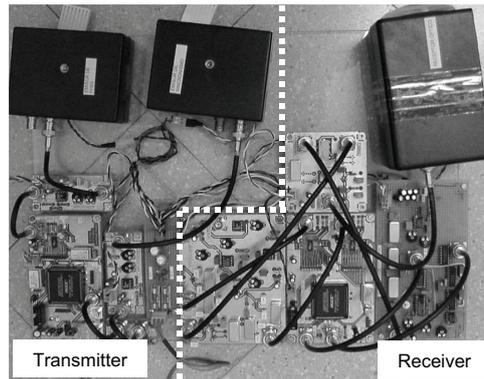


Figure 11: Designed transceiver.

5. MEASURES AND RESULTS

5.1 Simulation results

The system was simulated in order to verify the performance against narrowband interference, multipath propagation and additive white gaussian noise (AWGN). As interference signal we have used one of the frequencies of the FHSS set, with the same power than the receiver signal but opposed in phase. The effect of this interference is canceling the FHSS received signal during a chip interval. Data bit is recovered correctly because there are two more chip frequencies in the same bit time. If the interference had a value different from the FHSS values this effect would be even less significant over the demodulated data. Furthermore, the behavior of the receiver was checked in a multipath channel. In order to study this phenomenon it was added to the FHSS signal another replica, delayed one chip interval, with the same amplitude than the original signal. In such conditions the system operates correctly since the delayed signal is refused in the demodulator.

5.2 Prototype operation

For testing, we have used a laboratory configuration in which transmitted signals are reflected in order to simulate the real conditions of a quasidiffuse, 3 meters long, transmission system. Figures 12 and 13 show the FHSS signal and analog synchronization signal in the transmitter (tx) and in the receiver (rx). FHSS changes the frequency with every rising edge of the frequency update signal. The amplitude decreases as the frequency increases, this variation is caused mainly by the DDS.

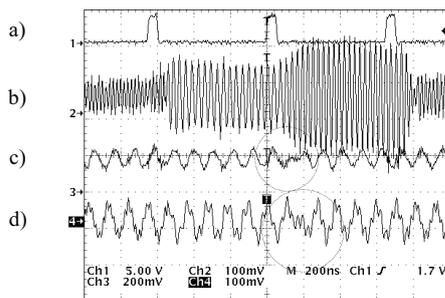


Figure 12: a) Frequency update (tx)
b) FHSS (LED current, tx)
c) Analog pilot (LED current, tx)
d) Optic receiver output (rx)

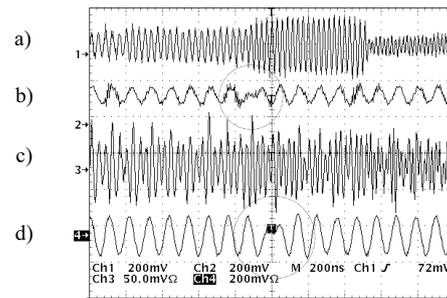


Figure 13: a) FHSS (LED current, tx)
b) Analog pilot (LED current, tx)
c) FHSS (high pass filter output, rx)
d) Analog pilot (band pass filter output, rx)

The Power Spectral Density (PSD) obtained in the optical receiver output is shown in figure 14. The different spectral positions of FHSS and the analog pilot produce minimum mutual interference.

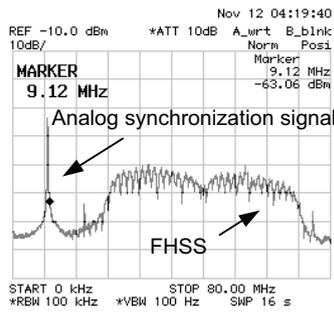


Figure 14: PSD obtained in the optical receiver output.

Figures 15 and 16 show both the PSD of the FHSS signal and the local oscillator associated. In both cases the transmitted frequencies are equal to the sixteen local oscillator frequencies minus the intermediate frequency value. The intermediate frequency signal at one branch of the demodulator is shown in figure 17 (zeros branch). The two upper signals indicate that the transmitter and the receiver are synchronized. Figure 18 shows the PSD of the intermediate frequency in the same branch, it is centered on 10.7 MHz and the main lobule bandwidth (3.072 MHz) is the double of the chip frequency (1.536 MHz).

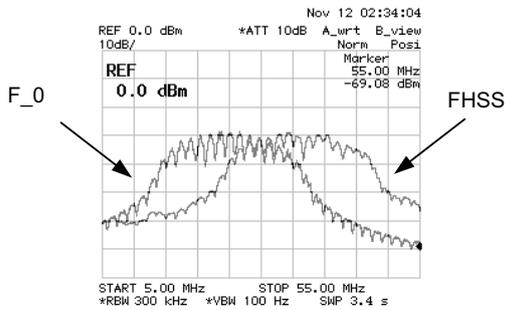


Figure 15: PSD of the FHSS signal when the transmitted data is "0" and the local oscillator associated (F_0).

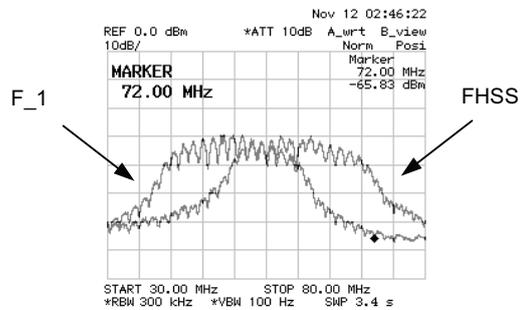


Figure 16: PSD of the FHSS signal when the transmitted data is "1" and the local oscillator associated (F_1).

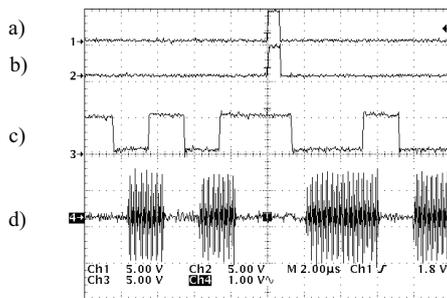


Figure 17: a) All flip-flops are in "1" state in the transmitter code generator.
 b) All flip-flops are in "1" state in the receiver code generator.
 c) Transmitted data.
 d) Intermediate frequency signal in the demodulator zeros detector branch.



Figure 18: PSD of the intermediate frequency signal in the demodulator zeros detector branch.

The transmitted and demodulated data are shown in figure 19. Data in the receiver are 1.2 μ s delayed. The demodulated data eye diagram is in figure 20.

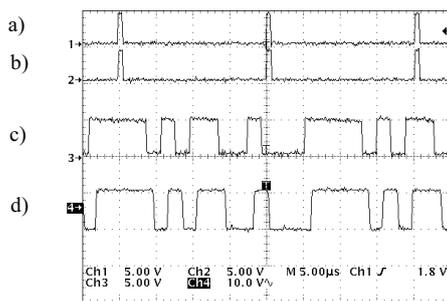


Figura 19: a) All flip-flops are in “1” state in the transmitter code generator.
 b) All flip-flops are in “1” state in the receiver code generator.
 c) Transmitted data.
 d) Demodulated data.

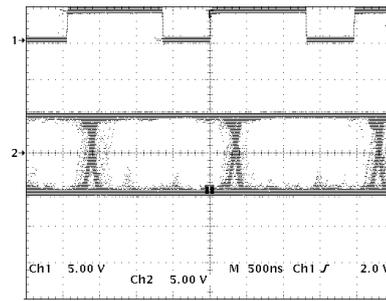


Figura 20: Demodulated data eye diagram.

6. CONCLUSIONS

In this work, the design and experimental characterization of a FHSS transceiver, suitable for indoor wireless optical communications, has been presented. We have tested its performances, as the increased robustness against narrowband interference, baseband noise and multipath-induced penalty over available bandwidth. We have also studied the characteristics of the proposed synchronous-CDMA architecture. It reduces significantly the complexity of the synchronization stage of the receiver without damaging the general performances of the whole net. These techniques are also applicable to sensor networks on domestic or industrial environments, where a simplified receiver structure reduces cost, weight and power consumption. Pilot signal is also robust as it cannot be interfered from outside of the transmission cell, as in radiofrequency-based wireless networks.

7. ACKNOWLEDGEMENTS

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