Low Power Voltage Limiter Design for a Full Passive UHF RFID Sensor

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***Abstract*— This paper presents a low power voltage limiter design that avoids possible damages in the circuits of the analog front-end of the RFID sensor due to voltage surges whenever reader and tag are very close. The proposed voltage limiter design takes advantage of the implemented bandgap reference and voltage regulator in order to provide low temperature and process deviation of the limiting voltage. The measured limiting voltage is 2.9V with a voltage variation of only +/-0.025V for the four measured dies. The current consumption is only 150nA when the reader and the tag are far away one to each other, not limiting the sensitivity of the tag due to an undesired consumption in the voltage limiter. The circuit is implemented on a low cost 2P4M 0.35µm CMOS technology.**

I. INTRODUCTION

Passive RFID technology is becoming a very suitable RF interface for Passive Wireless Sensors. The RFID tag is supplied by an Electromagnetic (EM) wave transmitted by the reader device, therefore no battery is required in the sensor node [1]. Low power inductive coupling, widely used in RFID near field tags, has been already proved as a suitable interface for wireless sensors, but in a reduced range (<30cm) [2-3]. In order to increase the operation range to some meters, Far Field RFID Tags working in the UHF Band are required [4-6].

Fig. 1 shows the block diagram of a passive UHF RFID sensor [1]. The RF input power is captured by the antenna, which is matched to the input impedance of the chip for maximum power transfer. The Voltage Multiplier block (VM) rectifies the incoming signal and stores the required energy to operate in the supply capacitor (C_{supply}). That way a sharp decrease in the supply voltage is avoided whenever short absences of RF power due to data communication exchange between the reader and the sensor node, or current peaks due to EEPROM operation, are produced. To assure a proper start-up of the complete tag a Power on Reset (POR) or voltage sensor circuit is typically implemented. This block senses the voltage in the supply capacitor and generates an enable signal once it is over the minimum required voltage for proper operation of the tag. The enable signal generated by the POR block turns on the voltage regulator, which provides the V_{dd} for the rest of the subsystems of the tag. A voltage limiter block (VL) is implemented in order to avoid possible damages in the circuits due to voltage surges whenever reader and tag are very close. The demodulator block is in charge of demodulating the ASK modulated commands coming from the reader device. Those commands are interpreted by the digital core which is in charge to control the communication flow between the reader and the tag and to access the EEPROM memory and the sensor. Finally the PSK modulator sends back to the reader the ID and sensor data from the wireless sensor node.

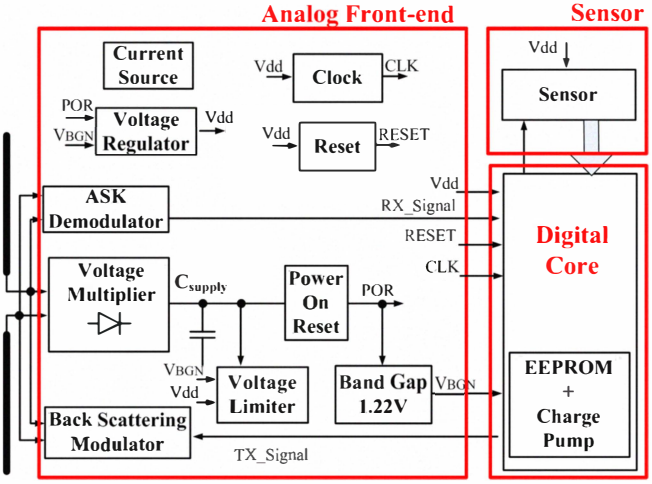

Figure 1. Block diagram of a passive UHF RFID sensor

To improve the reading range between the reader and the tag it is critical to reduce the power consumption of each block in the tag, since the available power from the reader transmitted signal reduces quadratically with the distance (Friis formula [7]). This fact imposes a design trade-off in the voltage limiter design, where a high shunt current is desired, whenever the reader and the tag are close, in order to avoid voltage surges at the output of the voltage multiplier that may

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damage the rest of the blocks in the tag. At the same time low shunt current is desired, whenever the distance between the tag and the reader is big and the voltage protection is not active, in order to not degrade the maximum communication distance (Fig. 2).

On the other hand, the sensor embedded in the tag requires a stable supply voltage for good measurement accuracy. For that purpose a dedicated voltage regulator is implemented on the tag. Due to the ultra-low power consumption of the voltage regulator (less than 0.7uW) it is desired that the voltage limiter provides a stable limiting voltage against process variations, otherwise extra PSRR performance would be needed in the voltage regulator that supplies the sensor, increasing the required power consumption in the voltage regulator. Therefore there is a strong motivation, in RFID sensor nodes, to provide voltage limiters with low variation on the limiting voltage against process variations (Fig. 2).

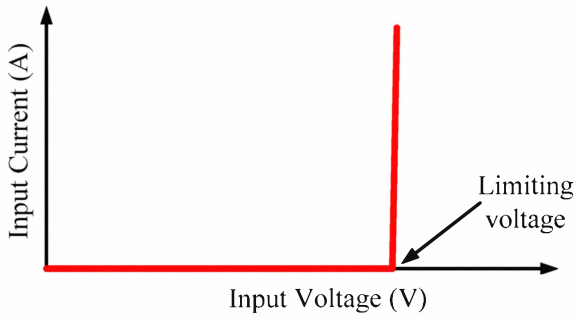


Figure 2. Ideal I-V characteristic of the voltage limiter

This paper proposes a new voltage limiter circuit that takes advantage of already existing circuits in the tag such as bandgap reference or power on reset to reduce the current consumption of the voltage limiter when the protection is not active and minimize limiting voltage variations due to process variations.

The paper is organized as follows. Section II presents the design of a conventional voltage limiter and introduces the new proposed circuit. Layouts of both circuits are presented in Section III. The measured results of both circuits are compared in Section IV. Finally, the main conclusions are summarized in Section V.

II. VOLTAGE LIMITER CIRCUITS

A. *Conventional voltage limiter circuit*

The ideal I-V characteristic of a voltage protection circuit is shown in Fig. 2. No current is drawn until a threshold is reached, after that the circuit behaves as a short. To approach this characteristic, a circuit based on the limiter proposed by [8] (see Fig. 3) was designed.

The chain of three NMOS transistors acts as a "zener diode." As soon as the output of the voltage multiplier (VM) exceeds the sum of all thresholds (M3-M5), current starts to flow through resistor R2. When the voltage drop across R2 reaches the threshold of PMOS transistor M2, this transistor will switch on, and in turn activates the NMOS transistor M1 which carries most of the current.

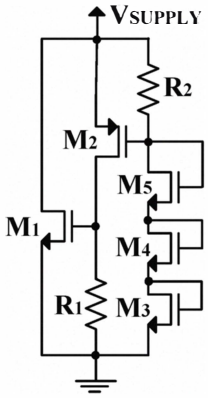


Figure 3. Conventional voltage limiter circuit

This circuit presents two disadvantages: on one hand the limiting voltage will be highly influenced by the threshold voltage variations of the different transistors (M1-M5) and resistors (R1-R2) variations, due to process variations, imposing extra PSRR performance requirements on the voltage regulator that supplies the sensor that will require extra current consumption. On the other hand, if the VL is designed to drawn a high current value (typically in the range of mA) when reader and tag are close, the drawn current by the VL when reader and tag are far away will be small but not negligible (typically in the range of μA) if compared to the whole current consumption of the complete tag. To overcome this two limitations the next subsection presents the new proposed voltage limiter.

B. *Proposed voltage limiter circuit*

Fig. 4 shows the schematic diagram of the proposed voltage limiter (VL) circuit [4].

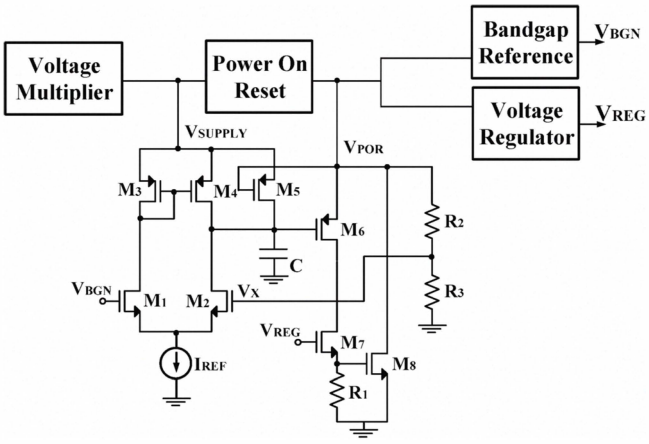


Figure 4. Proposed voltage limiter circuit

As shown, it takes advantage of already existing blocks, such as the bandgap reference and the voltage regulator to provide a very stable limiting voltage against process variations. The voltage regulator is needed to supply different parts of the RFID sensor and the bandgap reference is needed for both the voltage regulator and the EEPROM of the RFID chip. As shown in Fig. 4, the voltage limiter works as follows: the supply voltage (V_{SUPPLY} ~ V_{POR}) is divided down (V_X)

using R_2 and R_3 and compared with the band-gap reference (V_{BGN}) using differential amplifier M1-M4. When V_X is higher than V_{BGN}, transistor M6 switch on, and in turn activates transistor M8 which carries most of the current, preventing the supply voltage from increasing. The simulated limiting voltage variation (including voltage limiter, voltage regulator and band-gap reference blocks) against process and temperature (35 ° C to 45 ° C) variation is ±0.05V.

The proposed circuit has also the advantage that the drawn current by the VL, when reader and tag are far away and the VL is off, is negligible if compared to the whole current consumption of the complete tag.

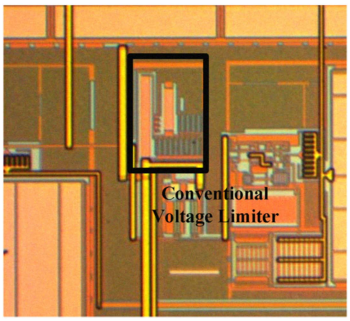
It is important to mention that the start-up of the bandgap reference and the voltage regulator must be quick enough to avoid any stability problem of the limiting voltage. Through simulation of the complete system a bandgap start-up time in the range of a few µs is enough to avoid any stability problem.

III. LAYOUTS

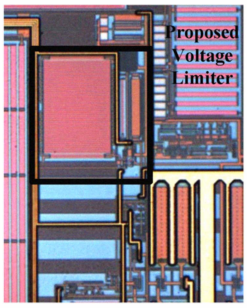
A low cost 2P4M 0.35µm CMOS standard process has been used to implement both voltage limiters. Schottky diodes, high resistive poly and EEPROM are also available in the process in order to implement other blocks of the RFID sensor such as the voltage multiplier, etc.

Fig. 5a shows a microphotograph of the conventional voltage limiter circuit. The total area occupied by the voltage limiter is 50x64µm^2.

Fig. 5b shows a microphotograph of the proposed voltage limiter circuit. Only the voltage limiter is shown, the bandgap reference and the voltage regulator are not shown. The total area occupied by the voltage limiter is 90x85µm^2.



(a)



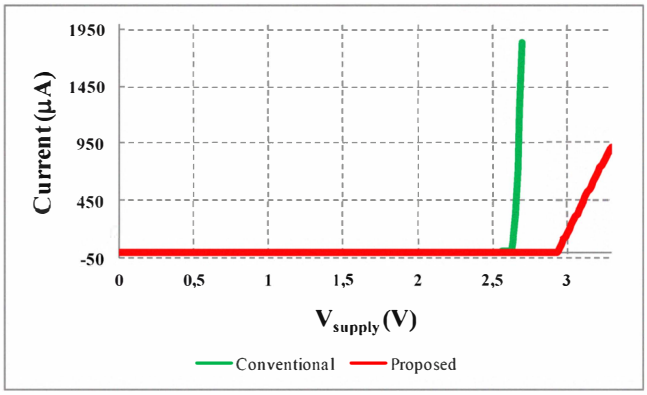
(b)

Figure 5. Microphotograph of the implemented (a) conventional voltage limiter circuit (b) proposed voltage limiter circuit

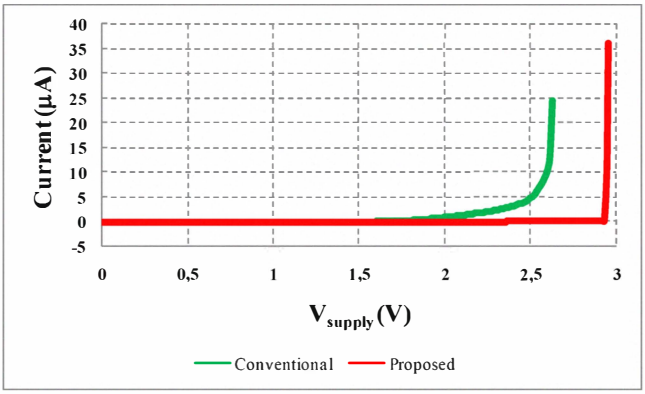
As shown in Fig. 5 both implemented circuits use M4 (the thick top metal layer) in parallel with M3 and a wide ground plane to draw the current whenever the reader and the tag are very close. This is important in order to avoid electromigration problems in those tracks when high current values are drawn.

IV. RESULTS

Fig. 6a shows the simulated I-V characteristic of both circuits; the conventional one and the proposed one. As it can be observed when the output voltage of the voltage multiplier exceeds 2.65V in the case of the conventional voltage limiter or 2.9V in the case of the proposed one, the circuit starts drawing current avoiding the voltage at the output of the voltage multiplier to increase. Fig. 6b shows a detail of the previous graph around the limiting voltage. As shown the drawn current by the conventional voltage limiter is around 5 µA at 2.5V, which is not negligible taking into account that the total current of the analog front end is 7.4µA. On the other hand, the proposed voltage limiter only draws 150nA until almost the limiting voltage, not limiting the sensitivity of the tag due to undesired power consumption in the voltage limiter.



(a)



(b)

Figure 6. Simulated I-V characteristic of (a) implemented voltage limiter circuits (b) detail around the limiting voltage

Both voltage limiters where implemented in two different RFID sensor tags. To measure the limiting voltage the set-up shown in Fig. 7 was implemented.

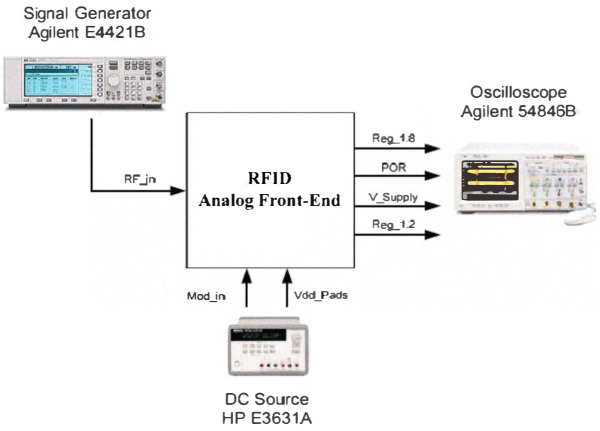
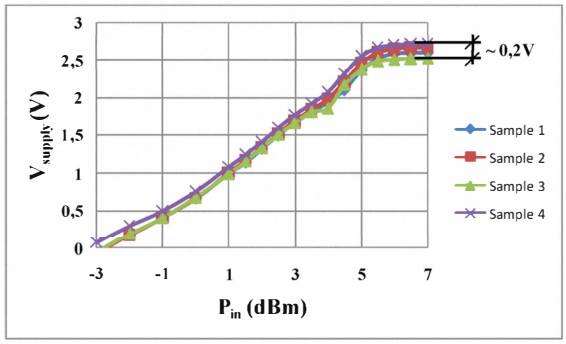
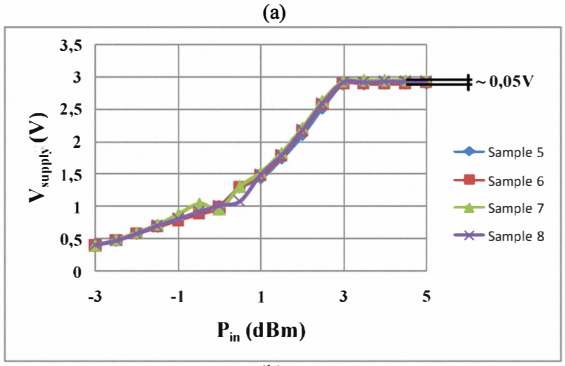


Figure 7. On-wafer measurement setup to obtain voltage limiter results

As shown in Fig. 8 for both circuits, as we increase the input power the voltage at the output of the voltage multiplier increases until the voltage limiter is on and limits the output voltage. Notice that the input of the chip is not matched to 50Ω that is the reason why a high input power between 3 and 5 dBm is necessary to turn on the voltage limiter. The conventional one and the proposed one, work properly limiting the output voltage of the voltage multiplier to 2.65V and 2.9V respectively. As it can be observed in Fig. 8, for the four measured dies of each limiter type, the limiting voltage of the proposed voltage limiter experiences less variation than the conventional one confirming the low process variation in the limiting voltage of the proposed voltage limiter.



(a)



(b)

Figure 8. Measured limiting voltage for both implemented voltage limiter architectures (a) Conventional one (b) Proposed one

V. CONCLUSIONS

This paper presents a low power voltage limiter design that avoids possible damages in the circuits of the analog front-end of the RFID sensor due to voltage surges whenever reader and tag are very close. Two designs are presented. The first one is based on a conventional architecture and the second one on a new proposed architecture which reduces limiting voltage deviations due to process and temperature variations and reduces power consumption whenever the tag and the reader are far away one to each other. The proposed voltage limiter design takes advantage of the implemented bandgap reference and voltage regulator in order to provide low temperature and process deviation of the limiting voltage. The measured limiting voltage is 2.9V with a voltage variation of only +/-0.025V for the four measured dies. The current consumption is only 150nA when the reader and the tag are far away one to each other, not limiting the sensitivity of the tag due to an undesired consumption in the voltage limiter. The circuit is implemented on a low cost 2P4M 0.35µm CMOS technology.

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