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Wide range fully integrated VCO with new cells-based varactor

Margarita Marrero-Martin*, Benito Gonzalez, Javier Garcia, Sunil L. Khemchandani, Antonio Hernandez and Javier del Pino

ULPGC, IUMA, Campus Universitario de Tafira, Pab A – Dcho 203, Las Palmas de Gran Canaria 35019, Spain

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This article presents a wide range inductance–capacitance voltage controlled oscillator (VCO) with a unit cells-based varactor. The unit cell represents the minimum possible integrated varactor based on p–n junction diodes, where N^+ diffusions are central rectangles, surrounded by doughnut shaped P^+ diffusions, with their respective contacts. The varactors are designed using the AMS 0.35 μm BiCMOS process. A physical model has been derived from the measurement of a set of eight fabricated varactors. Measurements indicate that the VCO, which is intended to be used in DVB-H, oscillates from 1.087 to 2.032 GHz, with a 61% tuning range. The phase noises of −124 dBc/Hz at 1 MHz offset and −108 dBc/Hz at 100 kHz offset are obtained.

Keywords: VCO; capacitance model; PN varactor; BiCMOS

1. Introduction

Radio frequency (RF) communication systems demand better and cheaper devices (Tiemeijer et al. 2004) with lower power consumption and higher data transfer rates. There are modules, for example voltage controlled oscillator (VCOs), which are important in many RF applications as transceivers for wireless communication (Gu 2005).

VCOs are oscillators in which the output frequency depends on an applied external voltage. Electronic systems, which require a source of variable frequency used for clock and data recovery, frequency synthesis, and other applications, utilise these subsystems. These circuits are particularly important in phase locked loops, used for clock generation and synchronisation (Craninckx and Steayert 1995). For the implementation of these circuits silicon-based technologies are used, like SiGe or BiCMOS (Larson, Case, Rosenbaum, and Rensh 1996).

One of the most widely used architectures for high frequency is the inductance–capacitance (LC) oscillator (Hegazy, Sharaf, and Ragai 2002). LC oscillators are based on the parallel resonance of an inductor and a capacitor. Usually, a negative resistance configuration is used to compensate tank losses, and consequently maintain the oscillation. To convert the oscillator in a VCO, the most common technique is to replace the capacitor with a varactor. The phase noise of LC-tuned oscillators is much better than other configurations, because they use the band pass characteristic of the LC-tank to reduce it. Other types of oscillators, like ring oscillators, suffer from switching effects

*Corresponding author. Email: margarita@iuma.ulpgc.es

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and can introduce noise in the power supply, causing a worse phase noise than LC-tuned oscillators (Kral 1998).

Integrated varactors can be made in several ways (Pedersen 2001; Gau et al. 2005). Those implemented by metal–oxide–silicon (MOS) capacitors (MOSVAR) or p–n junction diodes (JVAR) are usually by-product devices from a standard fabrication process, which is originally for CMOS transistors (Chan, Huang, Wu, Chen, and Chao 2007). The choice of one of them will depend on the application. The keys to this choice are the Q-factor and the tuning range. Thus, the Q-factor in p–n junction diodes (JVARs) is significantly superior to that in MOS capacitors (MOSVARs), primarily due to a lower resistance, whereas the tuning range, C_{max}/C_{min}, is lower (Chan et al. 2007).

In order to design a fully integrated VCO, where the LC-tank is on chip, cells-based varactors have been designed according to the tank requirements. The Q of the tank will determine the VCO's phase noise and power consumption (Maget et al. 2003). Therefore, they will be dominated by the Q of the inductor for low frequency range, and the Q of the varactor at higher range, such as mm-wave. In our case, the cells-based varactors have been designed and modelled to operate in the gigahertz-range.

The organisation of this article is as follows. In 'Designed varactors' section, we describe the cell-based varactors, and their model is presented in next section. A fully integrated VCO using 0.35 μm SiGe technology is described in 'Designed VCO' section. The next section is devoted to the VCO 'measurement and results'. Finally, the 'conclusions' are given.

2. Designed varactors

PN-junction in JVARs is created by implanting P^+ diffusions into N-wells. As they use electrons as majority carriers, Q-factors higher than those in N^+ to P-well junctions are expected. The JVARs' capacitance is associated with the depletion area between P^+ diffusions and the well. The P^+ substrate is usually connected to ground.

Varactor capacitance is strongly dependent on layout geometry, having a great impact on large size varactors. An efficient silicon area, to decrease the device cost, is obtained by reducing the size of the varactor (Aparicio and Hajimiri 2002). Thus, layout geometry has been modified to develop some novel varactors which are different to those supplied by the foundry (García et al. 2007).

In order to obtain the required capacitance, the first step of our methodology is designing a unit cell. This unit cell represents the minimum possible integrated varactor. Its layout, whose area is $12.9 \times 11.1\ \mu m^2$, is shown in Figure 1(a): N^+ diffusions are central rectangles, surrounded by doughnut shaped P^+ diffusions, with their respective contacts. In our case, N^+ diffusions are deep enough to reach an N^+ buried layer, according to Figure 1(b), diminishing the resistance of the device.

Then, the varactors are made up of horizontal and vertically overlapping unit cells on P^+ diffusions. As an example, Figure 2 illustrates a varactor with 42 unit cells.

3. Varactor model

Eight varactors based on cells have been designed and fabricated. They have been measured on-wafer by means of a Cascade Probe Station and Vector Network Analyzer

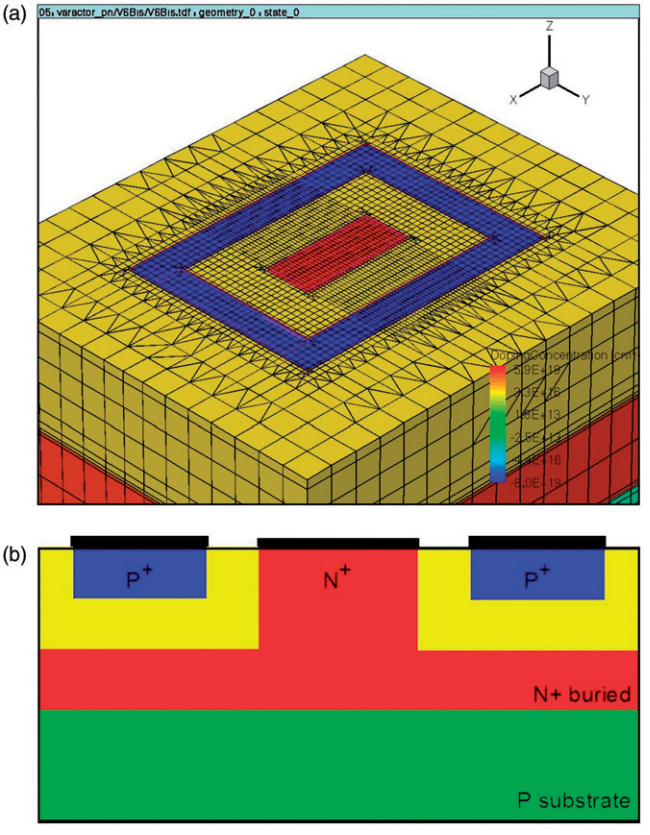

Figure 1. (a) Unit cell layout and (b) unit cell layer structure.

(Agilent 8720ES). Then, a capacitive model has been generated. Figure 3 shows the resulting equivalent circuit of varactors.

The varactor used in our VCO has 90 unit cells. All the values for the modelled components are given in Table 1.

Junctions capacitances, C_{j_1}, $C_{j_2}$and C_{j_3}, between P^+ diffusions and Nwell, substrate and N^+ buried layer, and Nwell and substrate, respectively, are modelled in the study of Marrero-Martín, García, González, and Hernández (2010) and given by

$$C_{j_k} = \frac{C_{A_k} \cdot A_k + C_{P_k} \cdot P_k}{\sqrt{1 - \frac{V}{V_{bi_k}}}} \quad k = 1, 2, 3 \tag{1}$$

where C_{A_k} and C_{P_k} are the capacitances per unit area and perimeter length of the different junctions, with area A_k and perimeter P_k, and V_{bi_k} the corresponding built-in voltage; V the applied voltage from anode to cathode.

The ground proximity effect from ports 1 and 2, C_{p_1} and C_{p_2}, and the substrate capacitance, C_s, depends on the number of cells.

With respect to resistors, R_s models the parasitic effects due to the substrate, R_{pn} the Nwell resistance, associated to the neutral region, R_{j1}, R_{j2} and R_{j3}, the resistances of every

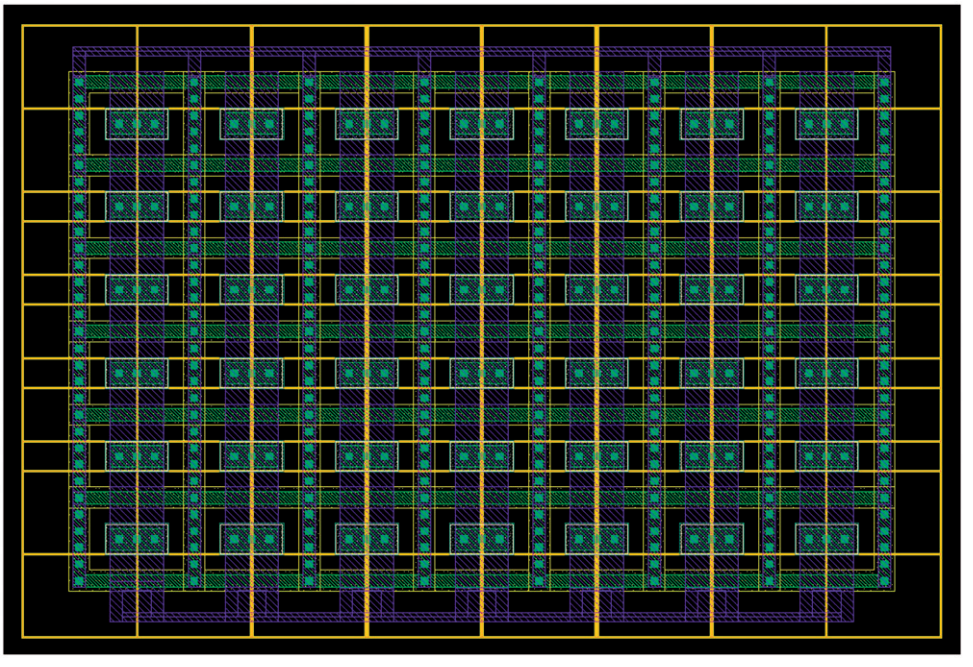

Figure 2. Varactor layout.

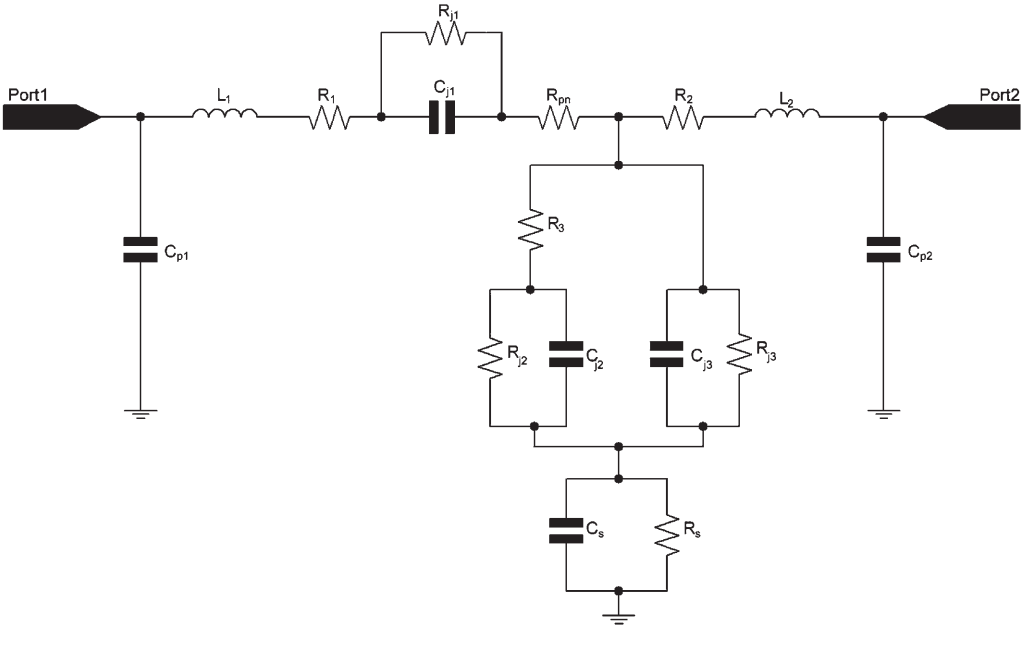

Figure 3. Inductors, resistors and capacitors of varactor equivalent circuit.

Table 1. Values of model components.

Model component	Value (Ω)	Model component	Value
R_1	0.42	C_{j_1}	1608.01 fF
R_2	0.97	C_{j_2}	702.41 fF
R_3	8e2	C_{j_3}	100.86 fF
R_{j1}	2.87e16	C_{p_1}	30 fF
R_{j2}	1.21e14	C_{p_2}	25 fF
R_{j3}	8.46e14	C_s	275.11 fF
R_s	15.84	L_1	55 pH
R_{pn}	0.2589	L_2	30 pH

depletion region in junctions, P^+ diffusions – Nwell, substrate – N^+ buried layer, and Nwell – substrate, respectively, R_1 and R_2 correspond to the resistances of interconnections on ports 1 and 2, and R_3, the resistance between Nwell and N^+ buried layer.

The inductances are associated with metal interconnections on ports 1 and 2; and exponentially depend on the number of cells.

Figure 4 represents the measured (with symbols) and modelled (with lines) capacitances of the varactor selected, from port 1 (a) and port 2 (b) in all the frequency range and an applied voltage at 0 V.

The corresponding relative error between modelled and measured capacitances from both ports is less than 8% in any case, as Figure 5 shows, where C_{11} and C_{22} errors are plotted with solid and open marks, respectively.

From Figure 6, which represents the varactor capacitance dependence on the applied voltage (from 0 to 3.3 V), at 0.88 GHz, a tuning characteristic of 33.48% is derived. Q-factor varies from 40.17 to 75.57 at the same frequency.

In order to point out the benefits of our design methodology, a varactor from AMS 0.35 μm BiCMOS library has been manufactured and measured, and compared with one of our varactors with similar capacitance. Their capacitive characteristic curves are represented in Figure 7, and Table 2 compares the relevant parameters. The tuning range is similar, around 31%. However, our varactor shows a higher quality factor and a significative lower area.

4. Designed VCO

To demonstrate the feasibility of the designed varactors, a VCO has been fabricated. The best inductor for the VCO tank is chosen with an automatic generation tool called IMODEL (Iturri, del Pino Suárez, Khemchandani, and Hernández 2008). The simplified schematic of the VCO is shown in Figure 8. This oscillator uses an LC oscillator topology, integrating all components of the tank on chip. The VCO core uses a cross-coupled transistor pair to build up the negative resistance. A differential topology provides a more stable frequency versus supply voltage characteristic, and improves the immunity to load variations. A buffer amplifier was also added to provide additional isolation from load variations and to boost the output power.

The inductors are designed so that the quality factor is the optimal one for the frequency of interest (Goñi Iturri et al. 2005), and the varactors have been selected

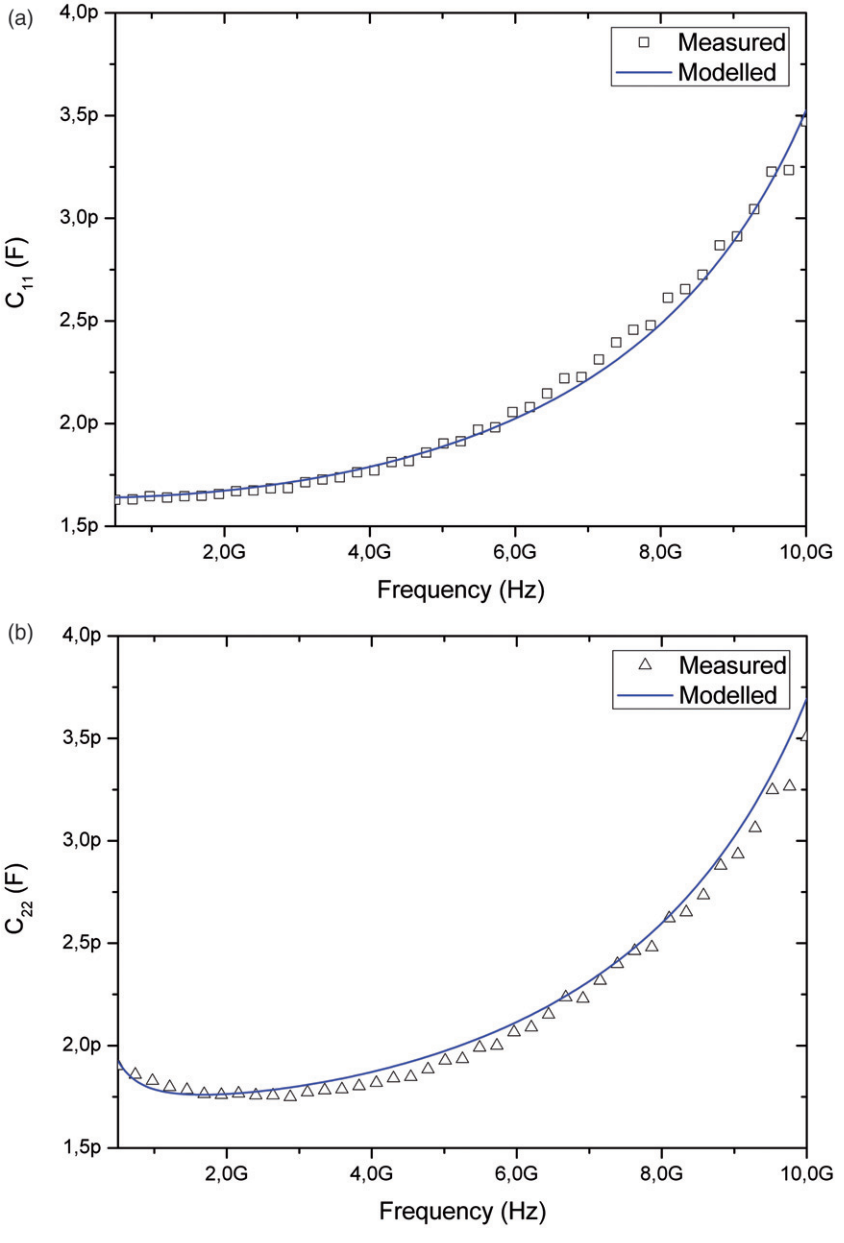

Figure 4. Capacitances versus frequency of the varactor selected from: (a) port 1 and (b) port 2.

according to our model. A voltage applied to the V_{TUNE} pin, which is connected to varactors, controls the VCO frequency.

Additionally, an array of switched capacitors is employed to increase the frequency range. It uses techniques like emitter degeneration, capacitor divider and optimum bias for minimum noise to improve phase noise requirements and oscillation amplitude (Khemchandani, del Pino, Diaz, and Hernandez 2009).

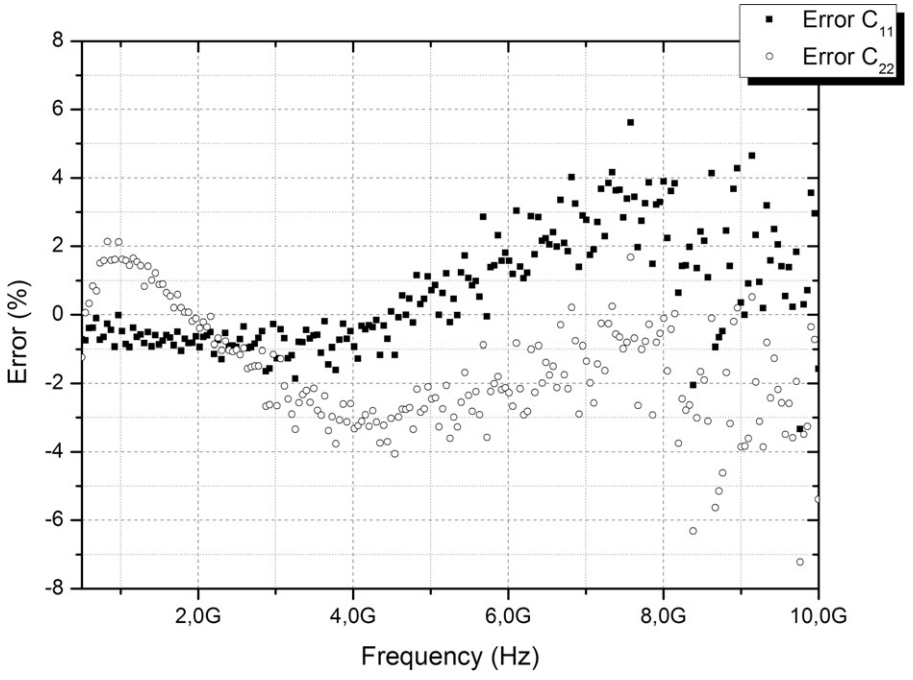

Figure 5. Relative error between measured and modelled capacitances from both ports.

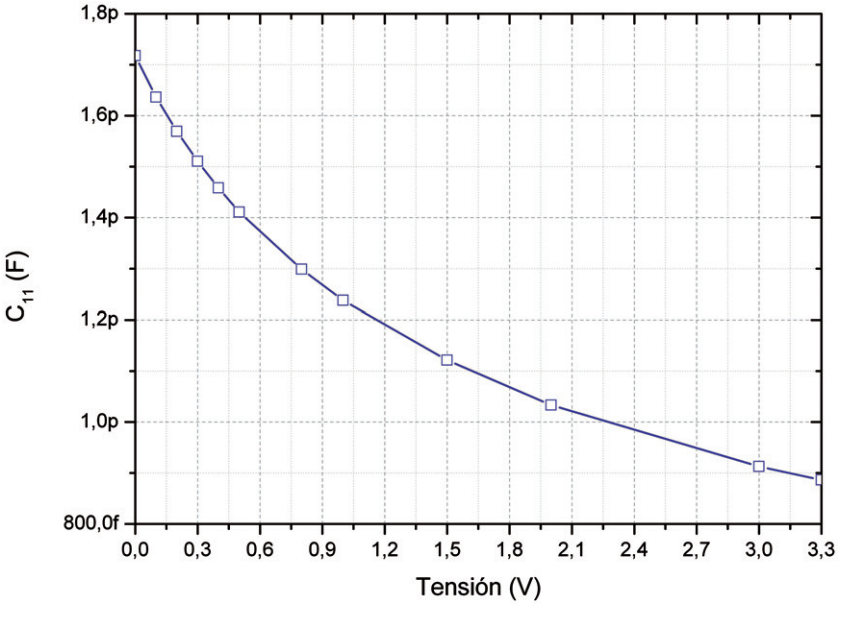

Figure 6. Capacitances from port 1 versus voltage.

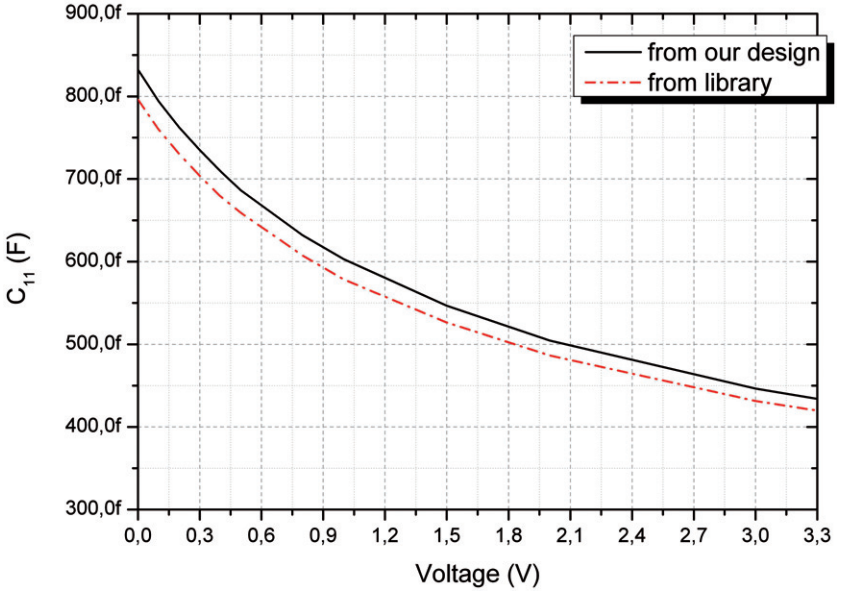

Figure 7. Capacitances from port 1 versus the applied voltage for the designed varactor and a varactor from the AMS BiCMOS library.

Table 2. Parameters of designed varactors.

	Own varactor	Library varactor
TR (%)	30.55	31.03
$Q_{\min\ (\text{at } 0.88\,\text{GHz})}$	97.84	58.14
$Q_{\max\ (\text{at } 0.88\,\text{GHz})}$	183.89	110.46
Area (μm^2)	1661.52	2120.4

The layout of the VCO, which is shown in Figure 9, is designed with the greatest possible symmetry between the two branches of the differential circuit. In order to reduce the influence of gradients of dispersion in the performance of the VCO, the elements are placed matched with a common centroid technique (Baker, Li, and Boyce 1998).

The layouts are designed to reduce the circuit area as much as possible and to introduce the minimum degradation with connecting tracks.

5. Measurement results

Measurement of the VCO was carried out on-wafer with 35 GHz signal-ground-signal (SGS) probes, using a Cascade SUMMIT 9000 probe station with an optical microscope Olympus SZ-CTV, and the 26.5 GHz Agilent E4440A spectrum analyser with phase noise measurement personality.

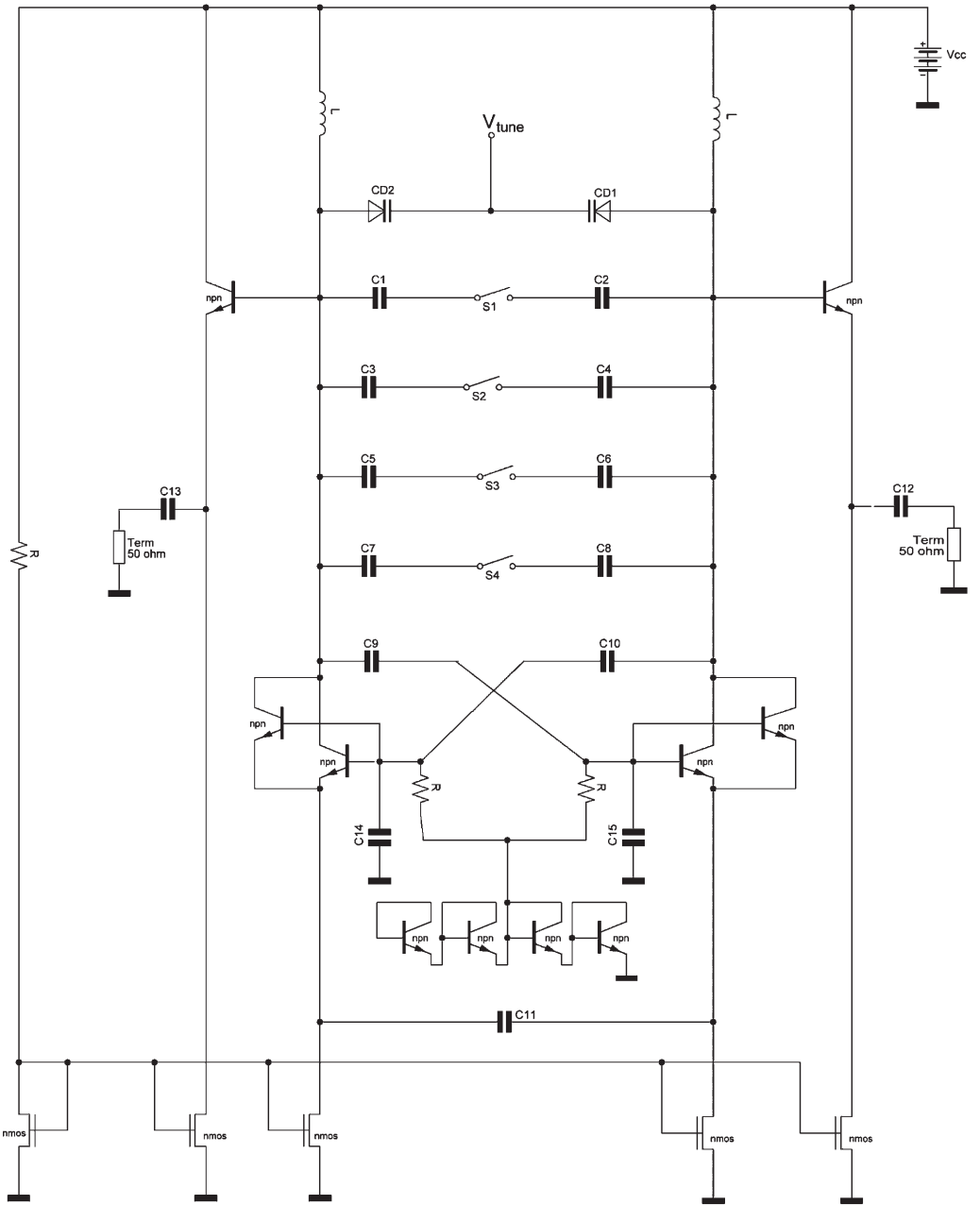

Figure 8. VCO schematic.

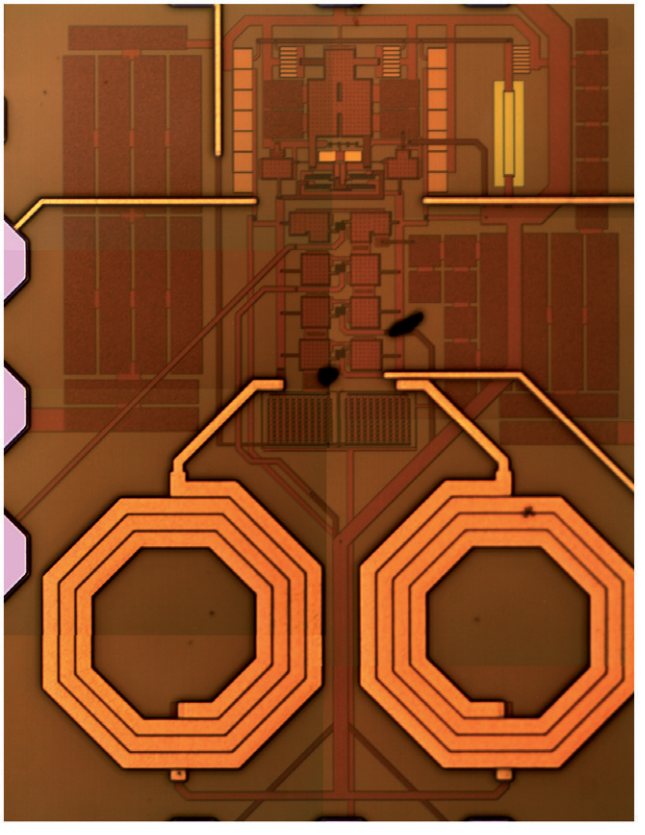

Figure 9. VCO layout.

Figure 10 shows the VCO tuning range and overlapping regions of the five subbands. VCO oscillates from 1087 to 2032 MHz, using only one core. The measured tuning range is 61% around 1.56 GHz, and the total chip area is 0.841 mm^2.

The VCO spectrum, when V_{TUNE} is set to 3.3 V and all switched capacitors (S1, S2, S3 and S4) are connected (Figure 8), was also measured and represented in Figure 11. Notice that a central frequency of 1087 MHz is derived.

As Figure 12 shows, the phase noises of −124 dBc/Hz at 1 MHz offset and −108 dBc/Hz at 100 kHz offset are obtained.

Finally, Table 3 compares the performance of our VCO with other published integrated VCOs (Herzel, Erzgraber, and Ilkov 2000; Tiebout 2002; Li and Kenneth 2003; Antoine et al. 2005; Berny, Niknejad, and Meyer 2005; Sung, Lee, Baek, Kim, and Park 2005). It oscillates in the same band by means of a figure of merit (FoM) according to the following formula

$$\mathrm{FoM} = 10 \cdot \log\left(\frac{f_{\max} - f_{\min}}{\Delta f}\right)^2 - 10 \cdot \log L(\Delta f)$$

where $f_{\max}$ and $f_{\min}$ are the maximum and minimum frequencies, Δf the offset frequency and $L(\Delta f)$ the phase noise at Δf. The combination of low phase noise and tuning range give

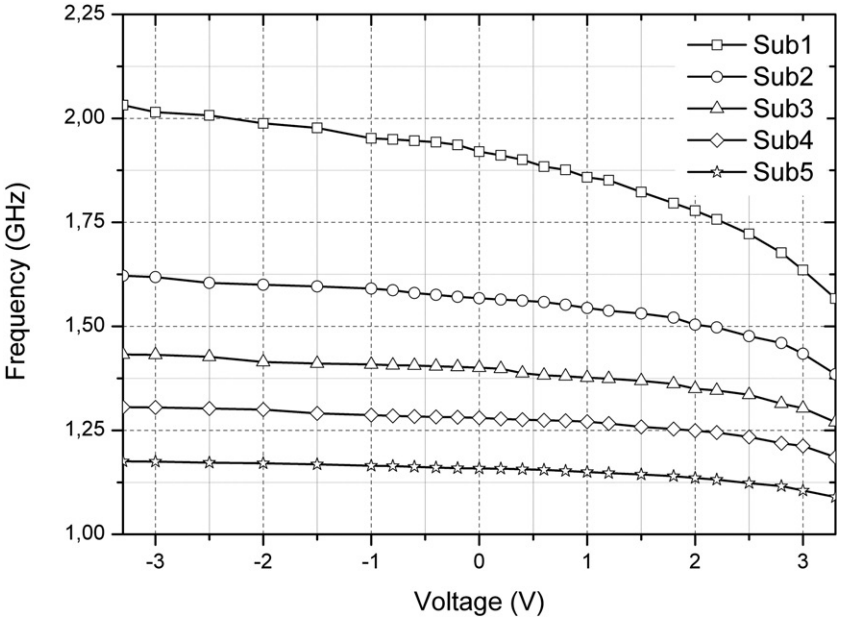

Figure 10. VCO tuning range.

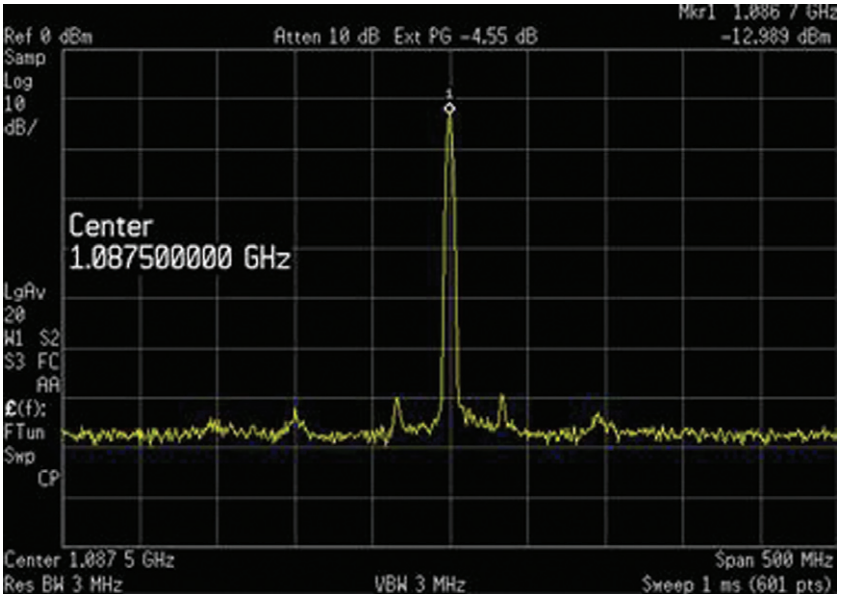

Figure 11. VCO spectrum with a 500 MHz span.

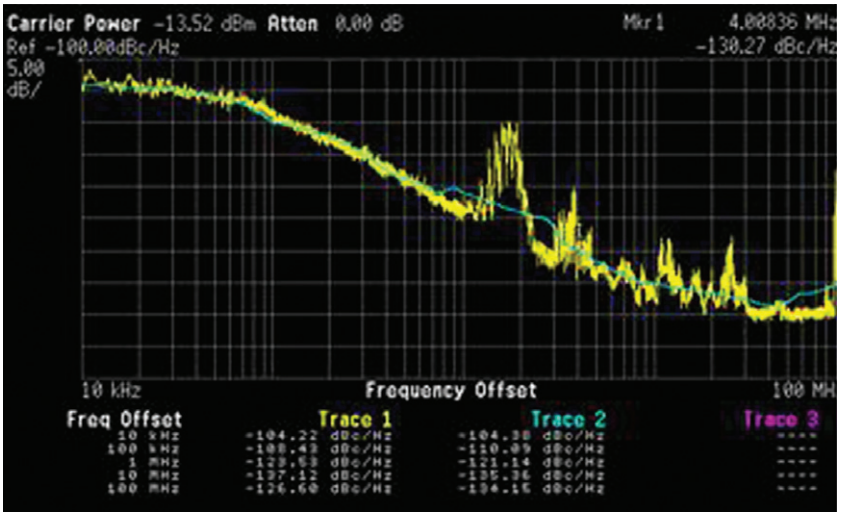

Figure 12. VCO measured phase noise for a 1087 MHz oscillation frequency.

Table 3. Comparison with published wide-band VCOs.

Author	L (1 MHz) dBc/Hz	Tuning range (%)	Band (MHz)	Technology (μm)	FoM (dB)	Type of varactor	Number of cores
This study	−124	61	1087–2032	BiCMOS 0.35	183.03	PN	Single core
Berny et al. (2005)	−126.50	72.20	1150–2450	CMOS 0.18	188.78	MOS	Single core
Herzel et al. (2000)	−116	46	1340–2140	CMOS 0.35	174.01		Single core
Li and Kenneth (2003)	−124	53.60	667–1156	CMOS 0.18	177.78	MOS	Single core
Sung et al. (2005)	−131	63.11	900–1730	CMOS 0.18	189.38	MOS	Single core
Antoine et al. (2005)	−135	82.10	420–1005	BiCMOS 0.35	176.88	MOS	Three cores
Tiebout (2002)	−127	69	978–2010	CMOS 0.25	175.97	MOS	Single core

to our design a good classification, even better than (Antoine et al. 2005), which uses a three-core VCO. The VCO with the best FoM (Sung et al. 2005) uses an external high Q inductor (it is not fully integrated).

6. Conclusions

In this article, we have modelled new cell-based varactors. The varactors are p–n junction diodes, designed using the AMS 0.35 μm BiCMOS process. A set of eight varactors has been fabricated and measured to test the varactors and validate the proposed physical model. One LC VCO was also fabricated and measured. The frequency range is from 1.087 to 2.032 GHz, with a 61% tuning range, and the phase noise is −124 dBc/Hz at 1 MHz offset. The proposed VCO exhibits a good FoM compared to other fully integrated VCOs operating in the same band.

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