Wide range fully integrated VCO with new cells-based varactor

ABSTRACT

This paper presents a wide range LC voltage controlled oscillator with a unit cells-based varactor. The unit cell represents the minimum possible integrated varactor based on p-n junction diodes, where N^+ diffusions are central rectangles, surrounded by doughnut shaped P^+ diffusions, with their respective contacts. The varactors are designed using the AMS 0.35 µm BiCMOS process. A physical model has been derived from the measurement of a set of eight fabricated varactors. Measurements indicate that the VCO oscillates in DVB-H standard, from 1.087 GHz to 2.032 GHz, with a 61% tuning range; the phase noise is -124 dBc/Hz at 1 MHz offset.

Keywords: VCO, capacitance model, PN varactor, BiCMOS.

I. INTRODUCTION

RF communication systems demand better and cheaper devices [1] with lower power consumption and higher data transfer rates. There are modules, for example VCOs, which are important in many radio frequency applications as transceivers for wireless communication [2].

VCOs are oscillators in which the output frequency depends on an applied external voltage. Electronic systems, which require a source of variable frequency used for clock and data recovery, frequency synthesis, and other applications, utilize these subsystems. These circuits are particularly important in PLLs, used for clock generation and synchronization [3]. For the implementation of these circuits silicon based technologies are used, like SiGe or BiCMOS [4].

One of the most widely used architectures for high frequency is the LC oscillator [5]. LC oscillators are based on the parallel resonance of an inductor and a capacitor. Usually, a negative resistance configuration is used to compensate tank losses, and consequently maintain the oscillation. To convert the oscillator in a VCO, the most common technique is to replace the capacitor with a varactor. The phase noise of LC-tuned oscillators is much better than other configurations, because they use the band pass characteristic of the LC-tank to reduce it. Other types of oscillators, like ring oscillators, suffer from switching effects and can introduce noise in the power supply, causing a worse phase noise than LC-tuned oscillators [6].

Normally, integrated varactors implemented by MOS capacitors (MOSVAR) or p-n junction diodes (JVAR) are usually by-product devices from a standard fabrication process, which is originally for CMOS transistors [7]. Integrated varactors can be implemented in several ways [8,9]. The choice of one of them will depend on the application. The keys to this choice are the *Q*-factor and the tuning range. Thus, the *Q*-factor in p-n junction diodes (JVARs) is significantly superior to that in MOS capacitors (MOSVARs), primarily due to a lower resistance, whereas the tuning range, C_{max}/C_{min}, is lower [7].

The varactor quality factor, which is coupled along with the inductor *Q*-factor, will determine the VCO´s phase noise and power consumption [10]. In order to design a fully integrated VCO, where the LC-tank is on chip, the varactors have been designed according to the tank requirements.

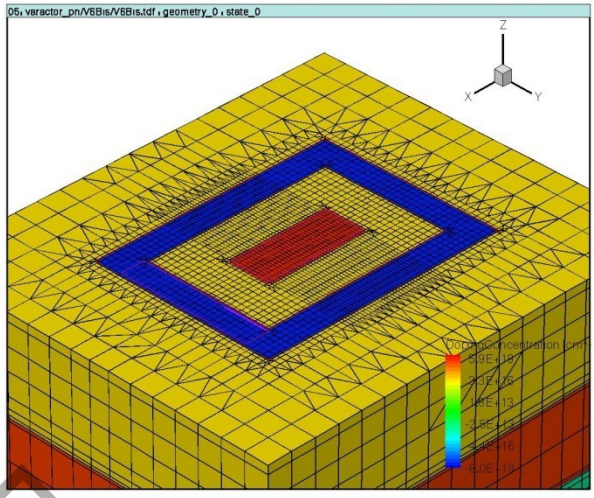
The organization of this paper is as follows. In Section II we describe the cell-based varactors, and their model is presented in Section III. A fully integrated VCO using 0.35 μm SiGe technology is described in Section IV. The next section is devoted to the VCO measurement and results. Finally, the conclusions are given in Section VI.

II. DESIGNED VARACTORS

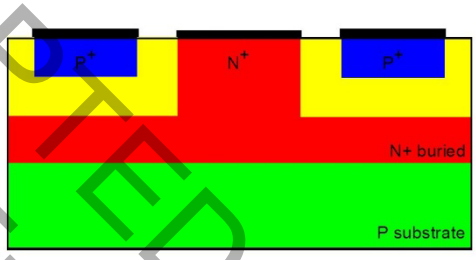
PN-junction in JVARs is created by implanting P^+ diffusions into N-wells. As they use electrons as majority carriers, *Q*-factors higher than those in N^+ to P-wells junctions are expected. The JVARs' capacitance is associated with the depletion area between P^+ diffusions and the well. The P^+ substrate is usually connected to ground.

Varactor capacitance is strongly dependent on layout geometry, having a great impact on large size varactors. An efficient silicon area, to decrease the device cost, is obtained by reducing the size of the varactor [11]. Thus, layout geometry has been modified to develop some novel varactors which are different to those supplied by the foundry [12].

In order to obtain the required capacitance, the first step of our methodology is designing a unit cell. This unit cell represents the minimum possible integrated varactor. Its layout, whose area is 12.9 × 11.1 μm^2, is shown in Figure 1(a): N^+ diffusions are central rectangles, surrounded by doughnut shaped P^+ diffusions, with their respective contacts. In our case, N^+ diffusions are deep enough to reach an N^+ buried layer, according to Figure 1(b), diminishing the resistance of the device.



(a)



(b)

Figure 1. (a) Unit cell layout. (b) Unit cell layer structure.

Then, the varactors are made up of horizontal and vertically overlapping unit cells on P^+ diffusions. As an example, Figure 2 illustrates a varactor with 42 unit cells.

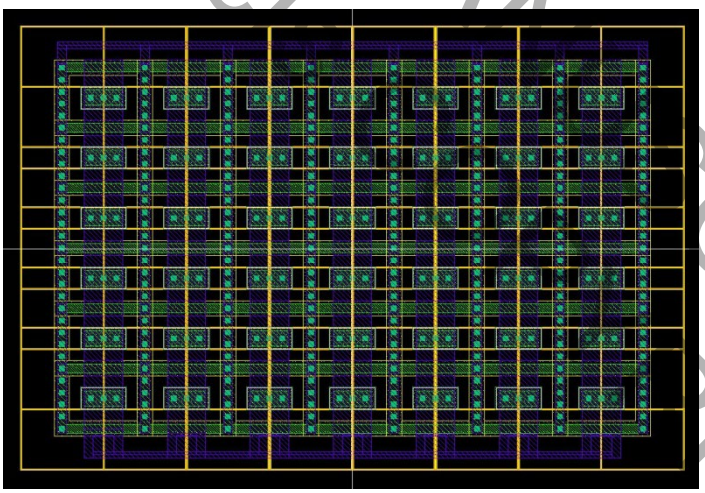


Figure 2. Varactor layout.

III. VARACTOR MODEL

Eight varactors based on cells have been designed and fabricated. They have been measured on-wafer by means of a Cascade Probe Station and Vector Network Analyzer (Agilent 8720ES). Then, a capacitive model has been generated. Figure 3 shows the resulting equivalent circuit of varactors.

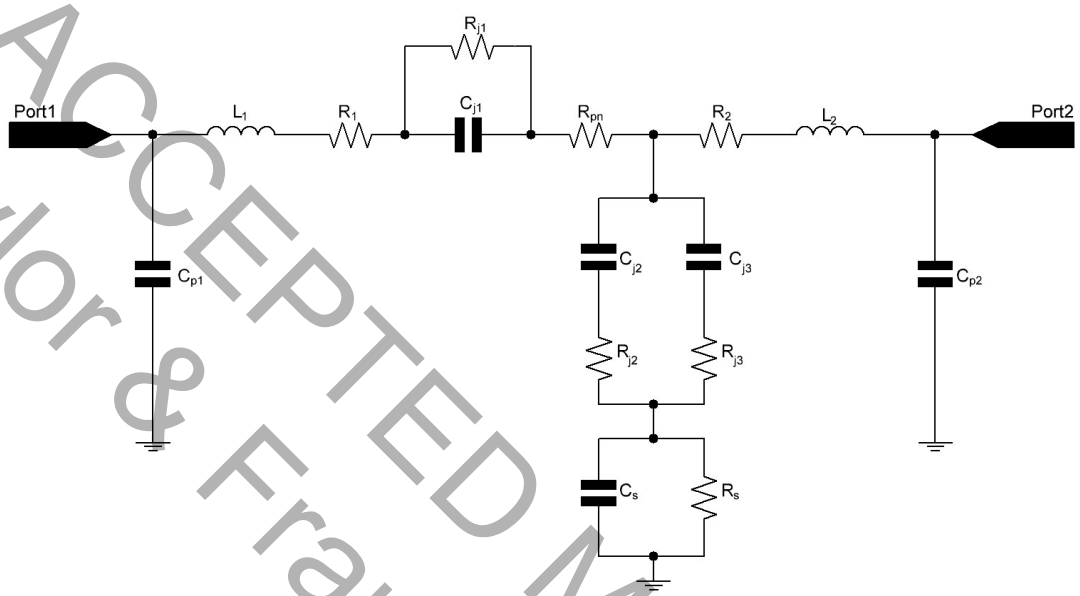


Figure 3. Inductors, resistors and capacitors of varactor equivalent circuit.

The varactor used in our VCO has 90 unit cells. All model components are shown in Table I.

TABLE I. VALUES OF MODEL COMPONENTS.

Model component	Value		Model component	Value
C_{j_1}	1608.01 fF		R_1	0.54 Ω
C_{j_2}	702.41 fF		R_2	0.97 Ω
C_{j_3}	100.86 fF		R_{j1}	2.87e16 Ω
C_{p_1}	30 fF		R_{j2}	1.21e14 Ω
C_{p_2}	125 fF		R_{j3}	8.46e14 Ω
C_s	275.11 fF		R_s	15.84 Ω
L_1	38 pH		R_{pn}	0.2589 Ω
L_2	49 pH			

Junctions capacitances, C_{j_1}, C_{j_2} and C_{j_3}, between P^+ diffusions and Nwell, substrate and N^+ buried layer, and Nwell and substrate respectively, have been modelled in [13] and are given by

$$C_{j_k} = \frac{C_{A_k} \cdot A_k + C_{P_k} \cdot P_k}{\sqrt{1 - \frac{V}{V_{bi_k}}}} \quad k = 1,2,3. \qquad (5)$$

where C_{A_k} and C_{P_k} are the capacitances per unit area and perimeter length of the different junctions, with area A_k and perimeter P_k, and V_{bi_k} is the corresponding built-in voltage; V is the applied voltage from anode to cathode.

The inter-metal parasitic capacitances, C_{p_1} and C_{p_2}, and the substrate capacitance, C_s, linearly depends on the number of cells.

With respect to resistors, R_s models the parasitic effects due to the substrate, R_{pn} is the Nwell resistance, associated to the neutral region, R_{j_1}, R_{j_2} and R_{j_3}, are the resistances of every depletion region in junctions, P^+ diffusions - Nwell, substrate - N^+ buried layer, and Nwell - substrate respectively, and R_1 and R_2 correspond to the resistances of interconnections on ports1 and 2.

The inductances are associated with metal interconnections on ports 1 and 2; and exponentially depend on the number of cells.

For all range of frequencies, figure 4 represents the measured (with symbols) and modelled (with lines) capacitances from port 1, and figure 5, those from port 2.

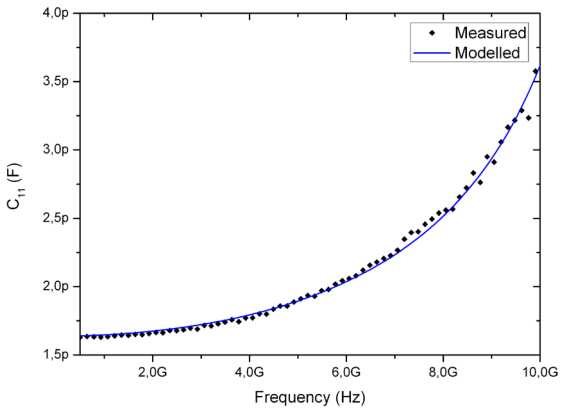


Figure 4. Capacitances from port 1 *vs* frequency of the selected varactor.

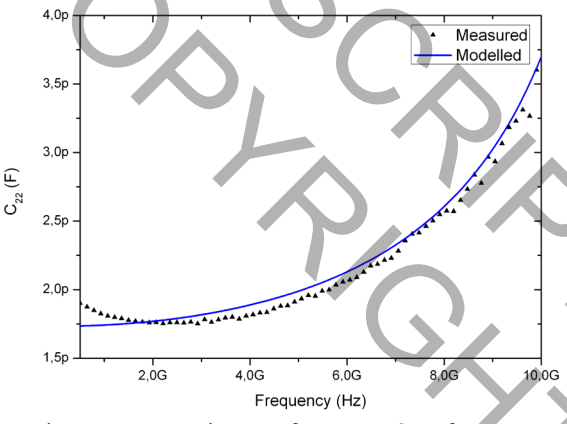


Figure 5. Capacitances from port 2 *vs* frequency of the same varactor.

The relative error between modelled and measured capacitances from both ports is less than 10% in any case, as shown in figure 6. C_{11} error is plotted with solid marks, and C_{22} error, open marks.

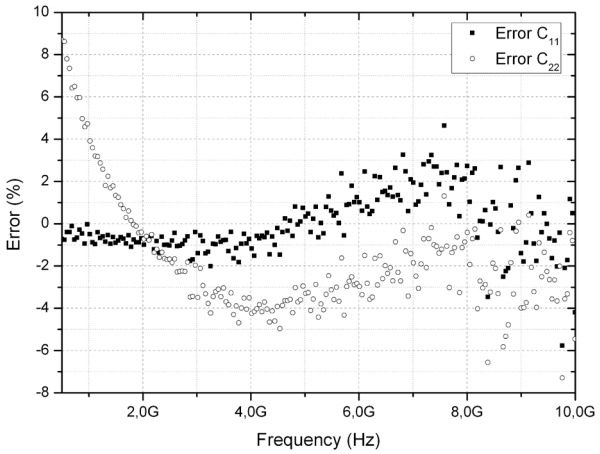
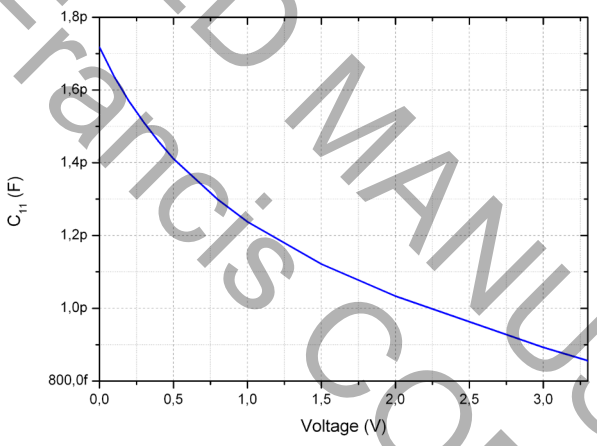


Figure 6. Error (%) between measured and modelled capacitances from both ports.

As the basic performance of the varactor, the tuning characteristic of the designed varactor is 33.48%. Figure 7 represents this varactor capacitance characteristic versus the variation of the voltage (from 0 to 3.3V) at 0.88 GHz. Q-factor varies from 40.17 to 75.57 at the same frequency.

Figure 7. Capacitances from port1 versus voltage.



To make a comparison between our varactors and those defined in technology kit has been included in RUN manufacturing two varactors: a own varactor and a library varactor with capacitances very similar, as shown in Figure 8 . The tuning range is similar although slightly higher in the library, 31.03% versus 30.55%. Instead, the quality factor at a frequency of 0.88 GHz is higher in our varactor due to less resistance because of its lower area. All these parameters are given in Table II.

TABLE II. PARAMETERS OF VARACTORS.

Parameters	Own varactor	Library varactor
TR	30.55%	31.03%
Q_{min}	58.14	97.84
Q_{max}	110.46	183.89
Area (μm^2)	2120.4	1661.52

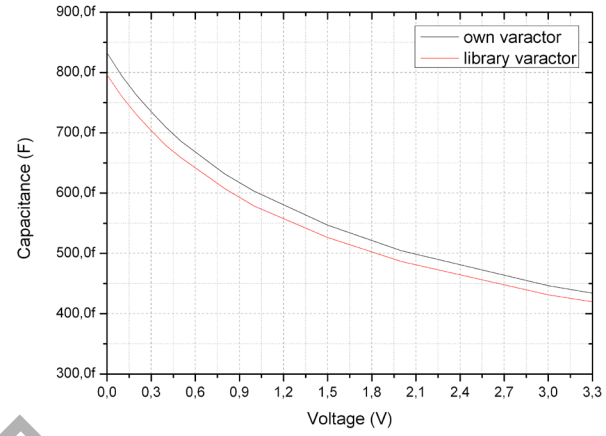


Figure 8. Capacitances from port1 versus voltage.

IV. DESIGNED VCO

To demonstrate the feasibility of the designed varactors, a VCO has been fabricated. The best inductor for the VCO tank is chosen with an automatic generation tool called IMODEL [14]. The simplified schematic of the VCO is shown in Figure 9. This oscillator uses an LC oscillator topology, integrating all components of the tank on chip. The VCO core uses a cross-coupled transistor pair to build up the negative resistance. A differential topology provides a more stable frequency versus supply voltage characteristic, and improves the immunity to load variations. A buffer amplifier was also added to provide additional isolation from load variations and to boost the output power.

The inductors are designed so that the quality factor is the optimal one for the frequency of interest [15], and the varactors have been selected according to our model (1,2). A voltage applied to the V_{TUNE} pin, which is connected to varactors, controls the VCO frequency.

Additionally, an array of switched capacitors is employed to increase the frequency range. It uses techniques like emitter degeneration, capacitor divider, and optimum bias for minimum noise to improve phase noise requirements and oscillation amplitude [16].

The layout of the VCO, which is shown in Figure 10, is designed with the greatest possible symmetry between the two branches of the differential circuit. In order to reduce the influence of gradients of dispersion in the per formance of the VCO, the elements are placed matched with a common centroid technique [17].

The layouts are designed to reduce the circuit area as much as possible and to introduce the minimum degradation with connecting tracks.

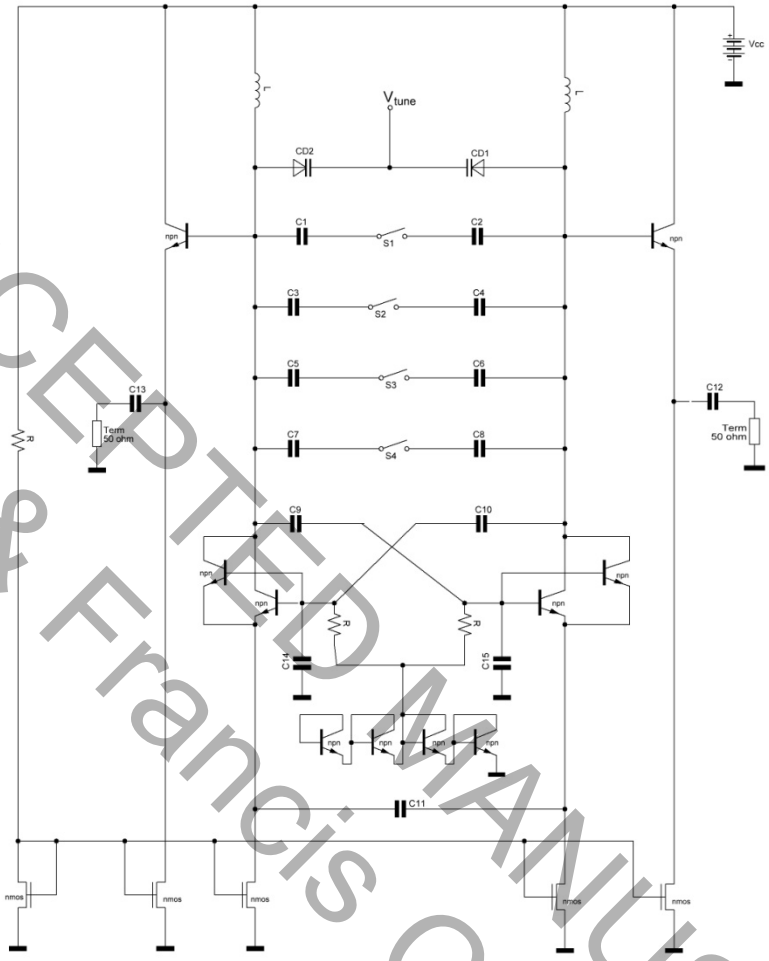


Figure **9**. VCO schematic.

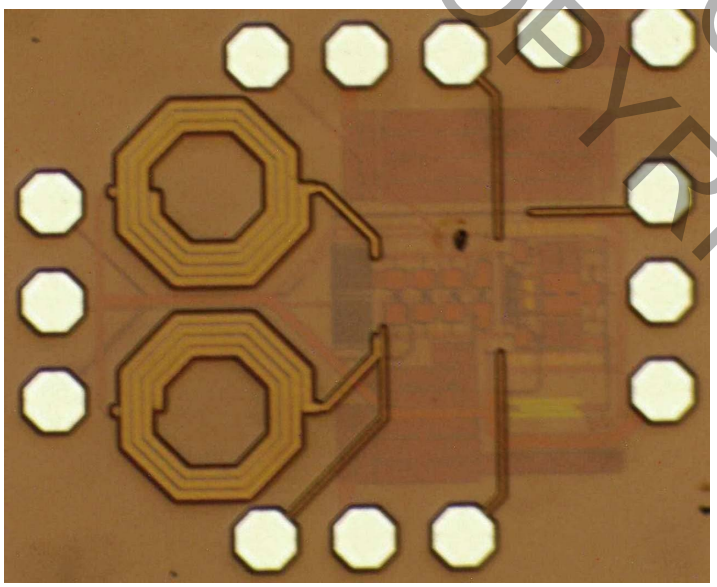


Figure 10. VCO layout.

V. MEASUREMENT RESULTS

Measurement of the VCO was carried out on-wafer with 35 GHz signal-ground-signal (SGS) probes, using a Cascade SUMMIT 9000 probe station with an optical microscope Olympus SZ-CTV, and the 26.5 GHz Agilent E4440A spectrum analyser with phase noise measurement personality.

Figure 11 shows the VCO tuning range and overlapping regions of the five sub-bands. VCO oscillates from 1087 MHz to 2032 MHz using only one core. The measured tuning range is 61% around 1.56 GHz, and the total chip area is 0.841 mm^2.

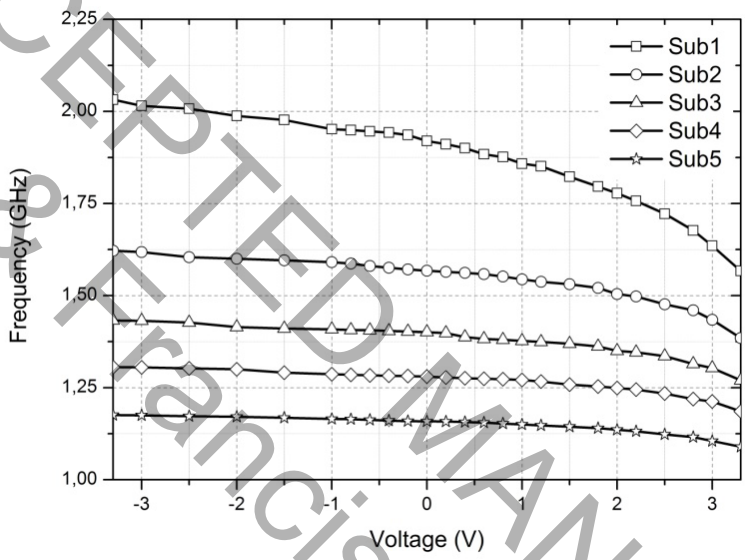


Figure 11. VCO tuning range.

The obtained VCO spectrum is shown in figure 12, in it, the central frequency is 1087 MHz. In this case, V_{TUNE} pin is connected to 3.3V, equal than S1, S2, S3 and S4. (see figure 9).

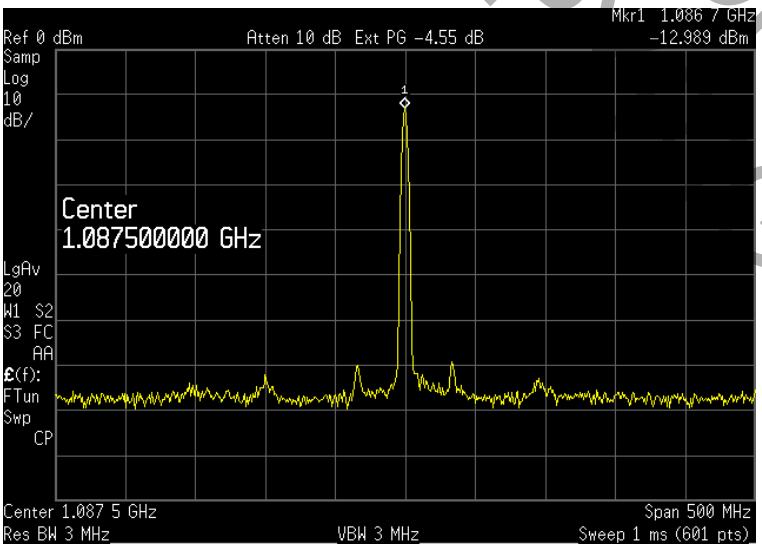


Figure 12. VCO spectrum with a 500 MHz span.

As Figure 13 shows, offsets of –124 dBc/Hz at 1 MHz and –108 dBc/Hz at 100 KHz are obtained.

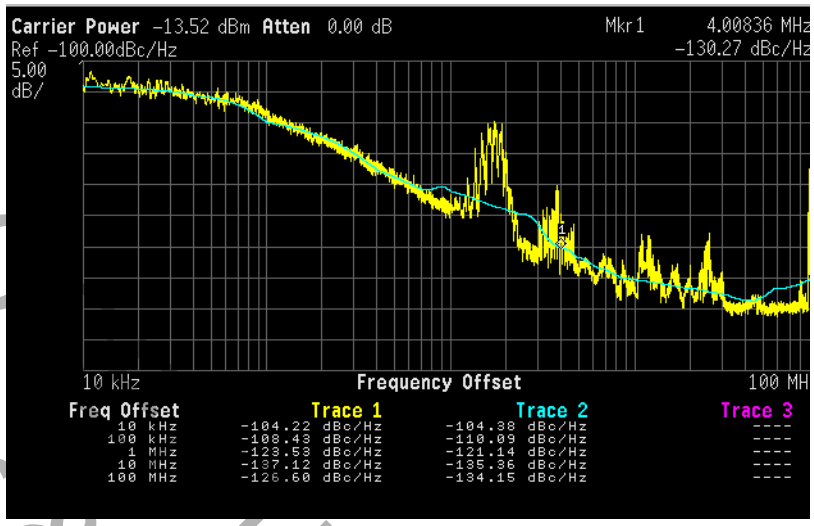


Figure 13. VCO measured phase noise for a 1087 MHz oscillation frequency.

Table III compares the performance of our VCO with other published integrated VCOs; it oscillates in the same band by means of a figure of merit (*FoM*) according to the following formula:

$$FoM = 10 \cdot \log\left(\frac{f_{max} - f_{min}}{\Delta f}\right)^2 - 10 \cdot \log L(\Delta f) \quad (7)$$

where f_{max} and f_{min} are the maximum and minimum frequencies, Δf is the offset frequency, and $L(\Delta f)$ is the phase noise at Δf.

As shown in Table II, the combination of low phase noise and tuning range give to our design a good classification, even better than [22], which uses a three-core VCO. The VCO with the best *FoM* [21] uses an external high *Q* inductor (it is not fully integrated).

TABLE III. COMPARISON WITH PUBLISHED WIDE-BAND VCOS

Author	L(1 MHz) dBc/Hz	Tuning range %	Band MHz	Technology µm	FoM dB	Type of varactor	Number of cores
This work	–124	61	1087–2032	BiCMOS 0.35	183.03	PN	Single core
[18]	–126.50	72.20	1150–2450	CMOS 0.18	188.78	MOS	Single core
[19]	–116	46	1340–2140	CMOS 0.35	174.01		Single core
[20]	–124	53.60	667–1156	CMOS 0.18	177.78	MOS	Single core
[21]	–131	63.11	900–1730	CMOS 0.18	189.38	MOS	Single core
[22]	– 135	82.10	420–1005	BiCMOS 0.35	176.88	MOS	Three cores
[23]	–127	69	978–2010	CMOS 0.25	175.97	MOS	Single core

VI. CONCLUSIONS

In this paper we have modelled new cells-based varactors. The varactors are p-n junction diodes, designed using the AMS 0.35 µm BiCMOS process. A set of eight varactors has been fabricated and measured to test the varactors and validate the proposed physical model. One LC VCO was also fabricated and measured. The frequency range is from 1.087 GHz to 2.032 GHz, with a 61% tuning range, and the phase noise is –124 dBc/Hz at 1 MHz offset. The proposed VCO exhibits a good *FoM* compared to other fully integrated VCOs operating in the same band.

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