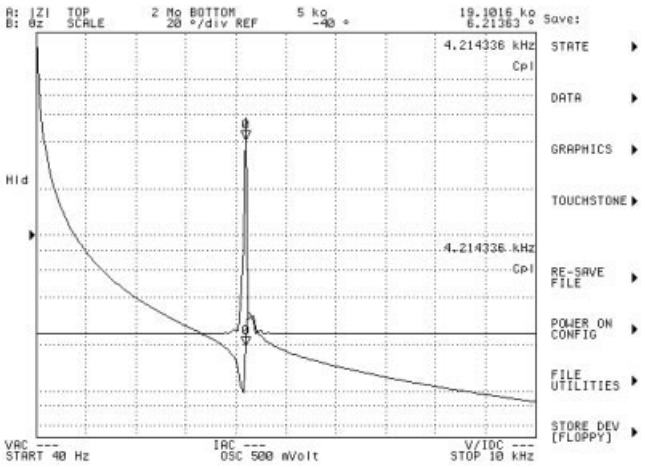
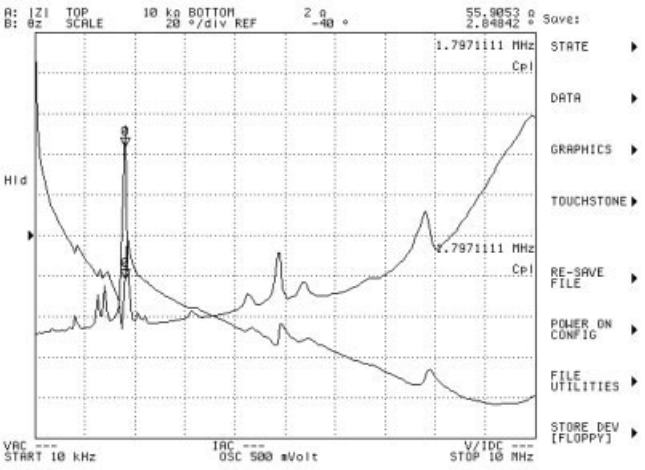


(a) first mode around 4 kHz



(b) second mode around 1.8 MHz

Figure 3 Resonance of the cantilever

of the tuned circuit is 2×10 mm^2. The cantilever is fixed in its position by conductive silver conductive epoxy [7].

3. MEASUREMENTS AND ANALYSIS

The device has been measured using a network analyzer up to 40 GHz. CPW to microstrip transition is used for the RF probes measurements. The measured return loss coefficients as a function of frequency are shown in Figure 2. At zero-bias, the spacing between the fixed shunt microstrip line and the movable bender assumes it is minimum value and the coupling assumes its maximum value. In this case, the electrodes are separated by 250 μm. With bias, the movable electrode is raised and the coupling decreases because of the increase in gap. The tuning range achievable with the present concept does not depend on the short and long range surface nonplanarities, that is, roughness and warpage as in [8]. The tuning voltage may be reduced in future versions by using multilayer actuators.

Furthermore, we compare the present data with several recent literature examples as shown in Table 1. These data illustrate that this work reports the highest quality factor preserving a moderate tunability and required a low technological effort for fabrication.

3.1. Mechanical Characterization

The following experiment setup is set to characterize the mechanical resonance frequency: the bender is fixed into a metal base with an adhesive by adjusting the free length to ~9 mm and measuring the impedance characteristic with the Agilent 4294 by using low-voltage conditions. Connecting the bender with wires, about 4 cm long to the Agilent. The measurement results are shown in Figure 3. What can be observed is that there are two main resonance frequency, one at about 1.8 MHz and the other at 4.2 kHz. The bending mode is at 4.2 kHz. More important is that no distinct resonance can be noticed in the band up to 4 MHz. So in other words, the bender is only like a capacitor up to 4 MHz.

4. CONCLUSIONS

Tunable resonator using a macro PZT-based MEMS is introduced. The device shows a moderate tunability with the highest reported continuous tunable piezoelectric based devices. One of the coupled microstrip lines is replaced by a macro MEMS piezoelectric actuator. When bias is applied, the coupling between the two lines is tuned, and by consequence, the center frequency is shifted. The bender was fixed at one end with a free length of approximately around 9 mm, resonance can be observed at about 4 kHz and 1.8 MHz. No bending at higher frequencies is observed when the cantilever is driven by a radio frequency signal.

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A FULLY INTEGRATED SINGLE CORE VCO WITH A WIDE TUNING RANGE FOR DVB-H

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ABSTRACT: *This article presents a fully integrated LC VCO in a low cost 0.35 μm BiCMOS technology for DVB-H standard. The VCO was designed for a direct conversion receiver architecture. To facilitate the integration of inductors and capacitors, the circuit oscillates at twice the required UHF frequency. Techniques like emitter degeneration, capacitor divider, and optimum bias and tank design have been used to improve phase noise requirements. The obtained phase noise is −112*

dBc/Hz at 100 kHz offset and the tuning range is 47.6%. © 2009 Wiley Periodicals, Inc. Microwave Opt Technol Lett 51: 1338–1343, 2009; Published online in Wiley InterScience (www.interscience.wiley.com). DOI 10.1002/mop.24318

Key words: *digital video broadcasting-handheld (DVB-H); direct conversion receiver; voltage controlled oscillator (VCO); phase noise; integrated inductor*

1. INTRODUCTION

Digital video broadcasting-handheld (DVB-H) technology adapts the digital video broadcasting-terrestrial (DVB-T) system for digital terrestrial television to the specific requirements of handheld, battery-powered receivers. DVB-H can offer a downstream channel at high data rates that can be used standalone or as an enhancement of mobile telecoms networks which many typical handheld terminals are able to access anyway [1, 2].

This article deals with the design of the RF part of a DVB-H transceiver, particularly with the design of a fully integrated voltage controlled oscillator (VCO), which is the synthesizer key element. In the last years, VCO research has largely focused on optimizing phase noise, but not on tuning range. However, several applications need wideband VCOs with low phase noise. An example of this is DVB-H. The goal of this work is to design a single core, low phase noise and wide tuning range (>30%) VCO for DVB-H in a low cost 0.35 μm BiCMOS technology. In this article, the use of different techniques to minimize the overall VCO phase noise will be employed.

The organization of this article is the following. In section II the DVB-H standard is described, including some calculations to obtain VCO specifications. Section III deals with the VCO design. The next section is devoted to the VCO layout implementation and measurement results discussion. Finally, some conclusions are given in section V.

2. DVB-H STANDARD AND VCO SPECIFICATIONS

DVB-H standard works in the IV and V of UHF bands, from 470 to 862 MHz. The relationship between the channel center frequency and the channel number (N) is the following:

$$f_o = (470 + 4 + (N - 21)\cdot 8)\text{MHz}, N = 21,\ldots,69 \qquad (1)$$

The channel separation is 8 MHz and the channel bandwidth is 7.61 MHz. In case that mobile communications under the standard GSM 900 is used in the same terminal as DVB-H, the usable frequency range is limited to channel 49 (698 MHz).

For the receiver, direct conversion architecture has been selected, thus only one phase locked loop (PLL), working at the channel center frequency, should be designed. In addition, it also avoids the need for an off-chip image reject filter. In double conversion architectures, two different PLLs are needed, one fixed at the higher possible frequency, and the other, at a lower frequency, which is in charge of channel selection. Both PLLs are easier to design than the one proposed here, however the complete receiver would have more power consumption and larger area. On the other hand, the direct conversion architecture suffers from drawbacks such as local oscillator leakage (self-mixing effect) and frequency pulling that appears because the synthesizer operates at the RF signal frequency. Generally, the proposed direct conversion solution is cheaper than the double conversion architecture, so the VCO frequency range is from 474 to 858 MHz.

VCO phase noise limits the receiver selectivity and its specification can be calculated from maximum interferer signal in the N+1 channel. This happens for an analog PAL-G interferer channel as shown in Figure 1 [1].

A 27 dB signal to interferer ratio (SIR) has been selected, 8 dB greater than the carrier to noise ratio (C/N) for the worst case described in the standard, which is 19.2 dB.

The maximum phase noise at 4 MHz offset is:

$$L(4MHz) = P_{WS} - P_{IS} - \text{SIR} - 10\cdot\log(B) = -138\text{dBc/Hz} \qquad (2)$$

where P_{WS} and P_{IS} are the wanted and interferer signals power. Assuming that this value is in the $1/f^2$ part of the phase noise curve according to Leeson [3], the slope is -20 *dB/dec*. This gives a phase noise requirement of -103 dBc/Hz at 100 kHz offset.

3. VCO DESIGN

The VCO was designed using Austria Mikro Systeme BiCMOS 0.35 μm technology with SiGe HBTs as active devices. These HBTs are npn bipolar transistors with a thin pseudomorphically grown $Si_{1-X}Ge_X$ alloy layer as the base.

The VCO is implemented as an LC oscillator topology [4], integrating all the components of the tank on-chip. The phase noise of LC-tuned oscillators is much better than other configurations because they use the band pass characteristic of the LC-tank to reduce the phase noise. Other type of oscillators, like ring oscillators, suffer from switching effects and they can introduce noise in the power supply, having a worse phase noise than LC-tuned oscillators.

A simplified schematic of the VCO is shown in Figure 2. The core uses a cross-coupled transistor pair to build-up the negative resistance. A differential topology provides a more stable frequency versus supply voltage characteristic and improves the immunity to load variations. A buffer amplifier was also added to provide additional isolation from load variations and to boost the output power. A voltage applied to the V_{TUNE} pin, which is connected to the varactors, controls the VCO frequency. Also, an array of switched capacitors was employed to sweep the whole frequency range.

The close-in phase noise behaviour at an offset Δf from the carrier frequency f_o of a differential LC tuned VCO is given by Leeson's model [3]:

$$L(\Delta f) = \frac{2\cdot K\cdot T\cdot R\cdot F}{V_o^2}\left(\frac{f_o}{2\cdot Q\cdot \Delta f}\right)^2\left(1+\frac{f_c}{\Delta f}\right) \qquad (3)$$

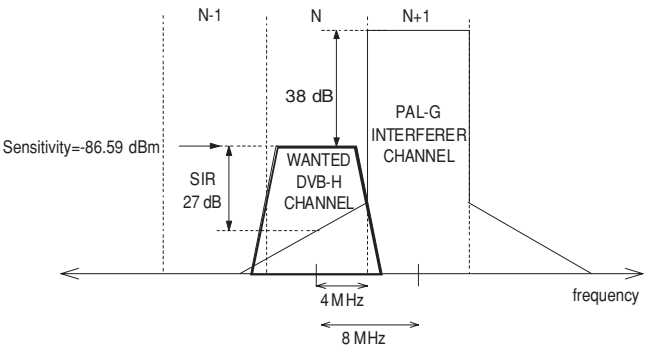

Figure 1 Graphic representation of the interferer and the wanted channel for phase noise calculation

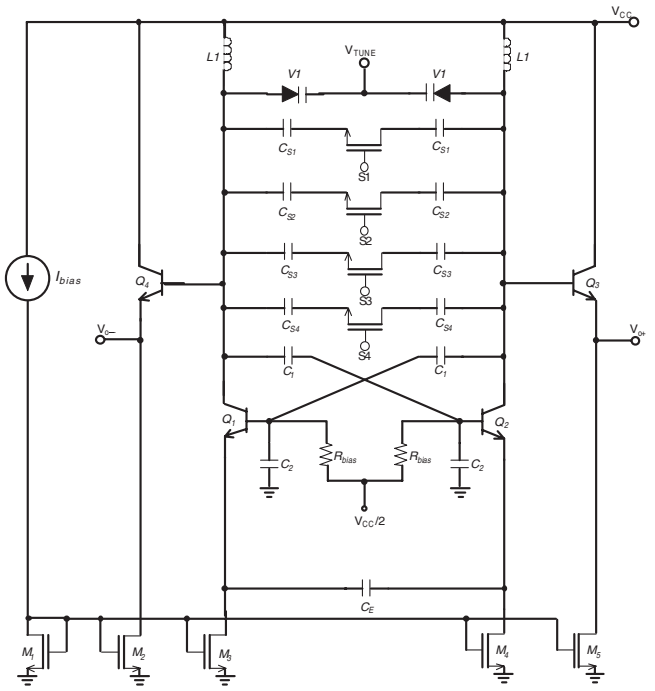

Figure 2 VCO simplified schematic

where K is Boltzmann's constant, T is the absolute temperature, R is the tank parallel resistance, V_o is the amplitude of oscillation, Q is the resonator loaded quality factor, f_c is the flicker noise corner where flicker noise and thermal noise are equal in importance and F is the excess noise factor. This equation leads to the typical plot of phase noise versus offset frequency of Figure 3.

From equation (3) and for a given f_o, the VCO phase noise can be minimised by:

Reducing the excess noise factor F.

Improving the tank, i.e, increasing the tank quality factor Q, which implies a reduction of the tank parallel resistance R.

Increasing the amplitude of oscillation V_o.

In the following sections, different techniques for minimising the VCO phase noise acting over the previous points will be discussed.

3.1. VCO Optimum Bias

The excess noise factor represents the excess noise injected by noise sources other than the losses in the tank, i.e, the noise from the cross-coupled differential transistor pair and the tail current source taking the nonlinear operation of the oscillator into account [5].

The noise in a transistor is proportional to the transistor base r_b and to the transistor small-signal transconductance $g_m = I_C/V_T$, where V_T is the thermal voltage and I_C is the collector current. To minimize g_m and r_b, the collector current must be low and transistor area must be high. However, if the transistor area is increased the input capacitance will also increase, attenuating the input signal. This will raise the noise factor and, as a result, it will reach a minimum for a particular combination of area and bias current.

As stated above, the function of the cross-coupled transistor pair is to perform negative impedance transformation. For a given tank, the negative resistance is fixed and, as a consequence, the transistor g_m is also fixed. The problem is that for a particular transistor area, this g_m fixes a specific collector current which rarely coincides with that for minimum noise.

To minimize the cross-coupled differential transistor pair excess noise factor, the transistor design stage first involves finding the optimal noise current density. Figure 4 depicts the minimum noise figure (NFmin) versus bias current for a 1 μm transistor. This figure shows that for the technology used here, a tail current of 25 mA is optimal, i.e. a current density of 12.5 mA/μm. As the minimum noise figure and the optimum noise current density are practically independent of emitter length [6] the transistor areas are then adjusted so that the negative resistance equals the tank parallel resistance R at the minimum noise current density. After this process, the transistor size and its bias current are determined.

A VCO designed using this method would present a minimum excess noise factor but with a considerable power penalty. When power constraints are taken into account a less than optimum current density should be used. This, on the other hand, improves the design reliability because, as Figure 4 shows, a slight increase in I_C would result in a considerable increase in NFmin. In our case, a tail current of 14 mA or, equivalently, a current density of 7 mA/μm, has been selected.

3.2. Tank Design

A major challenge for the receiver design is frequency generation for the down mixers, which needs to cover nearly an octave of tuning range (from 470 to 858 MHz), while at the same time meeting stringent phase noise requirements.

One of the difficulties in realizing a fully integrated VCO is creating the high-quality inductor necessary. For the design of the oscillator coil, several considerations must be made. First of all, the losses of the coil must be as low as possible for low noise and low power. One could use a small coil for this since this will have

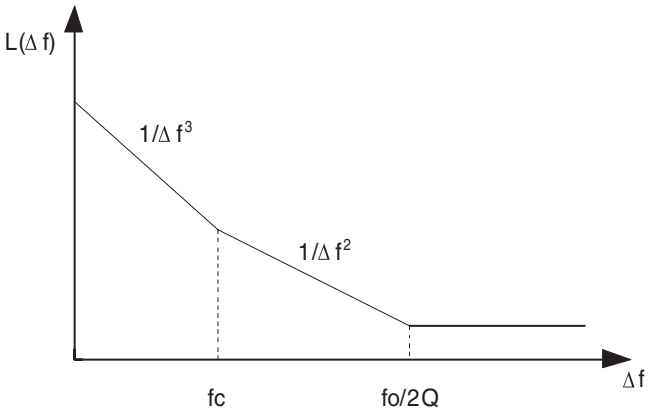

Figure 3 Phase noise versus frequency

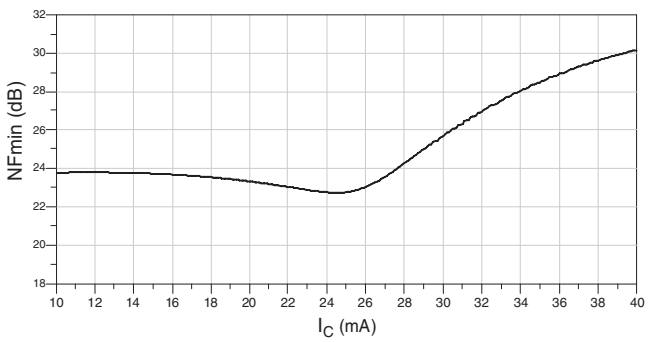

Figure 4 Minimum noise figure versus bias current for a 1 μm transistor

small resistance, but this will require a large capacitance to set the desired frequency. In addition, as the power required for a stable oscillation is proportional to $R\cdot(2\cdot\pi\cdot f_0\cdot C)^2$, using a too small inductance value will require a large power consumption [4]. On the contrary, an extremely large inductance is not recommendable because it will require a small capacitance. This capacitance value will be almost achieved with the parasitics of the coil and the amplifying transistors, leaving no room for an extra tunable capacitance [4].

To facilitate the integration of inductors and capacitors, the VCO should run at twice the required UHF frequency (from 948 to 1716 MHz). If the VCO were designed for generating the required frequencies directly, the inductors and capacitors needed would result in extremely large values. For example, if a 5 nH inductor were chosen, a maximum capacitance of 23 pF would be needed for 474 MHz, which occupies a large area.

The required inductors were selected using a commercially available planar electro magnetic (EM) simulator (Momentum©) [7]. This allows us to gain insight in the different tradeoffs between coil radius, conductor width, and number of turns, to achieve the inductor with the best quality factor at the center of the band. Nevertheless, getting precise results from a general purpose EM simulator is not a simple task. The substrate and metallization layers provided by the technology should be carefully defined, and the simulator has to be adequately set up so the results fit the measurements. To do this, a small number of inductors have been fabricated and measured. With these data, the required simulation parameters, and the best metallization layer approximation have been defined [8].

Spiral inductors with different geometry were simulated. To improve its behavior all the designed inductors share some common characteristics. First of all, the spacing between the metal lines should be as small as possible. Increasing the spacing decreases the total inductance because of the decreasing of the mutual inductance. It also increases the series resistance and the total area. Therefore the spacing will be fixed in 2 μm, the minimum allowed by the foundry. It is well known that circular shape is the optimum for spiral coils and could bring Q at least 10% higher than squared ones [9]. However, octagonal shapes were used, since the technology allows 45° routing. Finally, inductors were designed with the top metal level, thick and conductive enough to present a low coil resistance, and far from substrate enough to work at high frequencies.

Following the guidelines described above, a number of high-performance inductors in the twice UHF frequency range were designed and simulated. As laying-out a spiral inductor by hand is a slow and error prone process, an automatic layout generator tool program has been used to generate the layout of each coil [10].

The parameters of the final optimal geometry for our problem are given in Table 1. As shown in Figure 5, with an inductance value of 4.1 nH, a quality factor as large as 9.5 at the frequency of interest is achieved. To take into account its behavior in the schematics and layout simulations the inductor was modeled using the well known pi model [11].

Tuning is achieved by a combination of continuous analog voltage control and digitally switching capacitors (see Fig. 2). The array of switched capacitors is arranged to give five digitally selectable sub-bands. The switching is made using NMOS transistors and the variable capacitor is a PN type varactor.

TABLE 1 Inductor Geometrical Parameters

Spacing	Number of Turns	External Radius	Width	L (nH)	Q_{max}
2 μm	3.5	150μm	15μm	4.1nH	9.5

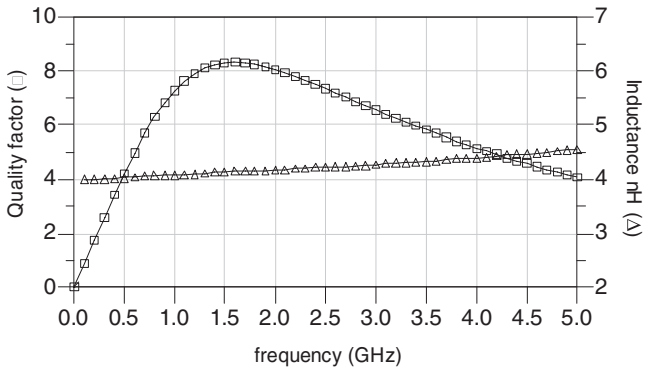

Figure 5 Quality factor and inductance simulation results of the tank inductor

3.3. Emitter Degeneration

Equation (3) leads to the conclusion that for the same noise factor and tank quality, the phase noise of a VCO can be minimized by increasing the amplitude of oscillation V_o. However, V_o decreases with frequency because of the reduced transistor gain. This is evident if the transformed negative impedance of the cross coupled transistor pair is considered. From Figure 6(a) the impedance *Zin* can be expressed as:

$$Zin \approx -2\left(\frac{1}{g_m}+s\frac{C_p\cdot r_b}{g_m}\right)=-2\left(\frac{1}{g_m}+s\cdot L_e\right) \qquad (4)$$

where C_p is the base-emitter capacitance and L_e denotes the equivalent inductance introduced by the cross coupled pair. As frequency increases, $s\cdot L_e$ dominates the negative impedance, diminishing the transistor gain. The consequence is a reduced amplitude of oscillation and, eventually, a loss of the condition to sustain oscillation.

To overcome this problem, capacitive emitter degeneration can be employed [12]. This method consists on introducing an extra capacitor, C_E, to cancel out the effect of the negative inductance

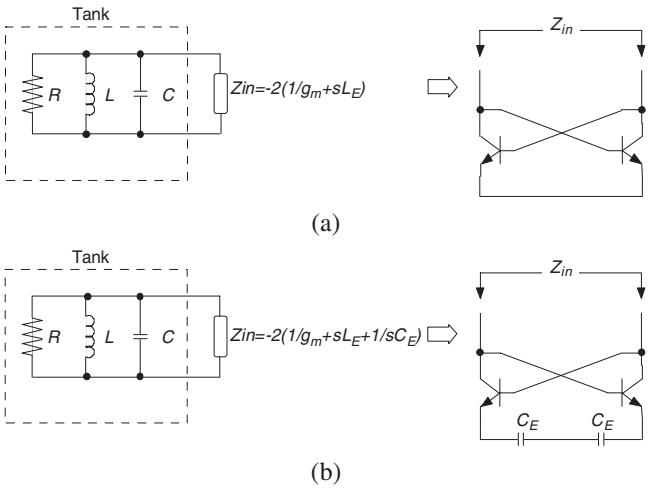

Figure 6 Negative impedance: cross-coupled transistor pair (a) without capacitive emitter degeneration and (b) with capacitive emitter degeneration

introduced by r_b and C_p (see Fig. 6) (b). Equation (5) represents the transformed negative impedance of the cross coupled transistor pair with capacitive degeneration.

$$Z_{in} \approx -2\left(\frac{1}{g_m} + s \cdot L_e + \frac{1}{s \cdot C_E}\right) \quad (5)$$

The capacitor C_E is selected so that, at the oscillation frequency, it cancels out the impedance introduced by L_e. As the selected inductance was 4.1 nH, the required capacitance was $C_E \approx 3.5$ pF. This includes the output capacitance of the bias circuit because it introduces extra degeneration.

3.4. Capacitive Divider

Another technique used here to increase the output voltage is a capacitive divider [13]. It uses a capacitive voltage division network to decrease the swing at the bases of the cross-coupled transistors, with respect to the tank voltage swing (C_1 and C_2). This prevents the transistors saturate heavily at high swing at the output. DC biasing of the base terminals is done with 2 kΩ resistors (R_{bias}).

To validate this technique, a simulation of the VCO output for different capacitance ratios has been carried out. An increase of 330 to 714 mVp has been achieved.

3.5. Output Buffer

The output buffer is an emitter follower configuration. It has been matched adjusting the output transistor collector current to get an output impedance close to 50 Ω.

4. EXPERIMENTAL RESULTS

4.1. Layout Implementation

VCO performance is influenced by random mismatches due to microscopic fluctuations in dimensions, doping, implant thickness and other parameters. Good differential pair behavior depends on base to emitter voltage matching. To minimize this mismatch the following rules was taken into account:

- Place transistors in close proximity, keeping transistors layout as compact as possible.
- Orient transistors in the same direction.
- Differential pair devices should have the same boundary conditions. This is accomplished by adding dummy components.
- Place transistors well away from the power devices.
- Use common centroid to obtain the best common mode rejection ratio (CMRR) in the differential pair. This technique constructs devices symmetrically about a common center in the layout.

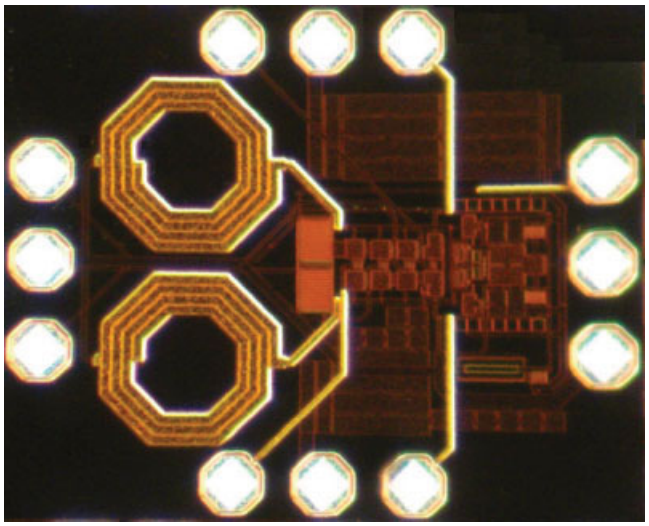

Figure 7 VCO layout. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

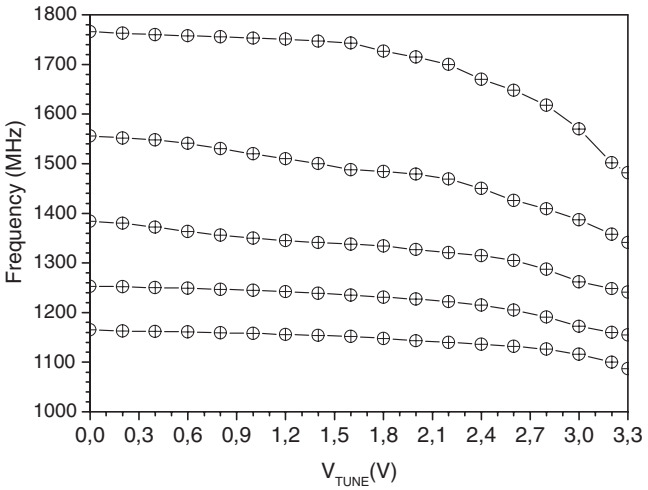

Figure 8 VCO tuning range

The circuit was designed to be measured on wafer with a probe station. The probe pads were octagonal, optimized for RF. Four signal-ground-signal (SGS) pad structures with 150 μm pitch were used, as depicted in Figure 7. The chip size is 826 × 1020 μm.

4.2. Measurements

The VCO was measured on wafer using a Cascade SUMMIT 9000 probe station, 35 GHz signal-groun-signal (SGS) probes and 26.5 GHz Agilent E4440A spectrum analyzer with phase noise measurement personality. Figure 8 shows the VCO tuning range and the overlapping regions between the five sub-bands. The VCO oscillates from 1085 MHz to 1766 MHz, covering nearly the entire band using only one VCO core. The VCO measured tuning range is 47.6%.

For phase noise measurement, free running VCO was biased with batteries to minimize the noise from the power supply. The

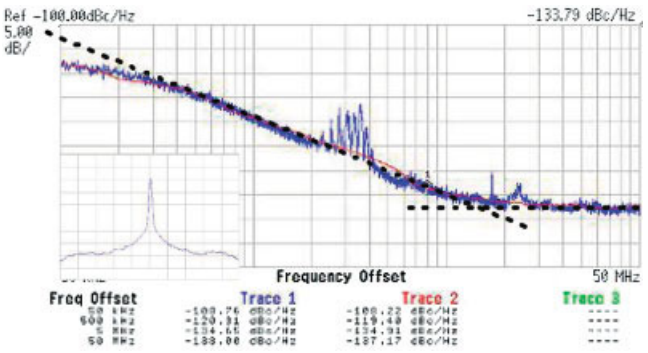

Figure 9 Measured phase noise for 1740 MHz oscillation frequency. [Color figure can be viewed in the online issue, which is available at www.interscience.wiley.com]

TABLE 2 Comparison with Recently Published Wide-Band VCOs

Author	L (1 MHz)	Tuning Range	Band	Technology	Core Power Consumption	*FoM*	Number of Cores
This work	−130 dBc/Hz	47.6%	1087–1766 MHz	BiCMOS 0.35 μm	19.8mW	177.76 dB	Single core
[14]	−126.5 dBc/Hz	72.2%	1150–2450 MHz	CMOS 0.18 μm	10 mW	177.71 dB	Single core
[15]	−116 dBc/Hz	46%	1340–2140 MHz	CMOS 0.35 μm	−	−	Single core
[16]	−124 dBc/Hz	53.6%	667–1156 MHz	CMOS 0.18 μm	21.7mW	167.12 dB	Single core
[17]	−131 dBc/Hz	63.11%	900–1730 MHz	CMOS 0.18 μm	14 mW	178.62 dB	Single core
[18]	−135 dBc/Hz	82.1%	420–1005 MHz	BiCMOS 0.35 μm	22.2mW	174 dB	Three cores
[19]	−127 dBc/Hz	69%	978–2010 MHz	CMOS 0.25 μm	13.5mW	175.5 dB	Single core

obtained VCO spectrum was quite clear, as shown in Figure 9. Due to the very low 1/f device corner frequency in SiGe BiCMOS technology the phase noise is −20 dB/dec until the noise floor of the measurement setup is reached. It has been achieved a −112 dBc/Hz at 100 kHz offset. These specifications are suitable for the proposed receiver requirements. The VCO output power is −14 dBm and the current consumption for a 3.3 V supply is 6 mA.

Table 2 shows a comparison with recently published integrated VCOs oscillating in the same band. The *FoM* for the VCO is calculated according to the following commonly adopted formula [20]:

$$FoM = 10 \cdot \log\left(\left(\frac{f_o}{\Delta f}\right)^2 \cdot \frac{1}{L(\Delta f) \cdot P}\right) \quad (6)$$

where f_o is the oscillation frequency, Δf is the offset frequency, $L(\Delta f)$ is the phase noise at Δf, and P is the power consumption in mW. As shown in Table 2, the combination of low phase noise and reduced power consumption give to our design the second best *FoM*, even better than [18], which uses a three core VCO. The VCO with the best *FoM* [17] uses an external high Q inductor, so it is considered not fully integrated.

5. CONCLUSIONS

A fully integrated, single core, wide tuning range and low phase noise VCO for DVB-H was designed in a low cost technology. To cover the entire band, an array of switched capacitors and PN varactors were used. The tank inductor has been custom designed and verified with an electromagnetic simulator. Techniques like emitter degeneration, capacitive dividers and optimum bias and tank design were used to improve the VCO performance. The circuit was validated experimentally and the measured phase noise was −112 dBc/Hz at 100 kHz offset, which makes the designed VCO suitable for DVB-H applications. The proposed VCO exhibits the highest *FoM* compared to other fully integrated VCOs operating in the same band.

ACKNOWLEDGMENTS

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