DESIGN AND CONSTRUCTION OF A BROADBAND (1MHZ) DIGITAL HF TRANSCEIVER FOR MULTICARRIER AND MULTICHANNEL MODULATIONS

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Abstract

This paper describes a broadband (1MHz) digital HF transceiver for the HF band (3-30MHz) specifically designed for the transmission and reception of multicarrier and multichannel modulations. The wide modem bandwidth (1MHz) is not meant for the transmission of a single 1MHz wide signal, since the goal is to achieve flexible transmission and reception using several channels with a common standard bandwidth.

1 Introduction

This paper describes the design and construction of a broadband (1MHz) digital HF transceiver for the HF band (3-30MHz), specifically designed for transmission and reception of multicarrier and multichannel modulations.

This transceiver is the result of several years of mutual collaboration between CeTIC (ULPGC) and GAPS (UPM) on multicarrier modulations (OFDM and OFDM-CDM) in data and interactive digital voice communications in the HF band, leading to the development of HFDVL (High Frequency Data+Voice Link) architecture [3]. The last step undertaken has been the development of a system supporting both high availability and link quality for highly demanding applications, such as RADAR data transmissions [4]. Due to these restrictions, increased availability and quality, the new system is based on a combination of multicarrier and multichannel techniques. Thus, these stringent requirements have led to the design and construction of a broadband transceiver capable of meeting them.

It is important to highlight that the wide modem bandwidth (1MHz) is not meant for the transmission of a single 1MHz wide signal, since the HF spectrum is highly populated and strongly regulated. The goal is to achieve flexible transmission and reception using several channels with a common standard bandwidth. The transceiver digital baseband subsystem is in charge of implementing proper system channelisation.

Figure 1 shows the digital transceiver receiving section (RX) block diagram. The transmission section (TX) has the same blocks but with an inverse flow signal.

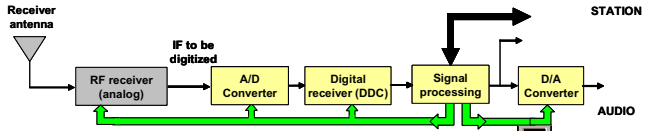

Figure 1: Receiving section block diagram

All the broadband transceiver blocks are described in this paper, pointing out specific multicarrier modulations aspects. The transceiver consists of a radio frequency (RF) front-end that moves the chosen 1MHz band portion to an intermediate frequency (IF, 10.7MHz). These front-end implements a double conversion superheterodyne architecture based on Direct Digital Synthesis (DDS) oscillators. After the A/D converter stage follows a multichannel Digital Down Converter (DDC) with an 8KHz bandwidth channel. This multichannel output signal enters into the signal processing unit implementing the modem OFDM algorithms (data) and OFDM-CDM algorithms (interactive digital voice). An Altera FPGA (CycloneII EP2C70), a fixed point DSP (Texas Instrument TMS32C6416), and software running on a GNU/Linux Personal Computer (PC) comprise the digital part.

Figure 2 shows a photograph of the RF front-end and FPGA setup. The front-end has been built to fit inside a 19'' subrack, thus offering a standard and modular structure.

The paper continues with a description of the analog part (RF front-end), then a description of the digital part (FPGA and DSP) and finally a conclusions section.

2 Analog part: RF front-end

The basic architecture of the wideband RF front-end is that of a double conversion superheterodyne. [2]. The general block diagram for the front-end is shown in Figure 3, while in Figure 4 and Figure 5 more detailed diagrams for the reception and transmission parts are shown, respectively. Intermediate frequencies and frequency ranges for the different comprising modules are also shown in Figure 4 and Figure 5.

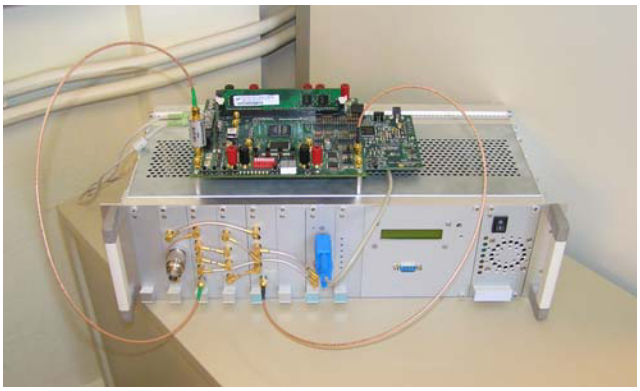

Figure 2: RF Front-end and FPGA setup

By virtue of being a half-duplex transceiver, there are two common blocks to receiver and transmitter: local oscillators and control unit. The control unit manages the front-end and it also interacts with the operator by means of a personal computer. Moreover, it programs the oscillators in order to change the reception and transmission frequencies, it acts on the different parts of receiver and transmitter in order to change gains and switch on or off several parts of the circuit, and lastly it switches the TX/RX relay.

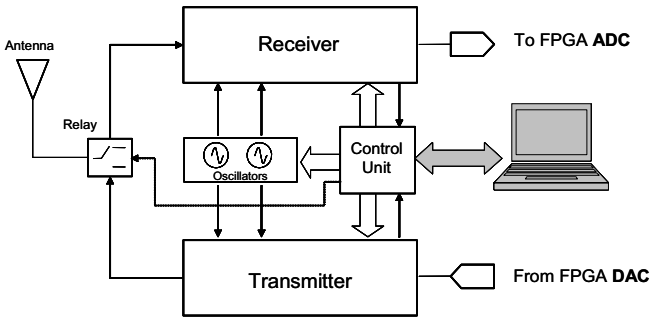

Figure 3: RF Front-end block diagram

In the receiver depicted in Figure 4, the signal at the antenna is filtered in the HF band (3-30MHz), to be then amplified. The first mixer is in charge of translating the RF frequency to the selected first IF, by means of the first local oscillator. Once at first IF, the signal is in-band amplified and then it is mixed with the second local oscillator at the second mixer so that to be translated to second IF frequency. Just before entering the A/D converter, the signal is filtered and amplified. The Automatic Gain Control (AGC) circuit, managed by the control unit, is in charge of keeping a constant signal power at the input of the A/D converter.

In the transmitter shown in Figure 5, the baseband signal is filtered, amplified when necessary, and translated to first IF. Then the signal is converted to the selected RF frequency making use of the output mixer, after having been filtered in the second IF filter. Lastly, the RF signal is amplified and in-band filtered to then be sent to the antenna. The Automatic Level Control (ALC) block keeps a constant power level at the output, in order not to saturate the power amplifier. The control unit also manages this block. Due to the power amplifiers need for at least 5W in order to be able to be excited, an external pre-amplifier unit has been developed. This unit is capable of delivering around 8W.

RF filters without any special needs, such as narrow bandwidths or high Q as the IF filters, are implemented with capacitors and inductors, both axial and toroidal. 10.7MHz filters in charge of filtering the output of the D/A converter in the transmitter or the input of the A/D converter in the receiver have been acquired in KRFilters [5]. These high quality filters have very narrow bandwidths at a centre frequency of 10.7 Mhz (1Mhz and 3 MHz). In the case of the 112MHz IF a 1MHz bandwidth Surface Acoustic Wave (SAW) filter has been selected, as the only kind of filter with such a narrow bandwidth at said centre frequency.

It is important to highlight that the pass-band filter at the input of the receiver is composed of 4 relay-switched tunable pass-band filters. The passive diode ring mixers are all model TUF-1 from Minicircuits.

Oscillators unit is based on DDS. Thus, design and integration are simplified, while microhertz resolutions, fast frequency steps, phase control and improved phase noise can be achieved. The DDS integrated circuit employed has been Analog Devices AD995.

In Figure 6 and Figure 7 several pictures of the system modules are shown. In Figure 6 part of the RF backplane can be seen. All digital control signals for the different RF front-end modules are routed through the backplane bus. All radiofrequency signals are connected in the subrack front. The 3U form board (100x160mm) with the two DDS-based oscillators and DIN41612 connector is shown in Figure 7.

The following list summarises the main RF front-end characteristics:

- Double conversion superheterodyne (up-mixing).
- 1st IF: 112MHz and 2nd IF: 10.7MHz.
- Frequency steps: 1Hz.
- Sensitivity (@1MHz): -70dBm.
- Microcontroller-based RX, TX, AGC and ALC control.
- Modular assembly.
- Output power -20dBm.
- External power amplifier (linear class A).

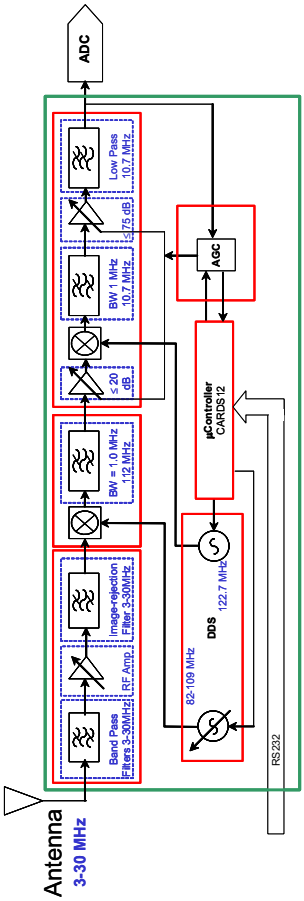

Figure 4: Receiver block diagram

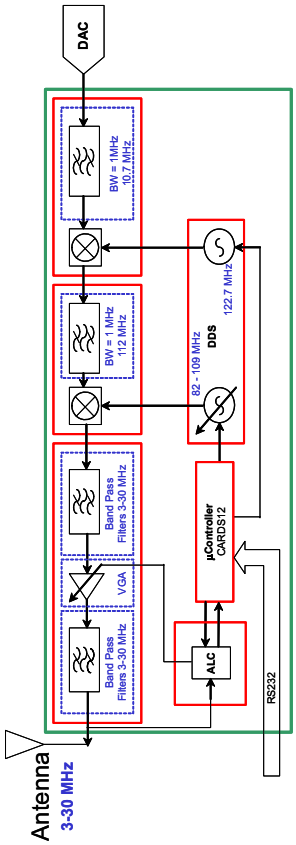

Figure 5: Transmitter block diagram

2.1 Measurements

A capture of a spectrum analyzer's display, connected at the output of the frontal IF while a multicarrier signal, with a centre frequency of 20MHz is being received [1], is shown in Figure 8. This multicarrier signal has been generated by a function generator with a multitone function selected. This signal is composed of 9 unmodulated tones spaced 100KHz apart (bandwidth of 900KHz), with a -70dBm level and a 26dB carrier to noise floor ratio. As shown, the output frequency is centred at 10.7MHz, while the function generator carrier to noise floor ratio has been degradated 4dB only. In Figure 8 it is also shown how the receiver output signal exhibits some curvature due to the SAW filter's frequeny response (112MHz). Thus, tones on the edge of the signal have lower values than those central ones.

3 Digital part: FGPA and DSP

The RF analog front-end has been described in the preceding section. Both input and output signals in the front-end correspond to a multicarrier signal centred at a 10.7MHz intermediate frequency and with a bandwidth of 1MHz. The next step is to (bidirectionally) translate this signal to baseband, to be digitally processed in order to recover its information.

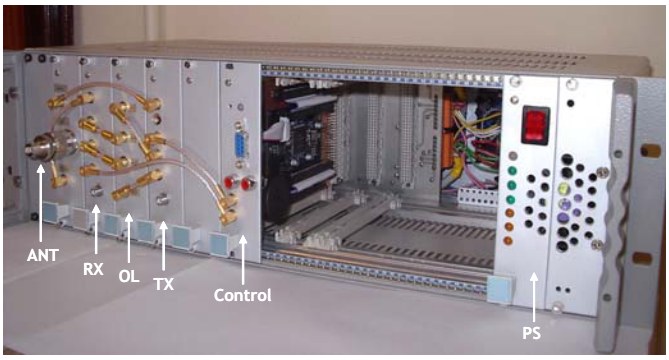

Figure 6: RF Front-end subrack 19"

The first step in this process corresponds to the signal digitalisation by means of an A/D converter. Once digitalised, the signal is placed in baseband through a Digital Down Converter (DDC), and then the output of this converter is processed in order to recover the information. This final step of processing can be carried out in a PC or partly or completely in a DSP.

The design of the digital stage has been carried out implementing the multichannel DDC and Digital Up Converter (DUC) in a FPGA, while the processing stage has been implemented by a combination of PC and fixed-point DSP. Some parts of this design can be seen in Figure 9.

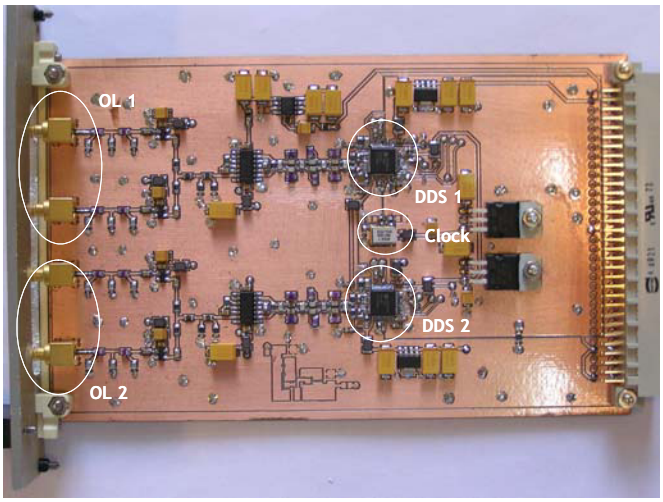

Figure 7: Oscillators board

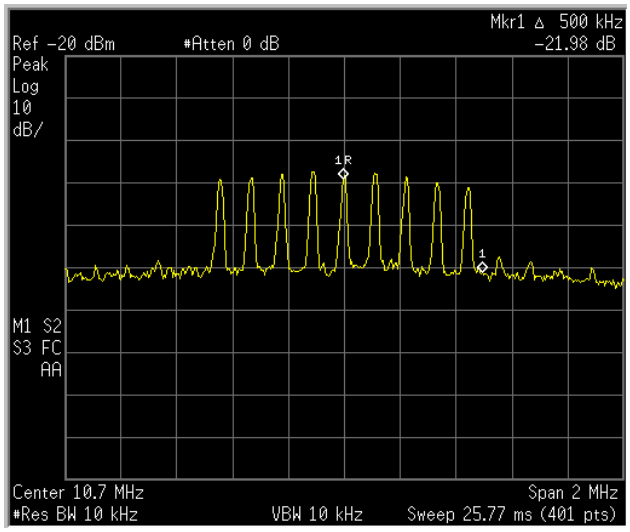

Figure 8: IF output 10.7MHz (signal to FPGA A/D)

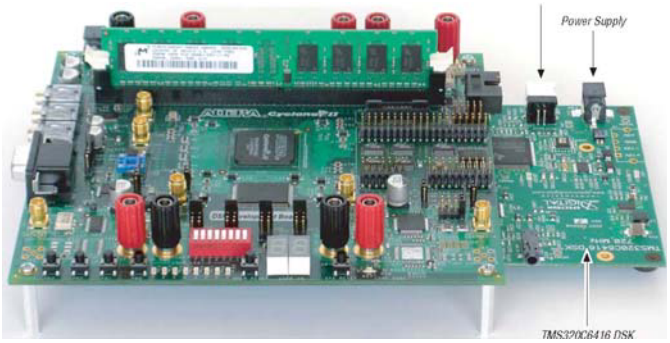

Figure 9: Altera FPGA and 'c6416 DSP development board

3.1 DDC and DUC

The mission of a DDC is to translate the interest frequency band to baseband and to downsample the digitalised signal. Through a DUC,.the inverse process is achieved.

The basic blocks of a DDC are shown in Figure 10, comprising at least the following subsystems:

- A Number Controlled Oscillator (NCO), with I and Q outputs and two mixers in charge of translating the interest frequencies to baseband.
- A CIC low-pass filter, with the mission to decimate the signal in order to reduce the sampling rate.
- A FIR filter to compensate the sinc-like response of the CIC filter. Optionally, it can also decimate the signal once more.
- A FIR filter to correctly channalise the signal in order to guarantee the baseband spectral mask imposed requirements .This last stage of filtering can be also used to decimate once again the signal, or to interpolate it, in order to adapt the output sampling rate of the whole filtering chain.

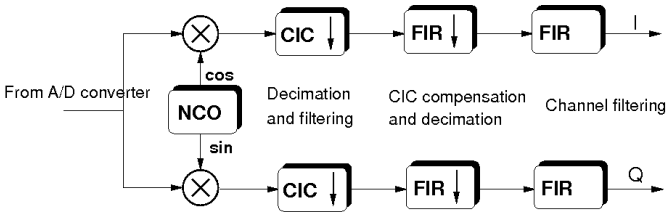

Figure 10: Monochannel DDC building blocks

The DDC and DUC blocks have been implemented on an Altera FPGA development kit (CycloneII EP2C70), comprising A/D and D/A converters. The tools used have been:

- Altera DSP Builder. It enables simulating the block behaviour of the FPGA programmable logic inside Matlab's Simulink.
- Altera Megacore. This tool provides a set of programmable logic blocks optimised for some signal processing common operations: NCO, CIC, FIR, FFT, Reed-Solomon and Viterbi coding and decoding, etc.
- Altera QuartusII. It allows synthesising and implementing the programmable logic generated by the aforementioned tools.

Initially, monochannel DDC and DUC were implemented. In order to turn them into multichannel, the possibility of reusing structures instead of repeating them was investigated, in order to save both space and processing time. Reused resources correspond to those of the filtering chain. The elements of this filtering chain communicate with one another by means of a proprietary bus by Altera, called Avalon Streaming Interface. This interface makes it possible to multiplex in time the different channels, so that to avoid the necessity for repeated

whole structures. Thus, input data for each channel are packed and multiplexed using a dedicated block, Avalon Packet Format Converter. This block generates multiplex signals and data from each individual channel data and signals.

Furthermore, two solutions have been developed to interconnect the FPGA with the PC, in order to further free from processing load the PC where the modem programs are ran. The first solution corresponds to the usage of the audio input and output lines (Line IN and Line OUT) in the FPGA development board, in order to implement an audio codec capable of communicating with the PC through a commodity sound card used by the software modem. This option is capable of processing whichever two channels, sent to the PC in the left and right channels of the sound card.

The second option, partially implemented at the moment, enables the connection of more than two channels, making use of the network card coupled to the FPGA development board. Thanks to this network card, but also by integrating a microprocessor inside the FPFA (NiosII) equipped with a operating system (uClinux), the transmission of the baseband data between the FPGA and the PC is possible, by means of an Ethernet connection.

The microprocessor inside the FPGA running uClinux operating system, also allows controlling both DDC and DUC through a telnet connection.

4 Conclusions

In the frequency spectrum, HF band holds several peculiar characteristics, as it enables trans-horizon links with limited power and without the need for artificial repeaters. These properties have given rise to many studies aiming to optimise its use and improve its range. However, as HF is a rather hostile environment due to noise but also to the high number of high power stations, the design of communication systems working in this band is a challenge.

A broadband HF modem as the one developed by the authors' research groups, with channelisation implemented in baseband, makes for an excellent tool to study frequency diversity techniques, propagation, etc. It should be kept in mind that commercially available modems have a bandwidth no higher than one hundredth of the aforementioned modem.

The whole chain assembly in a 19'' minirack is shown in Figure 11. An SPE Expert 1K FA commercial amplifier is used as final power stage.

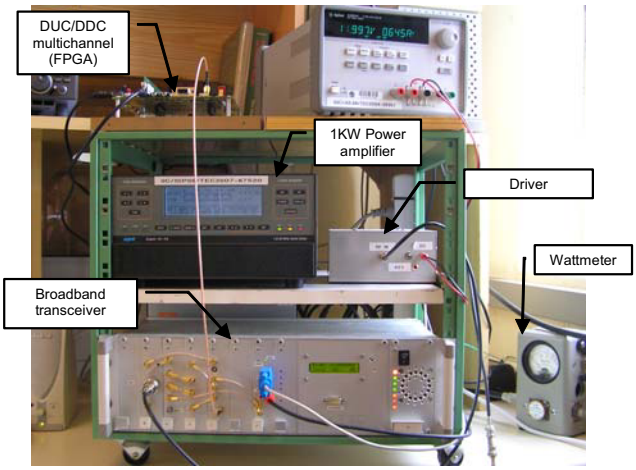

Figure 11: Broadband digital HF transceiver

However, this broadband system introduces a number of challenges in its operation. Firstly, it needs to coexist with the traditional narrowband systems, and so it needs to tackle arising problems, such as sensitivity of the broadband receiver to strong narrowband signals, requiring the use of further filtering or signal processing, as those narrow signals affect receiver AGC silencing it. One more factor to take into account when working with broadband signals is the low linearity of commercial power amplifiers. Thus, they generate intermodulation products dirtying the spectrum and interfering other users. Moreover, it is necessary to have broadband antennas available capable to work with these kinds of signals without altering their characteristics.

Acknowledgements

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