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Area Efficient Dual-Fed CMOS Distributed Power Amplifier

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Abstract: In this paper, an area-efficient 4-stage dual-fed distributed power amplifier (DPA) implemented in a 0.35 µm Complementary Metal Oxide Semiconductor (CMOS) process is presented. To effectively reduce the area of the circuit, techniques such as using multilevel inductors and closely-placing conventional spiral inductors are employed. Additionally, a novel technique based on stacking inductors one on top of others is implemented. Based on these techniques, a 32% area reduction is achieved compared to a conventional design without a noticeable performance degradation. This reduction could be further exploited as the number of stages of the dual-fed DPA increases.

Keywords: distributed power amplifier; dual-fed; stacked inductor; multilevel inductor; area reduction

1. Introduction

The conventional distributed amplifier (DA) has been broadly used for wide-band small-signal applications due to its ability to combine multiple amplifying devices without compromising the gain bandwidth product [1]. However, its success in power applications has been limited for several major reasons, such as the unequal distribution of output power between active devices, which results in the underutilization of some of the active devices [2–4] and the wasted power at the inactive output port that reduces efficiency [5–7].

Several alternative topologies have been proposed in the literature to overcome these drawbacks, such as output line tapering [7] and improved circuit optimisation [2–4]. A variation of the DA topology, the dual-fed distributed amplifier, has been proposed in order to harness the power in the backward waves [5,6]. The schematic of this topology is shown in Figure 1b. The working principle of this topology is to use both input ends to inject the input signal using a hybrid and all the available output power from both output ports is withdrawn using another hybrid. The addition of the forward and reverse gains for the splitted input signals results in a 6 dB increase in the overall gain, while the combination of both output ports increases the output power 3 dB. Nonetheless, forward and reverse gains have a different frequency behaviour. While the forward gain of a conventional DA is broadband, the reverse gain is narrowband and, as a consequence, the dual-fed DA frequency response is also narrowband. Some authors have proposed using composite right/left-handed (CRLH) transmission lines to operate at high frequencies [8]. In this case, the frequency response changes from low-pass to pass-band, but the bandwidth is still limited by the narrowband response of the reverse path. In both scenarios, the frequency limitation of the small-signal response in the reverse path results in a large-signal response also limited in frequency. This opens up the possibilities of improving one of the main drawbacks of distributed amplifiers, which is their large area consumption. This paper

proposes effective area reduction techniques using stacked inductors for a dual-fed CMOS distributed power amplifier that does not affect its large signal performance. To our knowledge, the combination of these techniques has not been implemented in previous works.

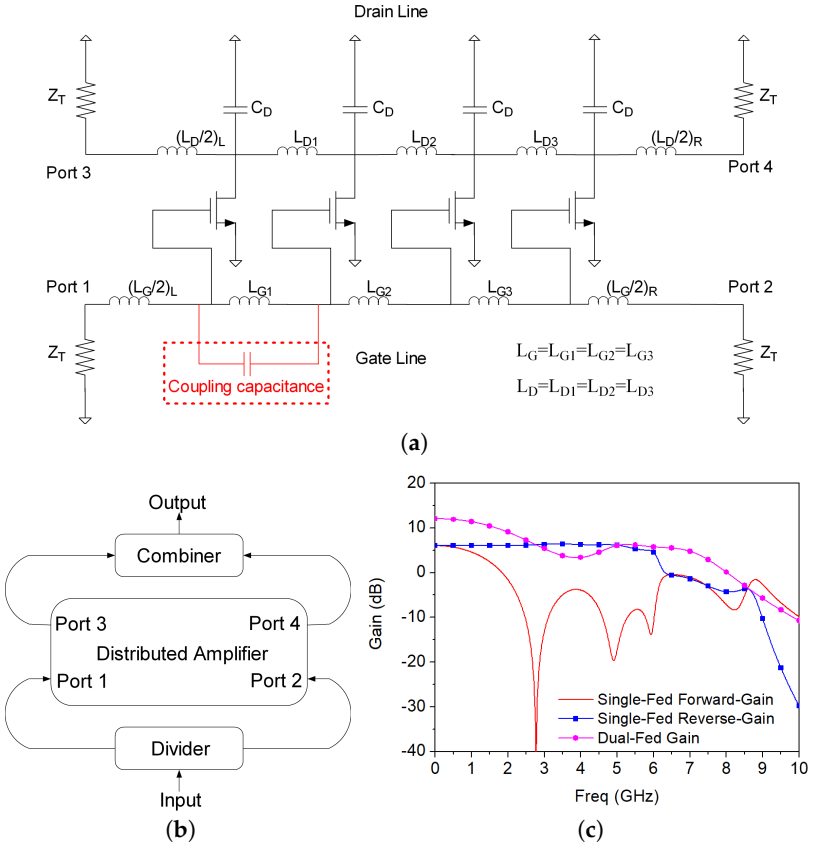


Figure 1. (**a**) conventional DA; (**b**) dual-fed DA; (**c**) small signal gains.

2. Single-Fed and Dual-Fed DAs

The circuit diagram of a conventional low-pass DA is shown in Figure 1a. In this topology, as the input signal flows through the gate transmission line, the output currents from each gain stage are added in the drain line. If the losses are not considered, the gain of a DA rises linearly as the number of stages is increased while the bandwidth stays constant. This is due to the fact that the parasitic capacitances of the transistors are assimilated into the gate and drain lines, forming lumped-element T-section constant-k filters, whose cut-off frequency limits the bandwidth of the circuit [1]. The characteristic impedance (Z_0) and cut-off frequency (f_c) of both transmission lines (TL) are given by:

$$Z_0 = \sqrt{\frac{L_{TL}}{C_{TL}}}, \tag{1}$$

$$f_c = \frac{1}{\pi\sqrt{L_{TL}C_{TL}}}. \tag{2}$$

Since Z_0 and f_c of both lines are identical, their capacitances and inductances should also be equal. As the drain-to-bulk capacitance (C_{db}) of a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is typically lower than its gate-to-source capacitance (C_{gs}), a capacitor (C_d) is included at the drain so both capacitances are equivalent:

$$L_g = L_d, \tag{3}$$

$$C_{gs} = C_{db} + C_d. \tag{4}$$

When losses are taken into account, the signal at each stage of the DA is attenuated. The main contributors to these losses are finite Q inductors and the drain-to-source resistance (r_{ds}) in the drain line. Under these conditions, the gain of the DA is typically described as follows:

$$A = -gm\frac{Z_0}{2\sqrt{1-\left(\frac{f}{f_c}\right)^2}} \cdot \frac{e^{-N\left(A_g+A_d\right)/2} \cdot sinh\left(N\frac{A_d-A_g}{2}\right)}{sinh\left(\frac{A_d-A_g}{2}\right)}, \tag{5}$$

in which A_d and A_g are the attenuation of the drain and gate lines, g_m is the MOSFET transconductance and N is the total number of stages. In this equation, the following assumptions are considered:

- Unilateral MOSFET model (ignores C_{gd}),
- Image impedance matched terminations,
- Equal gate and drain phase velocities.

The optimum number of stages that maximises the gain is a function of gate and drain line attenuation. These attenuations are complex functions and depend on the specific MOSFET parameters, as well as on the operating and cut-off frequencies. As the signal travels along the gate line towards the termination, less signal is available for each MOSFET due to the attenuation and, as a consequence, the overall gain decreases resulting in an increased number of stages. The number of stages for this work is chosen as 4.

The required g_m can be found from the low frequency gain of Equation (5) when the gain, number of stages and drain-line inductance and capacitance are known, as shown in Equation (6):

$$g_m = \frac{2A}{N}\sqrt{\frac{C_d}{L_d}} \Rightarrow g_m = \frac{2A}{N \cdot Z_0}. \tag{6}$$

Hence, the transistor width-length ratio can be derived from:

$$\frac{W}{L} = \frac{g_m}{\mu_n C_{ox}\left(V_{gs} - V_T\right)}, \tag{7}$$

where:

- W, transistor gate width,
- L, transistor gate length,
- n, electron mobility,
- C_{ox}, gate oxide capacitance per unit area,
- V_T, threshold voltage,
- V_{gs}, gate-source voltage.

Finally, the device length and width can be found by combining Equation (7) with the following expression:

$$W \cdot L = \frac{C_g}{C_{ox}}. \tag{8}$$

Conventional DA designs feature gate and drain transmission lines with low-pass characteristics and equal electrical lengths ($\theta_g(\omega) = \theta_d(\omega)$). As a consequence, the forward gain adopts a wideband nature, in which the corner frequencies of the unit cells are the limiting factor. On the contrary, the reverse gain follows a low-pass behaviour, as seen in Figure 1c.

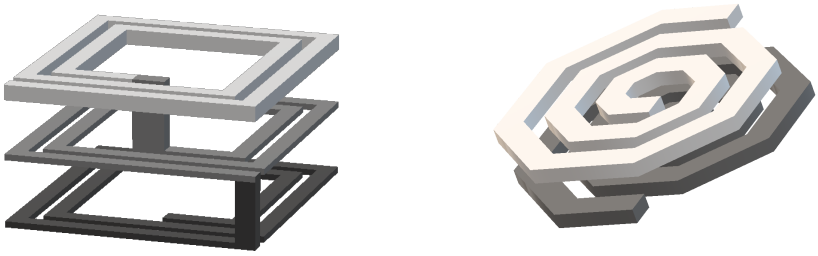
The dual-fed configuration shown in Figure 1b benefits from the forward and reverse gains of the DA, improving both power and gain when its performance is compared to the single-fed topology. This increase will only occur at low frequencies, since the reverse gain has low pass frequency response despite the fact that the forward gain has a broadband response. This can be seen in Figure 1c, where the small-signal gain of a dual-fed DA is plotted.

3. Area Reduction Techniques

One of the main drawbacks of distributed amplifiers is that they are formed by a noticeable amount of inductors that occupy most of the layout. Hence, it is paramount to analyse the influence of the coils and their placement on the circuit.

The most obvious method is to place the inductors closer together, which results in a more compact layout. However, this causes positive mutual coupling between the inductors when they are coiled in the same direction. Otherwise, the coupling would be negative [9]. To summarise, in DAs with inductors placed close together, it is crucial to properly orientate the inductors in order to reduce the chip area by minimising the effect of mutual coupling [10].

By using multilevel inductors instead of the conventional single-level or planar inductors, area minimization can also be accomplished [11–15] (see Figure 2a). In the multilevel structure, the coil is expanded vertically, while in the single level structure, the inductor is implemented using a single metal layer. Typically, the top layer is used to enhance the quality factor of the coil, since the lower metal layers are thinner. This means that, for a given inductance, the single-level structure shows a much larger area compared to a multilevel one. Using the thinner lower metal layers causes an increase of both the substrate capacitance and metal resistance. However, this disadvantage is compensated by the lower substrate losses due to their reduced area. This way, only a slight degradation of the performance of the stacked inductor is achieved compared to that of the planar spiral inductors.



(**a**) (**b**)

Figure 2. (**a**) multilevel inductor; (**b**) stacked inductor.

Both methods show that it is possible to reduce the area without significantly modifying the small-signal circuit response [9]. However, a further reduction in area can be achieved if some inductors could be placed on top of others, as seen in Figure 2b, where they should be winded in the opposite direction in order to reduce the mutual inductance and capacitance that appears between them. Even though this method could minimise the area considerably, the increased capacitance between the inductors would lower the cut-off frequency of the artificial transmission lines, reducing the small-signal behaviour of the DA. This can be exploited to make a dual-fed distributed power amplifier due to its low-pass frequency response. The increased capacitance when two of the coils of the gate line (L_{G1} and L_{G2}) are placed one on top of the other is shown highlighted in Figure 1a. Figure 3 shows a simulation of the forward and reverse gains when the coupling capacitance between both inductors is varied. As it can be seen, the frequency response of the forward gain is reduced, but the reverse gain remains the same. Therefore, if a dual-fed DA is made based on this topology, its gain will not be affected due to its low-pass frequency response.

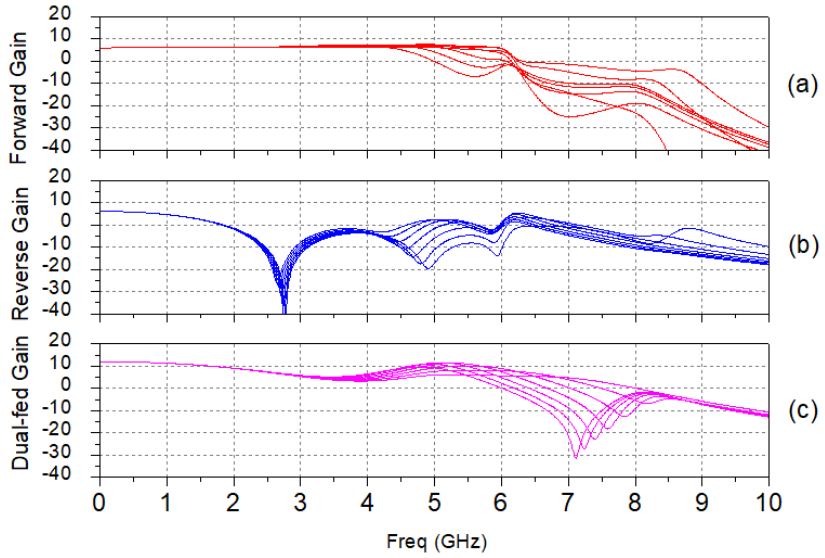


Figure 3. (**a**) single-fed forward gain; (**b**) single-fed reverse gain and (**c**) dual-fed gain for different values of the coupling capacitor between L_{G1} and L_{G2} (from 0 to 0.7 pF).

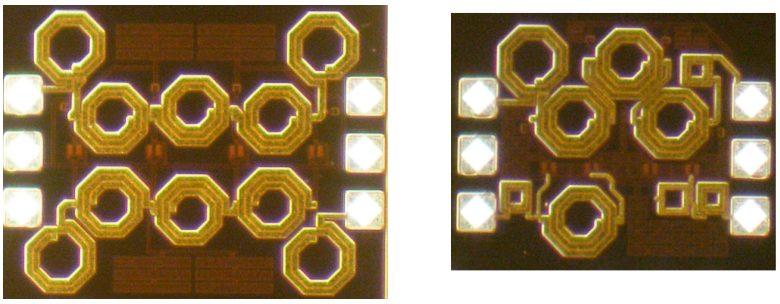
4. Experimental Results

In this section, the suggested area reduction techniques will be corroborated. To do so, two four-stage DAs have been designed in a standard 0.35-µm CMOS technology using the component values shown in Table 1, which were obtained following the procedure explained in Section 2.

Table 1. Component values.

Component	Value
$L_g = L_d$	1.465 nH
C_d	586 fF
L	0.425 µm
W	4.42 µm

The fabricated circuits are shown in Figure 4, where DA1 and DA2 correspond to a conventional and a compact design, respectively. DA1 uses conventional spiral inductors without implementing any area reduction technique. The total area of this circuit is 0.742 mm^2 including the pads. On the contrary, DA2 uses the area reduction techniques discussed in the previous section. First, a more compact layout has been obtained by placing the coils close to each other. To avoid the effect of the mutual coupling between the inductors, the coils have been oriented in the opposite direction. Additionally, multilevel inductors have been used on the gate line (L_{G3}, $(L_G/2)_R$ and $(L_G/2)_L$). Finally, two of the spiral inductors of the gate line (L_{G1} and L_{G2}) have been placed one on top of the other (stacked) to share the same area. This circuit still uses conventional inductors in the drain line since the multilevel inductors cannot withstand the current going through this path. However, $(L_D/2)_R$ has been implemented using a multilevel coil given that the current flowing through this inductor is lower since the circuit is biased using Port 3. By applying these modifications, the compact design occupies an area of 0.503 mm^2, which results in a 32% area reduction.



(**a**) (**b**)

Figure 4. Chip microphotograph of (**a**) DA1 (0.742 mm^2) and (**b**) DA2 (0.503 mm^2).

Measurements were performed with on-wafer probing with two bias tees connected at the input and output ports. To implement the dual-fed versions, a power divider and combiner were included externally to the single-fed prototypes.

The measured forward and reverse small-signal gains are presented in Figure 5a. The experimental results were obtained using the same DC bias conditions: 3 V on the drains and 0.8 V on the gates. As expected, the forward gain of DA2 is reduced compared to that of DA1 due to the coupling capacitance between the inductors placed one above the other. However, the reverse gains are very similar.

The relation between the measured output power and the input power for both configurations at 1 GHz is shown in Figure 5b. Note that, to compare the performance, the input power level between the dual and the single-fed prototypes must be shifted 3 dB. As explained in Section 1, in the dual-fed configuration a 3 dB output power increment and a 6 dB gain boost is achieved when compared to the single-fed DA.

Figure 5c depicts the measured results of power-added efficiency (PAE) as a function of the input power at 1 GHz. The obtained values are close to the theoretical limit of 40%, which meet those obtained in previous works [8,16]. The PAE for the dual-fed configuration for a 14 dBm input power is shown in Figure 5d as a function of frequency. As expected, the low-pass frequency response of conventional DAs results in a PAE decrease as the frequency increases. Note that the bandwidth for both DAs is similar, provided that the frequency response of the dual-fed DA is limited by the reverse gain, which is similar for both circuits.

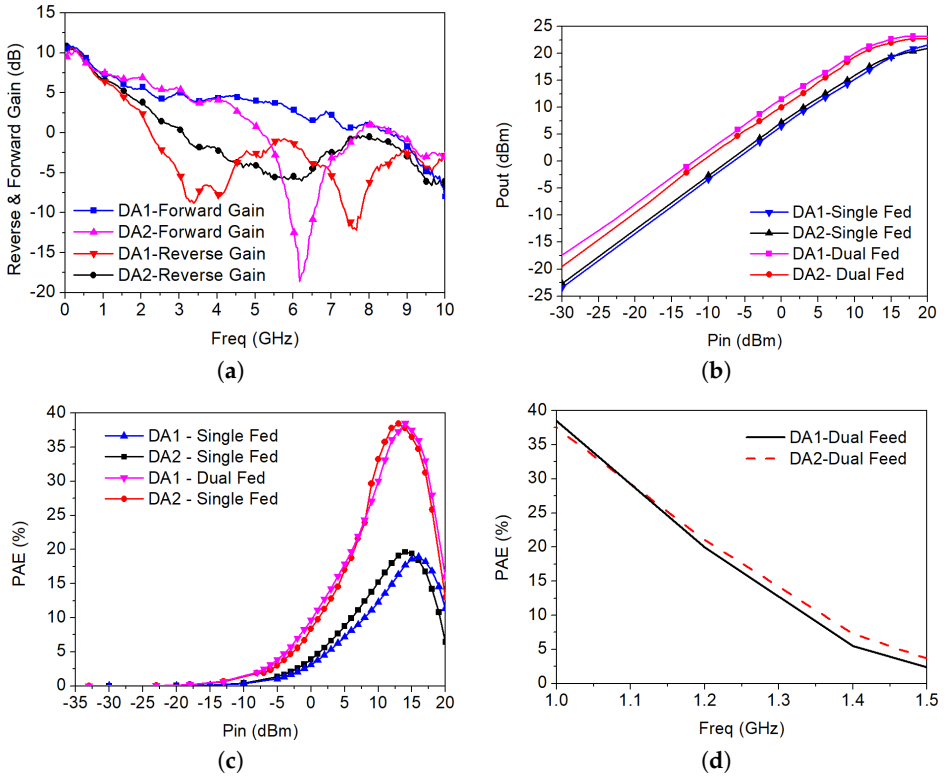


Figure 5. Measured DPAs (**a**) s-parameters; (**b**) output power vs. input power at 1 GHz; (**c**) PAE vs. input power at 1 GHz; (**d**) PAE vs. frequency (Pin = 14 dBm).

5. Conclusions

In this paper, several area reduction approaches have been implemented in a dual-fed DA. The first of them consists of placing the inductors closer together, considering that it is essential to properly orientate the coils in order to minimise the mutual coupling issue. The other techniques deal with the area occupied by the inductors, by using multilevel inductors and placing inductors one on top of the other.

The application of these techniques achieves a 32% area reduction, where the variation of the circuit performance is negligible. The large signal parameters, output power and PAE, remain practically the same. Even though there is a discrepancy between the small signal parameters of both versions, they are almost identical at the operating frequency, which is 1 GHz. It should be noted that the area of the circuit could be further minimised as the number of stages increases.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

CMOS	Complementary Metal Oxide Semiconductor
CRLH	Composite Right/Left-Handed
DA	Distributed Amplifier
DC	Direct Current

DPA	Distributed Power Amplifier
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
PAE	Power-Added Efficiency

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