Thermal Resistance Characterization for Multi-Finger SOI-MOSFETs

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***Abstract*— Thermal conductance in multi-finger SOI-MOSFETs is usually modeled at room temperature with a linear dependence on the total gate width, which is valid only when thermal coupling saturates. This paper presents a physically based model for calculating the thermal resistance of SOI-MOSFETs that accounts for progressive thermal coupling as the number of fingers increases and the substrate temperature. The model, extracted from a variety of gate geometries using the AC conductance method, correctly predicts the temperature rise in the device channel up to a substrate temperature of 150 ºC. Finally, this simple thermal resistance model, which is applicable to nanometer-scale transistors, can easily be added to circuit simulators.**

Index Terms—**SOI-MOSFET, thermal resistance, electrothermal characterization, substrate temperature, multi-finger model.**

I. Introduction

Miniaturization of metal oxide semiconductor field effect transistors (MOSFETs) has led to massive integration levels, where heat generation causes chip temperatures that can prevent the circuits' reliable operation, especially at nanometer length scales where the geometry in novel MOS devices tends to make heat removal more difficult.

Silicon-on-insulator (SOI) MOSFETs for the next generation of automotive, industrial and medical applications, will operate in the temperature range of −40 °C to 175 °C. When SOI technology is used, the very low thermal conductivity of the buried oxide layer (BOX in Fig. 1) significantly impedes heat transfer toward the substrate, particularly for thicknesses greater than 100 nm [1]. Additionally, confined dimensions can still augment self-heating [2], as the thermal conductivity of internal thin films is much lower than the corresponding bulk value [3-7]. In consequence, heat dissipation is sensitive to external contacts and gate geometry design, which must be optimized to efficiently reduce overheating in device performance [1][8][9].

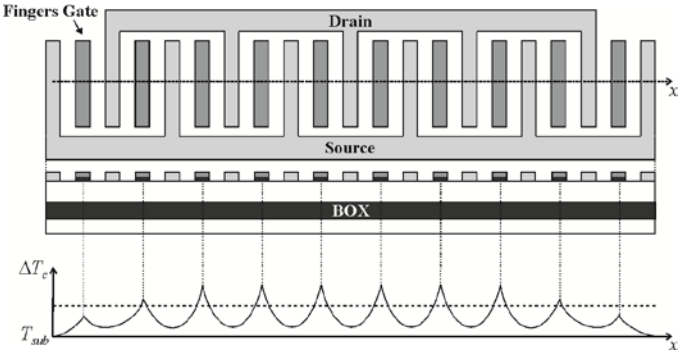

Fig. 1. Multi-finger device thermal coupling: Top view of transistor and schematic representation of the typical temperature rise in the channel, along the heat source in *x* direction.

Several precise techniques have been developed to measure thermal resistance in FETs. They are based on the AC conductance method [10][11], pulsed characteristics [12][13], IR and Raman thermographs [14], or even by extraction of a traps activation energy [15]. However, more progress is still needed to effectively model the thermal characteristics in SOI-MOSFETs, due to the thermal coupling that takes place in devices with nano-scale dimensions [1][2]. It can even lead to negative output conductance in low-frequency regimes [12].

The microelectronics community has made remarkable efforts towards the development of thermal models for MOSFETs [1][2][16-18]. Although detailed thermal models are desirable in order to achieve an exhaustive physical description [1][18], simplification is mandatory when dealing with compact models, such as BSIMSOI [19][20], for circuit simulation purposes. Thus, the thermal conductance in SOI-MOSFETs is usually modeled with a linear dependence on the gate width [21], without taking into consideration the number of fingers (no matter which gate configuration is used, the device's thermal resistance is estimated through the gate width), which is valid only when the thermal coupling is saturated. That is, when internal fingers determine the transistor temperature due to overheating [2][22][23]. For example, Fig. 1 shows a schematic distribution of the typical temperature rise in the channel of multi-finger devices, similar to that obtained using three-dimensional thermal TCAD simulations [22], where the thermal coupling between the gate

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fingers increases the measured average temperature ΔT_c (dashed line).

Regarding variation in thermal resistance with gate length, SOI-MOSFETs' thermal resistance increases with reductions in channel length in the micrometer range (when BOX is thin enough). However, this dependence becomes weak in the cases of very long and short channel devices [20], as heat is mainly dissipated through the substrate (with the thermal resistance being evaluated as in [24]) and terminal contacts (as contacts do not scale with gate length), respectively. According to the International Technology Roadmap for Semiconductors (ITRSs) [25], and given that the BOX layer in the SOI-MOSFETs we investigated was thick enough to avoid heat dissipation through the substrate, this work does not consider variation in thermal resistance with gate length.

In this paper, we propose a simple model for circuit simulators for the thermal resistance of SOI-MOSFETs, accounting for the gradual thermal coupling when the number of fingers increases and including the substrate temperature dependence. The approach could be applied to higher drain current devices, which support higher operating temperatures, such as III-V devices and, particularly, GaN-based transistors (HEMTs) for high-power RF applications [26].

Thus, the SOI-MOSFETs under consideration, by varying the gate geometry, are presented in Section II. The experimental set-up for electrothermal characterization is described in Section III. Section IV devotes to thermal resistance characterization, extraction and modelling, and discusses the results. Finally, the conclusions are summarized in Section V.

II. Fabricated Devices

In order to validate the proposed model, eight partially depleted SOI N-channel MOSFETs, body tied to prevent the floating-body effect, were studied. The devices, which gate length was 180 nm, were built using XT018 0.18μm HV SOI-CMOS technology (by XFAB) within an 8-inch p-type SOI wafer process.

To this end, different multi-finger devices were designed, composed of 5, 10, 20, and 30 parallel fingers (N_f) (to exhibit considerable self-heating), each finger being 2 μm wide (W_f). Therefore, the total gate width ($W = N_f W_f$) was 10, 20, 40, and 60 μm, respectively. Identical gate widths were used to build four single-finger devices (to minimize self-heating), for comparison.

The devices were embedded in ground–signal–ground (GSG) on-wafer test structures, with co-planar waveguide access pads and grounded guard rings, to enable high frequency measurements [12][27]. For every transistor, three additional structures (single-open, single-short, and thru) were designed to perform the subsequent de-embedding technique [28], based on the four steps in [29], in order to eliminate the parasitic effects introduced by pads and the guard ring.

III. Experimental set-up

On-wafer measurements were performed with a CASCADE-Summit 9000 probe station. DC measurements were obtained using an Agilent B1500A Semiconductor Analyzer and the substrate temperature, T_{sub} (30 ºC to 150 ºC, in 20 ºC increments, to avoid damaging or degrading the performance of the device under test –DUT– through excessive threshold voltage displacement) was set through a thermal chuck.

The scattering parameters (*S*-parameters) were measured from 50 MHz to 1 GHz at the substrate temperatures indicated, using the Agilent 8720ES Vector Network Analyzer (with internal bias tees) and Cascade GSG microprobes as shown in Fig. 2(a), using the Agilent B1500A Semiconductor Analyzer for biasing. In order to calibrate the measurement system, the short-open-load-through method was implemented in a previous step.

For pulsed measurements, see Fig. 2(b), an Agilent HP8133 signal generator applied a pulse to the gate of the SOI-MOSFETs ($V_{g\text{-}pulse}$), with the pulse base being set at a level, 0 V, where the device is off; a PSPL5370 pick-off tee was used in the gate to allow non-intrusive monitoring of the gate pulse voltage, as in [27]. An Agilent HP54754 digitizing oscilloscope recorded the voltage pulse of the drain ($V_{d\text{-}pulse}$) through a bias tee, [30]. The bias tee has two roles in this set-up: it applies DC signals to the device (drain-to-source

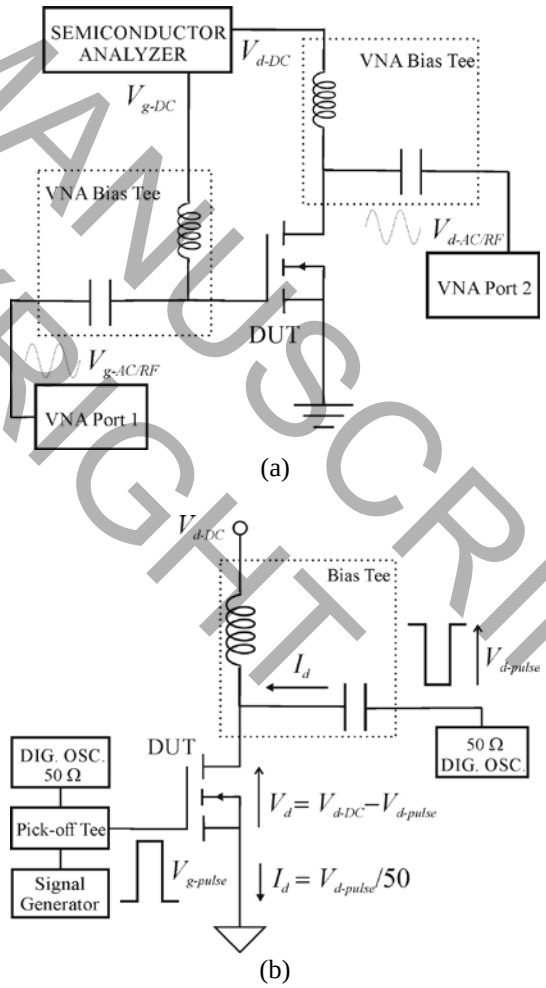


Fig. 2. Schematic of the measurement system: (a) AC/RF and (b) pulsed.

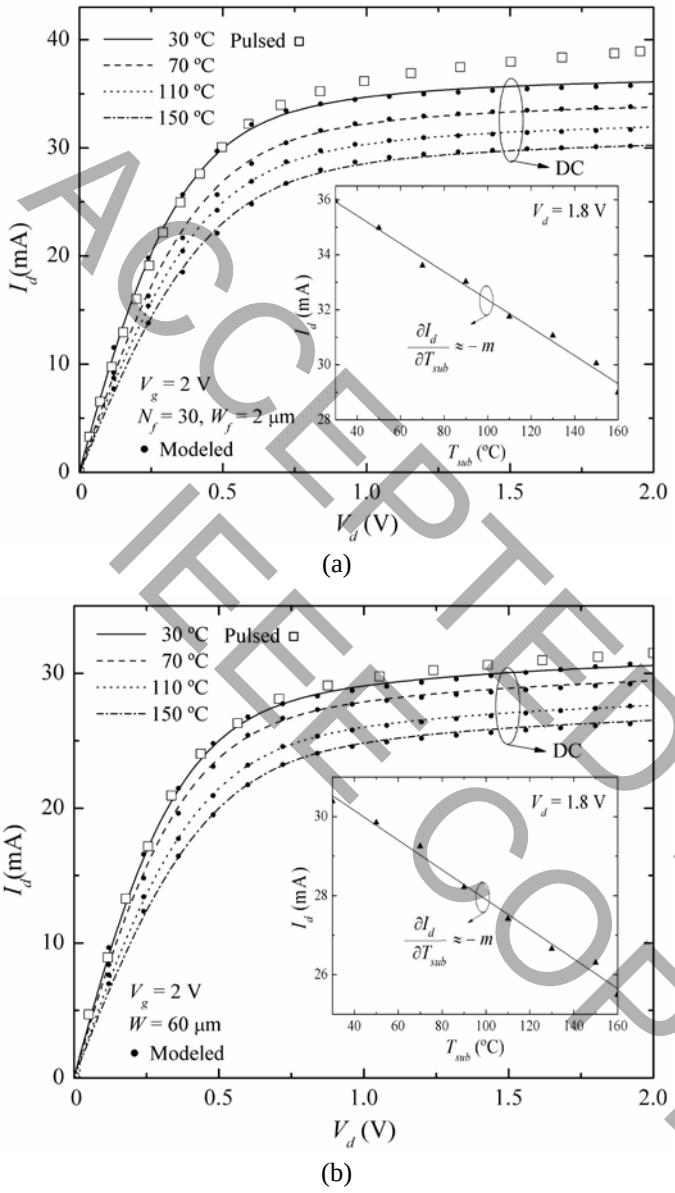


Fig. 3. Measured (lines) and modeled (circles) DC output characteristics at different substrate temperatures for (a) a multi-finger SOI-MOSFET (where N_f = 30 and W_f = 2 µm) and (b) a single-finger transistor (with W = 60 µm), and corresponding pulsed output characteristics at 30 °C (open squares); V_g = 2 V. The inset plot shows the resulting linear temperature dependence of the drain current with the substrate temperature, for V_d = 1.8 V.

voltage $V_{d\text{-}DC}$) whilst isolating the power supply from pulsed signals, and it allows pulsed signals to pass through the bias tee capacitor. Thus when the gate switches from 0 V to $V_{g\text{-}pulse}$, the (I_d, V_d) value switches from (0, $V_{\text{d-}DC}$) to ($V_{d\text{-}pulse}$ /50, $V_{d\text{-}DC} - V_{d\text{-}pulse}$). Output characteristics can be generated by varying $V_{d\text{-}DC}$. Finally, pulses 50 ns wide with a 0.01% duty cycle were used to avoid self-heating [12].

IV. Thermal Resistance Characterization

Self-heating effects were primarily demonstrated in the fabricated SOI-MOSFETs, by measuring their output characteristics using nanosecond pulses, as previously indicated. The corresponding results for the 30-fingers and single-finger transistors with the same total gate width (60 µm), a substrate temperature of 30 °C and a gate bias voltage of 2 V (to enhance self-heating effects) are presented (open squares) in Fig. 3(a) and 3(b) respectively, with DC measurements (solid lines) for comparison. It should be noted that in the saturation region the current increment cannot be obviated when self-heating is prevented (by using pulsed measurements), particularly in the case of the multi-finger device, where self-heating effects are more marked and the drain current greater, due to lower contact resistance at the source/drain terminals.

Therefore, thermal resistance characterization is mandatory in SOI technology. For this purpose, and because self-heating assessed by the pulsed technique might be underestimated [12], the AC conductance method is used as follows.

A. Extraction

The thermal resistance, R_{th}, is obtained for substrate temperatures up to 150 ºC by applying the AC conductance technique [10][12] as

$$R_{th}=\frac{g_{ddo}-g_{ddT}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT}+V_g g_{gdT}+I_d\right)} \quad (1)$$

where g_{ddo} and g_{ddT} are the conductance, g_{dd}, at low frequency (with dynamic self-heating present) and at high frequency (with dynamic self-heating removed), respectively, and g_{gdT} is $g_{gd}=\partial I_d/\partial V_{gd}$ without dynamic self-heating, which are derived from corresponding S parameters [12]. The rest of the parameters (g_{ddo}, which is approximated by the DC output conductance as source and drain access resistances are very low, I_d, and $\partial I_d/\partial T_{sub}$) are obtained from output characteristics at different substrate temperatures (lines and inset plot in Fig. 3(a) and 3(b)).

In SOI-MOSFETs, when dynamic self-heating vanishes g_{dd} plateaus at around 100 MHz [11][12][31][32]. Then, it is observed that $V_g g_{gdT} \ll V_d g_{ddT}$ and the thermal resistance can be approximated by

$$R_{th}\approx\frac{g_{ddo}-g_{ddT}}{\frac{\partial I_d}{\partial T_{sub}}\left(V_d g_{ddT}+I_d\right)} \quad (2)$$

The measured g_{dd} frequency response for a substrate temperature of 30 ºC (in a saturation regime where V_d = 1.8 V and V_g = 2 V, to enhance self-heating effects) is represented by lines in Fig. 4(a) and 4(b) for multi-finger and single-finger transistors, respectively. Similar results are obtained for the rest of the temperatures.

The increase in output conductance over a wide frequency range is due to substrate-related effects (majority carriers) at frequencies of some hundreds of megahertz, and gate resistance in the gigahertz range [11]. Inset plots show that conductance remained constant between 150 MHz and 200 MHz, where average g_{ddT} can be measured to be used in (2).

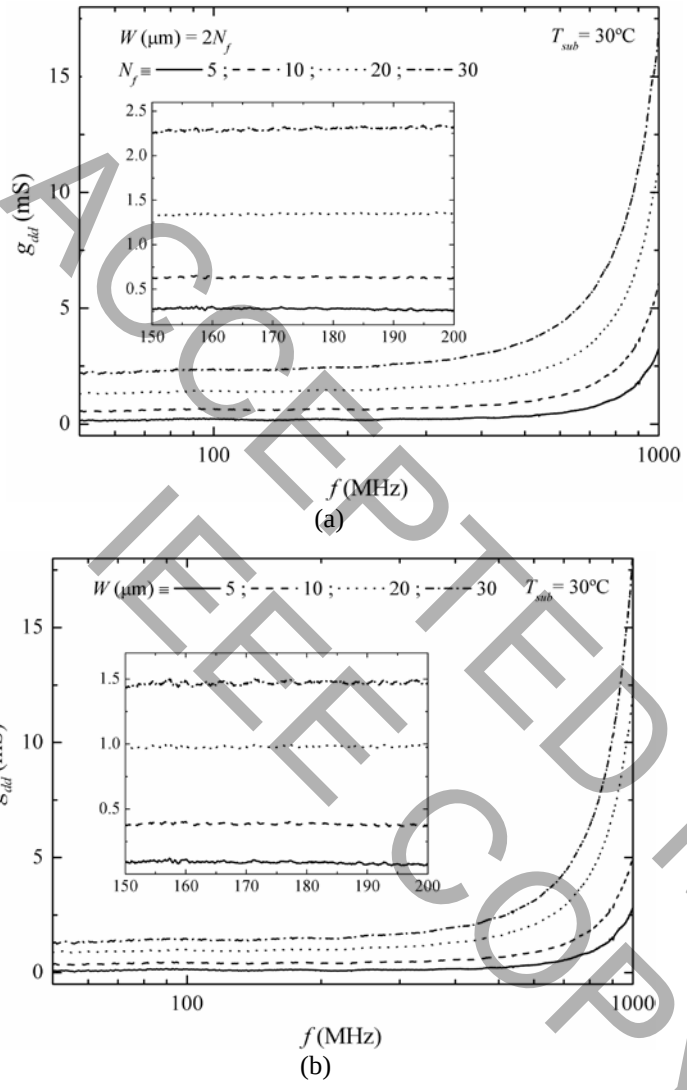


Fig. 4. Output conductance frequency response at 30 °C for (a) multi-finger transistors, and (b) single-finger transistors; V_g = 2 V, V_d = 1.8 V. Inset plots show the conductance plateau and the corresponding frequency range, where average g_{ddT} can be evaluated.

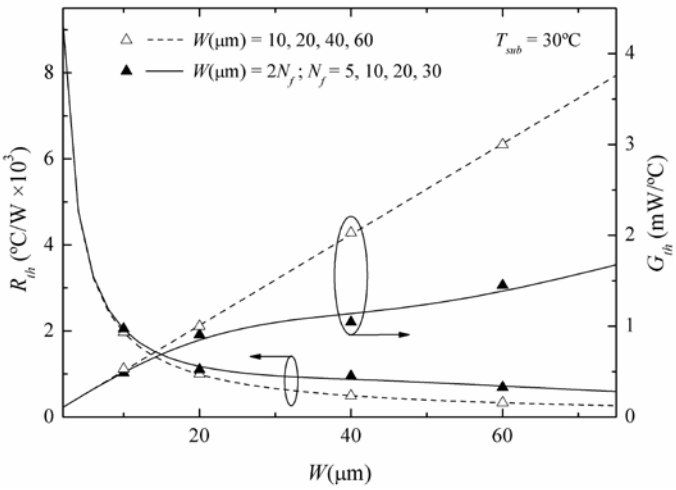


Fig. 5. Comparison of the thermal resistance (left axis) and conductance (right axis), as a function of gate width, extracted and modeled for multi-finger transistors (with solid symbols and solid line, respectively), and single-finger transistors (with open symbols and dashed line, respectively); T_{sub} = 30 ºC.

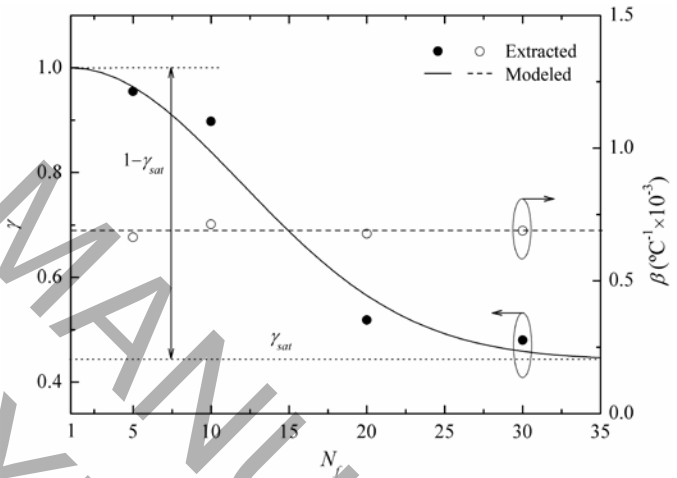


Fig. 6. Extracted (scattered), and modeled (line) finger width coefficient (left axis) and temperature coefficient (right axis), as a function of the number of fingers.

B. The model

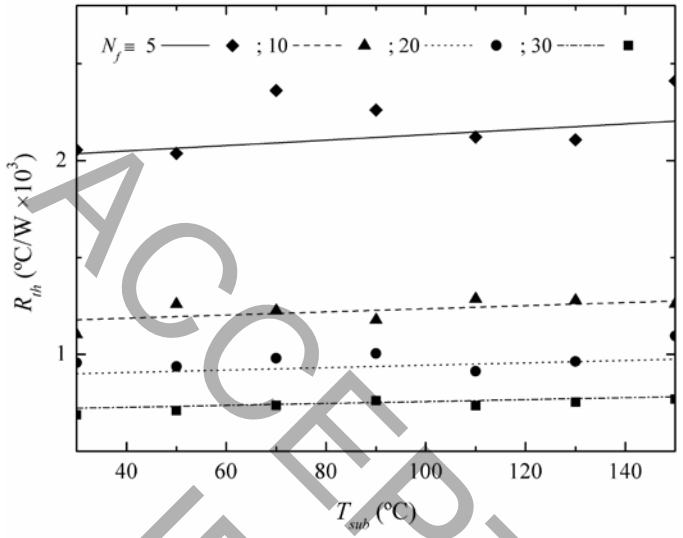
The measured thermal resistance for the transistors, at a substrate temperature of 30 ºC, depends on the gate width, W, as indicated in Fig. 5, left axis; open and closed symbols represent single-finger and multi-finger devices, respectively. Similarly, the corresponding measured thermal conductance is represented on the right axis.

As mentioned previously, thermal resistance in SOI-MOSFETs is strongly dependent on technology and needs to be characterized experimentally for each one, making comparison of normalized thermal resistances (R_{th}×W) a difficult task. Nevertheless, in this work the measured thermal resistance of single-finger devices was of the same order of magnitude as that of SOI-MOSFETs in [20] [32] [33], when normalized. Moreover, similar normalized thermal resistances were measured for multi-finger transistors in [11] for FinFETs.

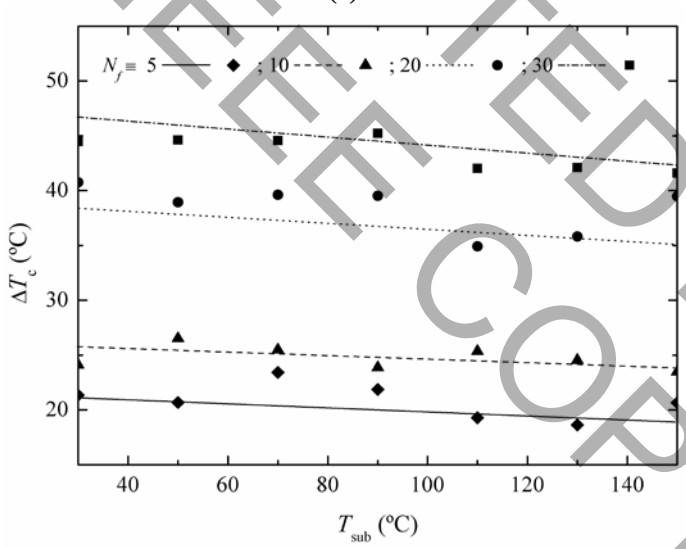
Note that for the single-finger SOI-MOSFETs under investigation, the measured thermal conductance, $G_{th} = 1/R_{th}$, has a linear dependence on the gate width. Thus, it can usually be modeled as $G_{th} = (\alpha + W)/R_{tho}$ [21], where α = 0.19 µm and R_{tho} = 2×10^4 ºC-µm/W, which are technologically dependent fitting parameters. The modeled thermal conductance and the corresponding thermal resistance are plotted with dashed lines in Fig. 5, showing a good agreement with measured data.

Conversely, in multi-finger transistors, thermal coupling increases as the number of fingers, N_f, increases; this is made evident through the non-linear dependency of the measured thermal conductance on the gate width. In this case, the G_{th} augmentation with W diminishes as the number of fingers increases, with a linear dependence that is estabilished, because thermal coupling saturates, when the number of fingers is high enough (N_f » 10), as in [21][23].

The linear thermal conductance model for a single-finger transistor at 30 ºC can be extended to multi-finger devices, defining an effective finger width, $W_{f\text{-}eff}$, as



(a)



(b)

Fig. 7. Thermal resistance (a) and temperature rise in the channel (b), as a function of the substrate temperature, extracted from measurements (scattered) and modeled (lines) for multi-finger devices; V_g = 2 V, V_d = 1.8 V.

$$\frac{1}{R_{th\text{-}30ºC}} \approx \frac{\alpha + N_f W_{f\text{-}eff}}{R_{tho}}, \tag{3}$$

where the effective finger width accounts for the thermal coupling, $W_{f\text{-}eff} = \gamma W_f$ ($\gamma < 1$).

The finger width coefficient, γ, is extracted from the measured data using (3) and depends on the number of fingers as shown in Fig. 6 (left axis, with symbols). It can be modeled using a Gaussian function (with solid line) as:

$$\gamma = \gamma_{sat} + (1 - \gamma_{sat}) e^{-\frac{(N_f - 1)^2}{2\sigma^2}} \tag{4}$$

where γ_{sat} = 0.44; this being the reduction coefficient when thermal coupling saturates ($N_f \to \infty$), and σ = 10.9 is the standard deviation. Both fitting parameters are technologically dependent. Thus, a good agreement between modeled and extracted data for γ in multi-finger SOI-MOSFETs is achieved, as well as for G_{th} and R_{th}, with modeled data being represented by the solid line in Fig. 5. Note that for N_f = 1 (γ = 1) the thermal resistance predicted tends to be the same as that for a single-finger transistor 2 μm wide (i.e. the finger width).

Once thermal resistance has been characterized at 30 ºC, the substrate temperature incidence is analyzed. It was observed that the thermal resistance linearly increases with the substrate temperature, as Fig. 7(a) shows for multi-finger devices (with symbols), which can be modeled as in [34].

$$R_{th} \approx R_{th\text{-}30ºC}(1 + \beta \Delta T_{sub}) \tag{5}$$

where $R_{th\text{-}30ºC}$ is given by (3), ΔT_{sub} is the substrate temperature increment, T_{sub} – 30 ºC, and the temperature coefficient β is a technologically dependent fitting parameter, which is represented in Fig. 6 (right axis, with symbols). Practically no variation in temperature coefficient is observed for a different number of fingers, and an average value (the dashed line), $\beta = 7\times10^{-4}$ (ºC^{-1}), which is comparable to that found in [4] with SOI technology, is enough to model the substrate temperature dependence of the thermal resistance for any device. Fig. 7(a) shows the resulting thermal resistance modeled for multi-finger SOI-MOSFETs (with lines), with a maximum relative error of 10% with respect to measured data at any substrate temperature. Similar results are obtained for single-finger SOI-MOSFETs.

Finally, the temperature rise in the device channel above substrate temperature, $\Delta T_c = T_c - T_{sub}$, is obtained as $R_{th} V_d I_d$ in the saturation regime (with V_d = 1.8 V and V_g = 2 V, to enhance self-heating effects). For single-finger transistors, ΔT_c remains almost constant at approximately 19 ºC, for any substrate temperature. In the case of multi-finger devices, as expected, ΔT_c strongly depends on the number of fingers (by thermal coupling), as Fig. 7(b) indicates for measured data (with symbols). Furthermore, as substrate temperature rises, a slight decrease in ΔT_c is observed, its dependence diminishing as the number of fingers reduces. In case of the multi-finger SOI-MOSFET with 30 parallel fingers (i.e. the worst case), the channel temperature, $T_c = T_{sub} + \Delta T_c$, reaches around 190 °C (on average, along the channel) at a substrate temperature of 150 °C, which is close to the typical maximum operating temperature (200 °C) for complementary metal-oxide semiconductor (CMOS) logic.

When accounting for (5) and the linear temperature dependence of the drain current, $I_d \approx I_{d\text{-}30ºC} - m \cdot \Delta T_{sub}$ (see inset plot in Fig. 3(a) and 3(b)), the resulting model (lines in Fig. 7(b)) predicts the measured temperature rise in the channel, with the same maximum relative error as obtained in the case of thermal resistance, 10%.

Additionally, electro-thermal simulations were performed with BSIMSOI (version 3.1) using the thermal-electrical analogy. BSIMSOI models DC self-heating by introducing an

internal temperature node into the device. This node is connected to ground through the thermal resistance, which is given by (5), and the nodal "voltage" is actually the device temperature when the current flowing through the thermal resistance equals the electrical power dissipated in the device, V_dI_d. Modeled output characteristics for 60 µm-wide multi-finger and single-finger SOI-MOSFETs at different substrate temperatures (with V_g = 2 V) are presented (closed circles) in Fig. 3(a) and 3(b) respectively, showing a good agreement with the corresponding DC measurements (lines).

Lastly, thermal coupling analysis also demands the extraction of thermal capacitance in order to determine the thermal cross talk/temperature rise and thermal time constant; this will the object of future work.

V. Conclusions

A thermal resistance model for SOI-MOSFETs, accounting for the multi-finger thermal coupling and the substrate temperature, has been presented. The model, incorporating the number of fingers, predicts device overheating for substrate temperatures up to 150 ºC, when the temperature rise in the channel ascends to 45ºC with maximum thermal coupling. Furthermore, as substrate temperature increases the temperature rise in the channel slightly diminishes, dependence vanishing as the thermal coupling is reduced. Finally, this modelling approach for thermal resistance can easily be added to other well-established models in circuit simulators.

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