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Título de la Tesis

APORTACIONES AL DISEÑO DEL SISTEMA DE RECUPERACIÓN Y ESTABILIZACIÓN DE ENERGÍA PARA SENSORES INALÁMBRICOS PASIVOS DE LARGO ALCANCE

Título de la Tesis (English):

CONTRIBUTIONS TO THE DESIGN OF THE ENERGY RECOVERY AND STABILIZATION SYSTEM FOR LONG RANGE PASSIVE WIRELESS SENSORS

Tesis Doctoral presentada por D. Ricardo Morales Ramos

Dirigida por el Dr. D. Juan Antonio Montiel Nelson
Codirigida por el Dr. D. Andrés García-Alonso Montoya

El Director, **El Codirector,** **El Doctorando,**

Andrés G-Alonso

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"Cuando quieres realmente una cosa,
todo el Universo conspira para ayudarte a conseguirla."

Paulo Coelho, Novelista, compositor de canción popular, periodista y dramaturgo brasileño.
24 de agosto de 1947 a –.

A mis padres,

a los amigos de verdad,

y a los que creen en el amor.

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List of Acronyms

2P4M 2 Poly 4 Metals

AC Alternating Current

ADC Analog to Digital Converter

ASK Amplitude Shift Keying

BICMOS Bipolar Junction Transistors and CMOS

BJT Bipolar Junction Transistor

BW BandWidth

CC Charge of a Capacitor

CCD Charge–Coupled Device

CEIT Centro de Estudios e Investigaciones Técnicas de Gipúzcoa

CEPT Conférence Européenne des administrations des Postes et des Télécommunications

CMOS Complementary Metal Oxide Semiconductor

CTAT Complementary To Absolute Temperature

CW Continous Wave

dB deciBel

DC Direct Current

EEPROM Electrically Erasable Programmable Read Only Memory

EIRP Equivalent Isotropically Radiated Power

EM ElectroMagnetic

EPC Electronic Product Code

ERP Effective Radiated Power

ERS Energy Recovery System

ES Enable Signal

ETSI European Telecommunications Standards Institute

FCC Federal Communications Commission

GND GrouND

HF High Frequency

I-V Intensity–Voltage characteristic

IC Integrated Circuit

ID IDentification

IEEE Institute of Electrical and Electronics Engineers

IIS Institut fuer Integrierte Schaltungen

ISM band Industrial, Scientific and Medical radio bands

ISO International Organization for Standardization

ITU International Telecommunication Union

IUMA Instituto Universitario de Microelectrónica Aplicada

LDO Low Drop Out

LF Low Frequency

MEMS MicroElectroMechanical Systems

MMS Modified Mode Selector

MMS' Modified Mode Selector (adjusted)

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

MS Mode Selector

MS' Mode Selector (adjusted)

NMOS N–channel MOSFET

OOK On–Off Keying

PIE Pulse Interval Encoding

PMOS P–channel MOSFET

Poly Polysilicon

POR Power On Reset

POR' Power On Reset (adjusted)

PSFTP Power Supply Feed Through

PSK Phase Shift Keying

PSRR Power Supply Rejection Ratio

PTAT Proportional To Absolute Temperature

PW$_{SR}$ Power Slew Rate

PWM Pulse Wave Modulation

Q Quality factor

RAM Random Access Memory

RF RadioFrequency

RFID RadioFrequency IDentification

RISC Reduced Instruction Set Computer

ROM Read Only Memory

SAW Surface Acoustic Wave

SOI Silicon On Insulator

SOS Silicon On Saphire

TDC Time to Digital Converter

TK Temperature Coeficient

UGF Unity Gain Frequency

UHF Ultra High Frequency

VHF Very High Frequency

VL Voltage Levels

VM Voltage Multiplier

VNA Vectorial Network Analyzer

VP Voltage Protection

VS Voltage sensor

W/L Transistor Dimensions: Width/Length

WISEN WIreless SENsors

Part I

PhD. Dissertation (English)

Abstract

Sensor networks to realize ubiquitous computing require not only a small, simple, and low–cost RF terminal with sensing device, but also a very low–power consumption and a long–distance communication range. Radio frequency identification (RFID) systems are one of the most appropriate RF terminals for sensor networks, satisfying previous requirements. In recent years, RFID tags have become very popular in many applications such as manufacturing, product distribution, sales, security and surveillance. They have a number of additional advantages over the traditional barcode labels namely, larger storage capacity, write capability and larger distance range, among others. Passive RFID systems working in the UHF band will probably be the next generation of RFID systems. Battery–life–less operation, reading distance of few meters and international standards availability, are some of their features.

The integration of a sensor in a long range RFID transponder keeping its operation range of some meters will multiply the application range of the current RFID Tags. However there are some technical barriers to push this idea into practice. This barriers are the AC into DC power conversion efficiency the high power consumption of the sensors and the circuits in the tag. Till now, there is not any RFID sensor operative in the state–of–the–art, although there is a great scientific interest in UHF RFID technologies, both in readers and in tags as well as in ultra low power consumption sensors.

The goal of this PhD. Dissertation is to realize contributions to the design and implementation of the energy recovery and stabilization system for long range passive wireless sensors based on passive UHF RFID technologies. The contributions proposed in this PhD. Thesis as well all the research carried out have been probed with the design, implementation, fabrication and measurement of several microelectronic circuits.

Chapter 1

Introduction

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Abstract: This Chapter introduces the two concepts which are the starting point of this PhD. Dissertation; on the one hand, the wireless sensors, and on the other, the RFID technologies. Other elements concerning the system as the communication protocol or the frequency band are also dealt in this Chapter.

1.1 Wireless sensing

Sensor networks to realize ubiquitous computing require not only a small, simple, and low–cost RF terminal with sensing device, but also a very low–power consumption and a long–distance communication range. Based on this idea there are two main approaches:

- Active wireless sensors and
- passive wireless sensors

1.1.1 Active wireless sensors

Active wireless sensors require batteries for power supply. The use of batteries limits the performance of the wireless sensor in terms of power supply, size, prize, environmental conditions and life time among others.

Figure 1.1 shows the typical architecture of an active wireless sensor [8, 9]. The supply voltage from the battery is distributed to the complete system by the Energy management unit. A processor with internal or external memory controls all the elements of the system. Its main functions are: enabling the Radio unit for transmitting or receiving data, monitoring of charge available on the battery, reading and processing data acquired by the sensors.

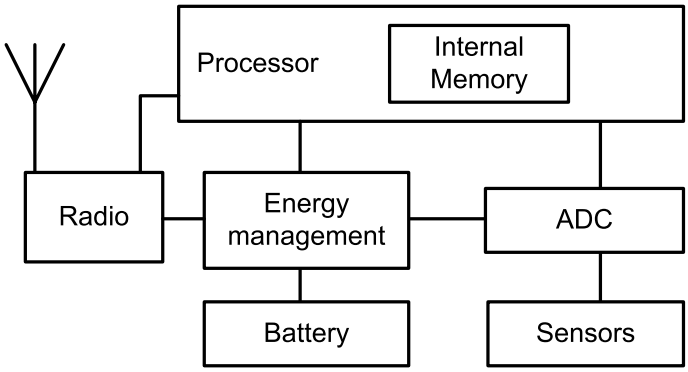

Figure 1.1: Block diagram of an active wireless sensor.

In recent times, there is a great interest for reducing the power consumption of each individual blocks of the architecture. Power consumption of Radio transponders reported in the last years has decreased dramatically falling below 1mW in receive mode [10, 11] and around 3 mW in transmit mode for distances up to 16 meters [12]. Simultaneusly, great advances in ADC and processor for ultra-low-power consumption has been reported[13, 14] achieving consumptions under 1mW in each case. In spite of the last promising results, batteries can not be avoided.

1.1.2 Passive wireless sensors

Passive wireless sensors do no require batteries for power supply. They get energy from the environment and convert this energy in a DC voltage able to supply the system [15]. The most common method to transport wirelessly power is the inductive coupling. DC power is converted into AC power and radiated throw a primary coil by the interrogator device. A remote secondary coil matched with the primary coil collects AC power from the primary coil. Finally this AC power is converted back in DC power for system supply. The principal drawback of this systems comes from the fact that the field strength path of a magnetic antenna along the coil x axis follows the relationship $1/d^3$ in the near field [16]. This corresponds with a damping of 60dB per decade of distance between coils. This huge attenuation of magnetic field limits severely the range of these systems. Sensors reported in the bibliography reaches ranges from a few centimetres up to 1 meter [17, 18, 19].

In order to increase the operation range without introducing batteries, alternative ways to wirelessly supply the system must be found. It has been reported several attempts

like [20], where a pressure sensor is excited optically. In this work a LC network is resonated by help of a silicon tunnel diode. The inductance of the resonant network is also an antenna, and the capacitance is a capacitive MEMS sensor. An antenna tuned in the average resonance frequency and with an adequate bandwidth gets remotely the sensor response.

Another alternative is using solar cells for power generation [21]. Of course this approach presents problems in low–light environments and requires special process to fabricate photovoltaic cells.

However, in the field of wirelessly powered electronic, RFID technologies are pioneers. They used firstly inductive coupling and, in the last decade, also electromagnetic coupling to power up identification chips [1]. In particular electromagnetic coupled system permits long range supplying and communications. Precisely, the idea of using RFID electromagnetic coupling transponders as RF and power interface is the starting point of this Ph.D. Dissertation. Next section introduces RFID systems, in order to give a general idea of how this systems works. Then Electromagnetic coupling systems are described with more detail.

1.2 RFID systems

Radio Frequency IDentification systems (RFID) or smart labels are identification systems based on an electronic device that can be wirelessly interrogated. An RFID system is always made up of two components:

- the transponder or tag, which is located on the object to be identified;
- the interrogator or reader, which, depending upon the design and the technology used, may be a read or write/read device.

The Reader begins the communication protocol interrogating all the Tags inside its coverage range. Once, a Tag receives a request from a Reader it sends back to the interrogator the required information. Finally, Reader processes the incoming data and presents complete information to the end–user. Figure 1.2 illustrates the fundamental operation of a radiofrequency identification system.

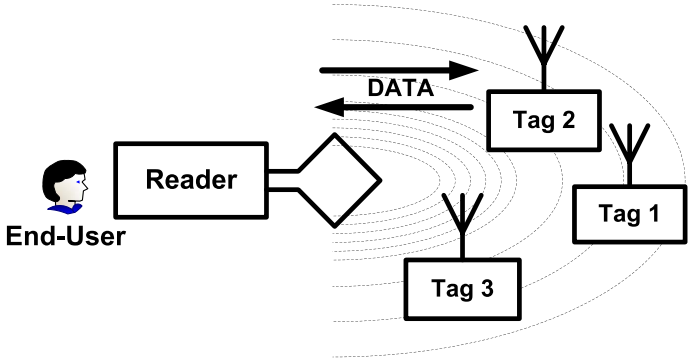

Figure 1.2: Operation scheme of a radiofrequency identification system.

Each particular tag possesses an identification code stored in an internal memory. After the identification code has been read, the interrogator device identifies the smart

label in its data base. This basic scheme finds application in plenty of fields. Some examples of RFID systems applications are enumerated below:

- Contactless Smart Cards like smart cards for mobile phones or bank cards.
- Public transport, to replace the conventional paper tickets.
- Ticketing, for fast check–in at the airport, to fast control enter to sport events, or to ski lift.
- Electronic access control system, to automatically check the access authorization of individuals to buildings or rooms, or even as a electronic key implanted in the human hand [22].
- Transportation System, for train tracking and control. An example of this is the Eurobalise [16], a project which aim is to control trains all around Europe.
- Animal identification. An RFID tag is implanted in both pets and wild animals.
- Electronic immobilization as an anti–theft systems widely used in automobile industry.
- Container identifications, for container tracking around its travel.
- Industrial automation, as a tool for process identification or assembly line monitoring.

For instance, building access control, in all kind of identification: goods in warehouses, pets of wild animals, persons (intelligent ID card), or products in an assembly line. In general, as a substitute of the traditional barcodes, as anti–fake method or as anti–theft device.

1.2.1 RFID systems classification

Once the potential of the RFID system and its applications has been introduced, it is the moment to present the different types of RFID systems. The most important differentiation criteria for RFID systems are the operating frequency of the reader, the physical coupling method and the range of the system. RFID systems are operated at widely differing frequencies, ranging from 135 kHz longwave to 5.8 GHz in the microwave range. Electric, magnetic and electromagnetic fields are used for the physical coupling. Finally, the achievable range of the system varies from a few millimeters to above 15 m.

Close coupling systems

RFID systems with a very small range, typically in the region of up to 1 cm, are known as close coupling systems. For operation, the transponder must either be inserted into the reader or positioned upon a surface provided for this purpose. Close coupling systems are coupled using both electric and magnetic fields and thus can theoretically be operated at any desired frequency, between DC and 30 MHz, because the operation of the transponder does not rely upon the radiation of fields. The close coupling between data carrier and reader also facilitates the provision of greater amounts of power and so even a microprocessor with non–optimal power consumption, for example, can be

operated. Close coupling systems are primarily used in applications that are subject to strict security requirements, but do not require a large range. Examples are electronic door locking systems or contactless smart card systems with payment functions. Close coupling transponders are currently used exclusively as ID–1 format contactless smart cards (ISO 10536) [23]. However, the role of close coupling systems on the market is becoming less important.

Inductive coupling systems

Systems with write and read ranges of up to 1 m are known by the collective term of remote coupling systems. Almost all remote coupled systems are based upon an inductive (magnetic) coupling between reader and transponder. These systems are therefore also known as inductive radio systems. At least 90% of all RFID systems that are currently sold are inductively coupled systems. For this reason there is now an enormous number of such systems on the market. There is also a series of standards that specify the technical parameters of transponder and reader for various standard applications, such as contactless smart cards, animal identification or industrial automation. These also include proximity coupling (ISO 14443, contactless smart cards) and vicinity coupling systems (ISO 15693, smart label and contactless smart cards[24, 25]). Frequencies below 135 kHz or 13.56 MHz are used as transmission frequencies. Some special applications, e.g. Eurobalise, are also operated at 27.125 MHz.

Electromagnetic coupling systems

RFID systems with ranges significantly above 1 m are known as long–range systems. All long–range systems operate using electromagnetic waves in the UHF and microwave range. The vast majority of such systems are also known as backscatter systems due to their physical operating principle. In addition, there are also long–range systems using surface acoustic wave transponders in the microwave range. All these systems are operated at the UHF frequencies of 868 MHz (Europe) and 915 MHz (USA) and at the microwave frequencies of 2.5 GHz and 5.8 GHz. Typical ranges of 3 m can now be achieved using passive (battery–free) backscatter transponders, while ranges of 15 m and above can even be achieved using active (battery–supported) backscatter transponders. The battery of an active transponder, however, never provides the power for data transmission between transponder and reader, but serves exclusively to supply the microchip and for the retention of stored data. The power of the electromagnetic field received from the reader is the only power used for the data transmission between transponder and reader.

1.2.2 Components of RFID systems

The major elements involved in a RFID System are Reader and Tag. A description of both components is presented in the next lines.

Reader

Despite the fundamental differences in the type of coupling (inductive–electromagnetic), the communication standard, the data transmission procedure, and frequency range, all readers are similar in their basic operating principle and thus in their design. Readers

in all systems can be reduced to two fundamental functional blocks: the control system and the HF interface, consisting of a transmitter and receiver. Figure 1.3 illustrates the basic architecture of the reader.

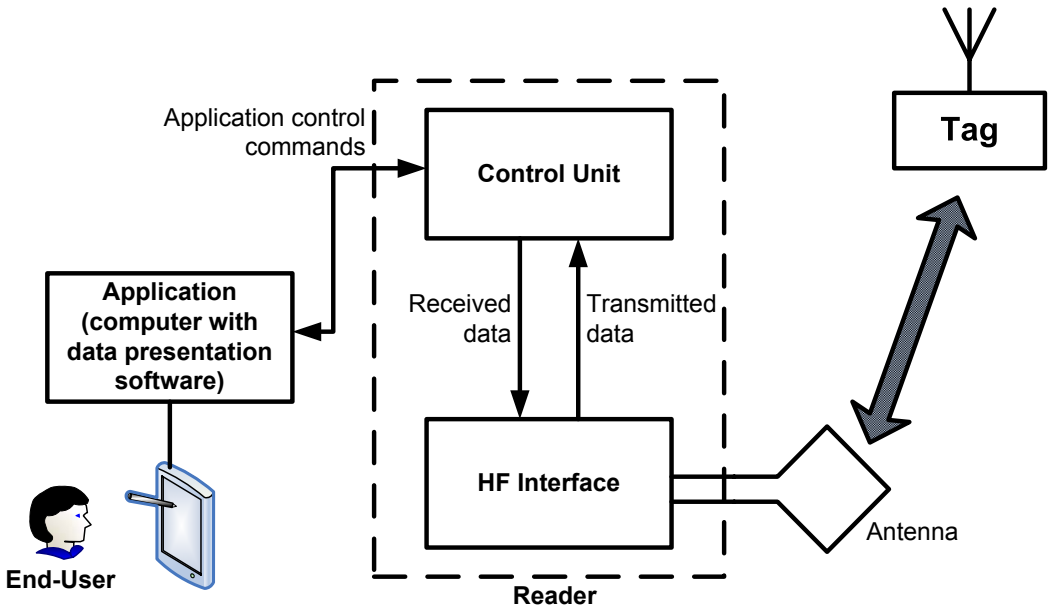

Figure 1.3: Generic architecture of a RFID reader.

Reader HF interface The reader HF interface performs the followings functions:

- generation of high frequency transmission power to activate the transponder and supply it with power,
- modulation of the transmission signal to send data to the transponder;
- reception and demodulation of HF signals transmitted by a transponder.

Reader Control Unit The reader Control Unit interface performs the followings functions:

- communication with the application software and the execution of commands from the application software;
- control of the communication with a trtansponder (master–slave principle);
- signal coding and decoding.

Other additional functions in complex systems are:

- execution of an anti–collision algorithm;
- encryption and decryption of the data to be transferred between tag and reader; and
- performance of authentification between tag and reader.

1.2.3 Tag

RFID tags also called data carriers must be differentiated between two fundamental operating principles: the electronic data carriers based on integrated circuits and data carriers that exploit physical effects for data storage. Both 1–bit transponders and surface wave components belong to the latter category. They do not integrate complex electronic circuits, they are basically a piezocrystal attached to an antenna [26]. The incoming RF wave is converted to a surface wave that travel along the crystal and it is back radiated to the reader. The velocity of the surface wave varies with the crystal configuration. This leads to a change of the phase that can be detected by the reader. This tag category is outside the scope of this Ph.D. Dissertation therefore, they will not be dealt in more detail.

Figure 1.4 depicts the general architecture of an electronic tag, and its components are described below.

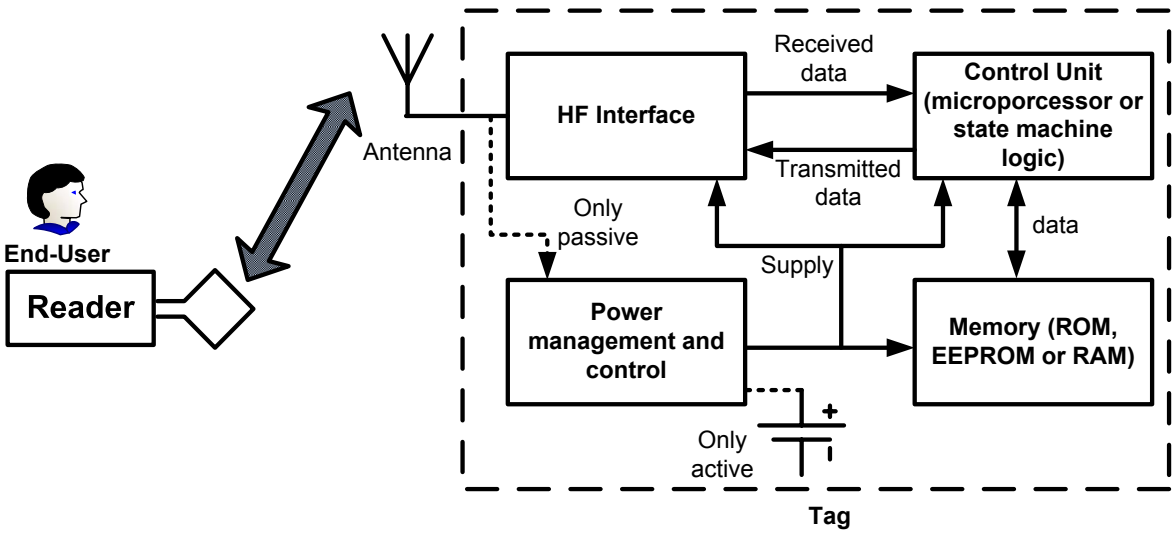

Figure 1.4: Generic architecture of an electronic RFID tag.

HF interface The HF interface forms the interface between the analog, high frequency transmission channel from the reader to the transponder and the digital circuitry of the transponder. The HF interface, therefore, performs the function of a classical modem (modulator–demodulator) used for analog data transmission via telephone lines.

Power management and control Power management and control is the block in charge of generating the required voltage level to supply the complete system. Passive transponders are supplied with energy via the HF field of the reader. To achieve this, power management draws current from the transponder antenna, which is rectified and supplied to the chip as a regulated supply voltage. On the other side, active tags are powered by a battery that also requires regulation and charge monitoring systems.

Control unit The control unit forms the intelligence of the transponder and controls all the processes on the chip. This is memory access, reader commands interpretation,

communication and security protocols implementation, cryptological functions and other additional functionalities.

The control unit can be implemented either by a state machine and the logic required for each function (non–programmable) or by a microprocessor (programmable). The former philosophy is more power and cost efficient at the expense of system flexibility. The latter include a programmable microprocessor that can also include an operative system giving a complete flexibility to the transponder. The drawback of the latter approach is higher power consumption and costs. Non–programmable control units are more suitable for passive tag due to its lower power consumption.

Memory The RFID transponders require of a non–volatile data storage system to store the identification code requested by the reader. The most used memories are ROM (read only memory), these memories can only be written once, and EEPROM (Electrical Erasable Read Only Memories), these memories can be electrically erased and rewritten several times. Additionally RAM (random access memories) can be implemented in the tag, especially in programmable architectures.

1.3 Long range passive UHF RFID systems

Once the different kinds of RFID systems and its components have been presented, it is necessary to return to the primary goal of this Ph.D. Dissertation, namely, long range wireless sensors. Thus, it is clear that the RFID system with the longest operation range is the electromagnetic (EM) coupled one. Therefore, EM coupled system is the most suitable RFID type to attempt long range passive wireless sensing. However, long range also implies very low incident RF power level at the tag side, due to the attenuation of the EM field in free space. The consequence of this is that very low power reaches the tag to supply the system. It can be concluded that the power recovery system in long range UHF RFID sensors is the most challenging task in the system design.

Regarding to the components, the reader architecture do not differ from the one used in commercial EM coupled systems. The reader basically radiates the maximal allowed power and implements a standard communication protocol. In principle, commercial readers can be used to interrogate RFID wireless sensors compatible with the standard communication protocol. It is obvious that the main problems are on the tag side. The introduction of a sensor in the tag increases the power requirements and gives additional system complexity. The research involved in this Ph.D. Dissertation is focused on the tag side.

This section describes more in detail Long range UHF RFID systems, with stress in tags. The first point is the communication standard specified for UHF RFID systems, next, the different kinds of tags are listed.

1.3.1 Frequency selection

The Figure 1.5 shows some of the common and less common frequency bands in which RFID systems operate. Also shown is the corresponding wavelength—the distance between points at which the field has a fixed value when the signal moves at the velocity of light.

Several issues are involved in choosing a frequency of operation:

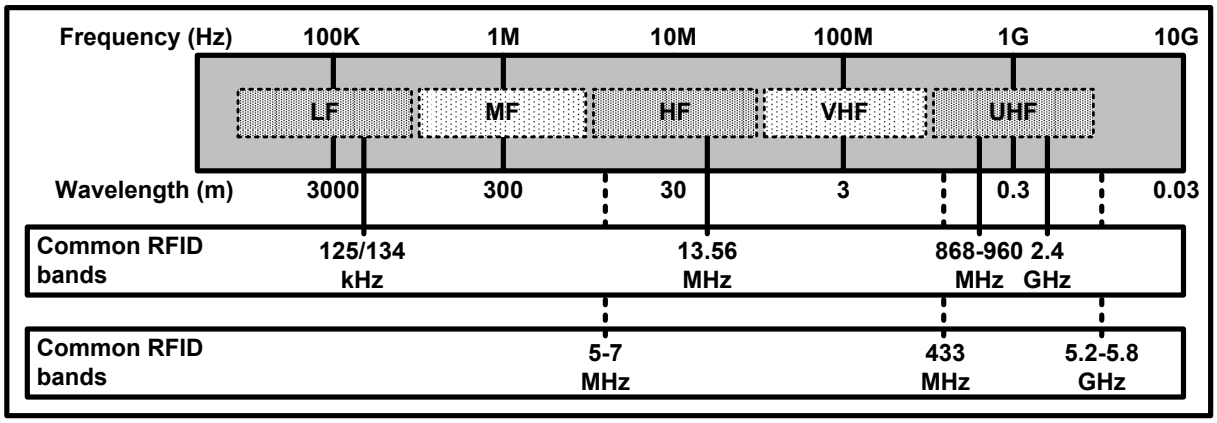

Figure 1.5: Frequency bands in which RFID systems operate.

- The Type of coupling to be employed, either inductive or electromagnetic.
  - Inductively–coupled systems are limited to short ranges comparable to the size of the antenna. In practice, inductive RFID systems usually use antenna sizes from a few centimeters to a meter, and frequencies of 125/134 KHz (LF) or 13.56 MHz (HF). Thus the wavelength (respectively about 2000 or 20 meters) is much longer than the antenna.
  - Electromagnetic–coupled systems use antennas comparable in size to the wavelength. The very common 900 MHz range has wavelengths around 33 cm. Reader antennas vary in size from around 10 to >30 cm, and tags are typically 10–18 cm long. These systems are not limited by reader antenna size but by signal propagation issues.
- The allocation of frequencies by regulatory authorities. In essentially every country in the world, the government either directly regulates the use of the radio spectrum, or delegates that authority to related organizations. In Europe, European Telecommunications Standards Institute (ETSI) [27] regulates the frequencies that radios are allowed to radiate, the power levels they can use, and other more technical aspects of their operation.
- The propagation characteristics of the resulting radiated fields. Lower frequencies diffract more readily around obstacles, but couple less well to small antennas. Radiated fields are absorbed by many common materials in buildings and the environment, particularly those containing water. The degree of absorption due to water increases gradually with increasing frequency.

Returning to the particular case of long range wireless sensors, it is clear that inductive coupling is not an option, since the range is up to around 1 meter. Thus, the remaining unlicensed[1] alternatives are 433 MHz, 860–960 MHz, 2.4 GHz and 5.8 GHz. On the one side, the antenna size limits the use of 433 MHz band, where antennas dimension

[1]The industrial, scientific and medical (ISM) radio bands were originally reserved internationally for the use of RF electromagnetic fields for industrial, scientific and medical purposes other than communications. The ISM bands are defined by the International Telecommunication Union - Radiocommunication sector (ITU-R) [28] and are unlicensed bands, whose particular frequencies can varies form one country to other.

around 30 cm are required. On the other side the attenuation in free space and possible obstacles limits severely the operation range at high frequencies (2.4 GHz and 5.2 GHz). As a conclusion, the band 860–960 MHz meets the best trade–off between antenna size (15–10 cm) [29] and operation range, in unlicensed bands.

1.3.2 Communication standard

RFID are called to be the next generation of barcodes. Since the goal of the barcodes is to identify a product or services everywhere and using devices of different manufacturers, it is mandatory the use of a standard that provides a framework to allows products, services and information about them to move all around the world efficiently and secure. The same way as barcodes, there are standards for RFID [23, 30]. In the particular case of passive UHF RFID, the most popular one is called EPCGlobal Class 1 Gen 2 [31]. This standard is the most widely accepted one for passive UHF RFID [32, 33, 34, 35].

EPCGlobal [36] is a division of GS1, a neutral, not–for–profit and global organization dedicated to the design and implementation of global standards for use in the supply chain [37]. EPCGlobal was set up to achieve world–wide adoption and standardization of electronic Product Code (EPC) technology in an ethical and responsible way. The main focus of the group currently is to create both a world–wide standard for RFID and the use of the Internet to share data via the EPCglobal Network.

EPCglobal Class 1 Gen 2

Approved by EPC global in December 2004, the Class Gen 2 air interface protocol provides a numbers of enhancements that will help solidify the adoption of RFID in the UHF band.

- It establishes a single UHF specification, where previously there were several, including EPC Class 1 [38], EPC Class 0 [39], and two from ISO [23, 30].
- It is designed for worldwide deployment, addressing emerging UHF regulations in different regions.
- It leverages and improves on the best features of preceding UHF specifications, and anticipates a range of future applications a product extension including higher–function sensor tags.

The most interesting features of the standard are listed in Table 1.1.

1.3.3 UHF RFID tags classification

Attending to supply method, UHF RFID tags can be classified into following types: an active tag, a semi–passive tag, and a passive tag.

Active tags The active tag has some external components such as a battery and a crystal, and transmits ID data of the tag using the battery. The active tag supports very long distance communication and can supply power to sensors. However, the active tag has several disadvantages such as finite battery life, large volume, and high cost. This kind of transponders presents a complete active RF front end, and microcontroller based architecture that can also support other communication standards like Zigbee [8], or Bluetooth [40].

Table 1.1: EPC Class 1 Gen 2 Features and Performance

Feature	Performance
Read speed ((Reads per second) running sort protocol; field performance highly dependent on application	- Up to 880 (US FCC) - Up to 450 (EU ETSI) - Speed adaptable to - RF nosie in enviroment
Write speed (for 96–bit EPC)	- 5 tags per second minimum - Rewritable many times
Tag sorting protocol	"Q" protocol: a random number algorithm with 2 persistent symetric states. It enables counting of multiple tags with same EPC, and on–the–fly adaption to size of tag population.
Tag data verification	16-bit CRC for reads and writes
Multiple reader operation	- Frequency hopping (US FCC) - Listen–before–talk (EU CEPT) Dense reader modes (channelization, variable subcarrier modulation) - Four reader "sessions" allowing parallel communications by multiple readers with one tag
Security	- 32-bit lock and kill passwords - Option for "handle"-based communication
Extensibility	- Up to 512 bit item ID - Unlimited user memory - Anticipates next generations (Class 2 & 3 systems)

Semi–passive tags The semi–passive tag has a battery and communicates to the base station using a backscatter method [41, 42] specified in EPCglobal. This means that the semi-passive tag only support EPCglobal as a communication protocol, but reduce the cost of active tags, since do not require additional external and expensive components such a crystal. The communication distance of the semi–passive tag is over 10 m since it operates with the battery, and some sensors can be included. However, the drawback is the limited battery life and it cost increase.

Passive tags The passive tag can communicate to the base station without a battery by using transmitted power from a base station. In view of this mechanism, low–power operation is required for the passive tag. The passive tag communicates to the base station using a backscatter method (specified in EPCglobal Class 1 Gen2), in which

Table 1.2: Comparison among Active tag, Semi–pasive tag and Passive

	Active tag	Semi–pasive tag	Passive tag
Communication Distance	Long	Moderate	Short
Incorporation of sensors	Easy	Possible	Difficult
Necesity of Battery	Need	Need	No need
Cost	High	Moderate	Low

the antenna impedance of the tag is modulated according to the data bit stream. This method is suitable for low power consumption because it does not require large transmission power. The communication distance of a passive tag is generally about 8–16 m because the received power is not sufficient for activating the tag over a greater distance [1, 43]. Table 1.2 shows a comparison of the tags.

From Table 1.2, it can be conclude that a trade off between cost and range must be found in order to find an adequate RF platform for the wireless sensor. This Ph.D. Dissertation is oriented towards the lowest cost direction, this is, passive tags.

1.3.4 Long range passive UHF RFID sensors

Long range passive UHF RFID systems are Electromagnetic Coupling Systems using passive Tags. The coverage range of this type of systems is up to some meters working on the ISM (Industrial, Scientific and Medical) band [44]. Passive tags do not require of batteries and its entire electronic can be integrated in a single chip with the exception of the antenna. Therefore, if the chips are produced in mass, the cost of a single tag can be minimized, around of 10 cents of dollar per unit [45].

The characteristics of passive UHF RFID systems, namely, long range, low cost and ability store data, make this technology very attractive for implement wireless interfaces for sensors. The integration of a sensor inside a long range RFID tag maintaining a coverage range of some meters would multiply the application fields of the current RFID systems.

However there are some technical barriers that have to be overcome to put this idea into practice:

- low RF into DC energy conversion efficiency,
- high power consumption of sensors, and
- high power consumption of the tag circuits.

This Ph.D. Dissertation is focused in the Energy recovery system for Long–Range Passive RFID sensors. For better understanding. the challenge that propose this Ph.D. Thesis, it is necessary to analyze the state–of–the–art in EM coupled RFID systems, passive wireless sensors and low power sensors in order to identify the technical barriers of integrating a sensor in the system.

Chapter 2

State–Of–the–Art

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Abstract: The goal of this chapter is give an overview of the state–of–the–art for better understanding of the challenges proposed in this dissertation. As already mentioned, this Ph.D. Dissertation is focused in the Energy recovery and stabilization system for long range UHF RFID sensors. For better understanding of the challenging problem it is essential to analyze the state–of–the–art in three fields:

- passive UHF RFID tags,
- Energy recovery system in passive wireless sensors, and
- low power sensors.

After the bibliography study it will be possible to identify the limiting factors in the system and to set the particular goals of this Ph.D. Dissertation.

This chapter is divided into three sections that correspond with the above mentioned fields. Thus, Section 2.1 deals with the current limits in RFID long Range. Section 2.2 reviews different philosophies for voltage stabilization and control and Section 2.3 studies different low power sensor alternatives and its power requirements.

2.1 Passive UHF RFID tags

The DC chip power consumption (P_{cons}) and the efficiency in the RF into DC power conversion (η) are the factors that limit the operation range of the passive tag. For better understanding of this statement, the Friis Transmission Equation [46] is introduced. This equation gives the power transmitted from one antenna to another in free space:

$$\frac{P_r}{P_t} = G_r G_t (\frac{\lambda}{4\pi d})^2 \tag{2.1}$$

where P_t is the power fed into the transmitting antenna at its input terminals, P_r is the power available at the output terminal of the receiving antenna, G_r and G_t are the gain of the receiving and transmitting antenna respectively, λ is the wavelength and d is the distance between antennas, see Figure 2.1.

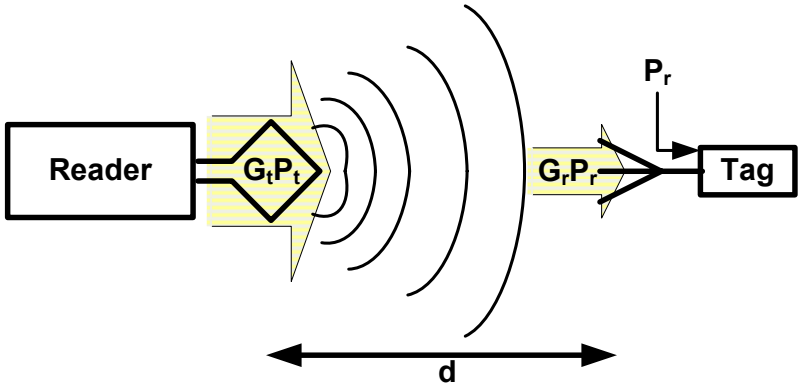

Figure 2.1: Illustration of the Friis Transmission Formula applied to UHF RFID systems.

Hence, it is indispensable for proper operation that:

$$P_r \geq \eta P_{cons} \tag{2.2}$$

Where P_{cons} is the upper bound of the power consumption on chip; and η is the RF into DC power conversion efficiency. In other case, there is not enough power available to supply the chip. Assuming that $P_t G_t$ is limited by governmental regulations in Europe to 2W ERP[1] [27], the frequency is 868 MHz, a typical value for G_r is 2.5 dBi and a polarization losses of 3dB; the function P_r vs d is as illustrates in Figure 2.2.

The figure shows the power that reaches the tag as a function of the distance, without consider obstacles and reflections. It is clear that tags consumption limits severely the operation range of the system. Thus, for an operation range of 6.5 meters, it will required a factor $\eta P_{cons} < 51\mu W$. Hence assuming $\eta = 20\%$, the upper bound of the power consumpion on chip with 6.5 meters between antennas is $P = 10\mu W$.

2.1.1 Limits of the passive RFID UHF systems

Next lines analyze the state of the art of passive RFID UHF tags in order to evaluate the limits of the actual technologies.

[1] Effective Radiated Power.

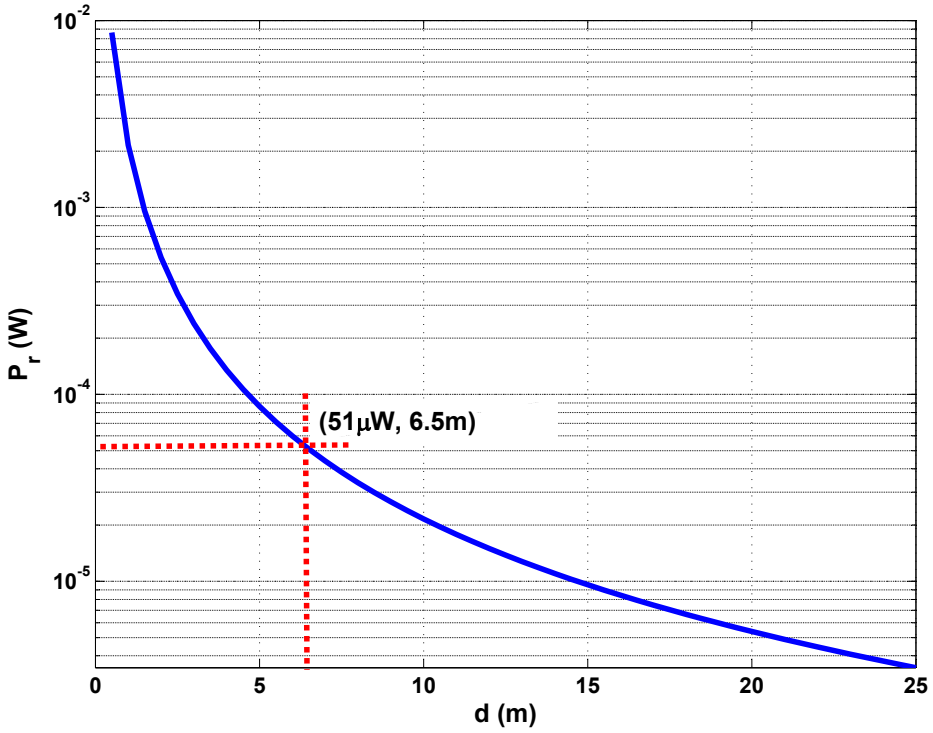

Figure 2.2: Available power at the output of the receiving antenna as a function of the distance.

In 2003, it was published the first passive UHF RFID chip [1]. This tag achieved a reading distance of 9.25 m working at 869 MHz and for a radiated power of 4 W of EIRP[2]. This paper is the first that applies the Dickson topology [47] for RF into DC conversion in passive UHF RFID tags. With this conversion method, it is possible to achieve high power conversion efficiencies. However, the author also remarks that the key to reach a wider range is not only the topology but also the use of a technology specially optimized for the application. This is schottky diodes with very low forward voltage. Another important point is the use of ultra–low power consumption circuits. The power consumption of the tag without taking into account the RF into DC power conversion is 2.25 μW in read mode and 3.57 μW in EEPROM write mode. The modulation for the communication Reader–Tag is PWM and a Backscatter modulation for the direction Tag–Reader.

Two years later in 2005, another passive UHF RFID tag was reported working in 2.4 GHz with a range of 12 meters [5], extrapolating theoretically this result to 868 MHz would result in a range of around 30 meters. The key to achieve this long range is the use of a silicon on isolator technology, namely, Silicon–on–Saphire (SOS). The most interesting features for passive RF systems are MOS transistors with very low threshold voltage, and very low parasitic capacitances at the frequencies of interest. In addition, the authors proposes a communication protocol optimized for ultra–low power consumption, which is not compatible with the EPC Global Class 1 Gen 2, already described and mostly accepted standard. Additionally, the Tag also includes modifications that reduce

[2]Equivalent Isotropically Radiated Power.

Table 2.1: Operation range of the actual UHF RFID tags at 900 MHz and EIRP=4W

Reference	Technology	Battery	Range (m)
[1]	CMOS 0.35μm + modified schottky	No need	9.25
[5]	SOS 0.5μm	No need	30
[42]	CMOS 0.35μm + Schottky	Need	24
[48]	CMOS/FeRAM 0.35μm	Need	3.51

performance and simplify the system in order to reduce as much as possible the consumption. This work can be considered as the theoretically maximal range reached by a passive RFID at the moment.

The first long range UHF RFID supplied with batteries was published in 2007 [42] . The philosophy to reach longer range in this work is reducing diode threshold voltage using batteries for diode biasing. The reported range is 3.51 meters at 2.45 GHz with 4 W EIRP and 24 meters at 868 MHz. The technology used is a 1μm CMOS that includes Schottky diodes and EEPROM.

The comparison of two last commented publications illustrates clearly the importance of the technology process to achieve a long range. In [42] with Schottky diodes specially suitable for RF detection and even batteries, the range reached is four times lower than in [5], where no batteries are required but a SOS technology with very low parasitic capacitances and transistor threshold voltage was used. At this point, it is declared that the maximal range of an passive UHF RFID system is set by the technology used to implement the tag. The reasons are mainly two: on the one side, the RF into DC power conversion is more efficient when parasitic capacitances and diode forward voltage are minimal. On the other side, the supply voltage can be dimensioned down when transistor threshold voltage decreases, in others words, the circuits require less power to operate when the technology improves.

In 2007 was presented another passive UHF RFID chip fabricated in a 0.35μm CMOS/FeRAM technology [48]. This work proved the benefits of using ferrorelectric capacitors with a high permittivity that increases the capacitance density per area and reduces the parasitic components. The novelty here introduced is the use of RAM instead EEPROM for data storing in the tag, which reduces the writing time. In addition, the ferroelectric capacitors are used for diode–connected transistor biasing in the RF into DC converter, reducing the forward voltage and improving the efficiency. However, the reached operation range is 3.5 meters at 868 MHz, a value well under the before cited papers, the reason is the elevated power consumption of the RAM. This work give an idea of the reachable range of a Tag with "high power" consumption (80μW) in a quasi–standard 0.35 μm process. Therefore, it is a god point of reference for this Ph.D. Dissertation, as the power consumption requirements of the sensor can be around 60–70 μW. Table 2.1 summarizes the features of the cited publications.

2.2 Energy recovery and stabilization system

First, the circuits involved in the RF into DC conversion are here introduced. Next the voltage control and stabilization circutry are presented.

2.2.1 DC voltage supply generation

The first step in the supply in wireless powering is the RF into DC power conversion. The block that carries out this function is the RF into DC converter more known as Rectifier or Voltage Multiplier. This circuit must be able to generate from the incoming RF signal a DC voltage. The power conversion efficiency of the rectifier is critical to define the complete power consumption of the transponder.

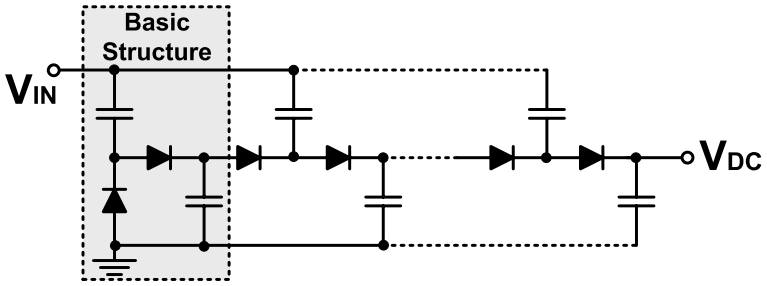

Figure 2.3: Rectifier for RF into DC power conversion, first proposed by [1].

In the particular case of long range UHF RFID tags, the mostly used topology to implement rectifiers is called Dickson Multiplier [1]. Figure 2.3 shows the Dickson topology, the idea is to charge the capacitors with each cycle of the input signal. The diodes avoid the discharge of the capacitors. In this way, the charge on the capacitors can be maintained from one cycle to other. By cascading the basic structure, the DC voltage on the output can be multiplied. Other topologies based on the idea of Dickson Multiplier can be founded in the bibliography [5, 49, 50, 51], however they do not present specially better performance than the former.

The conversion efficiency of the state–of–the–art rectifiers is around 10–20% [1]. This is, the 80% of the RF energy that reaches the tag is lost in the energy conversion. Moreover, the efficiency decays with the frequency due to the parasitic effects of the diodes and capacitors. A more detailed revision of the Rectifier state of the art is given in Chapter 5.

As already said, the Dickson Multiplier is the mostly used today rectifier. However, there are not mathematical models to characterize the performance of this circuit as a function of the power requirements of the system. Such a model would make possible the automation of the rectifier design if the power requirements of the system to supply are known.

2.2.2 Voltage supply condition

Some circuits are involved in the voltage supply condition. This section studies the state–of–the–art of this circuits. They were reported for inductive coupled wireless sensors and for EM coupled RFID tags.

Voltage supply condition in inductive coupled sensors

Several short range passive wireless sensors have been already probed [18], [52]. These systems include a sensor and the wireless power transmission is realized throw magnetic coupling. However, the operation range is shorted and the power levels that reaches the tag are higher than in the case of Electromagnetic coupled systems. Therefore, the power requirements are more relaxed in these systems. Nevertheless, it is important to study the circuitry used by these systems to condition and stabilize the supply voltage for the sensor and other blocks.

Authors of wireless passive sensors [18] and [52] agrees in the necessity of a voltage regulator in the sensor energy recovery system. The regulator stabilizes the DC voltage generated by the rectifier in order to condition properly the supply voltage for the system. The technology and the power requirements of the wireless sensor establish the supply voltage and current of the system. Once these values have been specified, the voltage regulator must be configured to deliver the required current and voltage under the complete system operation cycle.

The circuit used to regulate the supply voltage is known as series–types regulator. It consists in a PNP bipolar transistor (pass device) driven by an error amplifier that compares the output voltage with a reference. The error amplifier recognizes variations in the supply voltage and drives the pass devices to deliver more or less current. Therefore, the regulation effect is achieved.

However the power consumption reported is around 50 μA. This value is acceptable in inductive coupled systems, where reader and tag are very close to each other and the coupled energy is elevated. In long range wireless sensors, and regarding to the reported values, a dramatic reduction of the power consumption is requiered.

Two additional blocks are also present in the energy recovery system of a wireless sensor [18]. The first one is the start–up circuit to prevent malfunction of the power converter circuit at the onset of the monitoring. The second one is the limiter, a circuit that protects the circuitry against breakdown voltage. These two circuits must be designed attending at the requirements of the technology process. Obviously, the current consumption of both elements should be minimized.

Voltage supply condition in EM coupled RFID tags

Returning the case of long range RFID tags, several regulators, start up and limiter circuits have been reported. These circuits were optimized for ultra–low power consumption without to consider the additional requirements of having a sensor.

Regarding to the voltage regulators, two circuits have been reported by [53] and [54]. Both circuits present a low current consumption, under 200 nA at operating voltages under 1.5 V. The problem is that the maximal output current that they are able to deliver do not exceeds the 5μA, which is enough to supply a passive RFID but not sufficient for a sensor. Consequently, further investigations should be carried out in ultra–low power consumption regulators in order to increase the maximal delivered current maintaining a low current consumption.

At the output of the rectifier is commonly used a big capacitor that serves as a current storage to supply the system. The dimensions of the supply capacitor vary depending on the communications protocol, and the power requirements of the systems. The energy recovery system will be able to supply the system only when the supply capacitor is charged enough.

In order to check and control the charge of the supply capacitor two different blocks are used in the bibliography, namely, the voltage sensor and the high voltage protection.

The sensor checks the charge of the supply capacitor and turn on the system when there is sufficient charge. Two different alternatives to implement a voltage sensor were introduced in [5] and [4], both circuits presents very low power consumption but should be adapted to the supply voltage required by the sensor.

Finally, the protection limits the maximal voltage on the capacitor to avoid break down voltages. The typical implementation is a clamp limiter as reported in [6].

Figure 2.4 shows the block diagram of the energy recovery system necessary to wirelessly supply a sensor though electromagnetic coupling. This Ph.D. Dissertation propose a implementation of this architecture, specifically adapted to the requirements of a sensor and considering the restrictions involved in the long range wireless power transmission.

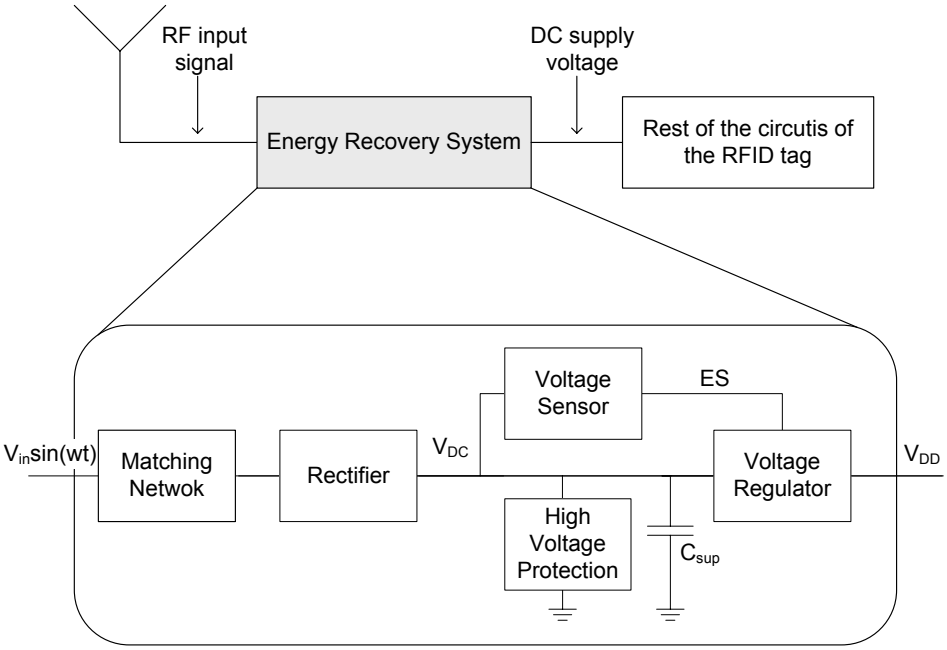

Figure 2.4: Architecture of the energy recovery system for EM coupled systems.

2.3 Low power sensors

There are a great number of sensors available in a standard integrated circuit process that may be sufficient for plenty of applications. Temperature, magnetic field, and capacitive fingerprint sensors have all been demonstrated in standard CMOS, as well as, megapixel cameras with on–chip image processing [55, 7, 56, 57, 58]. Integrated sensing of colored light can also be done in CMOS using metal grating patterns or variable depth PN junctions as a color filter [56, 59]. Imaging arrays are increasingly finding applications in non camera applications, such as motion–flow sensing in computer mice. Imaging of legacy dials, knobs, and lights in industrial environments combined with local signal processing at the sensor to transmit only the dial position is a potentially low–power, low data rate application.

There are a host of miniaturized sensors possible with MEMS technology: linear and angular rate acceleration, pressure, chemical, fluid flow, audio microphones, among others. While all of these sensors are also available off–the–shelf, custom designed MEMS sensors have the distinct advantages of low cost and size as well as the potential for integration with circuits.

Next subsections study different low power sensor structures and check their integration feasibility within a passive UHF RFID. The study will be limited to CMOS process compatible sensors emphasizing for Ultra–Low–power consumption.

2.3.1 Temperature sensors

Figure 2.5 depicts the basic block diagram of the most power–saving temperature sensor architectures reported in the bibliography [60].

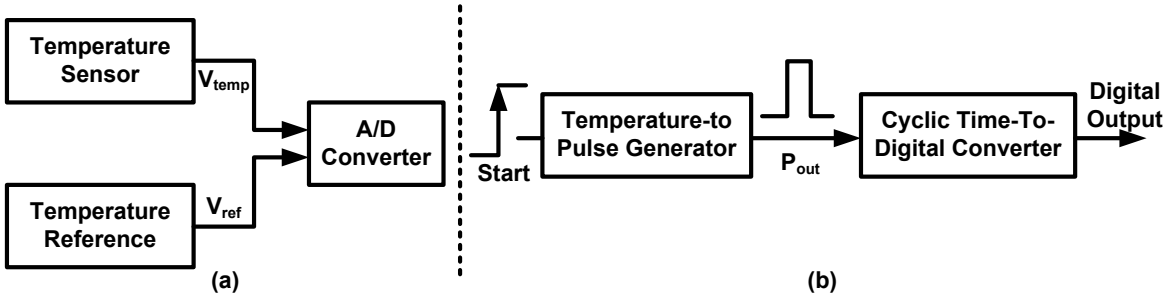

Figure 2.5: Power–saving temperature sensor architectures (a) conventional approach, and (b) recent approach.

Figure 2.5.a shows the conventional temperature sensor that consists of following blocks:

- Reference circuit that generates a temperature independent voltage or current (I_{ref} or V_{ref}). The most used voltage reference is called bandgap reference [61].
- Temperature sensing module. This circuit generates a current or a voltage (I_{temp} or V_{temp}) well defined with temperature. Depending on the behavior with temperature, it can be a PTAT (Proportional To Absolute Temperature) circuit or a CTAT (Complementary To Absolute Temperature – reduces with increasing temperature) circuit.
- Analog to digital converter that generates a bit stream at the output proportional to $\frac{I_{temp}}{I_{ref}}$ or $\frac{V_{temp}}{V_{ref}}$.

Figure 2.5.b illustrates an alternative architecture for low–power consumption temperature sensor [62]. A time–to–digital converter (TDC) instead of a voltage of current ADC is adapted to be the conversion core of the digital output. Since a duration of time rather than a magnitude of voltage or current is required at the TDC input, the need for BJT–based temperature sensing techniques in conventional circuits is eliminated successfully, reducing the power consumption. A temperature–to–pulse generator is used to generate a pulse with a width proportional to the measured temperature. Subsequently,

Table 2.2: Comparison of low power temperature sensors

Sensor	Resolution (° C)	Error (° C)	Power Cons. (μW)	Area (mm^2)	Conversion Rate (samples/s)	Temp. Range (° C)	CMOS Tech. μm
[55]	0.625	± 1	7	1.5	50	-40–120	2
[63]	0.25	± 1	1	3.32	10	-55–125	0.6
[62]	0.16	-0.7–+9	10	0.175	10k	0–100	0.35

the output pulse is fed to the input of a cyclic TDC to generate the corresponding digital output.

Table 2.2 compares the tree low power temperature sensors. All the sensors can be fabricated with CMOS technology. However [55] and [63] require vertical bipolar transistors normally available in standard CMOS technologies. Regarding to power consumption there is a correspondence with the conversion rate, the lower is the sample rate the lower is the average power consumption. The average power consumption for reduced conversion rates varies from 10 to 1 μW. Other parameters of the temperature sensor like resolution, error and temperature range are also present in the table for giving an idea of maximal performance that can be reached with such a low power consumption.

2.3.2 Magnetic field sensors

A Hall effect sensor is a transducer that varies its output voltage in response to changes in magnetic field. Hall sensors are used for proximity switching, positioning, speed detection, and current sensing applications.

In its simplest form, the sensor operates as an analogue transducer, directly returning a voltage. With a known magnetic field, its distance from the Hall plate can be determined. Using groups of sensors, the relative position of the magnet is deduced.

Electricity carried through a conductor will produce a magnetic field that varies with current, and a Hall sensor is used to measure the current without interrupting the circuit. Typically, the sensor is integrated with a wound core or permanent magnet that surrounds the conductor to be measured.

Hall sensors are commonly used to time the speed of wheels and shafts, such as for internal combustion engine ignition timing or tachometers. They are used in Brushless DC electric motors to detect the position of the permanent magnet for speed regulation.

Hall magnetic sensors present an almost perfect compatibility with microelectronics technology[64]. The optimal material characteristics, device structures and dimensions, and fabrication processes are similar to those readily available in semiconductor industry. Therefore, the development in Hall magnetic sensors does not require much of specific investments in fabrication processes.

Table 2.3 summarizes the performance characteristics of a recent published integrated hall sensor [7]. The most interesting point is the power consumption that amounts to 21 mW. Such a supply power can not be achieved with the state–of–the–art long range passive UHF RFID tags. Therefore Hall sensors are not suitable for passive UHF RFID sensors, an active tag or an inductive coupling passive transponder will be required

Table 2.3: Performance characteristics of an integrated Hall sensor [7]

Specification	Value
Offset (μT)	3.65
Thermal offset drift (nT/K)	8
Short–term offset stability (nT)	10
Long–term offset stability (nT)	250
Noise($\mu T/\sqrt{Hz}$)	0.3
V_{dd} (V)	5
I_{dd} (mA)	4.2
Size (mm^2)	2.9
B Full Scale (mT)	$\pm$10.8

for implementing wireless Hall sensors. The typical parameters used for characterize integrated Hall sensors as offset, stability and noise, are not discussed in this document. A more detailed study of state–of–the–art in integrated Hall sensors can be carried out analyzing references:[65, 66]

2.3.3 Fingerprint sensors

Fingerprint recognition or fingerprint authentication refers to the automated method of verifying a match between two human fingerprints. Fingerprints are one of many forms of biometrics used to identify an individual and verify their identity.

A fingerprint sensor is an electronic device used to capture a digital image of the fingerprint pattern. The captured image is called a live scan. This live scan is digitally processed to create a biometric template (a collection of extracted features) which is stored and used for matching. There are tree main alternatives for implementing this kind of sensors: optical, ultrasonic or capacitive. The last one can utilize the principles associated with capacitance in order to form fingerprint images.

Capacitive fingerprint sensors using the CMOS process have been developed for low-power, low-cost, and small-size fingerprint identification systems [67, 68]. These chips have a sensor array that captures a fingerprint image when a finger is placed in direct contact with the surface. The array is composed of sensor cells. Each sensor cell consists of a sensor plate and a sensing circuit covered with passivation film. The principle of fingerprint sensing is based on the detection of the capacitance formed between a finger and the sensor plate. The capacitance varies with the pattern of skin ridges and valleys because they have different distances from the plates. The sensing circuit converts the capacitance to a voltage signal and outputs an analog signal that reflects the fingerprint pattern.

Table 2.4 present a list of the most recent works proposed in the state–of–the–art of integrated fingerprint sensors. Very low power consumptions have been achieved in some designs, until 250 μW in [67]. However this values are still too high to reach a long operation range in passive UHF RFID, consequently this system is suitable for an

Table 2.4: State–of–the–art of integrated fingerprint sensors

Reference	Cell number	Resolution (dpi)	Power consumption	Technology
[68]	160 x 192	423	35mW@3.3 V*	0.35 CMOS
[67]	300 x 300	500	250μW@1.8 V	0.5 CMOS
[69]	320 x 250	423	1.2mW@5V	Poly-Si TFT
[70]	200 x 200	390	550μW@1.8 V	0.7 CMOS

* This chip include a 32–bits RISC microcontroller for performing an identification algorithm.

active solution or for reduced operation ranges.

2.3.4 Image sensors

An image sensor is a device that converts an optical image to an electric signal. It is used mostly in digital cameras and other imaging devices. It is a set of charge–coupled devices (out of the scope of this study) or CMOS sensors such as active–pixel sensors.

The significant advantages of CMOS technology such as high integration density, high functionality, and low power have contributed to the emergence of CMOS imagers in recent years. The CMOS active pixel sensor allows the use of customized signal–processing circuits in order to realize smart imagers with relatively simple pixel architecture and dedicated on–chip signal–processing circuitry [71]. Unlike CCD image sensors, CMOS imagers offer the possibility of co–integration with analog readout and digital control electronics on the same chip even on pixel level [72].

Table 2.5 compares the state–of–the–art in CMOS image sensors in terms of number of pixel and power consumption in order to have an idea of the consumption of a single pixel. In the table is also present the optical dynamic range, defined as the capability of an image sensor to measure a scene having very dark and bright areas at same time. The dynamic range is one of the major parameters to classify the quality of an imager [73]. The process technology is also reported. From Table 2.5, it can conclude that the highest dynamic range is achieved by the lowest pixel number and by the smallest minimal gate length. In terms of power consumption, it is clear that the lowest values are achieved with 0.18 μm CMOS. However, the result obtained by [72] are in the same order of magnitude in a 0.5 μm CMOS, as the expense of dynamic range. The conclusion is that reducing dynamic range the power consumption can be reduced under 250 nW per pixel. Thus, an image sensor could be integrated in a long range UHF RFID assuming a reduced number of pixel and power consumption up to 20 μW. If the dynamic range and number of pixels increase, an additional power source will be required.

2.3.5 MEMS

Micro-Electro-Mechanical Systems (MEMS) can be defined as the integration of mechanical elements, sensors, actuators, and electronics on a common silicon substrate through microfabrication technology. While the electronics are fabricated using integrated circuit process sequences (e.g., CMOS, Bipolar, or BICMOS processes), the micromechanical components are fabricated using compatible "micromachining" processes that selectively

Table 2.5: Comparison of recent published CMOS image sensors

Reference	number of pixels	Dynamic range	Power consumption	Technology CMOS
[71]	256 x 256	96 dB	52mW⇒ 793nW x pixel	0.8μm
[72]	1025 x 1024	92 dB	300mW⇒ 286nW x pixel	0.5μm
[74]	28 x 28	130 dB	196μW⇒ 250nW x pixel	0.18μm
[73]	140 x 140	120 dB	30mW⇒ 1530nW x pixel	0.35μm

etch away parts of the silicon wafer or add new structural layers to form the mechanical and electromechanical devices.

The monolithic integration of CMOS and MEMS is not straightforward, it requires some additional steps in the traditional CMOS process. Figure 2.6 illustrates the modifications in the CMOS process for MEMS integration [75, 76]. The pre–processing step allows higher temperature budget for the MEMS and the inclusion of special substrate materials. In a second step, CMOS and MEMS structures are built and tied together. During the post-processing, additional MEMS processes independent of CMOS can be carried out, and MEMS may be placed directly above CMOS circuits.

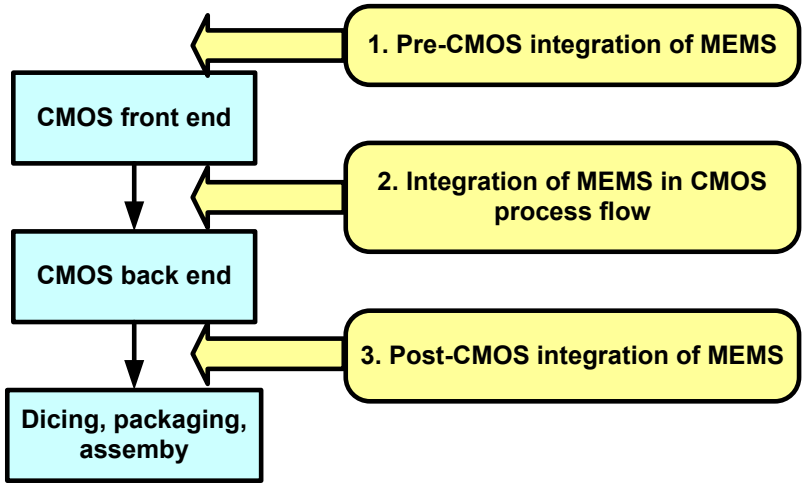

Figure 2.6: Modifications in the CMOS process required for MEMS integration.

Next subsections study of the characteristics of the most used MEMS sensors, namely, accelerometers, gyroscopes and pressure sensors.

Accelerometers

An accelerometer is an electromechanical device that measure acceleration forces. These forces may be static, like the constant force of gravity pulling at your feet, or they could

Table 2.6: Comparison of the characteristics of the most recent reported accelerometers

Reference	Range	Sensitivity	Power consumption
[78]	$+/-4$g	200mV/g	400μW
[79]	$+/-3$g	300mV/g	640μW
[80]	$+/-2.3$g	350mV/g	750μW

Table 2.7: Comparison of recent reported gyroscopes

Reference	Sensitivity	Noise floor	Power consumption
[81]	2mV/°/s	$0.02°/s/\sqrt{Hz}$	15mW
[83]	6mV/°/s	$0.05°/s/\sqrt{Hz}$	17.5mW

be dynamic – caused by moving or vibrating the accelerometer.

The basic MEMS accelerometer consists of a cantilever beam with a proof mass (also known as seismic mass) and some type of deflection sensing circuitry. Under the influence of gravity or acceleration the proof mass deflects from its neutral position. The deflection is measured in an analog or digital manner, normally based on capacitive measurements [77].

Table 2.6 compares the characteristics of the most recent reported accelerometers. The two accelerometers present performances in the same order of magnitude. The power consumption amounts to 400μW, this value is still outside the maximal power that can be delivered by a passive UHF RFID considering a distances over 1 meter. Such sensors will require batteries or inductive link for power supply.

Gyroscopes

A gyroscope is a device consisting of a spinning mass, typically a disk or wheel, mounted on a base so that its axis can turn freely in one or more directions and thereby maintain its orientation regardless of any movement of the base.

Vibrating structure gyroscopes are a type of gyroscope that can be fabricated using MEMS technology. Its physical principle is very simple: a vibrating object tends to keep vibrating in the same plane as its support is rotated. MEMS gyroscopes can be implemented as a tuning fork resonator [81]. Table 2.7 present a comparison of two gyroscopes, both report similar results un terms of sensitivity and noise floor. The power consumption is around 15mW, in this value is included the MEMS driver and sensing circuits. Such power consumption requires a battery to work as demonstrated in [82].

Pressure sensors

A pressure sensor measures the pressure, typically of gases or liquids. Pressure is an expression of the force required to stop a gas or fluid from expanding, and is usually stated in terms of force per unit area. A pressure sensor generates a signal related to the pressure

Table 2.8: Comparison of three low power pressure sensors

Reference	Operating range	Resolution	Consumption
[17]	0.5-1.5 bar	3.9mbar	70μA@3V
[84]	1–1.34 bar or 0-0.33	1.3mbar	200μA@5V
[85]	1–4 bar	–	21μA@3V

imposed. Typically, such a signal is electrical, but it might also include additional means, such as optic signals, visual signals and/or auditory signals. There are plenty of fields were pressure sensors are used, basically can divided into tree major categories: Pressure sensing (medicine, automobile, aircraft, microphones), altitude sensing (aircraft, rockets, satellites, weather balloons) and flow sensing.

MEMS pressure sensors are ultra thin silicon diaphragms obtained by performing bulk etching in a CMOS circuit. By placing piezoresistive elements in proper directions along the diaphragm edge, it is possible to convert applied pressure on the diaphragm into an electrical signal.

The main features of three pressure sensors with low power consumption are presented in Table 2.8. The operation range, resolution and power consumption vary dramatically with the applications, namely, intraocular inductively powered pressure sensor [17], pressure sensor for an intravascular catheter [84] and automotive industry [85]. As conclusion, there are pressure sensor with reduced power consumption 21μA @ 3V that can be supplied by a passive UHF RFID sensor. Additionally, passive intraocular pressure sensors have been already proved [17].

2.3.6 Analog to digital converters

An analog to digital converter (ADC) is an electronic device that converts an input analog voltage (or current) to a digital number. Incorporating an additional ADC on the RFID chip facilitate the measurement of physical variables. The idea is to convert the acquired analog data with the above described sensors into digital, to be sent by the RF interface. A detailed description of the different ADC architectures is out of the scope of this Ph.D. Dissertation. The point here, as in the case of the sensor structures, is to find the supply requirements of the most power saving ADC architectures reported in the bibliography, to analyze the integration feasibility in passive UHF RFID tags.

Table 2.9 presents a review of several low power consumption ADCs. The lowest power consumption was reported by [86] for a 100kS/s sampling rate and a 8 bits resolution in a 0.25μm CMOS process. Higher performance will require more power as shows the reference [87]. In general, a power consumption under some tens of μW can be achievable for moderate–resolution and moderate–speed.

2.3.7 Summary

Table 2.10 enumerates the different sensors reviewed in this section. The table also indicates the power consumption of each sensor and the integration feasibility of the sensors in full passive long range UHF RFID tags. Assuming that long range is an

Table 2.9: Comparison of recent reported low–power ADC

Reference	Sampling Rate	Power consumption	Resolution	Differential input level	Technology (CMOS)
[86]	100kS/s	3.1μW @1V	8	1V_{pp}	0.25μm
[88]	5kS/s	13μW@1.2V	8	0.9V_{pp}	0.13μm
[87]	1MS/s	20mW@3V	16	5V_{pp}	0.35μm
[89]	50kS/s	340μW@1V	8	0.85V_{pp}	1.2μm
[90]	1.538MS/s	40μW@0.9V	–	0.5V_{pp}	0.5μm

Table 2.10: Summary of the studied low power sensors and ADC

sensor	MEMS	Power Consumption	Full passive electromagnetic
Temperature	No	10μW	Yes
Hall sensor	No	4.2mW	No
Image Sensor	No	196μW	No
Fingerprints	No	250μW	No
Accelerometer	Yes	400μW	No
Gyroscopes	Yes	15mW	No
Pressure	Yes	42μW	Yes
ADC	No	3.1μW	Yes

operation distance longer than 3 meters power under 60μW, hence only temperature and pressure sensors are suitable to implement long range passive sensors, the rest require supply powers over 190μW. This amount of power is not possible to be recovered by a passive UHF RFID tag with the actual governmental regulations in terms of radiated power and at a distance over 3 meters. The alternative for these sensors would be batteries for power supply or operation range reduction.

Ultra–Low power consumption ADCs could also be integrated in passive long range UHF RFID, if its power consumption is around a couple of μWatts as the one reported in [86].

2.4 Conclusions

The main conclusions extracted from the state-of-the-art analysis are summarized in the next lines.

The maximal theoretical range of EM coupled RFID systems is 30 meters. However this range was probed in a SOI technology and is not compliant with the EPC standards.

Considering the attenuation of an EM wave due to free space propagation, the maximal operating range of an EM coupled RFID can be calculated. Assuming 20% of RF into DC power conversion efficiency and 40μW of chip DC power consumption, the

maximal operating range is around 4 meters.

The most used architecture for RF into DC conversion is the Modified Dickson topology. It has not been reported a mathematical model to automate the design of this circuit according to the power requirements of the system.

For supply voltage conditioning and stabilization are required a voltage sensor, high voltage protection and voltage regulator. These blocks have been reported for magnetic coupling sensors and for EM coupled RFID tags. However, they were not optimized for EM coupled sensors.

The low power sensors more suitable to be integrated inside an EM coupled passive tag due to its low power consumption are the temperature and pressure sensors. Ultra low power consumption ADCs could be also integrated.

Chapter 3

Context and Goals of this Ph.D. Dissertation

Contents

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3.2 Tag architecture description 34
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3.4 Memory Organization 36

Abstract: This work is part of an international research project, in which several institutions and researchers are involved. This chapter gives an overview of the research project and locates this Ph.D. Thesis inside it.

The second point of this chapter is to present the goals of this Ph.D. dissertation and describe the structure of the memory.

3.1 Ph.D. Dissertation context – WISEN project

This Dissertation is part of an international research project which goal is the design of passive wireless sensors using Long range passive UHF RFID technologies as radiofrequency interface.

The research carried out during the development of this Ph.D. Thesis is part of an international research project called WISEN (WIreless SENsors) [91]. Several research centers are involved in the WISEN project, namely, Instituto Universitario de Microelectrnica Applicada (IUMA), Centro de Estudios e Investigaciones Tcnicas de Guipzcoa (CEIT) and Fraunhofer Institut fuer Integrierte Schaltungen (IIS). The primary goal of this project is research in the field of the design and implementation of long range passive wireless sensors. This main objective is divided into more detailed targets:

- Design and implementation of passive UHF RFID transponders optimized for working as RF interface for wireless sensors.
- Design and implementation of an interrogator device for passive UHF RFID tags able to understand the data from the sensor.
- Design and implementation of ultra–low power consumption sensors with the possibility to be integrated in a passive UHF RFID tag.

- Study and Analysis of the possible applications of the technology

This Ph.D. Thesis is within the framework of the first listed target, this is, design and implementation of passive UHF RFID transponders optimized for working as RF interface for wireless sensors. Specifically, this work faces the difficulties involved in incorporating a sensor in a passive tag in terms of power conversion and transponder voltage supply generation and proposes solutions for the design and implementation of the energy recovery system for long range passive wireless sensors.

3.2 Tag architecture description

Wireless power transmission is quite inefficient, this is, the major part of the power radiated by the reader is lost and only a reduced portion reaches the tag. This fact implies that the power consumption of the tag should be as low as possible in order to reaches a longer range. The inclusion of a sensor in the system shrinks the specification in terms of power consumption. A way to reduce the power consumption is to keep the system as simple as possible. Figure 3.1 shows the basic architecture of the RFID tag, used in WISEN project to implement a passive wireless sensor.

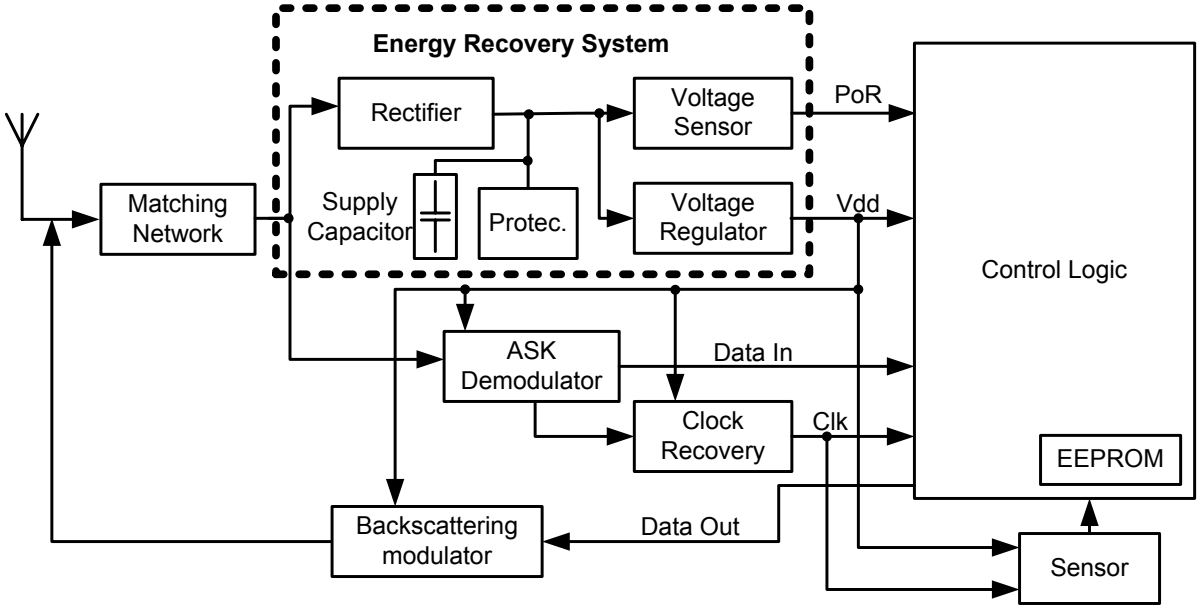

Figure 3.1: Basic architecture of the RFID sensor applied in WISEN.

Next, the different blocks of the system are described:

- Antenna and matching network. The chip is connected directly to the antenna. In order to suppress undesirable power reflections, impedance matching between chip and antenna is required. External components as capacitors or coils should be avoided to minimize the price of the tag. There are two possible solutions, either integration of the components in the chip or design the antenna with a specific impedance by mean of transmission lines.

- Rectifier. The rectifier also known as voltage multiplier is the circuit in charge of the RF into DC power conversion. This block rectifies the AC voltage captured

by the antenna in a supply DC voltage. The power conversion efficiency is a key aspect in the system, since it will determine with the chip consumption the maximal operation range of the tag.

- Supply capacitor. At the output of the Rectifier, a high capacitance capacitor is placed. It serves as an extra charge store to maintain the supply voltage. This extra charge is required for the current peaks of the digital circuitry and for the shorts absences of RF power due to the communication modulation.

- Voltage Sensor. The voltage sensor checks the charge of the supply capacitor at the very beginning of the communication. When the voltage on the supply capacitor reaches a level that guaranties tag proper supply, the voltage sensor generates the signal PoR that activates the wireless sensor.

- Voltage Regulator. DC voltage generated by the Rectifier present undesirable ripples and variations that must be eliminated from the supply voltage. The regulator stabilizes the supply voltage from the rectifier and generates the voltage V_{dd} to supply the complete system.

- High–Voltage Protection. The voltage generated by the Rectifier is very dependent on the distance Reader–Tag, for short ranges the voltage generated by the rectifier can exceed the breakdown voltage of the supply capacitor. In order to avoid high voltages on the supply capacitor, the protection circuit is included in the system.

- ASK Demodulator. This circuit demodulates the signal from the Reader. The communication standard specifies an ASK modulation for the communication Reader–Tag of two states optimized for ultra–low power consumption also known as On–Off Keying (OOK).

- Backscattering modulator. The EPC Global Class 1 Gen 2 specifies the backscattering modulation in the communication Tag–Reader. This modulation consist in mismatch the antenna and the chip in order to reflect or not the incoming RF signal from the reader. Then, the reader is able to detect if there is reflected wave or not. On the tag side, the modulator consist in a capacitor that can be switched on and off with the antenna terminals.

- Logic Control. The intelligence of the system is located in this block. The principal function of the logic control is the implementation of the communication protocol, encryption functions, memory accesses and sensor control.

- Sensor. In principle the system is designed for a generic sensor. The requirements of the sensor from the point of view of the RFID tag are given in terms of power consumption. The rest of specifications are set by the application.

The research involved in this Ph.D. Dissertation deals with the blocks involved in the Energy Recovery System, namely, rectifier, voltage sensor, high voltage protection, and voltage regulator. The location of the Energy Recovery system is high lighted in Figure 3.1.

3.3 Goals of the PhD. Thesis

This section summarizes the goals proposed in this Ph.D. thesis.

- Energy Recovery and Stabilization System design methodology of EM coupled passive sensors.
- Design methodology and mathematical model for the Rectifier attending to the power requirements of EM coupled passive sensors.
- Ultra low power design solutions for the Voltage Sensor and high voltage protection applied to EM coupled passive sensors.
- Ultra low power design solutions and design methodology for voltage regulators optimized for EM coupled passive sensors.

3.4 Memory Organization

Each of he above presented goals will serve as a topic of a chapter of this Ph.D. Memory. The chapter organization is as follows:

Chapter 4: Power supply System Design. This chapter begins with a description of the Energy Recovery system. The second point is the description of the restrictions involved in the energy recovery in terms of input power, input voltage and up– and down–link communications. Next, the selection of a proper technology process is presented. Last section deduces a basic specification of each particular block of the Energy Recovery system. This basic specification is the starting point for the block design.

Chapter 5: Rectifer. The Rectifier is the topic of this chapter. First, the state–of–the–art is analyzed and a proper circuit topology is selected. Next, the rectifier design is described and a design criterion is proposed. Subsequent section introduces a novel mathematical model to characterize the rectifier behavior in terms of input impedance and input voltage as a function of the process, and power requirements. Finally, simulated and measured results are discussed.

Chapter 6: Voltage Sensor and High Voltage Protection. Chapter 6 presents contributions to the design of Voltage Sensor and voltage protection. Firstly, the function of voltage sensor is described and the state–of–the–art solutions are presented. Next, two novel topologies are presented and compared with the previously reported ones. Simulation results are then probed by on–chip measurements. The second point of this chapter is the High Voltage Protection. After its operation description, it is presented a modification in the state–of–the–art circuit. The advantages introduced by the modifications are probed by measurement results.

Chapter 7: Voltage Regulator. The last block of the Energy Recovery System is the Voltage Regulator which is the topic of this chapter. After a short introduction, different implementation alternatives for the Voltage Regulator are presented and the Low Drop Out topology is selected and described. Next, a study of the state of the art reference

circuits is presented in order to find out the most suitable one for the Voltage Regulator. After that, Regulator design trade–offs are discussed and a design methodology oriented to long range passive wireless sensors is proposed. Final section presents simulations and measurements to probe the proposed solutions.

Chapter 8: Conclusions and Future Lines. To conclude this memory the main conclusions are summarized and the future lines are proposed.

Chapter 4

Energy Recovery System Design

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Abstract: The goals of this Chapter can be summed up in three points: first, description of the different blocks of the Energy Recovery System (ERS). Second, identification of the main design limitations; and third, formulation of a specification set for each particular block of the system. This specification is the starting point for a detailed design in subsequent chapters.

Section 4.1 presents Energy Recovery System. Next, the RF input signal from the antenna is analyzed attending to the input power, amplitude and input impedance. Section 4.3 study the system restrictions introduced by the communication protocols and modulations. After that, some general design consideration are reported, namely, technology process and design parameters. Finally, each particular block of the ERS is specified.

4.1 Energy recovery system description

The function of the Energy Recovery System (ERS) in passive UHF RFID tags is to generate a regulated DC supply voltage from the RF input power. Figure 4.1 depicts the block diagram of ERS.

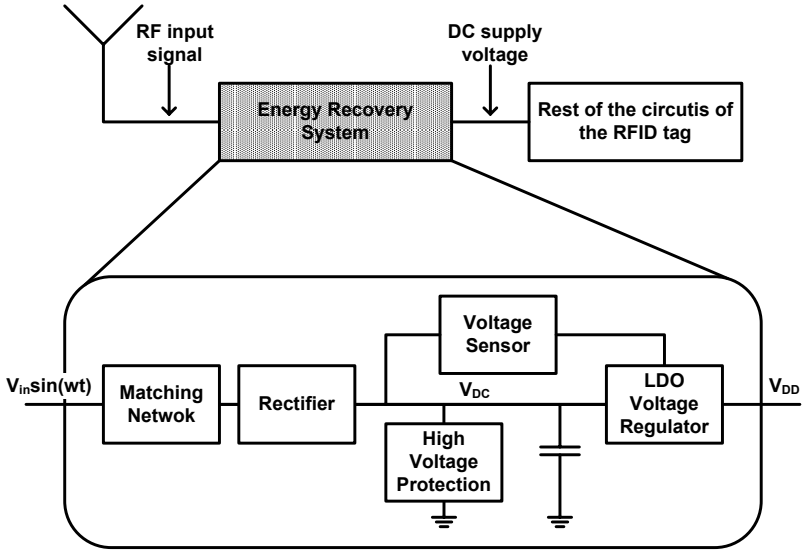

Figure 4.1: Energy recovery system block diagram.

The reader transmits the RF signal at the resonant frequency of the tag antenna. The input power in the tag antenna is then transferred to the Regulator using a matching network for maximum power transfer. The rectifier converts RF into DC power. The power conversion efficiency of the rectifier (η) is critical for the performance of the complete tag. Efficiency η is defined as the ratio between DC supply power at the output of the rectifier and the avaliable RF input power. Maximizing η reduces the minimum RF power required by the system to work (P_{th}).

On the one hand, the DC output voltage ($V_{DCunregulated}$, see Figure 4.1) of the Rectifier is very dependent on the load, RF input signal and communication modulation. As a result, the DC output of the Rectifier presents undesirable perturbations. On the other side, the sensor and the digital section requires a very stable supply voltage, consequently, the unregulated DC needs some kind of stabilization to avoid noise in the supply voltage. Therefore a series Low–Drop–Out (LDO) voltage regulator must be included in the ERS to generate a supply voltage independent of the DC output voltage of the Rectifier, load, temperature and additional perturbations.

Three additional blocks are required to complete the ERS: the supply capacitor, the wake up circuit and the protection against high voltages.

A big supply capacitor is placed at the output of the rectifier to avoid drops on the unregulated DC voltage by short absences of RF power due to the comunications protocol and modulation or by high current peaks in the digital section.

The wake up circuit turns on the DC output when the supply capacitor is enough charged to supply properly the complete tag.

Finally, to avoid too high unregulated DC voltages a shunt protection is used. The protection draws current to ground when a threshold voltage is reached.

4.2 Interface antenna – energy recovery system

The objective of this section is to analyze the ERS in order to specify the requirements of each particular block.

4.2.1 Input power

The Friis Transmission Formula [46] gives the power transmitted from one antenna to another in free space:

$$\frac{P_r}{P_t} = G_r G_t (\frac{\lambda}{4\pi d})^2 \tag{4.1}$$

Where P_t is the power fed into the transmitting antenna at its input terminals, P_r is the power available at the output terminal of the receiving antenna, G_r and G_t are the gain of the receiving and transmitting antenna respectively, λ is the wavelength and d is the distance between antennas.

Two limitations of the Friis' Formula must be taken into account. First, the formula should not be used when d is small,

$$d \geq \frac{2a^2}{\lambda} \tag{4.2}$$

where a is the largest linear dimension of either of the antennas. For a frequency of 868MHz and $a = 0.346m$, the distance between antennas should be higher than 0.7 m.

Second, the Friis' Transmission Formula is valid only for free space propagation. This means that multipath, atmosphere losses, interferences and other propagation phenomena are not considered. Additional terms should be introduced in the formula to take into account all this effects.

However, the Equation 4.1 gives a ratio between the available power on the tag antenna and the distance between reader and tag, which is very useful to calculate the read range-the maximum distance at which RFID reader can detect the backscattered signal from the tag.

At this point, two definitions are introduced: impedance matching and reflexion coeficient. The antenna and chip impedances are "matched" when all the power available on the source (antenna) is transferred to the load (RFID chip). In any other case, the source and the load are mismatched and part of the power is reflected. To study this situation, consider the general case of a one port network, shown in Figure 4.2, which represents a generator–load circuit with complex source and load impedance.

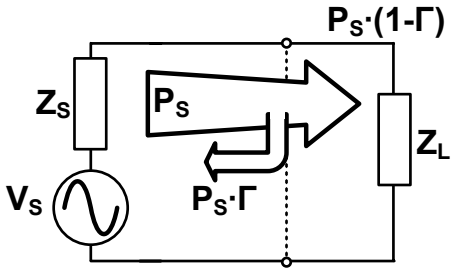

Figure 4.2: Generator–load circuit with two complex impedances.

Kurokawa [92] described a concept of power waves travelling between the generator and load. He introduced the following definitions for the power wave reflection coefficient s:

$$s = \frac{Z_L - Z_S^*}{Z_L + Z_S} \tag{4.3}$$

and the power reflection coefficient Γ

$$\Gamma = |s|^2 = |\frac{Z_L - Z_S^*}{Z_L + Z_S}|^2,\ 0 \leq |s|^2 \leq 1. \tag{4.4}$$

The power reflection coefficient Γ shows the fraction of the maximum power available from the generator that is not delivered to the load.

Now back to the particular case antenna and the RFID chip, the power delivered to the chip considering reflections is:

$$P_{in} = (1 - \Gamma) \cdot G_r \cdot EIRP \cdot (\frac{\lambda}{4\pi r})^2 \tag{4.5}$$

where, EIRP (equivalent isotropically radiated power), defined as

$$EIRP = P_t \cdot G_t \tag{4.6}$$

and is fixed by government regulations. In Europe the EIRP is limited to 3.3 W in 868 MHz band (866-869 MHz frequencies, Europe), whereas in US the limit is 4 W in 915 MHz band (902-928 MHz frequencies, US).

From Equation 4.5 it is clear that the only way to maximize P_{in} for a given range is increasing the gain of the tag antenna and reducing the reflections as much as possible. Both the gain and the impedance of the tag antenna are features that vary hugely with the antenna geometry, environment, materials and location regarding reader. RFID tag antenna performance strongly depends on the frequency dependent complex impedance presented by the chip. Tag input impedance must be closely monitorized in the design process in order to satisfy design requirements. Since antenna size and frequency of operation impose limitations on maximum attainable gain and bandwidth, compromises have to be made to obtain optimum tag performance and satisfy design requirements [29]. However, the antenna design is out of the scope of this Ph.D Dissertation.

Rectifier is the first circuit after the antenna, consequently its input impedance must be matched with the antenna impedance.

4.2.2 Analisys of rectifier input voltage (V_{in})

The performance of the rectifier is directly related with the amplitude of the RF signal V_{in} [1] is as follows:

$$V_{DC} = N(V_{in} - V_{th}) \tag{4.7}$$

where N is a integer related to the architecture of the rectifier and V_{th} is defined as the minimum input voltage amplitude required by the rectifier to work and is dependent on the process used to implement the RFID tag. From Equation 4.7 can be concluded that it is desirable to maximize V_{in} to achieve the required V_{DC} for tag supplying, and of course, using the minimum RF input power.

Figure 4.3 depicts the simplified impedance model of the antenna and the chip, which can be seen as series RLC circuit. The input impedance of the chip is capacitive

because of the supply capacitor of Figure 4.1 and the antenna impedance is inductive for achieving conjugate matching with the chip. The input impedance Z_{in} of the series RLC circuit is:

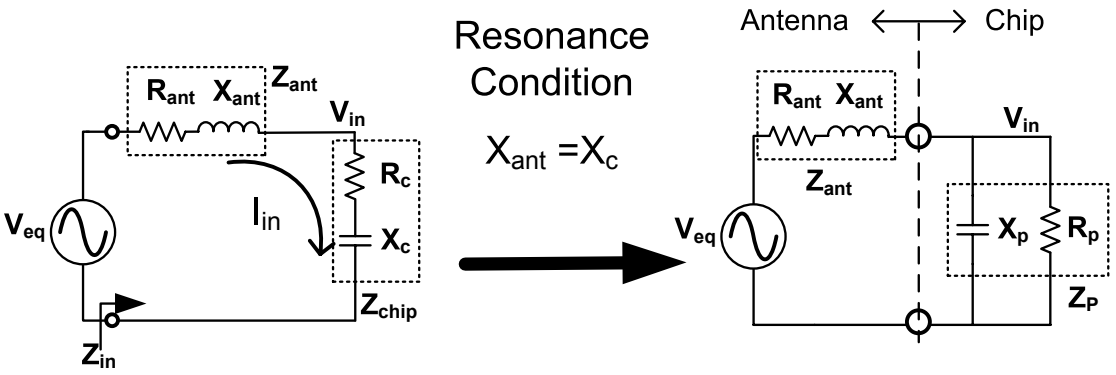

Figure 4.3: Antenna and chip as a series RLC circuit.

$$Z_{in} = R_{ant} + R_{chip} + X_{ant} + X_{chip} = R_{ant} + R_{chip} + j(wL - \frac{1}{wC}) \tag{4.8}$$

From inspection of the network (Figure 4.3), can be deduced that the impedance goes to infinity both at DC (because the capacitor acts as an open there) and at infinitively high frequency (because the inductor acts as an open there). As a conclusion, Z_{in} is essentially the impedance of the capacitor at very low frequencies, and the impedance of the inductor at very high frequencies. What divides "low" from "high" is the frequency at which the inductive and capacitive impedance cancel. Known as the resonant frequency, this is given by:

$$(w_0 L - \frac{1}{w_0 C}) = 0 \longrightarrow w_0 = \frac{1}{\sqrt{LC}} \tag{4.9}$$

The resonance is achieved for the frequency, where $X_{ant} = X_{chip}$. "Curiously" this is one of the conditions for maximal power transfer. For frequencies in the proximities of the resonance frequency the series chip impedance Z_{chip} can be converted in its parallel equivalent using the series–parallel impedance transformation:

$$R_p = \frac{R_{chip}^2 + X_{chip}^2}{R_{chip}} \tag{4.10}$$

$$X_p = \frac{R_{chip}^2 + X_{chip}^2}{X_{chip}} \tag{4.11}$$

At resonance the circuit can be simplified as shown in Figure 4.4.
In Figure 4.4, V_{in} is as follows:

$$P_{in} = \frac{V_{in}^2}{2R_p} V_{in} = \sqrt{2P_{in}R_p} \tag{4.12}$$

Since the value of P_{in} is already known from Equation 4.5, hence

$$V_{in} = \sqrt{2R_p(1-\Gamma) \cdot G_r \cdot EIRP \cdot (\frac{\lambda}{4\pi r})^2} \tag{4.13}$$

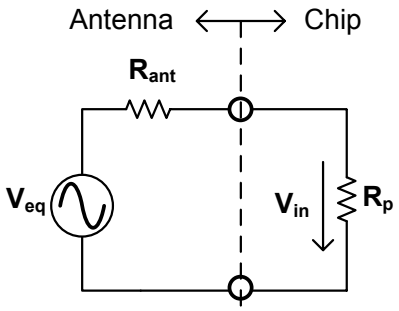

Figure 4.4: Simplified network representation of the antenna and chip at resonance.

Introducing the condition of resonance and substituting in Γ,

$$V_{in} = \sqrt{2R_p(\frac{4R_{ant}R_{chip}}{(R_{ant}+R_{chip})^2}) \cdot G_r \cdot EIRP \cdot (\frac{\lambda}{4\pi r})^2} \tag{4.14}$$

Figure 4.5 presents the influence of the input impedance and the antenna impedance on V_{in} for a constant link parameters and for resonance condition.

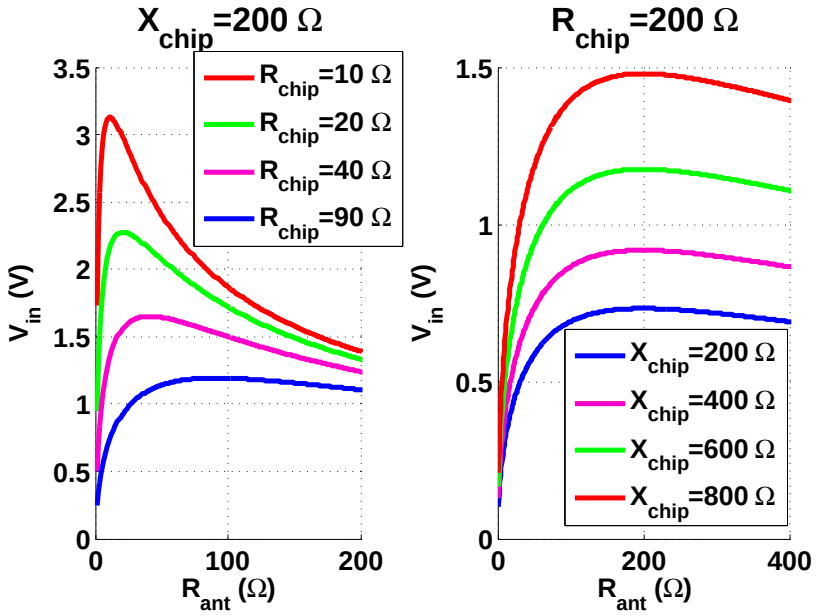

Figure 4.5: R_{ant} vs V_{in} (G_r=-0.5dB, EIRP=4W, r=1m and f=868MHz) a) for different R_{chip} values, and b) for different X_{chip} values.

Figure 4.5 shows that a maximum in V_{in} occurs when R_{ant} and R_{chip} are equal at resonance ($X_{ant} = -X_{chip}$). As a conclusion, the maximum in V_{in} is achieved for conjugate matching, i.e. for maximal power transfer. Another interesting characteristic can be extracted from Figure 4.5. Higher V_{in} peaks values are obtained for lower R_{chip}. From Equation 4.10 is clear that low R_{chip} values are translated into high R_p and therefore higher V_{in} (see Figure 4.4). Also note that the lower R_{chip} the sharper V_{in}, which means that low impedance mismatches between chip and antenna produce high drops in V_{in}. There is an important parameter to evaluate the grade of sharpness of V_{in}

in resonance, the quality factor (Q). The quality factor will be dealt more in detail later, first, the behaviour of V_{in} versus X_{chip} depicted in Figure 4.5 is analyzed. As can be seen in the figure, the higher X_{chip} the higher R_p and therefore higher V_{in}. However the sharpness of V_{in} increase softer than in the case of R_{chip}. The input voltage amplitude is above 3 V for $Z_c = 100 - j800\Omega$. This is a capacitor of 230 fF parallel to ground (see Figure 4.3). This value is extremely low, as an example, only the capacitance of a RF pad to ground is around 100 fF. Notice that, the input capacitance of the chip will be defined by the pad capacitance plus the input parasitic capacitance of the rectifier to ground.

4.2.3 Z_{in} Restrictions – Quality factor

The quality factor (Q) is an important and descriptive parameter always related to the resonance. Q can be defined as [93]:

$$Q = \omega_0 \frac{energy\ stored}{average\ power\ dissipated} \tag{4.15}$$

where ω_0 is the resonance frequency. Note that Q is dimensionless, and that it is proportional to the ratio of energy stored to the energy lost, per unit time. The concept of Q is applied both to resonant and nonresonant systems, for example the Q of a series RC circuit.

The quality factor of the chip input impedance is calculated considering that, at resonance, the energy is stored by the capacitor and the power is dissipated by the resistor [94]. The energy stored by a capacitor of capacitance C under a potential V is:

$$\epsilon_{cap} = \frac{1}{2}CV^2 = \frac{1}{2}\frac{I_{in}^2}{C\omega^2} \tag{4.16}$$

whereas the average power dissipated by a resistor R is:

$$P_{res} = R(\frac{I_{in}^2}{\sqrt{2}})^2 \tag{4.17}$$

Finally the Q of the input impedance is expressed as:

$$Q_c = \omega_0 \frac{\frac{1}{2}\frac{I_{in}^2}{C\omega^2}}{R(\frac{I_{in}^2}{\sqrt{2}})^2} = \frac{1}{\omega_0 RC} = \frac{X_{chip}}{R_{chip}} \tag{4.18}$$

where I_{in} is the amplitude of the current through the branch. Note that the definition of Q can be easily extended to the series RLC circuit. As at resonance the stored energy is constant and equal to $\frac{1}{2}CV_{cap}^2 = \frac{1}{2}LI_{in}2$, then

$$Q_{RLC} = \frac{\omega_0 L}{R} = \frac{1}{\omega_0 CR} \tag{4.19}$$

The voltage across the capacitor and inductor at resonance can differ significantly from the overall network voltage, which is due to the series resistance. (see Figure 4.6).

The voltage across the capacitor at resonance is as follows:

$$|V_L| = |V_C| = \frac{|I_{in}|}{Y} = \frac{|V_{ant}|}{R_{chip}Z_C} = \frac{|V_{ant}|}{\omega_0 CR_{chip}} = Q|V_{ant}| \tag{4.20}$$

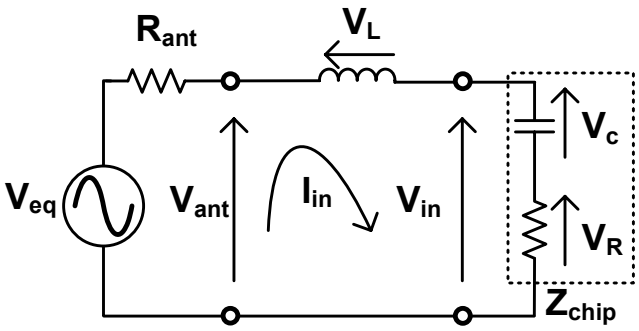

Figure 4.6: Equivalent circuit of antenna and chip to calculate V_{in} as a function of Q.

hence, the voltage across the chip input impedance is:

$$V_{in} = V_C + V_R = |V_{ant}|(1+Q) \tag{4.21}$$

This equation indicates that for a fixed $|V_{ant}|$, V_{in} can be done arbitrarily high by increasing Q. However increasing Q affects the frequency response of the I_{in}, as shows Figure 4.7

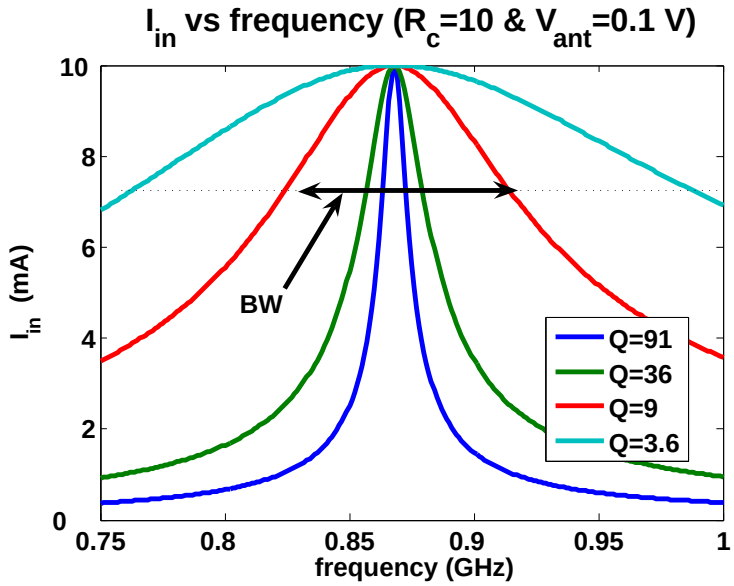

Figure 4.7: Frequency response of I_{in} for different Q values.

The frequency response of the series RLC circuit is also described using the quality factor, as can be seen in Figure 4.7:

$$Q = \frac{f_0}{f_2 - f_1} = \frac{f_0}{BW} \tag{4.22}$$

where f_0 is the resonance frequency, and f_1 and f_2 are the frequencies where I_{in} falls 3dB from its value at the resonance frequency. The bandwidth (BW) is defined as $f_2 - f_1$. As a conclusion, Q of the input impedance will be limited by the system bandwidth.

In the ISM band, the available frequencies depend on government regulations and differ among countries. The frequencies of interest for long range UHF passive RFID devices are 868MHz in Europa (ITU Region 1), 915 MHz in America (ITU Region 2) and 950 MHz in Asia (ITU Region 3). A RFID tag compatible with all the regions requires a bandwidth of around 100 MHz centred in 900 MHz that limits the maximal value of Q to 9. Figure 4.8 shows in the smith chart the ellipse of Q=9, the input impedances outside the ellipse should be avoided since bandwidth constraint is violated.

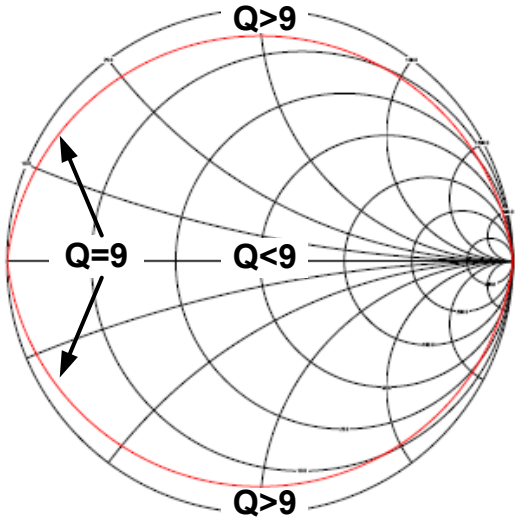

Figure 4.8: Ellipse of Q=9 draw on the smith chart.

4.3 Communications

The RFID tag is supplied by the RF wave from the reader. The same RF wave is also used for communication purposes. The Interrogator and Tag conform a half–duplex system which provides for communication in both directions, but only one direction at a time—not simultaneously. This section deals with the effects of the modulation of the RF signal on the RFID supply.

4.3.1 Interrogator to tag communications

An interrogator communicates with one of more tags by modulating the RF carrier using Amplitude–Shift Keying (ASK) with PIE (Pulse interval encoding) [31]. This modulation is also known as On–Off keying (OOK) and it is a type of modulation that represents digital data as the presence or absence of a carrier wave. The data are encoding using PIE, as is shown in Figure 4.9.

Tari is the reference time interval for Interrogator–to–tag signalling, and is the duration of a data 0. High values represent transmitted continuous wave (CW); low values represent attenuated CW. Interrogators shall communicate using Tari values between 6.25 μs and 25 μs, a modulation depth between 80 and 100 % and a maximum PW of 0.525Tari. As a conclusion, absences of RF input signal occurs when the reader issues commands. The maximal duration of this absences is 13.125 μs. Additionally,

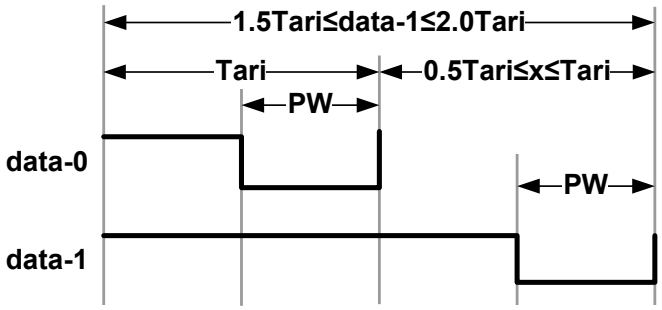

Figure 4.9: PIE symbols.

the interrogator does not send commands before the end of the maximum settling time interval[1].

As a consequence of the RF absences, the rectifier becomes an open circuit and the supply capacitor is discharged through the resistor R, it represents the RFID Tag current consumption, see Figure 4.10.

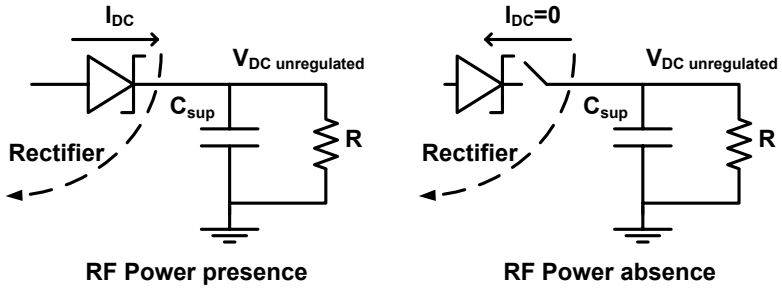

Figure 4.10: Discharge of the supply capacitor by absences of RF power.

The supply capacitor is dimensioned so that voltage on the resistor does not drop under the minimum supply voltage required by the RFID tag to work (V_{DCmin}). Supposing that the capacitor is charged to $V_{DC} > V_{DCmin}$, hence

$$C_{sup} = -\frac{13.125\mu s}{R\ln(\frac{V_{DCmin}}{V_{DC}})} \tag{4.23}$$

Notice that the supply capacitor is an integrated device, so its value can not be arbitrarily high as the area consumption becomes a problem. A trade–off has to be found among supply voltages, current consumption of the RFID Tag and area of the capacitor. Polysilicon on diffusion capacitors or stack capacitors [95], available on standard CMOS process, are more suitable for the supply capacitor implementation than the conventional double poly capacitor. The reason is because the former presents higher capacitance per area.

[1]Settling time interval is the time interval at the beginning of the communication between Reader and Tag where the Interrogator transmit a continuous wave. During the settling time the supply capacitor is charged, the supply voltage is stabilized and the analog and digital circuits of the tag are initialized. After the end of the settling time the tag must be ready to receive a command from the reader.

4.3.2 Tag to interrogator communications

A Tag communicates with an Interrogator using backscatter modulation, in which the Tag switches the reflection coefficient of its antenna, or the ICs input impedance, between two states in accordance with the data being sent.

A Tag shall backscatter using a fixed modulation format, data encoding, and data rate for the duration of the whole communication with the reader. The Tag selects the modulation format; the Interrogator selects the encoding and data rate [31]. The Interrogator commands the encoding choice and data rate at the beginning of the communication. Tags shall encode the backscattered data as either FM0 baseband or Miller modulation [2] of a subcarrier at the data rate. As example, the symbols and sequences of the FM0 are depicted in Figure 4.11

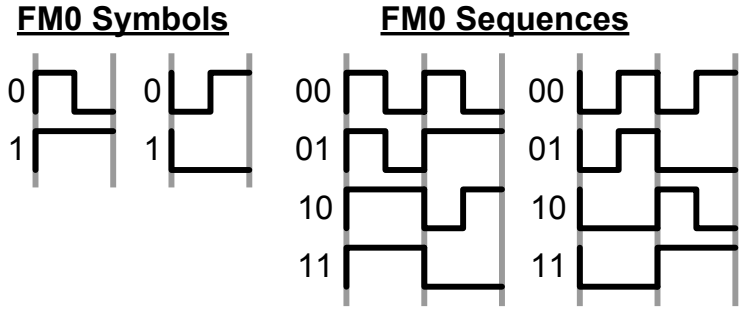

Figure 4.11: FM0 symbols and sequences.

The low values in Figure 4.11 correspond to the antenna–reflectivity state (State 1), i.e. Tag absorbing power, whereas the high values correspond to the antenna–reflectivity state (State 2), i.e. Tag reflecting power.

From the point of view of the Standard *EPCGlobal*, Tag backscatter shall use ASK and/or Phase–Shift Keying(PSK) modulation. The Tag vendor selects the modulation format and the Interrogators shall be capable of demodulating either modulation type.

The PSK modulation is achieved by changing the imaginary part of the input impedance with an equal amount of mismatch in both states, this is the reflection coefficient remain constant. On the other side, ASK modulation required the change of the real part of the input impedance. It have been probed [1] that ASK with constant reflection coefficient in both states is less power efficient than PSK. Therefore only ASK with power match in one of the two states and total reflection in the other state is considered (see Figure 4.12).

There are some studies about which modulation is more power efficient [1], [96], [5]. All of them conclude that PSK modulation is more power efficient than ASK when the Tag is the same amount of time in State 1(t_1) as in State 2 (t_2). The reason is because the reflection coefficient and therefore the chip input power remains constant in both states using a PSK modulation. On the other hand, the chip input power is maximal for one state and cero the other state, in ASK modulation. However when one of the states is active most of the time, (i.e. $t_1 << t_2 \approx 1$) ASK modulation becomes more power efficient at the expense of a much larger bandwidth. Another important advantage of

[2]Method of channel coding where a "one" data bit is encoded as a level transition in the middle of a bit cell, and a "zero" data bit yields a transition at the beginning of the bit cell, except in the case that a logic zero follows a logic one (see Figure 4.11).

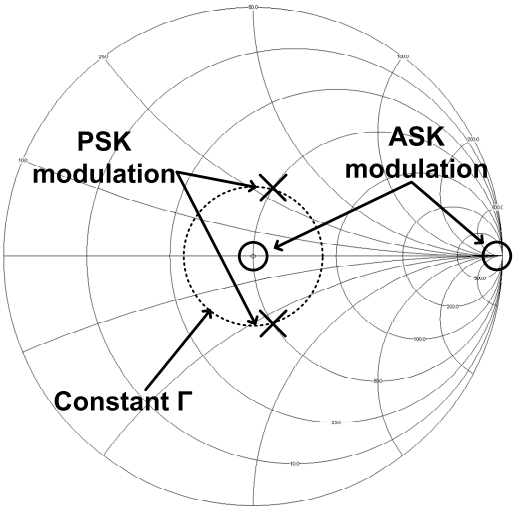

Figure 4.12: Antenna–reflectivity states for PSK and ASK modulation.

the ASK modulation over PSK is that the former do not requires any reactive element for its implementation. A simple CMOS switch is enough. Figure 4.13 shows the implementation of the ASK and PSK modulator, Figure 4.13(a) and Figure. 4.13(b), respectively. The ASK modulator is more simple than the PSK one that requires a capacitor. For proper antenna design no matching network is required in ASK, whereas for the case of PSK at least a reactive element is needed. This reactive element can be implemented on or off chip, in the last case an additional pad in the IC for the modulator is required.

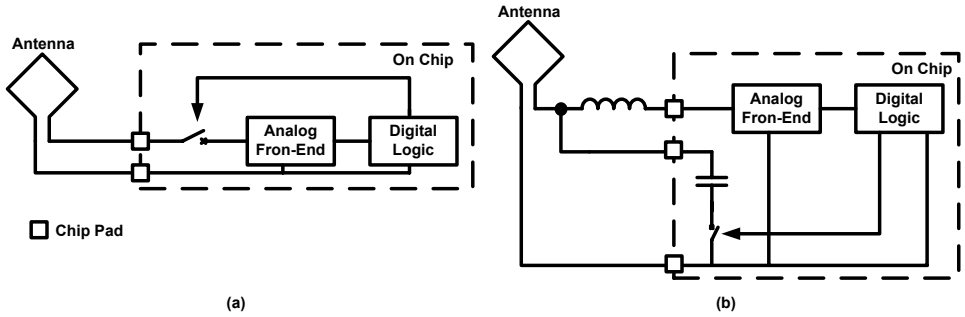

Figure 4.13: Possible implementation of the (a) ASK modulator and (b) PSK modulator.

4.4 General design considerations

This section analyzes the behaviour of the DC unregulated voltage across the supply capacitor during a whole link time between Reader and Tag.

Figure 4.14 presents the communication protocol during the link time according to the standard EPC global2 [31].

1. Reader begins the communication transmitting a CW with a maximal duration of

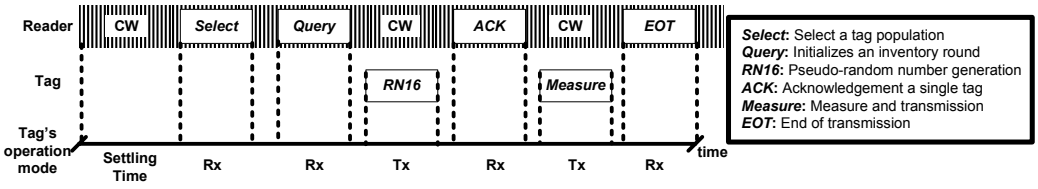

Figure 4.14: Link timing between tag and reader as described in the standard EPC global2.

1.5 ms. This period is referred as *settling time*, and charging the supply capacitor and turning on the complete system is required.

2. Reader start to sends OOK modulated commands. In other words, the reader switch on and off CW to transmitt information, as a consequence the power that reaches the IC fluctuates.

3. Reader waits for the Tags response and simultaneously transmits a CW. Tag reacts modulating the backscattered CW, this is, changing its input impedance. Variations in the input impedance of the chip affect de reflection coefficient. Therefore the power that reaches the IC also fluctuates during the Tags response.

The result of all these power fluctuations at the input of the rectifier are drops on the supply voltage that must be counteracted with the charge stored on the supply capacitor.

The followings equations defines the input power (P_{in}) and input voltage amplitude (V_{in}) of the RFID chip as a function of the reflection coefficient, distance and quality factor of the input impedance.

$$P_{in} = (1 - \Gamma) \cdot G_r \cdot EIRP \cdot (\frac{\lambda}{4\pi r})^2 \tag{4.24}$$

and as

$$P_{ant} = \frac{V_{ant}^2}{2R_{ant}} \tag{4.25}$$

hence

$$V_{in} = V_{ant}(1 + Q) = \sqrt{2P_{in}R_{ant}}(1 + Q) \tag{4.26}$$

From V_{in} the output voltage of the rectifier can be expressed as:

$$V_{DC} = N(V_{in} - V_{th}) \tag{4.27}$$

However, this equation does not model the behaviour of the rectifier completely since it does not give any idea about the load at the output of the rectifier. The output resistance of the rectifier varies with the input power and with the current consumption of the IC [97]. The higher is the input power the greater is the output resistance. On the other hand, the higher is the current consumption of the IC the lower is the output resistance of the rectifier. In the bibliography nobody express the input impedance of the multiplier as a function of the current consumption of the IC. However, this is a key issue to automate the design of the rectifier, to elaborate a proper power balance and to specify the rest of the circuits of the supply system.

In order to carry out a power balance, the DC supply requirements of the RFID sensor and the V_{th} of the rectifier have to be fixed. The both parameters are set by

the technological process used to implement the IC. The following section deal with the technology selection.

4.4.1 Technology selection

In the technology selection are involved technical (working voltage or V_{th}) and non–technical (price or availability) aspects. Next, the critical aspects that must be considered in the selection of a technological process for the fabrication of Passive RFID sensors are presented. That is:

- Supply voltage. The V_{DC} is generated from the input RF power that degrades with the square of the range. The lower supply voltage the higher range is achievable.
- Schottky diodes or low threshold MOS devices availability. Equation 4.7 shows that V_{DC} is directly proportional to the difference $V_{in} - V_{th}$. So reducing V_{th} the supply voltage increases for the same input voltage. In other words higher ranges can be achieved reducing the V_{th}.
- Parasitic capacitance. The parasitic capacitance to the substrate in parallel with the antenna input degrades the efficiency of the rectifier. At high frequencies the influence of parasitic capacitors are not negligible and part of the input current drop to ground through this capacitors.
- EEPROM as standard cell. The EEPROM (Electrically Erasable Programmable Read–Only–Memory) is the kind of memory used in RFID applications for data storing. Passive wireless sensors require a reduced data store capacity (around 10 bits [16]). Usually foundries offer standard EEPROM blocks of at least 256 bits, which suppose a waste of more than 200 bits in Passive RFID sensors, this is a waste of complexity, area and power. Some foundries offer latches as standards cells, so the memory can be optimally dimensioned for the application.
- High density Capacitors. An integrated capacitor stores energy for a proper IC supply. High capacitance is desirable for maintain the supply voltage when RF absences occurs. On the other side, the size of the capacitor can not be arbitrarily large as the cost becomes prohibitive. Since the larger is the capacitor the higher is its capacitance, a trade–off between area and capacitance must be found. The ratio Capacitance–Area of high density capacitors is higher than the traditional integrated poly–poly capacitor. However the formers requires a special process step and are not available in all the CMOS technologies.
- Economical factors. The cost should be keep at its minimum, as the price of each Passive RFID sensor should not be higher than some tens of cents. This means that standard CMOS processes instead of high performance technological processes are considered.

Table 4.1 shows a comparison among tree different foundries XFAB, ATMEL and AMIS. The first two are included because they are the most widely used in the work environment where the project WISEN [98] is going to accomplished. This is an advantage for processes with equal characteristics since it would simplify the design work. XFAB is included in this list because a first look to its processes showed that they might have one

Table 4.1: Comparison of different technology process

characteristic	XFAB XL035LV	AMIS C5F/N	ATMEL SMOS3EE
Runs per Year	4	11	4
Min. Area (mm^2)	10	5	n.a.
Shottky V_{th} @ 10μA (V)	0.16	0.25	0.235
C density ($fF/\mu m^2$)	4.24	0.95	1.25
Low working voltge (V)	1 to 3.3	2.5 to 5	1.8 to 5.5
Min. EEPROM size (bits)	1	n.a.	256
EEPROM Voltage (V)	1.8 to 3.6	3 to 5.5	1.8 to 5.5
Bipolar	yes	no	yes
Charge pump	yes	no	yes

specially focused on RFID projects, and it is also common in the working environment. Finally, ATMEL is included because the RFID tag [1] that involved one of the greatest advantages in UHF passive RFID was built with its technology.

From Table 4.1, it can be concluded that the technology with the best process, looking at the specifications sheets and the information available, is XFAB since presents the lowest supply voltage, the lowest V_{th}, highest capacitance per area unit and 1 bit latches are available.

4.4.2 Parameters definition

Some parameters, that influence the power recovery system, have been already defined by mean of the communication protocol, technological process or governmental regulations. This subsection summarizes the parameters to carry out the power balance that will serve to specify each particular block of the power recovery system.

Technology

First, the parameters defined by the technology selection are listed in Table 4.2. The values of current consumption of the different circuits of the Tag were extracted from a prototype built in the selected technology [98]:

Communication protocol

Second, the parameters defined by the communication standard and governmental regulations are detailed in Table 4.3.

Other parameters

Finally, other parameters related with the antenna and ERS are enumerate in Table 4.4.

Table 4.2: Design parameters based on technology process

$V_{DCanalog}$	The range of the supply voltage stabilised by the process for proper work of the analog circuits is from 1 to 3.3 V.
$V_{DCdigital}$	The range of the supply voltage stabilised by the process for proper work of the EEPROM is from 1.8 to 3.6 V.
V_{DC}	The breakdown voltage on the supply capacitor is 3.6 V and sets the maximum V_{DC}.
V_{th}	The threshold voltage of the schottky diodes is 0.33 V.
Maximal capacitance	The maximal area occupy by the supply capacitor should not be larger than 0.5 mm^2 since for larger sizes the prize becomes a constrain. This area corresponds with a capacitance of 2.12nF.
Current consumption	12.5μA that correspond with of the analog Front-End and the digital part.
Sensor current consumption	12.1μA.

Table 4.3: Design parameters based on communication standard and governmental regulations

frequency range	The frequency range specified by the standard goes from 860 MHz up to 960 MHz. Therefore, the input impedance of the RFID tag requires a Q of 9.1 or less to resonate properly in the whole band.
Data rate for the communication Reader–Tag	The lowest bit rate allowed by the standard is selected for the study, because for this case the absences of CW are longer and; therefore, the most restrictive conditions for the ERS (20kbits/s).
Data rate for the communication Tag-Reader	This parameter has influence on the ERS only if the backscatter signal is ASK modulated. The most restrictive data rate for the ERS is the lowest one (40Kbits/s).
Reader Radiated Power	In Europe, the maximal Effective radiated Power (ERP) is 2 W which is equivalent to 3.28 W EIRP. In US, Japan and other regions the radiated power levels are higher

Table 4.4: Design parameters based on antenna restrictions

Tag antenna gain	The gain of the antenna is 0 dBi.
Antenna impedance	Conjugate matching between chip and antenna is supposed.

4.5 Specification of energy recovery system

Once the parameters have been defined, the electrical characteristic of the ERS blocks can be specified. The objective of the power balance is to specify the requirements of the ERS in order to achieve the theoretical maximal operation range. Table 4.5 lists the elements and values that will be specifed.

Table 4.5: Elements and values to specify inside the ERS

Modulation	EPC Global2 allows two modualtions PSK vs ASK.
Rectifier Input impedance	Z_{in} is required to fabricate the antenna
Rectifier Power Efficiency	This value is critical to define the maximal range of the system.
Capacitance of the supply capacitor	The goal is a trade–off between area and performance.
Threshold voltage of the Voltage Sensor	This value decribes the behaviour of the voltage sensor.
Threshold voltage of the High–Voltage Protection	Maximal voltage allow in the supply capacitor.
Current through the High–Voltage Protection	To be wasted when the protection reaches its threshold.
Regulated DC voltage	A proper value that sets supply voltage of the RFID sensor.

4.5.1 ASK vs PSK

Figure 4.15 shows V_{DC} during the tag settling time (from 0 to 1ms), receiving time (from 1 to 3 ms) and transmitting time (from 3 to 5 ms). PSK modulation is used for the communication Reader–Tag ($\Gamma = 0.3$ the whole time). Different distances have been simulated. The current consumption of the IC was modelled with a resistance of value 90 kΩ this is a current consumption of 25 μA at 2.25 V.

The maximal operation range is around 4 meters. At higher distances the supply voltage drops under 1.8 V, which is the minimum voltage required by the EEPROM to work. The ripple produced during the receiving time is consequence of the OOK modulation used by the reader, the amplitude of the ripple can be reduced by increasing the capacitance of the supply capacitor.

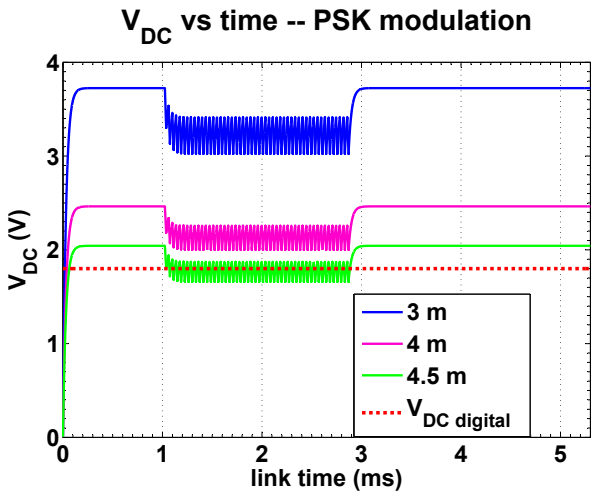

Figure 4.15: Behavior of V_{DC} during settling, receiving and transmitting time ($R_L = 90k\Omega$).

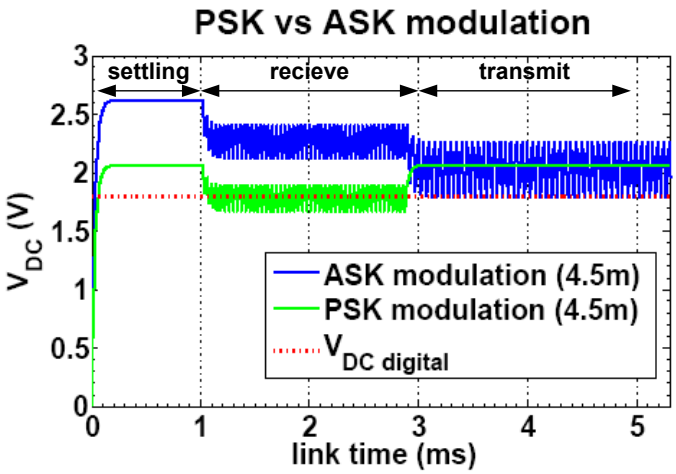

Figure 4.16: Behavior of V_{DC} for ASK and PSK modulation ($R_L = 90\ k\Omega$).

Figure 4.16 illustrates V_{DC} of two tags under the same conditions, one transmitting ASK and the other PSK. During the settling time, and receiving time, the V_{DC} is clearly higher for the ASK Tag, since $\Gamma \approx 0$. However, a ripple is produced due to the Γ switching when the ASK Tag transmits. This ripple can be attenuated increasing the capacitance of the supply capacitor.

4.5.2 Rectifier

Two paramenters: efficiency and input impedance specifies the performance of the rectifier. The former describes the amounth of input power lost in the RF into DC power conversion. The latter influences, on the one side, the amplitude of the RF voltage that reaches the rectifier and, on the other, the output impedance of the antenna.

Efficiency

Figure 4.16 shows that using V_{DC} during the settling time as a reference: first, V_{DC} decays 0.45 V in receive mode with PSK. And second, V_{DC} drops 0.9 V in transmit mode with ASK. In conclusion, the required V_{DC} is 2.25 V in PSK tags and 2.7 V in ASK tags in order to accomplish the limitation set by EEPROM minimum operating voltage. Knowing this limitation and the resistance that models the tag current consumption, the required efficiency of the rectifier versus range is calculated as (see Figure 4.17):

$$\eta = \frac{\frac{V_{DC}^2}{R_{load}}}{P_{in}} \tag{4.28}$$

where P_{in} is calculated from Equation 4.5.

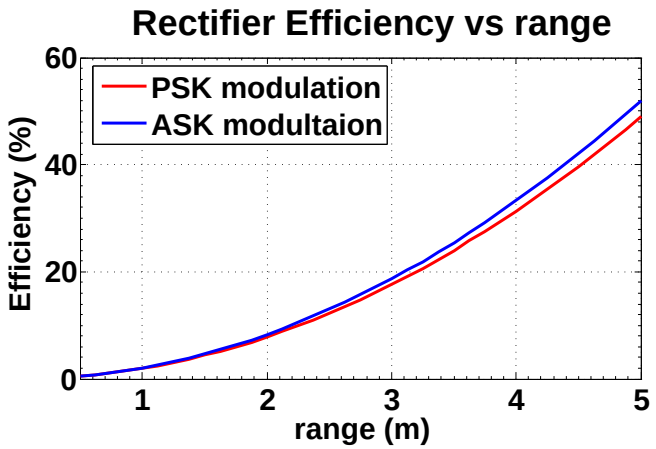

Figure 4.17: Rectifier efficiency as a function of the distance between reader and tag ($R_L = 90k\Omega$).

The required rectifier efficiency increases with the distance since for short ranges the available power on the rectifier is considerably higher (see Figure 4.17). Efficiency is similar in both modulations, specially for short ranges. Notice that although P_{in} in ASK tags is higher than in PSK due to the lower reflection coefficient, ASK tags require more rectifier efficiency since V_{DC} is higher.

Input Impedance

The input impedance of the rectifier is related with V_{in} and Γ. As the reflection coefficient is defined by the type of backscatter modulation, the input impedance is selected considering its effect on V_{in}:

$$V_{in} = |V_{ant}|(1+Q) = \sqrt{2P_{ant}R_{ant}t}(1+Q) \tag{4.29}$$

Considering that $R_{ant} = R_{chip}$, hence

$$V_{in} = \sqrt{2P_{ant}R_{ant}}(1+\frac{|X_{chip}|}{R_{ant}}) \tag{4.30}$$

On the other hand, the minimum V_{in} is defined by the minimum V_{DC}, V_{th} and the architecture parameter N.

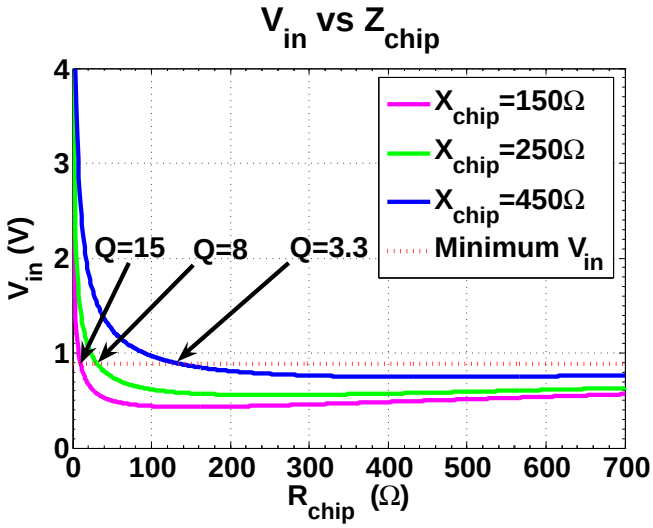

Figure 4.18: Rectifier input voltage as a function of its input impedance ($R_L = 90k\Omega$).

Figure 4.18 shows V_{in} as a function of the input of R_{chip}, for tree different values of $|X_{chip}|$ and for a range of 4.3 m using PSK modulation. The dashed red line indicates the minimum V_{in} to generate the required V_{DC}. The higher $|X_{chip}|$ the more relaxed is the Q requirement for a given range. The parasitic capacitances to the substrate at the input of the chip reduces the value of $|X_{chip}|$, therefore, they should be minimized.

4.5.3 Supply capacitor

In the supply capacitor, design must be considered following aspects: area, charging time and ripple on the V_{DC}. Figure 4.19 presents V_{DC} versus time for different capacitances. The pink line represents a capacitance of 2.2nF. This capacitor achieves low ripple at the expense of excessive charge time and area. On the other hand, the blue line depicts a capacitance of 0.7nF that means a reduction in area and charging time. However, the minimum $V_{DCdigital}$ is violated due to the excessive ripple. Finally, the green curve with 1.2nF shows an proper trade–off between ripple size and charge time.

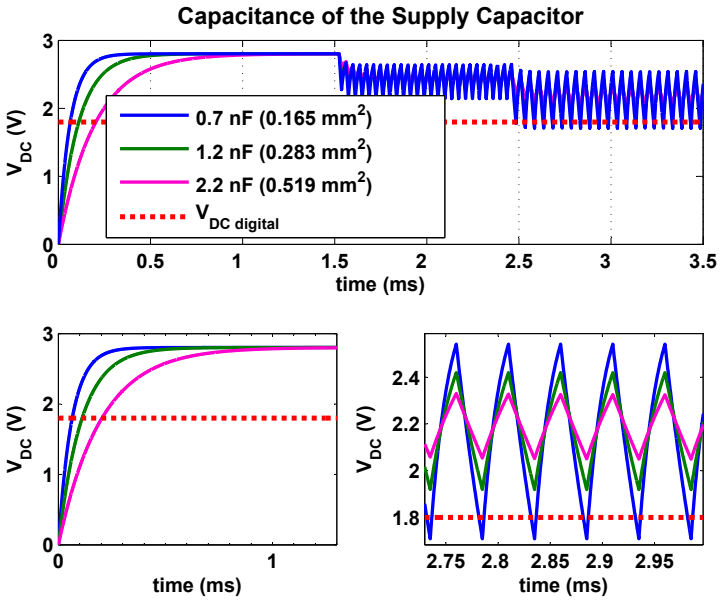

Figure 4.19: Behavior of V_{DC} for different supply capacitor capacitances ($R_L = 90k\Omega$).

4.5.4 Voltage Sensor

The Voltage Sensor circuit checks the charge of the supply capacitor and turns on the RFID chip when V_{DC} is enough to supply the system. When the threshold voltage of the Voltage Sensor circuit (V_{ESth}) is reached, the Voltage Sensor circuit turns on the Voltage Regulator, that supplies the complete chip.

V_{ESth} must be anough high to proper supply of the voltage regulator. On one side, the lowest voltage of the technology is 1V, hence, $V_{ESth} > 1$. On the other, voltage regulator requires a voltage reference circuit. The most poular voltage reference is the bandgap reference which generates a reference voltage of 1.2 V [99] and requires a supply of 1.6 V. This value will set $V_{ESth} = 1.6$ V.

4.5.5 High voltage protection

Three phenomenons occur simultaneusly in the energy recovery system, due to the characteristics of the rectifier. First, the level of the received RF power increases quadratically as the distance between reader and tag decreases. Second, the voltage on the supply capacitor increases with the level of RF power at the input of the rectifier, when the current consumption of the tag remains constant. And third, the CMOS process limits the voltage on the supply capacitor to 3.6 V. As a conclusion, the supply capacitor must be protected against high voltages produced when the Reader is close to the tag.

The formula for minimum separation distance between the source and reference UHF antennas is often quoted in the literature [100] as $d >= \frac{2a^2}{\lambda}$, where a is the largest aperture dimension of the antenna. As the reader antenna presents the larges aperture dimension around λ, the minimum distance is 2λ. At this point the power at the input of the rectifier is:

$$P_{inmax} = \frac{1}{(8\pi)^2} P_{eirp} G_{tag} \tag{4.31}$$

Hence, the maximum power at the rectifier output is 4.21 mW, supposing[42] $P_{eirp} = 3.28W$, $G_{tag} = 2.1dB$ and a rectifier efficiency (for the best case) of 50 %, then the current that drops on the protection must be 1.17 mA @ 3.6 V.

Additionally, when the RFID tag does not require protection the current consumption of the High Voltage Protection should be kept as low as possible.

4.5.6 Voltage regulator

The DC voltage generated by the rectifier (V_{DC}) varies along the link time with the distance, communication protocol and current consumption of the IC. On the other side, a stable voltage is mandatory for proper supplying of digital and analog circuits and sensor. Therefore a regulation circuit is required to generate a constant supply voltage (V_{DD}).

A voltage regulator is a circuit that provides a well–specified and stable dc voltage whose input to output voltage difference can vary [101]. The dropout voltage is defined as the value of the input/output differential voltage where the control loop stops regulating. The dropout should be as low as possible (less than 0.1 V), as it will be sum to the required V_{DC}.

The efficiency of the regulator is limited by the quiescent current and the input/output voltages, and is expressed as

$$Eff_{reg} = \frac{I_O V_{DC}}{(I_O + I_q)V_{DD}} \tag{4.32}$$

where I_O and V_{DD} correspond to the output current and voltage, V_{DC} is the input voltage and I_q the quiescent current. In passive RFID systems, high efficiency is a priority and for the regulator can not be lower than 90 %. Since the estimated current consumption of the complete tag (included the sensor) is 25 μA, the voltage regulator quiescent current can not exceed 2 μA supposing a dropout of 0.1 V.

The technology allows low working voltage (1 V). However, the EEPROM requires a supply voltage of $V_{dd} = 1.8\ V$. Power consumption can be reduced by generating two different supply voltages, one for circuits that allow low voltage operation and the other for the EEPROM and digital circuits. The low working voltage is set to $V_{aa} = 1.2\ V$, this value is 0.2 V higher than the minimum allow by the technology to make the system more robust against temperature and process variations.

4.5.7 Specification summary

Next, the discussed specification of the ERS are summarized in Table 4.6. For better undestanding of Table 4.6, the ERS block diagram is depicted again.

The specifications are divided in the different blocks that form the energy recovery system. The Rectifier is specified in terms of minimal V_{DC} depending on the modulation, Q of the input impedance and efficiency. The best trade–off between area and charge for the supply capacitor is 1.2 nF. Current consumption and threshold voltage of Voltage Sensor circuit and High Voltage protection are predicted, as well as, the protection current ($I_{protection}$) to avoid breakdown voltage on the supply capacitor. Finally, the voltage regulator specifications are: dropout, supply voltages for the system and for the EEPROM and current consumption.

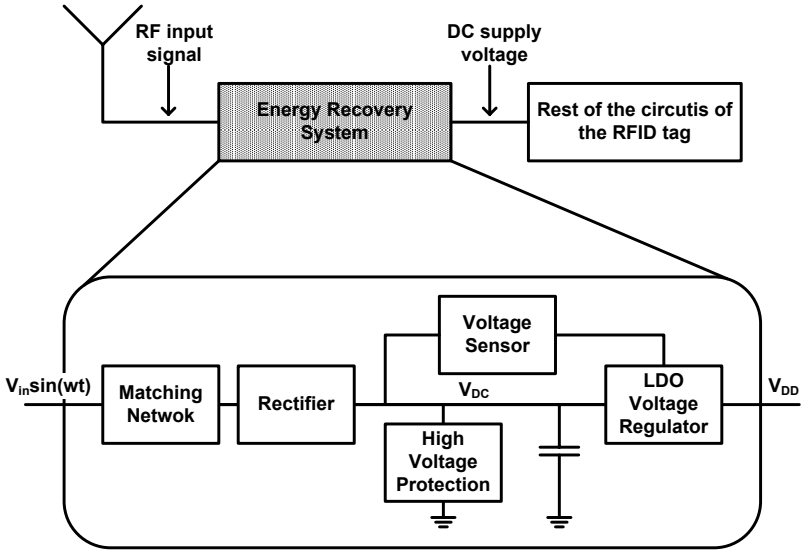

Figure 4.20: Energy recovery system block diagram.

Table 4.6: Energy Recovery System Specifications

Rectifier	
V_{DC} ($R_{load} = 90K\Omega$)	2.35V (PSK modulation) and 2.8 V (ASK modulation).
Q factor	< 9
η (r=3m)	20%
Supply Capacitor	
C	1.2nF
Voltage sensor	
V_{ESth}	$1.6V$
$I_{consumption}$	$<$ 100nA
High Voltage Protection	
$I_{protection}$	1.17mA @ 3.6V
V_{thHVP}	3.6V
$I_{consumption}$	<100nA
Voltage Regulator	
dropout	<0.1V
V_{dd}	1.8V
V_{aa}	1.2V
I_q	$< 2\mu A$

4.6 Conclusions

Next, the conclusions extracted from this chapter are enumerated:

- The interface Antenna–Chip has been analyzed in terms of input power, input voltage and quality factor (Q) for the particular case of passive RFID sensors. The result of this analysis limits the value of the input impedance and restricts the quality factor to $Q < 9$ in order to assure an adequate input voltage and bandwidth.
- The pros and cons of the different backscatter modulations allowed in the standard were identified and evaluated considering the restrictions of passive RFID sensors.
- A reasoned selection of the technology process has been carried out taking into account technical and non–technical aspects for comparing several foundries.
- The electrical behaviour of all components of the Energy Recovery System, optimized for maximal operating range, has been specified on basis of well defined parameters. The resulting values are start point of the design of each particular block of the ERS, namely, Rectifier, Wake–Up, High–Voltage Protection and Voltage Regulator.

Chapter 5

Rectifier

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Abstract: The circuit in charge of the RF into DC energy conversion is known as Rectifier. The energy conversion efficiency together with the DC power requirements of the tag will determine the maximal reading range as explained in Chapter 2.1. Passive wireless sensors present more restricted power requirements than pure passive UHF RFID tags, consequently, the rectifier design have to be optimized for the new requirements. The major goal of this chapter is to optimize the design of rectifiers for passive wireless sensors. The location of the rectifier inside the ERS is illustrated in Fig. 5.1.

Section 5.1 presents the state–of–the–art in the field of Rectifiers for passive UHF RFID applications. In the next section, the rectifier design is described considering the trade–offs involved in wireless sensing. Section 5.3 proposes a mathematical model to characterize the operation of the rectifier

in terms of input impedance, and output voltage as a function of the power requirements, technology and its input power. Finally, experimental results prove the proposed design methodology and mathematical model.

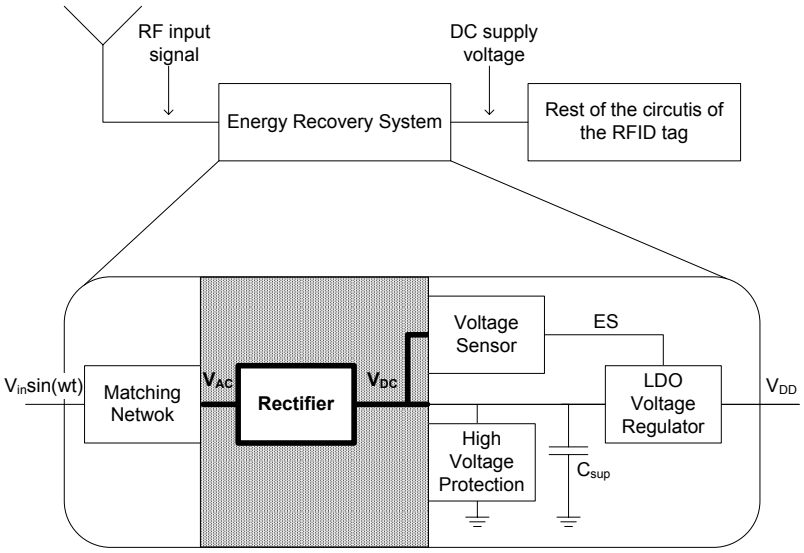

Figure 5.1: Energy recovery system block diagram.

5.1 Rectifiers: State–of–the–Art

The very first approach for AC–DC conversion is known as Cockcroft–Walton multiplier [102] and dates back to 1932. This circuit found application in the Nuclear Physics for generating very high voltages required to produce high velocity positive ions. More recently in 1975, Dickson [47] presented an improved voltage multiplier configuration specially suitable to be integrated. The first motivation of the Dickson multiplier was to generate the relative high voltages (30–40V) to write or erase information in non–volatile memories. In 2003, it was published the first passive UHF RFID tag [1], where Dickson multiplier was modified and used to generate the DC supply voltage of the chip (see Figure 5.2).

The modified Dickson Topology and its variants are used a AC–DC converter in all reported passive and active integrated UHF RFID tags [1, 5, 51, 41, 103, 48, 42]. As no other alternatives have been reported, this architecture is adopted as an AC–DC converter. Figure 5.2 shows the schematic of the modified Dickson Topology.

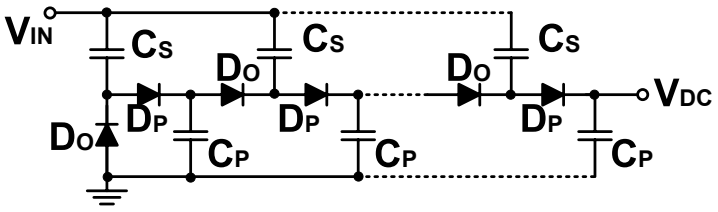

Figure 5.2: Modified Dickson rectifier.

The diodes are switched with the AC input voltage (V_{in}) pumping current towards the output and multiplying the voltage of the capacitors. Note that the amplitude of the input AC voltage V_{in} must be higher than the diodes threshold voltage (V_{th}), for a proper diode switching. Then, Odd Diodes (D_o) conduct, Pair Diodes (D_p) are open circuits and the Serial Capacitors (C_s) are charged in the negative cycles of V_{in}, see Figure 5.3.a. In the positive cycles of V_{in}, D_p conduct, D_o are off, and the C_p capacitors are charged, see Figure 5.3.b. If the capacitors are big enough, the voltage is maintained until the next input–signal cycle, so the output can be considered as a DC voltage. The value of V_{DC} depends on the number of diodes of the rectifier, as follows:

$$V_{DC} = N(V_{in} - V_{th}) \tag{5.1}$$

where N is the number of diodes of the rectifier.

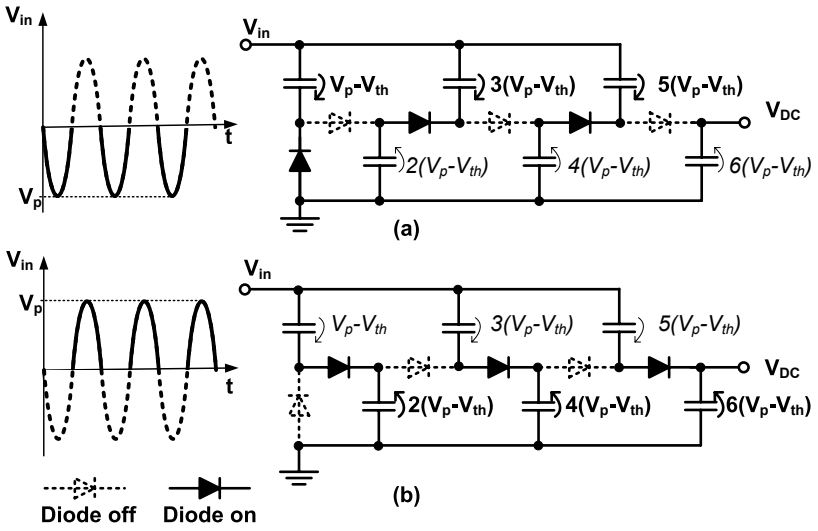

Figure 5.3: Basics rectifier operation. (a) For the negative cycles of V_{in}, (b) for the positive cycles of V_{in}.

5.1.1 Topology selection

The reported variants of the modified Dickson multiplier can be split into three different approaches:

- Classical: It was introduced in 2003 by [1]. This approach directly implements the schematic depicted in Figure 5.2. The diodes are either Schottky diodes due to its low forward voltage or low (zero) threshold diode–connected MOS transistors [51, 103].

- Biased: The second approach replaces the diodes for biased transistors. The biasing of each transistor is carried out connecting voltage (V_{bth}) between the gate and drain terminals. As a result the equivalent V_{th} of the transistors is reduced and the Equation 5.1 is rewritten as follows:

$$V_{DC} = N(V_{in} - V_{th} + V_{bth}) \tag{5.2}$$

The drawback of this approach is the need of a bias voltage. At this point, some authors make use of batteries [41, 42] to generate V_{bth}, as a consequence the RFID tag is no more passive but active or semi-active. An alternative is to use a internal V_{th} cancellation circuit based on ferroelectric capacitors[48]. Ferroelectric capacitors are not available in standard CMOS process, therefore, the fabrication price increases considerably.

- Full-wave rectifier: The modified Dickson Rectifier is first symmetrized and then the capacitors are rearranged so that every rectifying diode is excited with the same input signal amplitude [97] (see Figure 5.4). The relation between the number of diodes and V_{DC} remains as in the classical circuit (see Equation 5.1). The authors of [97] related a reduction of the input impedance; however they do not test this feature. As a conclusion, there is not a particular interesting advantage of the full wave rectifier regarding to the classical approach, and the circuit complexity is increased. Additionally, this approach was only implemented in silicon–on–sapphire (SOS) CMOS technology; which is a high performance process with low threshold voltage CMOS transistors and isolated devices, that presents very low parasitic capacitance compared to the standard process.

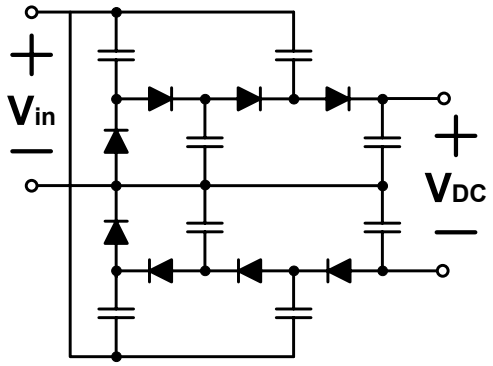

Figure 5.4: Two–stage full–wave rectifier.

On one hand, the biased rectifier requires either batteries or expensive technologies, both items are outside the system specifications related in Chapter 4.1. On the other hand, the full–wave rectifier have been only proved in a high performance technology, does not present proved advantages over the classic approach and increase the design complexity of the rectifier. As a conclusion, the biased and full–wave approaches are discarded. The rectifier will be implemented using the classical approach with the Schottky diodes, since this approach has been proved in several CMOS standard process with schottky diodes and it was adopted for most of the authors.

5.2 Rectifer design

There are three fundamental variables involved on the design of a UHF RFID rectifier:

- diode size,
- series and parallel capacitor size, and

- stage number.

The design parameters used to find the best arrange from the above mantioned variables are listed below:

- Input impedance (Z_{in}). Necessary to evaluate Q and to design the antenna matching network.
- Efficiency(η). The power conversion has to be as efficient as possible to reach largest ranges. The efficient (η) is defined as:

$$\eta = \frac{P_{DC}}{P_{in}} 100 = \frac{V_{DC}^2}{P_{in} R_L} 100(\%) \tag{5.3}$$

  where P_{in} is power that reaches the rectifier, P_{DC} is the DC output power, and R_L the resistance that models the current consumption.

- Output DC voltage under load conditions. The rectifier must generate sufficient DC voltage for proper RFID sensor supplying.

This section describes: first, the devices that form the rectifier, namely schottky diodes and capacitors. Next, the design variables are presented and their effect on the design parameters is discussed. Finally, the results of a study to find out the best arrange are discussed and the best solution is presented.

5.2.1 Integrated Schottky diodes

Schottky diodes have been used for over 25 years in the power supply industry [104]. The primary advantages are very low forward voltage drop and switching speeds, that approach zero time making them ideal for output stages of switching power supplies. This latter feature has also stimulated their additional use in very high frequency applications, including very low power involving signal and switching diode requirements of less than 100 picoseconds. These require small Schottky devices with low capacitance.

Design considerations with Schottky devices are limited in some applications compared to pn junction rectifiers, because their reverse leakage currents are many times higher. Also Schottky rectifiers have maximum rated junction temperatures typically in the range of 125° C to 175° C, compared to the typical 200° C for conventional pn junctions which further influence leakage current behaviour.

In the design of UHF rectifiers, where low V_{th} values and high speed switching are mandatory, Schottky diodes are the best choice [1]. Reverse leakage current must be minimized in the design phase, since the efficiency of the multiplier is directly related with this magnitude. Figure 5.5 depicts the Voltage–Current characteristic of a Schottky diode.

The parameters illustrated in Figure 5.5 are:

- V_f Forward Voltage,
- I_f Forward Current,
- R_D Differential Resistance also known as Series Resistance,
- I_r Reverse Current,

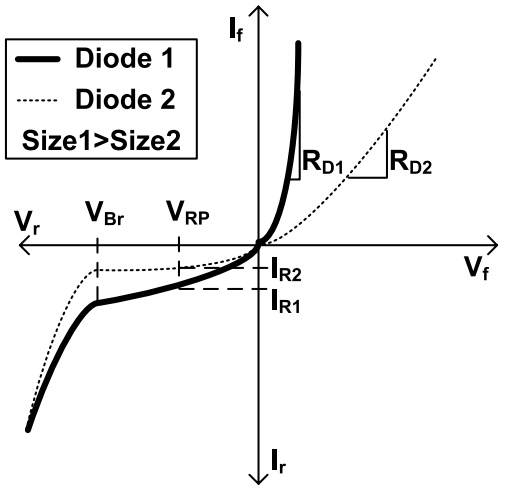

Figure 5.5: Schottky voltage–current characteristics and typical parameters.

- V_{Br} Reverse Break–Down Voltage (18 V in the chosen technology process),
- V_{RP} Working Peak Reverse Voltage

Figure 5.5 also shown the Voltage–Current behaviour of two diodes with different sizes. Larger diodes present lower V_{th} and R_D but higher reverse currents than smaller diodes. Therefore, a trade–off must be found to fix the diode size.

An additional diode parameter is the diffusion capacitance between anode and cathode. In the particular case of Schottky diodes, C_D is equal to the junction capacitance C_j, which arises due to the charge dipole of the depletion region near the metallurgical junction [105]. The junction capacitance is dependent of the reverse voltage applied on the diode.

The parasitic capacitance and resistance to the substrate is the last point to complete characterization of the diode. Parasitic elements are created between the terminals of the cathode and the substrate. The parasitic capacitance and resistance are proportional to the device size. Thus, small diodes are preferred to reduce the parasitic effects.

Figure 5.6 shows the RF–model of an integrated Schottky diode [2]. The ideal diode would have $R_f = 0$, $R_r, R_P = \infty$ and $C_D, C_P = 0$, of course, they are ideal values. However, the elements of the model can be adjusted, rising the diode dimensions. Table 5.1 displays the model values of three diodes with different sizes.

The size of D3 is the minimum allowed by the technology, therefore, D3 presents the lowest diffusion capacitance and parasitic effects. Nonetheless, small diodes have high forward resistance, as the P–region that forms the anode of the diode presents a very high sheet resistance per square. This resistance can be reduced introducing more contacts, therefore, increasing the area. Notice that the forward current is considerably increased when the diode size rises.

From Table 5.1 can be extracted that the area of D1 is excessive as its parasitic resistance is too low, and will produce prohibitive DC current losses. In passive RFID sensors, where the power losses are critical, the parasitic resistance must be as low as possible. The same occurs with R_r, the reverse DC current that flows through the diode

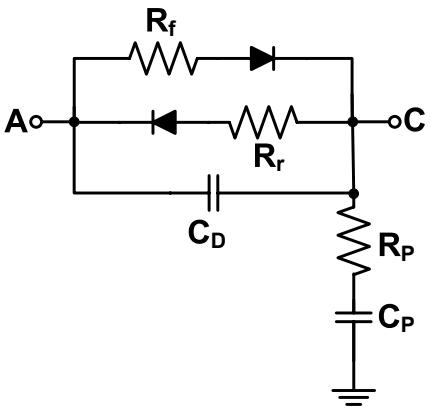

Figure 5.6: RF–model of an integrated Schottky diode [2].

Table 5.1: Electrical characteristics of several Schottky diodes in XL035–XFAB

	Diode Size (μm^2)	R_f (Ω)	R_r (Ω)	C_D (fF)	R_P (Ω)	C_P (fF)
D1	16x20	17.5	2.4k	570	6.8k	227
D2	14x2.4	332	55k	30	63.5k	24
D3	7x1.2	665	91k	15	250k	6

when they are off, discharges the capacitors and hence does not contribute to the voltage multiplication. The smallest diodes present the highest R_r and R_p, this is the lowest power losses.

Additionally, C_D and C_p affect negatively the voltage multiplication as their "steal" charge from the rectifier capacitors. Consequently, low C_D and C_p, i.e., small diodes, are highly desirable.

5.2.2 Integrated capacitors

The equivalent circuit of an integrated capacitor is shown in Figure 5.7.a.

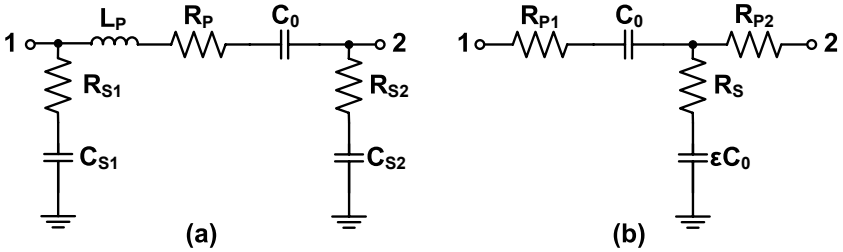

Figure 5.7: RF–model of an integrated capacitor, (a) general model, (b) simplified model for an integrated parallel plate capacitor.

Where C_0 is the ideal capacitance between terminals 1 and 2, L_P and R_P are the parasitic series inductance and series resistance, respectively. The sources of R_P are finite

sheets resistance of the capacitor plate material, contacts and vias. These elements are common of any physical capacitors integrated or discrete. The remaining elements are specific of integrated capacitors and comprise substrate resistances (R_{S1} and R_{S2}) and substrate capacitance (C_{S1} and C_{S2}). These elements arise because of the proximity of the chip substrate, which acts like a ground plane.

In general, the integrated capacitor is an asymmetric device. The most common capacitor type, the parallel plate structure, is strongly asymmetric since the top late is shielded from the substrate by the bottom plate. Thus, if terminal 1 is taken to be the top plate terminal, $R_{S1} \approx 0$ and $C_{S1} \approx 0$. Since the selected process only allows parallel plate capacitors, the model of Figure 5.7.a can be simplified to that of Figure 5.7.b. Notice that C_{S2} has been relabeled as ϵC_0 to empathize that the parasitic capacitor is proportional to C_0 with a process dependent Bottom Plate Coefficient (ϵ). The bottom plate coefficient is approximately given by

$$\epsilon = \frac{x_{top}}{x_{sub}} \tag{5.4}$$

where, x_{top} and x_{sub} are the vertical distances of the bottom plate from the top plate and the substrate, respectively. Hence:

$$C_0 = \frac{\epsilon_0 \epsilon_r A}{x_{top}} \epsilon C_0 = \frac{\epsilon_0 \epsilon_r A}{x_{sub}} \tag{5.5}$$

where, A is the area of the plates, ϵ_0 is the permittivity of the free space and ϵ_r is the dielectric constant of the inter–plate dielectric. Additionally, at frequencies and capacitor sizes of interest, L_P is usually negligible and has been removed. Finally, the parasitic resistance has been split into two resistances, which model the parasitic resistance introduced by each plate that forms the capacitor.

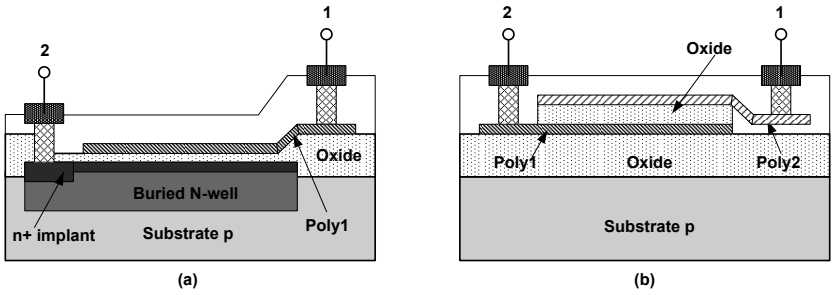

Figure 5.8: Cross section for the capacitors available on the technology process, (a) polysilicon on diffusion capacitor ($Cpod$), (b) polysilicon to polysilicon capacitor (Cpp).

Two types of capacitor structure are available in the process, polysilicon to diffusion capacitors ($Cpod$) and polysilicon to polysilicon (Cpp) capacitors. The cross section of these structures are shown in Figure 5.8. $Cpod$, depicted in Figure 5.8.a, presents a high capacitance density (4.24fF/μm^2). The bottom plate is a buried n+ diffusion region and the top plate is polysilicon, the oxide thickness is the same as the gate oxide thickness in the MOSFETs. $Cpod$ has the disadvantage that its bottom plate is in contact with the substrate, resulting in a large parasitic pn junction capacitance. Figure 5.8.b shows the other alternative, formed by two polysilicon plates. Since this capacitor is placed on top of the thick–field oxide, parasitic effects are kept to a minimum. However, the

Table 5.2: $Cpod$ AND Cpp SHEET RESISTANCES

	Top plate	Bottom plate
C_{pod}	Poly1 $R_s = 3.2\Omega/\square$	n+ implant$R_s = 500\Omega/\square$
C_{pp}	Poly2 $R_s = 100\Omega/\square$	Poly1 $R_s = 3.2\Omega/\square$

oxide between plates is considerably thicker than in $Cpod$ resulting a lower capacitance density (0.85fF/μm^2).

From the point of view of parasitic capacitance $Cpod$ offers better performance, since for the same C_O requires 5 times less area than Cpp. However, there are other aspects that must be considered, namely sheet series resistance and voltage linearity coefficent.

The sheet resistance of the capacitor plates increases the parasitic series resistances Rp lowering the capacitor Q. Table 5.2 shows the $Cpod$ and Cpp sheet resistances.

Strategies for lowering R_P and improve the Q of parallel plate capacitors rely on using low resistance layers (typically interconnect metallization) as equipotentials. Such layers are used to break up the parallel plates into smaller section, thereby, reducing current flow lengths in the higher resistance plate material (and thus R_P). Here again, the bottom plate is more of a concern. This is because while the top plate can be completely covered with metal, the bottom plate cannot be. Another point to note is that any resistance lowering strategy increases the area of the bottom plate (due to wiring and contact overheads), effectively increasing ϵ.

The last feature that differs $Cpod$ from Cpp is the capacitance voltage linearity coefficient. This coefficient describes how the capacitance changes as a function of the applied voltage on its terminals. The voltage linearity coefficient of Poly–Poly capacitors is considerably lower than the one of $Cpod$ capacitors. In other words, the capacitance of Cpp is more stable against voltage changes on its terminals. The reason is that the depletion regions of the oxide–diffusion interface (bottom plate of $Cpod$ capacitors) changes with the applied voltage more abruptly than in the polysilicon bottom plate of Cpp capacitors.

5.2.3 Designing a rectifier

A rectifier arrange is defined using three variables: Schottky diode sizes, capacitors sizes and number of stages (N).

The optimal rectifier is defined as the one that fulfills the specifications discussed in (4.5.2) using the less amount of input power:

- V_{DC} $(R_{load} = 90\ k\Omega)$ $=$ $2.35\ V$
- $Q < 9$

At this point, introducing the efficiency of the rectifier is as follows:

$$\eta = \frac{P_{DC}}{P_{in}} \tag{5.6}$$

where, P_{in} is the power dissipated in the complete passive RFID sensor and P_{DC} is the power dissipated at the output of the rectifier. Maximizing η is the main issue in the design of rectifiers.

Steps to design a rectifier (see Figure 5.9) are the following. First, power requirements are specified and technology is selected. Second, the diode size is minimized in order to maximize R_p and R_r and to reduce C_D. Next, the capacitor with the lowest power losses and parasitic elements is selected and dimensioned according to the diode size. Finally, the one–stage rectifier is cascaded to achieve the desired V_{DC}.

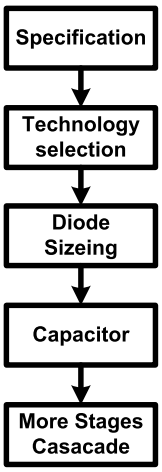

Figure 5.9: Steps to design a rectifier.

Diode size

A one–stage rectifier is depicted in Figure 5.10. It is compose of a series capacitors C_s, parallel capacitors C_p and diodes with its parasitic capacitance (C_D). The former is in the way of the RF signal; therefore, its parasitic capacitance and resistance is critical. On the other hand, C_p is parallel to the DC output and its bottom plate is connected to GND, that means that the parasitic capacitance is short–circuited. Therefore, the parasitic of C_p can be neglected.

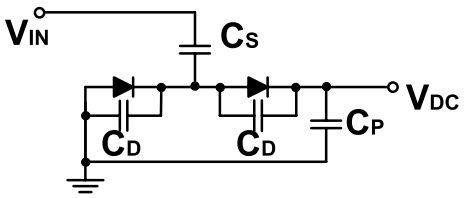

Figure 5.10: One–Stage rectifier, diode diffusion capacitance (C_D) is included.

Two design considerations very useful to dimension C_s and C_p are extracted from Figure 5.10:

- The time constant (τ_c) of the rectifier capacitors must be very much higher than the period of the input signal ($\tau_c >> 1/f$). Because the capacitors have to keep

the charge from one cycle to the other of the input signal. τ_c is calculated as $\tau_c = RC_{s,p}$ where R is the resistance that discharge the capacitor. In the rectifier R is calculated from:

$$R = \frac{V_{cap}}{I_L + I_r + I_{par}} \tag{5.7}$$

where, V_{cap} is the DC voltage on the capacitors, I_L is the output current of the rectifier, I_r is the diode reverse current ($I_r = \frac{V_d}{R_r}$) and I_{par} is the DC current that flows though the diode parasitic resistance to substrate ($I_{par} = \frac{V_{cathode}}{R_{par}}$). Notice that R_r and R_{par} are diode parameters that depend on its size. As a result, diodes and capacitors have to be dimensioned together. This is, big diodes with low R_r and R_{par} will require high capacitance to maintain the charge.

- Diode diffusion capacitance (C_D) must be very much lower than rectifier capacitors ($C_D << C_{p,s}$). Since both pair of capacitors forms a voltage divider, the voltage drop on C_D must be minimized as it does not contribute to the voltage multiplication.

Both considerations lead to a minimization of diode size, in order to maximize R_r and, R_{par} and to reduce C_D. The drawbacks of reducing diode size is higher diode V_{th} and therefore, lower V_{DC}. The solution to this problem is to increase the stage number. As a conclusion, the lower diode size is the most power efficient election.

Capacitor size

In the ideal rectifier, the voltage on the diodes for a steady state is: $(V_p - V_{th}) + sin(2\pi f)$. This is the input signal plus a DC offset (see Figure 5.11). As result, once the steady state condition is reached, the diode is mostly off. Notice that the capacitor has to be large enough to maintain the charge between successive signal cycles. In other words, R_r should not discharge the capacitors.

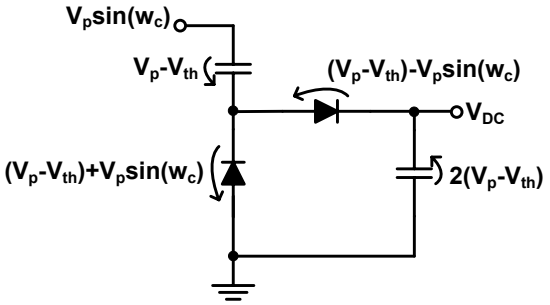

Figure 5.11: Voltages on the diodes and capacitors of the rectifier at steady state.

Capacitors are dimensioned considering R_r. The diode size is the minimum allowed by the technology (see $D3$ in Table 5.1), this is, $R_r = 91k\Omega$. With this value, the minimum capacitance required to maintain the 99% of the charge on the capacitor can be calculated from the equation of the capacitor discharge:

$$V(t) = V_0 e^{-\frac{t}{R_r C}} \tag{5.8}$$

where, V_0 is the initial voltage on the capacitor, R is the resistance that discharge the capacitor and C is the capacitance. Hence the minimum capacitance is:

$$C \frac{\tau}{0.01R_r} \approx 1.26pF \tag{5.9}$$

where τ is the half of the period: $(\frac{1}{2f})$. Notice that bigger capacitors would be discharged slower which would be apparently better for the rectifier performance. However, the area of the capacitor is directly proportional to the parasitic capacitance. The parasitic of C_p does not affect the efficiency of the rectifier, since one of its terminals is shorted to ground. This capacitor is sized over the calculated minimum capacitance just increasing the percent of the charge to be maintained by the capacitor in Equation 5.9.

On the other side, low capacitance linearity coefficient is highly desirable to reduce the effects of the substrate noise. As mentioned before, the capacitor linearity is considerably lower in Cpp two orders of magnitude lower than $Cpod$ in the technology process. Thus, C_P must be implemented with Cpp to isolate, as much as possible, the effect of the substrate noise on the rectifier performance.

From the point of view of the parasitic capacitance, the best choice is $Cpod$, as deduced in Section 5.2.2. However, looking into the parasitic resistance, the balance declines clearly to Cpp. The parasitic series resistance introduced by the C_s in the signal path reduces the voltage swing on the diodes resulting a reduction in the voltage multiplication as can be seen in Figure 5.12.

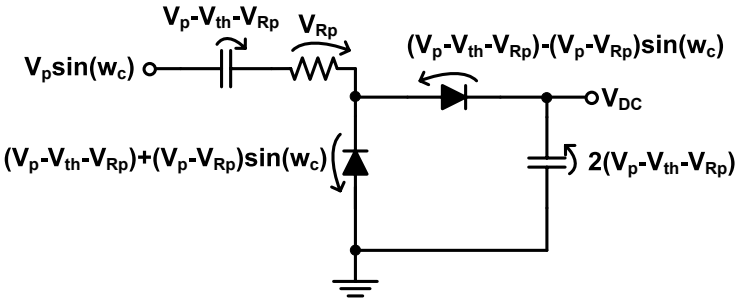

Figure 5.12: Voltages on the diodes and capacitors of the rectifier at steady state considering the parasitic series resistance (R_p) of C_s.

R_p is critical as it reduces both the DC charge on the capacitors and the AC amplitude on the diodes. Moreover, its effect is multiplied with the stage number. As a conclusion, R_p must be reduced at its minimum in rectifier design. The first way ro reduce R_p is by proper selection of the capacitor type.The R_P of $Cpod$ capacitors is two orders of magnitude higher than for the case of Cpp capacitors (see Table 5.2). Therefore, V_{Rp} is considerably higher in $Cpod$. For this reason, Cpp capacitors are preferable in the rectifier implementation. Additionally, there are layout techniques to reduce the series resistance that must be considered in the capacitor implementation, as ringing the capacitor with contacts to the lower plate [106].

Once the best capacitor type have been chosen, the remaining issue regarding is to determine the optimal way to connect the capacitors.

- C_P. The way to eliminate the parasitic effects is to connect the bottom plate to ground and the top plate to V_{DC}.

- C_S. Two possible connections of C_s are depicted in Figure 5.13. If the top plate of C_s is connected to V_{in}(Figure 5.13.a), then the parasitic capacitance of C_s is added to the parasitic capacitance of the diode (C_D). This reduces the voltage swing on the diodes and consequently the multiplication factor. The other alternative is to connect the bottom plate of C_s to V_{in} (Figure 5.13.a). In this configuration the parasitic capacitance does not have any effect on the voltage multiplication but the imaginary part of Z_{in} and consequently Q is reduced.

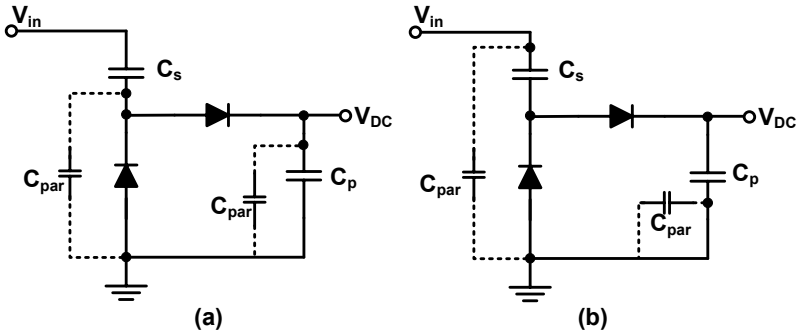

Figure 5.13: Capacitor connection possibilities, (a) top plate to V_{in} and (b) bottom plate to V_{in}.

Number of stages

Stage number (N) affects the rectifier performance in the following ways:

1. Increase of the ratio $\frac{V_{DC}}{V_{in}}$. Since more diodes are involved in the multiplication, less V_{in} is required to obtain the required V_{DC}.

2. Rectifier efficiency falls. Although the required V_{in} for a given V_{DC} decreases when N rises, does not the required AC input current. As the number of devices is scaled up, the same do the power losses due the parasitic elements. The parasitic resistances introduced by the diodes are especially critical as they multiply the rectifier DC current consumption by N.

3. Reduction of Q of the input impedance. The parasitic capacitance introduced by the series capacitor rises with the stage number. The consequence, a reduction of the imaginary part of the input impedance. As a result, Q (defined as the ratio $\frac{|X_s|}{R_s}$) will fall with the stage number.

5.3 Rectifier mathematical model

This section introduces a novel mathematical model for the Rectifier. The goal of this model is to describe the behavior of the rectifier in terms of input impedance and input voltage as a function of the process, components, stage number and power requirements. In the next section, the mathematical model is compared with simulations and measurements.

5.3.1 Input impedance of one stage recitifier

The series input impedance of the rectifier fix the input impedance of the RFID sensor. Its estimation is of great importance to design the antenna. The Z_{in} has a capacitive imaginary part and a real part. As already mentioned, the ratio $\frac{Im(Z_{in})}{Re(Z_{in})}$ defines the Q of the chip. At resonance, Z_{in} can be expressed with its parallel equivalent, that gives a more graphical idea of which elements affect more in the real part or in the imaginary part of the input impedance, see Figure 5.14. The imaginary part is almost the same in parallel and in series, since high Q is desirable ($Im(Z_{in}) >> Re(Z_{in})$). The series–parallel equivalence is only valid for a unique frequency. However in this work, the impedance calculations are valid for the complete bandwidth of the system. Expressions to express parallel elements as a function of series elements and vice versa are easily deduced from the equality:

$$Rs + jX_s = R_p//jXp \tag{5.10}$$

R_p models the active power dissipated by the complete RFID sensor. This power is

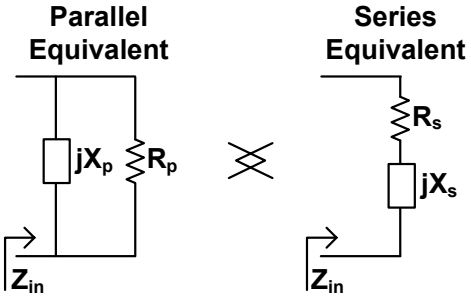

Figure 5.14: Series and parallel equivalent of Z_{in} at resonance.

dissipated in the load, in the internal resistances of the diodes and in the parasitic resistance of the capacitors.

Imaginary part

The parallel equivalent imaginary part of the rectifier (X_p) can be deduced from Figure 5.15 where all the capacitors included in the rectifier are represented.

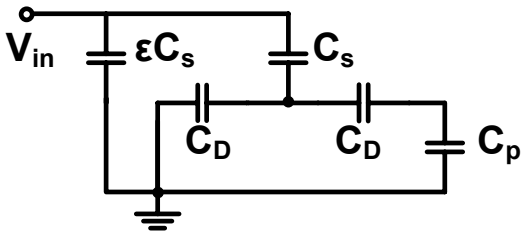

Figure 5.15: Elements at the input of the rectifier that contribute to the imaginary part of Z_{in}.

Thus, X_p can be expressed as:
$-jX_p = \frac{1}{jw\epsilon C_s}||(\frac{1}{jwC_s} + (\frac{1}{jwC_D}||(\frac{1}{jwC_D} + \frac{1}{jwC_p})))$

The diode area must be minimize in order to reduce diode parasitic capacitance(C_D), whose value is under 10fF. On the other side, C_P and C_S are in the order of the picofarads. Therefore, it can be assumed that $C_s, C_p >> C_D$ to simplify the expression of X_p as follows:

$$X_p = \frac{1}{w(\epsilon C_s + 2C_D)} \tag{5.11}$$

Usually, $\epsilon C_s >> C_D$, consequently, the expression to deduce X_p can be simplified to:

$$X_p = \frac{1}{w\epsilon C_s} \tag{5.12}$$

The parasitic capacitance included by the output pad changes, considerably, the imaginary input impedance of the rectifier, as it places a capacitor parallel to ground at the input of the rectifier. The value of the parasitic capacitance included by the pad is estimated using extraction tools. Its values swings between 70 to 300fF depending on pad dimensions, geometry and materials. Thus:

$$X_p = \frac{1}{w(\epsilon C_s + C_{pad})} \tag{5.13}$$

Real part

The estimation of the Real part of the input impedance of the rectifier is not as straightforward as the imaginary. The real part of the input impedance is related with the average active power dissipated in the transponder at resonance as follows:

$$P_{in} = \frac{1}{2} I_p^2 R_S \tag{5.14}$$

It is clear that when power consumption increases, R_S does the same. The power dissipated in the chip is splited into: power dissipated in the rectifier and power dissipated on the rest of the sub–circuits of the chip. The last one can be modeled either as a resistance or as a DC current source at the output of the rectifier. V_{DC} is related with V_{in} through Equation 5.1. Hence, the power consumption and consequently R_S rise with V_{in}. Notice that there is a self–regulating effect on this, since when R_S rises Q falls, consequently, V_{in} goes down as

$$V_{in} = V_{ant}(1 + Q) \tag{5.15}$$

neglecting the parasitic resistance of the capacitors and assuming that for AC considerations both diodes are parallel to ground, then diodes are, through its series resistance (R_D), the unique devices that dissipate power in the rectifier. As a result, from the point of view of the AC input signal, R_{in} is the parallel of the two R_D (see Figure 5.16). Notice that R_D is the average series resistance of a diode during a cycle of V_{in}.

$$R_p = R_D // R_D = 0.5 R_D \tag{5.16}$$

Schottky diode is modeled as a series resistance that changes its value depending on its polarization, between R_r and R_f where $R_r >> R_f$ (see Figure 5.6). When the steady state is reached the charge lost through the reverse. Parasitic and load currents is

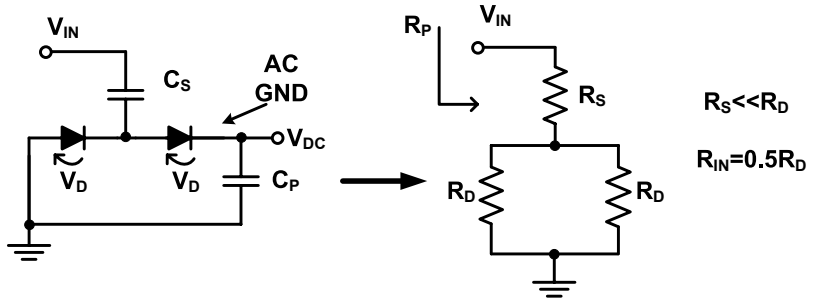

Figure 5.16: Rectifier equivalent circuit to calculate the real part of Z_{in}.

recharged by the diodes forward current. The input parallel equivalent R_p of the rectifier is calculated from the average current consumed in one cycle as follows.

First, the reverse current consumed by the diodes when they are off is:

$$I_r = \frac{V_D}{R_r} \tag{5.17}$$

where V_D is the DC voltage on the diodes. It is clear, observing Figure 5.16, that the sum of the DC voltage dropping in each diode is equal to V_{DC}. And as all the diodes are identical, V_D is the same in all diodes. From this statement can be extracted a very useful relation:

$$V_D = \frac{V_{DC}}{N} \tag{5.18}$$

where N is the diodes number of the rectifier. In the particular case of one stage rectifier $N = 2$.

Second the current consumed in the load is as follows:

$$I_L = \frac{V_{DC}}{R_L} \tag{5.19}$$

As the current consumed in the load has to be recharged by each diode, the average diode resistance is:

$$R_D = \frac{V_D}{(I_L + I_r)} \tag{5.20}$$

For a more accurate estimation of R_p additional points must be taken into account. First, the current that flows through the diode parasitic resistance to substrate (I_{par}) has not been considered. That is acceptable in the diode whose cathode is connected to AC GND (see Figure 5.16) but not in the other one. Second, it has been assumed that current flows through R_r during all the period, which is not true as when the diode is on, the diode resistance changes to R_f and the current flows in opposite direction. Hence, the effective R_{reff} in a period is:

$$R_{reff} = \frac{T}{t_{off}} R_r, \quad T = t_{off} + t_{on} \tag{5.21}$$

T is the period of the input signal, and t_{off} and t_{on} are the times where the diode are off and on, respectively.

The R_D of even diodes is

$$R_{De} = \frac{V_D}{I_L + I_r} \tag{5.22}$$

and the R_D of odd diodes is

$$R_{Do} = \frac{V_D}{I_L + I_r + I_par} \tag{5.23}$$

Hence, expressing V_D as a function of V_{DC} for a one stage rectifier:

$$R_p = R_{De} \| R_{Do} = \frac{\frac{V_{DC}}{2}}{\frac{V_{DC}}{R_L} + \frac{V_{DC}}{2R_r} + \frac{V_{DC}}{2R_{par}}} \| \frac{\frac{V_{DC}}{2}}{\frac{V_{DC}}{R_L} + \frac{V_{DC}}{2R_r}} = \frac{1}{\frac{2}{R_L} + \frac{1}{R_r} + \frac{1}{R_{par}}} \| \frac{1}{\frac{2}{R_L} + \frac{1}{R_{reff}}} \tag{5.24}$$

$$R_p = \frac{R_L}{2 \cdot 2} \| \frac{R_{reff}}{2} \| R_{par} \tag{5.25}$$

When the current consumption of the RFID sensor is modelled as a current source, the influence of V_{in} on R_p is slightly, only due to R_{reff}. I_L does not rise with V_{DC}. As a result, I_L current through each diode remain constant with V_{in}. The current through R_{reff} and R_{par} rises with the voltage on the diodes $V_D = \frac{V_{DC}}{N}$.

On the other side, if the RFID sensor current consumption is modelled as a Resistance then $I_L = \frac{V_{DC}}{R_L}$. It is already known that $V_{DC} = f(V_{in})$. Hence, from Equation 5.24 can be concluded that $R_p = f(\frac{1}{V_{in}})$. In other words, R_p is a decreasing function of V_{in}.

Input impedance of several stages

The rectifier basic structure (see Figure 5.10) must be cascaded to achieve DC voltage higher than $2(V_{in} - V_{th})$. For a given V_{in}, it is clear from Equation 5.1 that when stage number rises the same does V_{DC}.

In the same way, the cascading of several stages will also vary the input impedance of the rectifier. Z_{in} is calculated cascading the results obtained for one stage rectifier. Thus, the parallel equivalent imaginary part is:

$$X_p = \frac{X_{p\ 1st}}{\frac{N}{2}} = \frac{1}{w(C_{pad} + \frac{N}{2}(\epsilon C_s + 2C_D))} \tag{5.26}$$

where N is the number of diodes. And the parallel equivalent of the real part of Z_{in} is:

$$R_p = \frac{R_L}{N^2} \| \frac{R_{reff}}{N} \| \frac{R_{par}}{\frac{N}{2}} \tag{5.27}$$

where $R_L = \frac{V_{DC}}{I_L}$ if the load is modelled as a current source.

5.3.2 Calculus of V_{in}

This subsection analyzes and proposes a more accurate expression to calculate V_{DC} from V_{in}. This expression take into account the load at the output of the rectifier.

Figure 5.17 shows graphically the current that flows through a diode during a period. The striped surface represents the current that discharge the capacitor, and the doted surface the current that recharge the capacitor. The area of the two surfaces is the same when the steady state is reached.

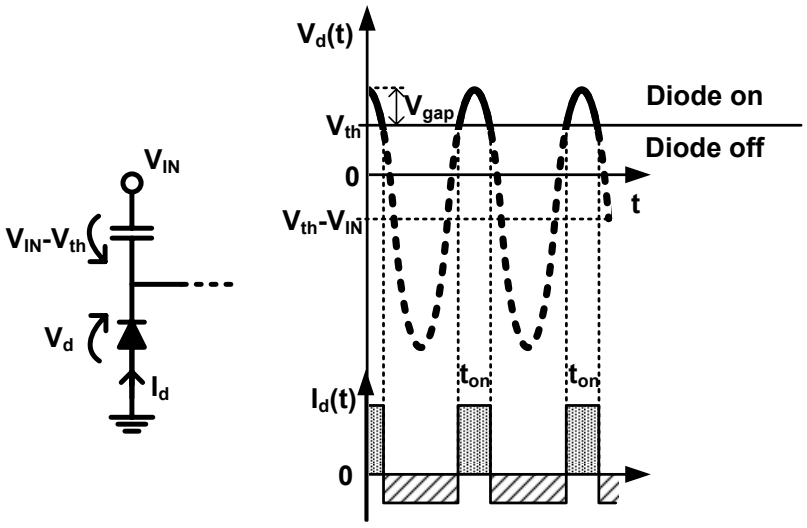

Figure 5.17: Current that flows through a diode during a period of V_{in}.

To calculate t_{on} a new magnitude V_{gap} is introduced, which is defined as the voltage drop on the diodes over the V_{th} necessary to draw towards the capacitor the current consumed by the rectifier and in the load (see Figure 5.17). To deduce t_{on}, the first diode of the rectifier will be studied. By observing Figure 5.17, it is clear that the voltage V_D of all diodes is the same.

V_{gap} reduces the DC voltage on the capacitors, as the voltage required to polarize the diodes will not be used to charge the capacitors. Consequently, the equation to calculate V_{DC} is rewritten as:

$$V_{DC} = N(V_{in} - V_{th} - V_{gap}) \tag{5.28}$$

This equation gives more accurate value of V_{DC} since the effect of the load at the output of the rectifier is included. To complete the model, V_{gap} has to be rewritten as a function of I_L.

The voltage on the diode, see Figure 5.17, is:

$$V_{in}cos(wt) - \frac{V_{DC}}{N} \tag{5.29}$$

Hence $\frac{t_{on}}{2}$ is obtained working out the value of the following equation:

$$V_{in}cos(w\frac{t_{on}}{2}) - \frac{V_{DC}}{N} - V_{th} = 0 \Rightarrow \frac{t_{on}}{2} = \frac{1}{w}arcsin(\frac{V_{DC}}{NV_{in}}) \tag{5.30}$$

Substituting V_{in}, hence

$$\frac{t_{on}}{2} = \frac{1}{w}arcsin(\frac{Vout}{N(\frac{V_{DC}}{N} + V_{th} + V_{gap})}) \tag{5.31}$$

Equation 5.31 gives a relation between t_{on} and V_{gap} but there is not relation with the current that deliver the rectifier (I_L). This relation is obtained from the fact that in steady state the current consumed by each diode $(I_r + I_p)$ plus I_L is recharged by the diode in each cycle of V_{in}. In other words, the average current through each diode in a period satisfies next equation:

$$I_f = I_r + I_p + I_L \tag{5.32}$$

Hence integrating in a period of V_{in} the Equation 5.32

$$\frac{1}{T}\int_0^T I_f(t)\,dt = \frac{1}{T}\int_0^T [I_r(t) + I_p(t) + I_L(t)]\,dt \tag{5.33}$$

$$\frac{1}{TR_f}\int_{-\frac{t_{on}}{2}}^{\frac{t_{on}}{2}} [V_{in}cos(wt) - \frac{V_{DC}}{N} - V_{th}]\,dt = \frac{1}{T}\left(\int_0^{T-t_{on}} \frac{V_{DC}}{R_r}\,dt + \int_0^T (\frac{V_{DC}}{R_p} + \frac{V_{DC}}{R_L})\,dt\right) \tag{5.34}$$

Solving the integral and using R_{reff} results

$$\frac{1}{TR_f}(\frac{2V_{in}}{w}sen(w\frac{t_{on}}{2}) - (\frac{V_{DC}}{N} - V_{th})t_{on}) = \frac{V_{DC}}{N}(R_{par}\|R_{reff}\|\frac{R_L}{N}) \tag{5.35}$$

Substituting Equation 5.28 and Equation 5.31 in Equation 5.35, V_{gap} is expressed as a function of V_{DC}, N, V_{th}, R_f, R_r, R_{par} and R_L, which are all the design parameters.

Once V_{gap} is known, V_{in} is directly obtained from Equation 5.28.

$$V_{in} = \frac{V_{DC}}{N} + V_{th} + V_{gap} \tag{5.36}$$

To conclude with the model, the effect of the parasitic resistance of the C_s has to be included. The parasitic resistance of C_s and R_p form a voltage divider that multiplies the input voltage for the factor $\frac{R_p}{R_s+R_p}$. The resulting V_{in} is:

$$V_{in} = \frac{R_p}{R_s + R_p}(\frac{V_{DC}}{N} + V_{th} + V_{gap}) \tag{5.37}$$

The parasitic resistance of C_s is especially critical when R_p is low, i.e., when the current consumption of the rectifier and its load is high.

η and Q

Once the expressions to calculate Z_{in} and V_{in} have been obtained, the rest of characteristics that define the performance of a rectifier can be easily deduced. On one hand, the quality factor of the input impedance Q is obtained immediately

$$Q = \frac{|X_s|}{R_s} \tag{5.38}$$

On the other hand the rectifier efficiency is calculated as:

$$\eta = \frac{P_{DC}}{P_{in}} = \frac{\frac{V_{DC}^2}{R_L}}{\frac{V_{in}^2}{R_p}} \tag{5.39}$$

These two expressions 5.39 and 5.38 together with the ones for Z_{in} and V_{in}, describe absolutely the performance of a rectifier. Now, programming the equations and assigning values to the design parameters (diode– capacitor–size and stage number) can be found the optimal rectifier arrange for a given load conditions (V_{DC}, and R_L or I_L).

5.4 Results

The described design consideration regarding to the rectifier performance are proved, firstly, through simulations, and secondly, through measurements.

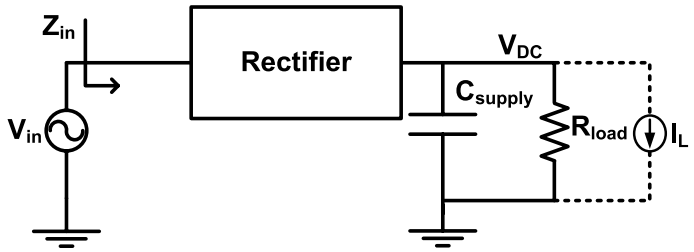

Figure 5.18: Simulation setup for rectifier characterization.

Figure 7.16 shows the simulation set up used to simulate the rectifier. The rectifier output is loaded with C_{supply} and R_L, these two elements model the supply capacitor and the DC chip current consumption, respectively. For some simulations a DC current source, implemented with a current mirror, a resistance and a DC voltage source has been used. The IC pad capacitance has not been included in the simulations as the aim is to study the rectifier characteristics. At 868MHz, a sinusoidal voltage source models the input signal. The amplitude of the input signal has been varied to evaluate the performance of the rectifier in terms of input impedance, input power, output DC voltage and efficiency.

5.4.1 Diode size

Three different implementations, varying the diode size, of a two stage rectifier have been simulated. The capacitors were dimensioned according to the Equation 5.9 for each particular diode size. All the implementations were loaded with a $R_L = 90k\Omega$. Figure 5.19 depicts the efficiency and R_p versus diode area of each implementation. They were simulated having $V_{DC} = 2.5V$. As already mentioned, the R_p is related directly with the active power consumption of the rectifier and load. The higher R_p the lower is the power consumptions. From Figure 5.19 is concluded that the rectifier with the lowest consumption and, therefore, the most efficient is the one implemented with the smallest diodes. This conclusion agrees the predictions of Section 5.2.1. From here on, diodes with area 8.4 μm^2 will be used.

5.4.2 Capacitor type

In Section 5.2.2, it was discussed what kind of capacitors is the best choice, either poly- poly(Vpp) or poly on diffusion($Cpod$) capacitors. After a theoretical analysis, was concluded that Cpp offers the best characteristics for the rectifier implementation, due to its lower parasitic resistance and lower voltage linearity. Figure 5.20 illustrates the input series impedance of two-stages rectifier under the same load conditions implemented using Cpp and $Cpod$ capacitors respectively. The equivalent parallel resistance of the rectifier implemented with $Cpod$ capacitors is clearly lower. The reason is that the parasitic resistance of $Cpod$ capacitors, which rises to 400 $\Omega/\square$ (around 100 times higher

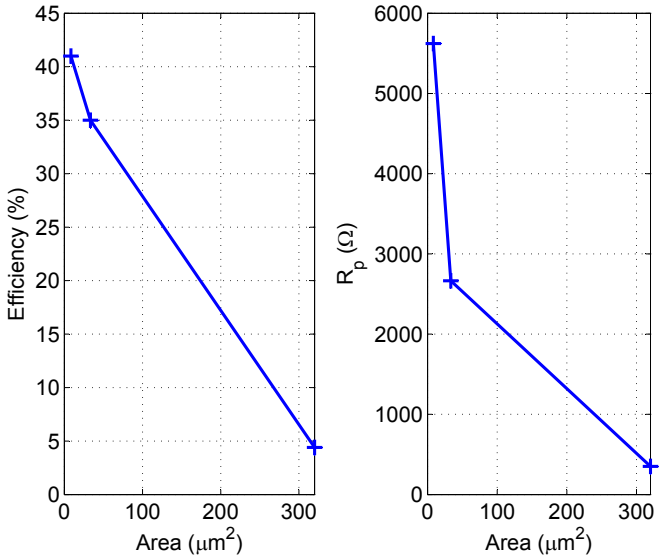

Figure 5.19: Efficiency and equivalent parallel resistance (R_p) versus diode area of a two stage rectifier loaded with $R_L = 90k\Omega$ and V_{DC}=2.5 V.

Table 5.3: Different ways to connect the poly–poly capacitors.

Terminal	aa	ab	ba	bb
to V_{in} (C_s)	Poly2	Poly2	Poly1	Poly1
to V_{DC} (C_p)	Poly2	Poly1	Poly2	Poly1

than for the case of Cpp), dissipates a considerably amount of active input power. The consequence is a efficiency reduction of the rectifier implemented with $Cpod$ capacitors.

Notice that the module of the imaginary part of the input impedance is higher in the case of $Cpod$, because the parasitic capacitance for the same capacity is lower in $Cpod$, as they are high density capacitors and requires less area than Cpp to reach a certain capacitance. However, this advantage of $Cpod$ over Cpp capacitors is not sufficient to select the $Cpod$ capacitor.

5.4.3 Capacitor orientation

Cpp capacitors are non–symmetric, two–terminal devices. Depending on the way the capacitor is connected its behaviour changes. As rectifier makes use of two capacitors under different voltage conditions, there are four combinations to connect the capacitors:

Observing Figure 5.21 some conclusions are follows. First, the orientation of C_p does not influence in the behaviour of rectifier. The reason is that its terminals are under a DC voltage and the parasitic capacitance to substrate can be neglected. And second, both the V_{DC} and the efficiency are higher when the bottom plate of C_s is connected to V_{in}. In this case the parasitic capacitance of the bottom plate has to be taken into account.

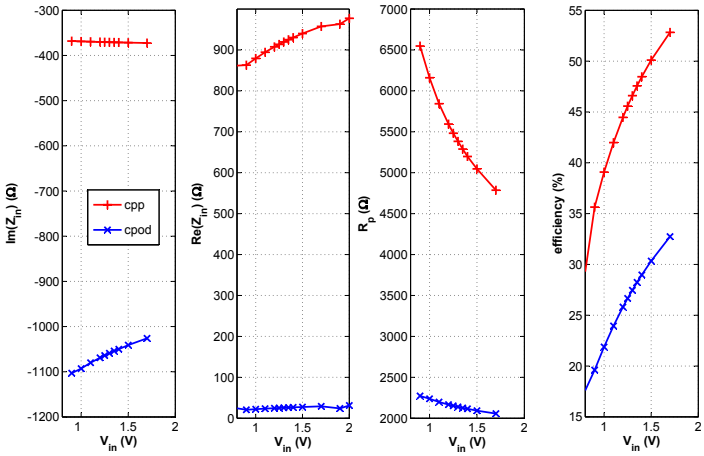

Figure 5.20: Input series impedance (Z_{in}), equivalent parallel resistance and efficiency versus V_{in} of a two stage rectifier loaded with $R_L = 90k\Omega$ and V_{DC}=2.5 V.

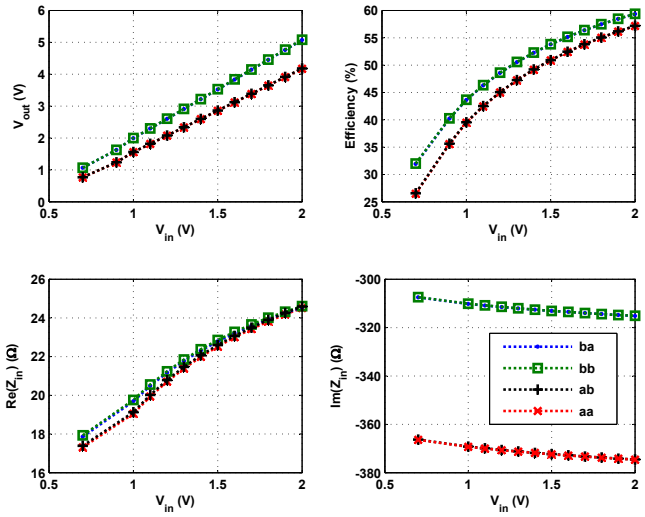

Figure 5.21: V_{DC}, Efficiency and Z_{in} versus V_{in} varying the way to connect the capacitors of a two stage rectifier loaded with $R_L = 90k\Omega$ and V_{DC}=2.5 V.

The C_s parasitic capacitor is summed with the parasitic capacitor of the diodes (C_D) when it is connected to the diodes and; the effect of the voltage divider formed between C_D and C_s increases, reducing the voltage swing on the diodes and consequently V_{DC}.

Notice in Figure 5.21 that, from the point of view of the input impedance, the combinations aa and ab present a higher Q as there are less parasitic capacitances between input and substrate. However, the combinations ba or bb are preferred as the efficiency is maximized.

5.4.4 Capacitor size

Equation 5.9 gives the capacitor size as a function of diode size and the percent of capacitor discharge in a period. The bigger capacitors are the fewer is the discharge and, consequently, higher V_{DC} is reached for a given V_{in}. However, a big C_s introduces parasitic capacitance to substrate that reduces the equivalent R_p of the rectifier. Figure 5.22 shows the behaviour of the input impedance when ϵC_s varies. On the other hand, in the limit case where $\epsilon C_s = 0$ then the input capacitance is only due to the C_D, and $R_s \approx R_p$ calculated from Equation 5.27. In the limit case, however, C_s is so small that it can not maintain charge from one cycle to the other and there is not voltage multiplication.

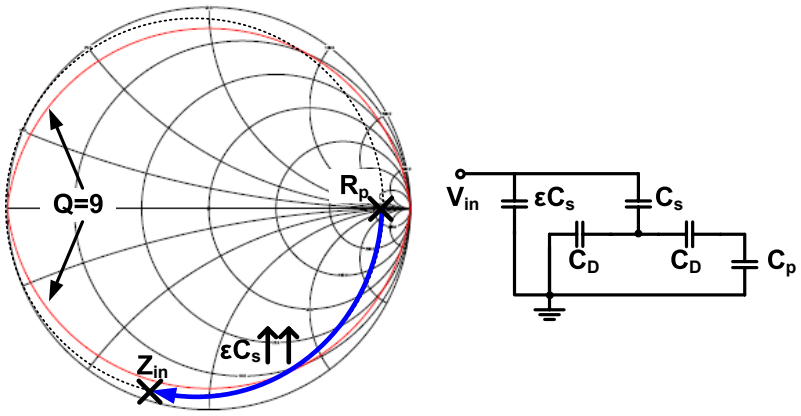

Figure 5.22: Change in the rectifier input impedance when the pad parasitic capacitance in included.

To summarize, P_{in} depends on R_p and V_{in} depends on Q, when ϵC_s rises R_p falls and Q increases. Thus, one effect counteracts the other and, consequently, the relation P_{in} versus V_{DC} is independent of the capacitor size. Figure 5.23 shows the behaviour of Q and R_p and V_{DC} versus P_{in} as a function of capacitor size.

The optimal capacitor size finds a trade–off between Q and the percent of capacitor discharge in a period. In Figure 5.23, the value $C_s = 1.5pF$ calculated from Equation 5.9 finds an interesting trade–off with a relative low $Q = 15$ and 1% capacitor discharge along a cycle. Larger capacitors do not introduces a great improvement in terms of multiplication efficiency, whereas Q increases, dramatically. Notice that the parasitic capacitance introduced by the pad, increases the rectifier Q, especially, if $C_{pad} \approx \epsilon C_s$.

Finally, the size of C_p does not affect the rectifier input impedance, consequently the only design consideration to take into account is the discharge in a cycle.

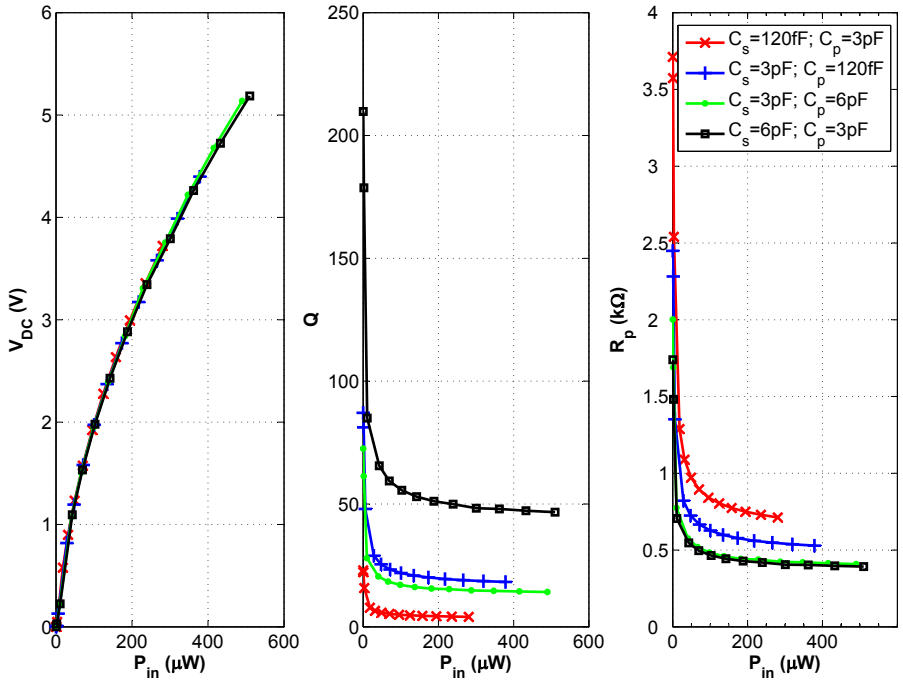

Figure 5.23: V_{DC}, Q and R_P versus P_{in} for diverse capacitors sizes in a two stage rectifier loaded with $R_L = 90k\Omega$.

Summarizing, Q of the input impedance is adjusted varying the size of C_s. Low C_s sizes reduce Q. However, the relation V_{DC} vs V_{in} get worse as the charge is not maintained from one cycle to the other by C_s, and the factor of the voltage multiplication is reduced. Finally, the pad capacitance must be taken into account to calculate Q for low values of C_s.

5.4.5 Stages number

More stages are stacked to obtain a higher V_{DC}, as the expense of a efficiency reduction. Figure 5.24 shows the efficiency and V_{in} required to obtain a certain V_{DC} varying the stage number.

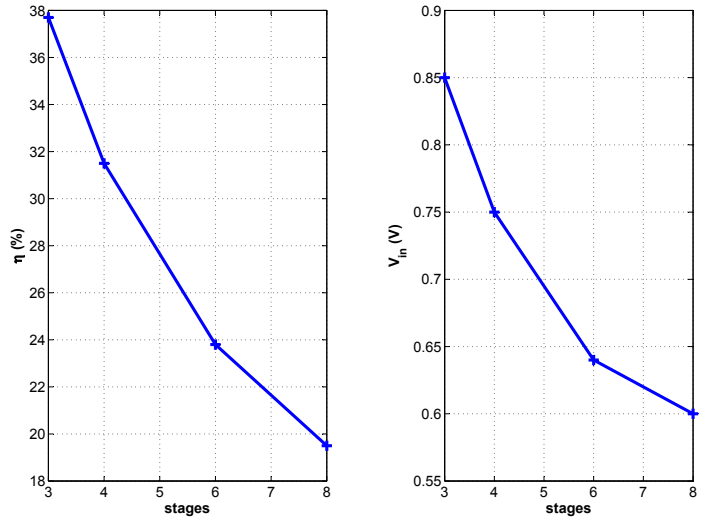

Figure 5.24: Efficiency and V_{in} versus stages for a $V_{DC} = 2V$ and a load of 90 kΩ.

Rectifiers with more stages are less efficient due to losses on the additional components. On the other hand, V_{in} decreases with the stage number, which means that the ratio $\frac{V_{in}}{I_{in}} = Z_{in}$ decreases with the stages. The reduction of Z_{in} has an advantage, Q decreases and the bandwidth of the system increases. Figure 5.25 shows the input impedance and V_{in} versus N for a constant V_{DC}=2 V and a fixed load.

5.4.6 Theoretical V_{in} and Z_{in} versus simulations

In this section, the theoretical functions to calculate Z_{in} and V_{in} deduced in Section 5.3 are compared with the circuit simulations at transistor level using real device models. For this aim different rectifier configurations have been simulated, for different load conditions and V_{in}. After this, Simulations and theoretical results are compared. Figure 5.26 shows graphically V_{in} and Z_{in} versus stage number of rectifiers with different diodes size under the same load conditions. The theoretical result follows clearly the tendency of the simulated ones. And the relative difference of theoretical and simulated results is less than 2% in the imaginary part of Z_{in} and V_{in}, whereas for the case of the real part of Z_{in} is higher.

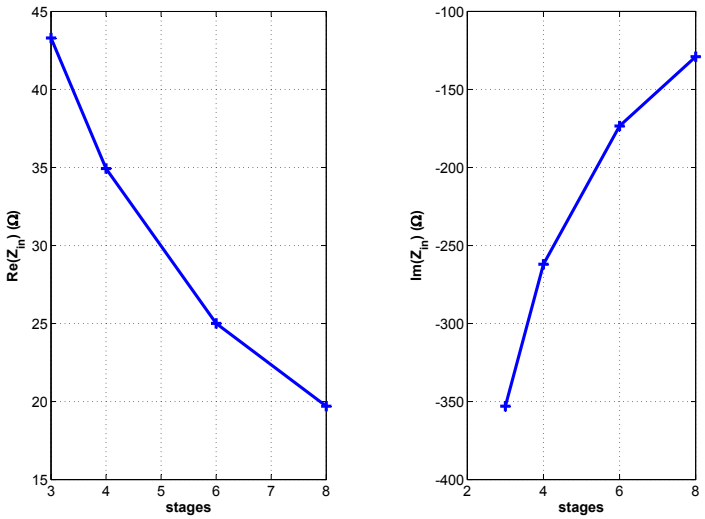

Figure 5.25: Input impedance versus stage number for a $V_{DC} = 2V$ and a load of 90 kΩ.

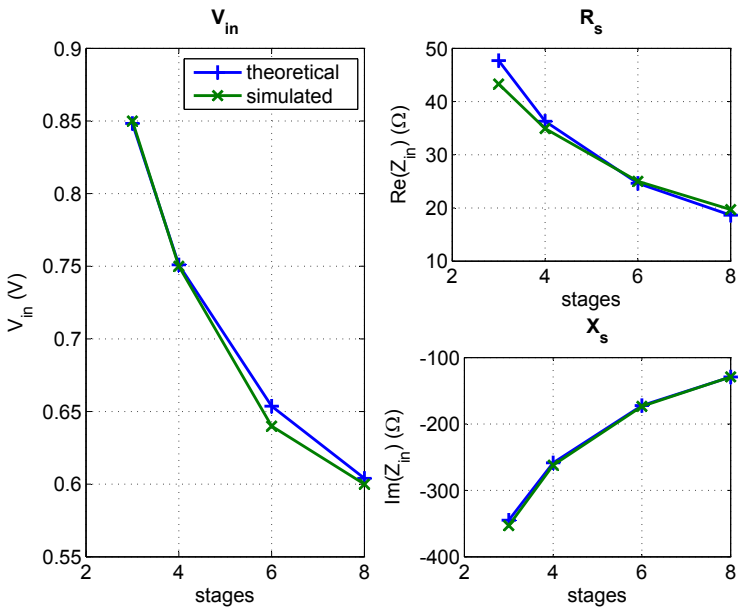

Figure 5.26: Theoretical and simulated input voltage and input impedance versus stage number for a $V_{DC} = 2V$ and a load of 90 kΩ.

Table 5.4: Relative difference between calculated and simulated results of 4 stages rectifiers

Diode Size (pm^2)	Cs (pF)	Err(Re(Z_{in})) (%)	Err(Im(Z_{in})) (%)	Err(V_{in}) (%)
7x1.2	0.76	0.25	1.52	0.80
7x1.2	1.52	7.42	0.61	0.53
7x1.2	3.04	5.90	0.75	0.53
14x2.4	0.76	18.8	0.19	0.80
14x2.4	1.52	8.01	2.22	1.84
14x2.4	3.04	3.12	1.44	4.33
average		7.25	1.12	1.47

Table 5.4 presents the relative difference between the calculated and the simulated results, of different 4 stage rectifiers, varying C_s and diode size. The relative error is specially high for the case of Re(Z_{in}) with an average error of 7.25% for the other two magnitudes, Im(Z_{in}) and V_{in}, the average relative error is 1.12% and 1.47%, respectively. As a conclusion the theoretical formulas to calculate Z_{in} and V_{in} can be used to automatize the rectifier design with considerably reliability.

5.4.7 Automation of rectifier design

Once the theoretical formulas to calculate Z_{in} and V_{in} have been proved. The optimal rectifier configuration for a given technology and specifications can be found out programming the formulas and testing all the possible rectifier configurations. In the case of the wireless sensor, the specifications were introduced in the program to obtain the parameters required to evaluate the rectifier: Z_{in}, P_{in}, efficiency (η). Figure 5.27 shows the effect of increase the diode area, as mentioned, the required input power increases with larger diodes and with the stages. As a conclusion, the smallest diodes are the optimal ones.

Regarding the capacitor size, the best choice for the smallest diodes is a capacity of 760fF and 1pF. In this range the trade off between discharge of the capacitor and parasitic at the input of the rectifier reaches the best results.

5.4.8 Measurements

Rectifiers with 4, 6 and 8 stages has been implemented and measured in the chosen technology (XFAB 0.35μm low power process). The photo of Figure 5.29 shows the complete chip and the rectifiers location.

For the measurement of the rectifier a nail station has been used, the input of the rectifier have been directly connected to the output of the vectorial network analyzer (VNA). At the output of the rectifier a resistance were connected as shows Figure 5.30. The output power of the VNA is varied among -5 and 5 dBm. The Z_{in}, V_{out} and Reflection coefficient have been measured to evaluate each rectifier.

Figure 5.31 depicts measures versus theoretical results of a four stages rectifier. The

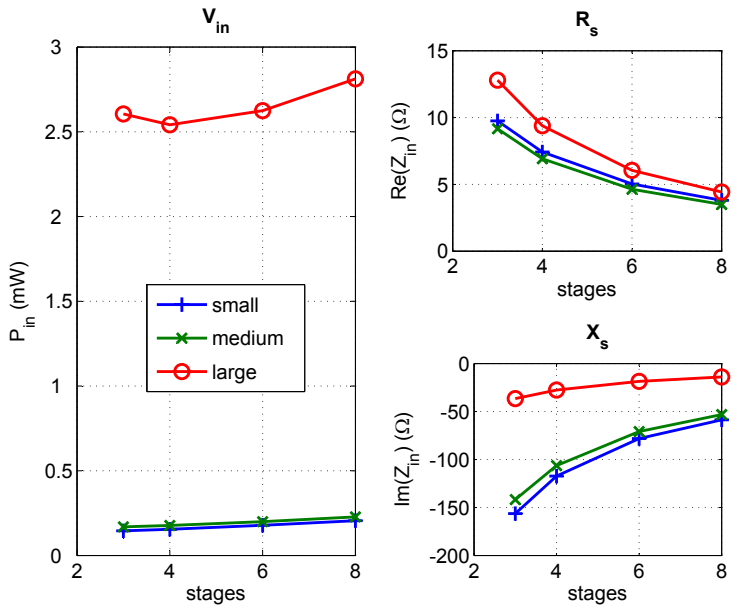

Figure 5.27: Input voltage and input impedance versus stage number and diode size for a $V_{DC} = 2V$ and a load of 90 kΩ.

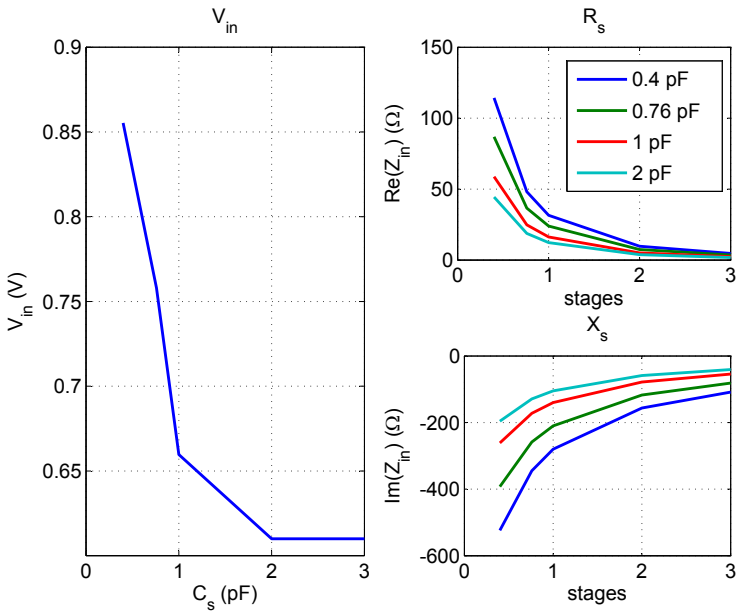

Figure 5.28: Input voltage and input impedance versus stage number and capacitor size for a $V_{DC} = 2V$ and a load of 90 kΩ.

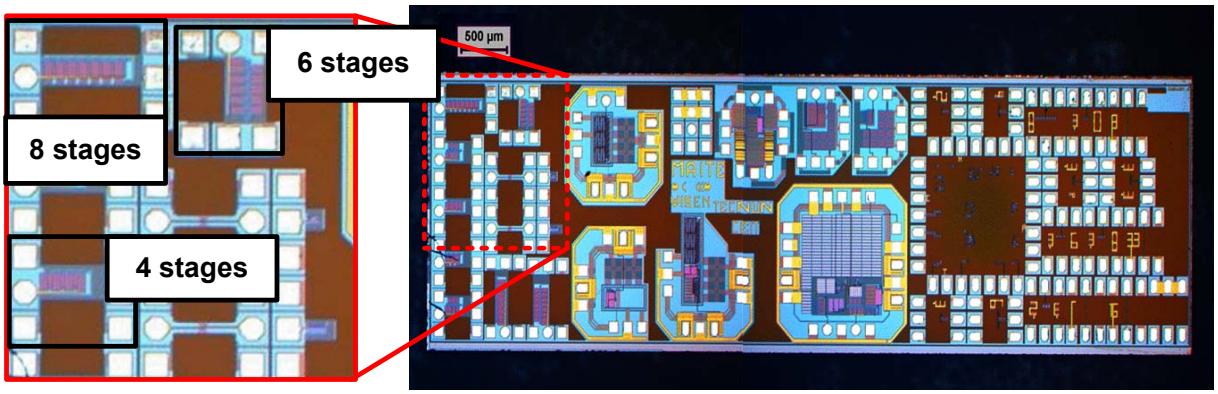

Figure 5.29: Microphotograph of the test chip.

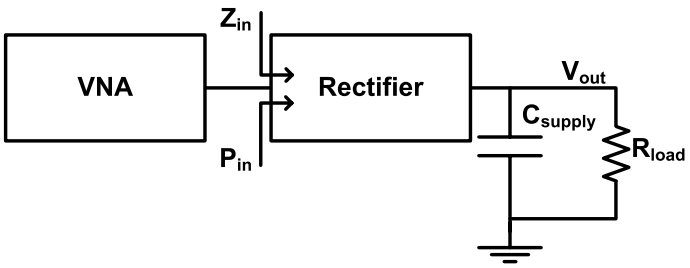

Figure 5.30: Test–bench used in the chip measurements.

rectifier is loaded with 136 kΩ (Figure 5.31.a) and with 52 kΩ (Figure 5.31.b). Both the tendency and the numerical results of the rectifier input impedance is well matched by theoretical results. On the other side, the input power measured is higher than the calculated one. The reason is that some ohmic losses (series resistance of the capacitor, pads, and other) were not taken into account. When the input current increases the same do the ohmic losses.

Figure 5.32 compares measured and calculated results of three rectifiers under the same load conditions. The measured rectifiers have 4, 6 and 8 stages and were loaded with a 1MΩ resistance. As in the previous figure, the input impedance is well matched by the theoretical predictions. The tendency of the input power is also well followed by the calculated results. However the calculated results are lower than the measured due to the mentioned ohmic losses, that were neglected in the calculations. To sumarize, the proposed theoretical calculations match quite well the measured results, specially the input impedance. The tendency of input power is met by the calculation. However, the calculated values are lower than the measured ones. As a consequence additional losses should be included to match completely the absolute values. The obtained results prove that the theoretical calculations are used to design easily and quickly rectifiers from the specifications given by the technology process, and the consumption requirements of the circuits to be supplied.

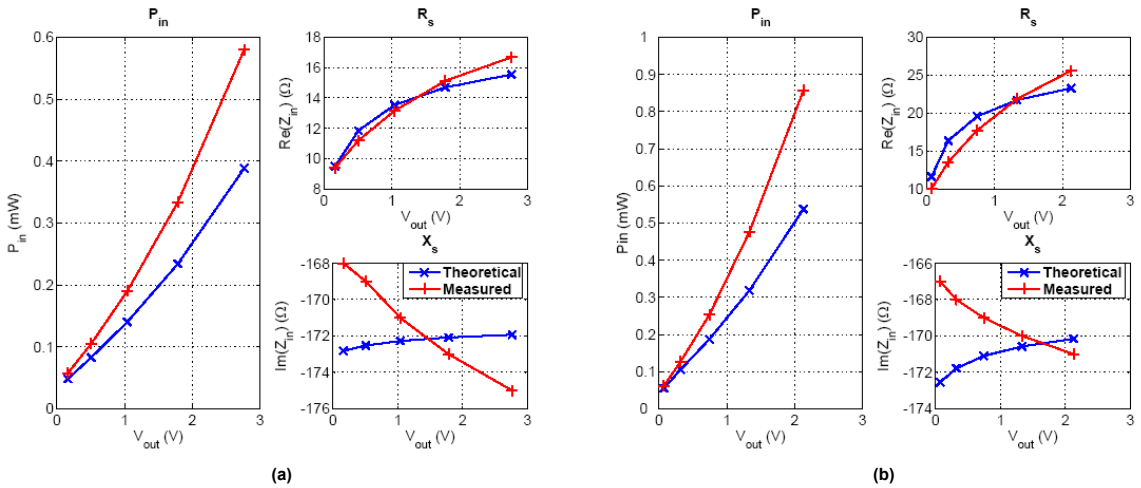

Figure 5.31: Measures versus theoretical results of a four stages rectifier.

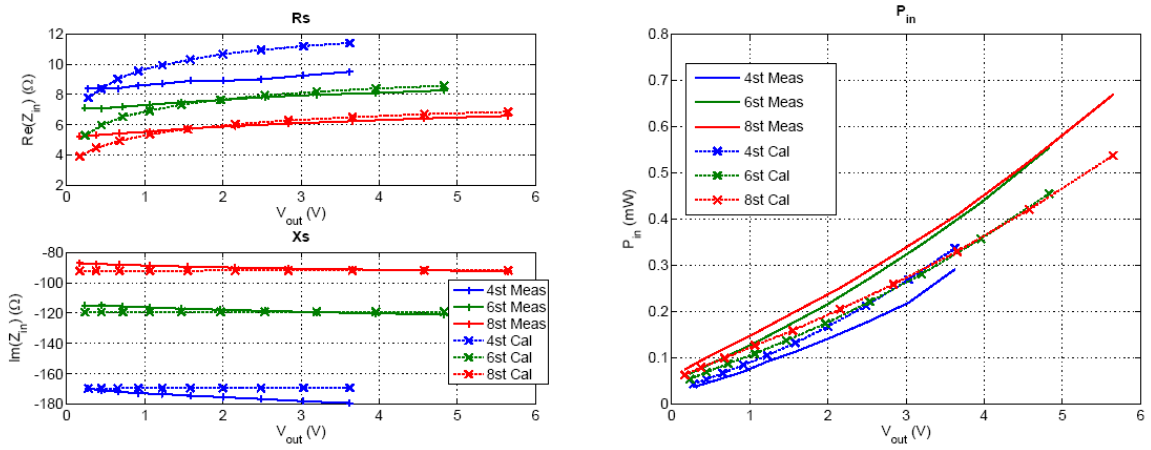

Figure 5.32: Comparison of measured and calculated results of three rectifiers under the same load conditions.

5.5 Conclusions

The rectifier is a key block in the wireless energy transmission, since it converts RF into DC power. This chapter has analyzed in depth this circuit in order to give some solutions to the design and modelling of this block. The main conclusions extracted from this chapter are summarized below.

The different topologies reported in the state–of–the–art to implement a rectifier have been analyzed and the Dickson topology with Schottky diodes has been selected as the best choice since reduce the complexity and has been already proved successfully in several process.

A design methodology to implement rectifiers attending to the power efficiency has been proposed. The more relevant design steps of this methodology are diode sizing, capacitor sizing and several stage cascading.

It was deduced and proved by experimental results that diode size must remains as low as possible to maximize the power efficiency. This way, the diffusion capacitance is minimized and the reverse and parasitic resistance maximized.

Regarding to the capacitors included in the rectifier topology, it was concluded that poly–poly capacitors are more efficient in the power conversion than poly on diffusion capacitors. Moreover, the series capacitors are the most critical in the power conversion, consequently its parasitic capacitances and resistance must be reduced as much as possible.

The consequence of increasing the stage number is higher V_{DC} at the expense of less efficiency. The reason is losses due to diode parasitic components, and Q reduction due to the increase on the parasitic input capacitance.

In this chapter, it was proposed a mathematical model to characterize the operation of the rectifier in terms of input impedance, and output voltage as a function of the power requirements, technology and its input power. The mathematical model was compared with simulations results to prove its feasibility in multiplier design. The average error of the model regarding to the simulations was 7.25 % and 1.12 % for real and imaginary part of Z_{in}, respectively, and 1.47 % for the V_{in}. Model and simulation agree well with experimental results of three rectifiers implemented in the CMOS 0.35 μm low power process of XFAB.

Chapter 6

Voltage Sensor and High Voltage Protection

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Abstract: The supply capacitor has to be properly charged before the Tag is operative. Therefore, circuits to check the charge of the capacitor are required. This chapter presents two ultra-low-power voltage sensors and a high voltage protection circuit, to optimize the charge of the Supply Capacitor in passive UHF RFID sensors. The state–of–the–art in the field is analyzed and compared with the proposed circuits using a XFAB 0.35 μm 2P4M CMOS process. The measured current consumption of the Voltage Sensors are 70 nA and 0.2 nA at 3.3 V, respectively. The Voltage Protection circuit consumes less than 60 nA at 3 V.

This chapter is estructured as follows. First, the Power Up mode is introduced. Section 6.2 deals with the Voltage Sensors, analyzes its state–ot–the–art, proposes novel circuits and presents experimental results. Next, the High Voltage Protection Circuits are the topic of Section 6.3. Finally, the main conclusions are sumarized.

6.1 Power–Up operation mode

Figure 6.1 shows the block diagram of the passive UHF RFID sensor. The RF input power is captured by the antenna, which is matched for maximizing power transfer. The Voltage Multiplier (VM), also called rectifier, converts RF into DC power. The

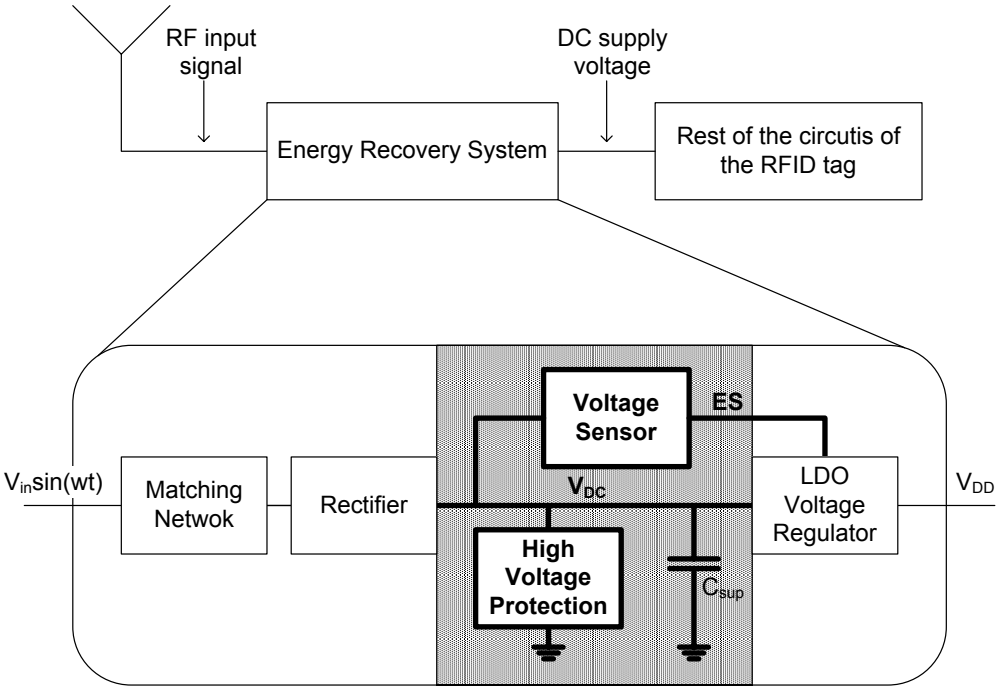

Figure 6.1: Location of the Voltage Sensor and high voltage protection inside the passive UHF RFID sensor architecture.

DC power produced by the VM charges the supply capacitor. This capacitor maintains the supply voltage when short absences of RF power or consumption current peaks occur. To assure a proper supply voltage, the tag is powered up only after the capacitor is enough charged. To handle the charging of the supply capacitor, two circuits are required: a Voltage Sensor and a Voltage Protection. The first one senses the charge of the capacitor and generates the Enable Signal (ES). This signal turns on the Voltage Regulator, which generates the V_{DD} for the rest of the subsystems of the transponder. High RF power on the antenna produces high voltages on the capacitor [4], that could damage the electronics. The voltage protection circuit protects the supply capacitor and the complete chip subsystems against breakdown voltage.

The power consumption of an RFID sensor is not constant along the time. There are three different operation modes with different power requirements [107]:

- **Power–Up**, Supply Capacitor is charged (below 1 μW),
- **Active**, Analog and Digital active (24 μW), and
- **Measure**, the Sensor is operative (50 μW).

A consequence of the different power consumption is that the input impedance changes with the operation mode. Therefore an optimal matching is not possible for all the operation modes. A solution is to match for the worst case (highest power consumption) and reduce the power consumption in the rest of operation modes. The power consumption must be especially reduced in the Power–Up mode since the mismatch is the highest.

This chapter deals with the design of the circuits which are active during the Power-Up mode, namely Voltage Sensor and High Voltage Protection.

6.2 Voltage Sensor

The Voltage Sensor (VS) senses the charge of the supply capacitor and generates the Enable Signal (ES) when a specified voltage threshold (ES_{th}) is reached on the capacitor.

6.2.1 State-of-the-art

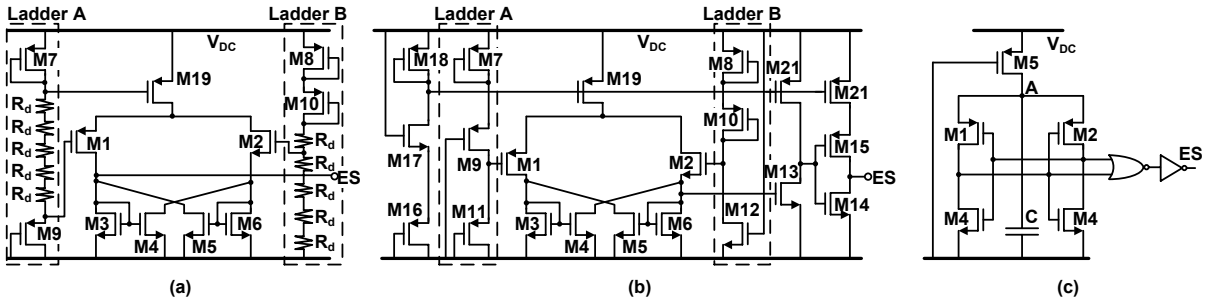

Figure 6.2: Circuits reported in the bibliography, (a) Mode Selector(MS) [3], (b) Modified Mode Selector (MMS) [4], and (c) Power on Reset (POR) [5].

The Mode Selector (MS) circuit [3] is shown in Figure 6.2.a. Two trip voltages are generated by two resistive ladders and compared by a hysteresis comparator formed with transistor M1–M6. The integrated resistances increase the area consumption dramatically and also the current consumption (reported as 5 μA).

The same authors propose the Modified Mode Selector (MMS) [4], see Figure 6.2.b. In this circuit, the ladders are implemented with transistor instead of integrated resistances reducing so the active area. The current consumption is also reduced to 900 nA, which is still excessive for passive UHF RFID systems in the Power–Up mode.

Other alternative is the POR circuit [5] of Figure 6.2.c. When a supply voltage is applied to V_{DC}, one of the two inverters takes advantage over the other. The NOR gate compares the output of the two inverters, and activates the ES. The capacitor C forces a delay between the rise of the V_{DC} and the ES.

6.2.2 Novel structures

Two novel structures are presented. Figure 6.3.a shows the Voltage Levels (VL) circuit. It is based on the voltage level reached at the gate of M11. The ladder composed of the transistors M1–M10 does not draw current until $V_{DC} > 5 \cdot V_{th}$ (around 2.5 Volts in 0.35 μm CMOS technology). However M11 begins to conduct a small current (i_{sth}) in Subthreshold Region ($V_{GS} < V_{th}$). The current i_{sth} discharges the small capacitor C and finally the inverter generates a rising edge. The Output Stage consumes current only in the transitions of the ES. The current peak on the transition depends on the capacity of C and on the dimensions of M13 and M14. Before the edge of ES (Power–Up operation mode), Ladder and M11 are still OFF and the current is below 1 nA.

Figure 6.3.b shows the second novel circuit based on the charge of a capacitor (CC). The ladder made up of M1–M4 charges the capacitor C1. When the charge on the capacitor is $2V_{th}$, M5 turns on and the rising edge of the ES is produced. M11 discharges C1 when the tag is turned off. CC circuit draws current only at the rising edge of the

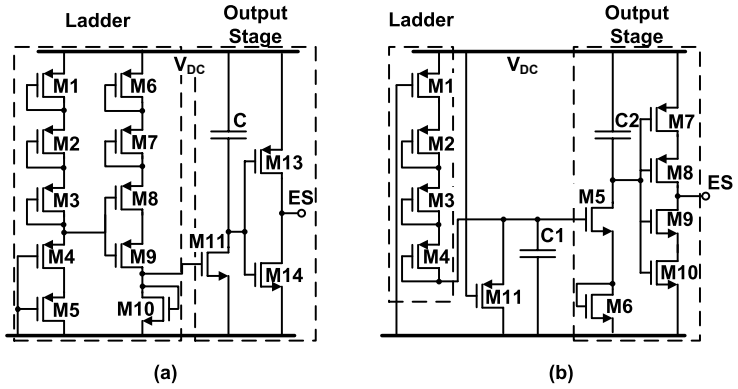

Figure 6.3: Proposed Novel Circuits based on: (a) Voltage Levels (VL), and (b) Charge of a Capacitor (CC).

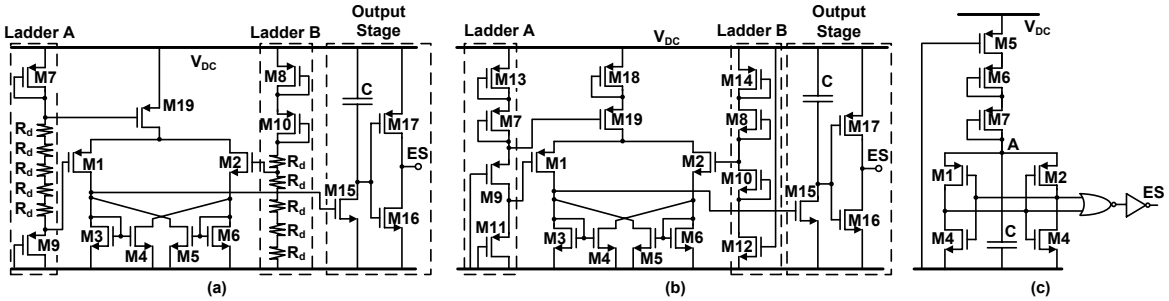

Figure 6.4: Modifications in state–of–the–art circuits. (a) MS', (b) MMS', and (c) POR'.

enable signal. Ladder and Output Stages are open circuits for the DC current thanks to C1 and C2.

6.2.3 Design considerations

The performance of the proposed circuits is very dependent on the technology and temperature because the V_{th} of the transistors is used as unique voltage reference. This is taken into account in the design. The dimension of each transistor is chosen so that, the threshold voltage and the current consumption of the circuit are for all technology corners (worse cases) as constant as possible.

Notice that the ES_{th} of the proposed circuits can be increased/decreased by inserting/removing diode–connected transistors in the ladders.

6.2.4 Comparison and measurements

Circuits of the state–of–the–art and novel structures have been simulated and compared at schematic level using the XFAB 0.35μm 2P4M CMOS process, then the circuits with the best features has been implemented and measured.

Table 6.1: Simulation Results of Voltage Sensor Circuit–Structures

$Circuit$	$\bar{I}$ (nA)	$\hat{I}$ (μA)	ΔES_{thc} (V)	ΔES_{tht} (V)	$Area$ (μm^2)	ref.
MS	800	1.87	1.10	0.40	30148	[3]
MMS	57	1.44	0.85	0.50	693	[4]
POR	1350	1.55	1.40	0.20	348	[5]
VL	47	1.65	0.90	0.45	352	Proposed
CC	< 1	0.50	1.10	0.49	590	Proposed

Performance parameters

The charge of the supply capacitor depends on the reader distance, the used Rectifier and the capacitance of the supply capacitor. We are interested in reducing power consumption and area of each structure, for standard operational conditions. To compare the different architectures, all the circuits were adjusted to set to high the ES node when V_{DC} is, for all the corners, between 2.5 V and 3.3 V (ES_{th}). All the eight simulation corners, as specified in the technology process, were simulated. V_{DC} is generated by a pulse source with voltage levels between 0 V and 3.3 V, and a rise time of 50 μs for quick charging time, or 1.5 ms for slow charging time. The parameters obtained from the simulations were:

- ES_{th} variation due to corner simulations (ΔES_{thc}) and due to charging time of the capacitor (ΔES_{tht});
- DC current consumption at 3.3 V ($\bar{I}$) and transient current consumption when the ES node is set to high ($\hat{I}$) i.e. when the output inverter switches;
- active area, which is calculated by adding the size of the required devices.

Modifications on MMS and POR structures

Adjusting ES_{th} to 2.5 V requires some modifications on the state–of–the–art circuits. In the MMS circuit (see Figure 6.2.b), we have modified the MOS resistive ladders A and B, as can be seen in Figure 6.4.b.

The ES_{th} in the original POR circuit is very low (some hundreds of mV), when it is implemented. In order to provide a fair comparison, the threshold voltage ES_{th} was increased to 2.5 V by introducing two transistors, M6 and M7 as shown in Figure 6.4.c.

Finally, the output stage used in VL is introduced in the MS and MMS circuits to reduce the DC current consumption, as can be seen in Figure 6.4.b. The modified state-of-the-art circuits are termed MS', MMS' and POR'.

Comparison results

Table 6.1 shows the simulation results. The DC current consumption is lower than 1 nA in the CC circuit because the capacitors C1 and C2 (Figure 6.3.b) behave as open circuits in DC. Current $\bar{I}$ is 47 and 57 nA in VL and MMS' respectively. The ladders are similar

Table 6.2: Measured Results of VL and CC Circuit–Structures

$Circuit$	$\bar{I}$@3.3V (nA)	$\hat{I}$ (μA)	ES_{th}@1ms (V)	ES_{th}@1μs (V)	$Area$ (μm^2)
VL (2.5V)	69	1.79	2	2.5	2584
VL (3.3V)	19	2	3	4.2	3380
CC (2.5V)	0.2	0.75	2	2.8	3762
CC (3.3V)	0.4	1.5	3	4.2	3843

but the MMS' includes an extra current consumption due to the comparator. The use of resistive ladders in MS' increase the $\bar{I}$ because of the limited value of the integrated resistances. Finally, the highest $\bar{I}$ correspond to the POR' which presents an unusual value, more than 1 μA. The POR circuit was designed for a ES_{th} of 1 V, an increment on this voltage increases the DC current consumption on the NOR gate.

Because all these architectures use the same inverter at the output, the peak current is similar in the MS', MMS', POR' and VL circuits (see Table 6.1). The peak current of the CC circuit is around 66% less than the above mentioned architectures. This is due to the transistors of the output inverter in the CC circuit have lower aspect ratio than in the other architectures.

The variation of ES_{th} due to technology corners is around 1 V, and the variation due to the charging time of the capacitor is about 0.4 V. For short charging times, ES_{th} is higher than for long ones. The reason is that the used transistors have low aspect ration (W/L$\simeq$0.09). This reduces the power consumption of the structures, but increase the time required by the transistors to switch.

Finally, the active area of the MS circuit is two orders of magnitude bigger than the other circuits. This is because this circuit requires high value integrated resistors (R_d in Figure 6.2.a) to reduce the current through the ladders A and B.

To sum up, MS' and POR' have the highest current consumption; and in the case of MS' the largest active area. The CC circuit presents the lowest current consumption. In terms of ES_{th} variation, VL and MMS' are the best circuits. However, $\bar{I}$ and area consumption of MMS' circuit are 2.85 and 1.97 times higher than in VL circuit, respectively. Finally, notice that the modified estate–of–the–art circuits, MMS' and MS' consume 18 and 6 times less current than the original ones.

The simulation results indicate that VL and CC circuits are the best structures. This two circuits were implemented, to verify the results of Table 6.1.

6.2.5 Measurement results

Figure 6.5 is the photograph of the test chip, the location of the VS circuits is highlighted and extended. For more detail the layouts of the circuits are also illustrated. Two versions of VL and CC circuits with different ES_{th} (2.5 V and 3.3 V) have been fabricated and measured. Table 6.2 shows the measured results. The DC current consumption at 3.3 V of VL and CC circuits are below 70 nA and below 1 nA, respectively. The current peak is below 2 μA in all cases. The ES_{th} is about 0.5 V lower regarding to the simulated results. The dispersion of ES_{th} with the slope of V_{DC} is between 0.5 and 1 V.

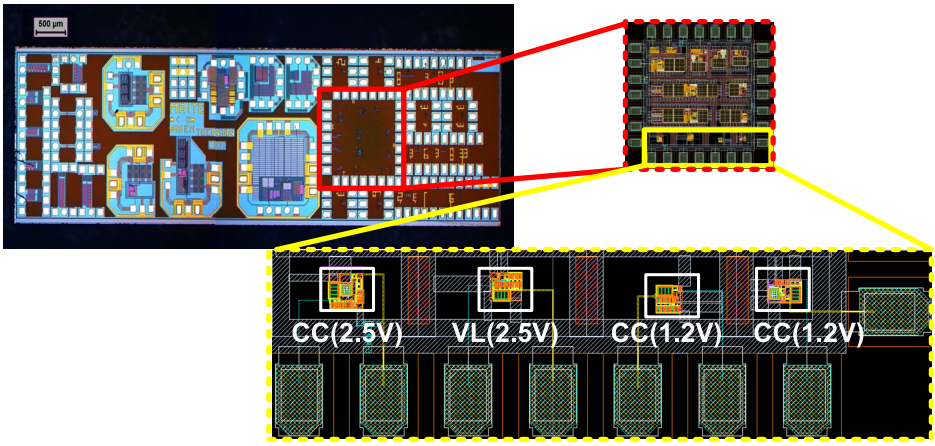

Figure 6.5: Microphotograph of the complete test chip and details of the voltage sensors.

6.3 High Voltage Protection

The voltage on the supply capacitor increases with the level of RF power at the input of the Voltage Multiplier (see Figure 6.1), when the current consumption of the tag remains constant. The level of the received RF power increases quadratically as the distance between reader and tag decreases (see Friis Transmission Formula [108]). On the other side, the CMOS process limits the voltage on the supply capacitor to 3.6 Volts. Therefore, the supply capacitor must be protected against high voltages produced when the Reader is close to the tag.

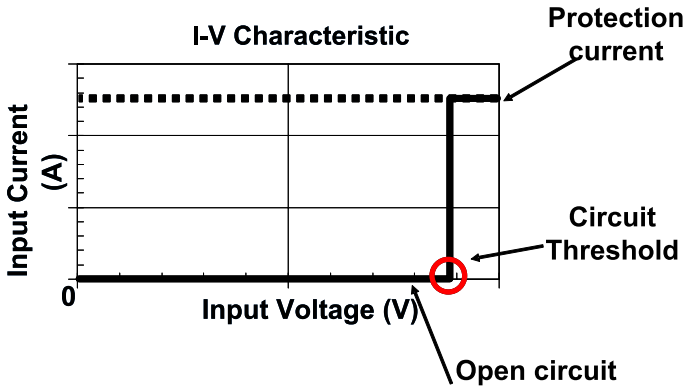

Figure 6.6: Ideal characteristic of the protection circuits.

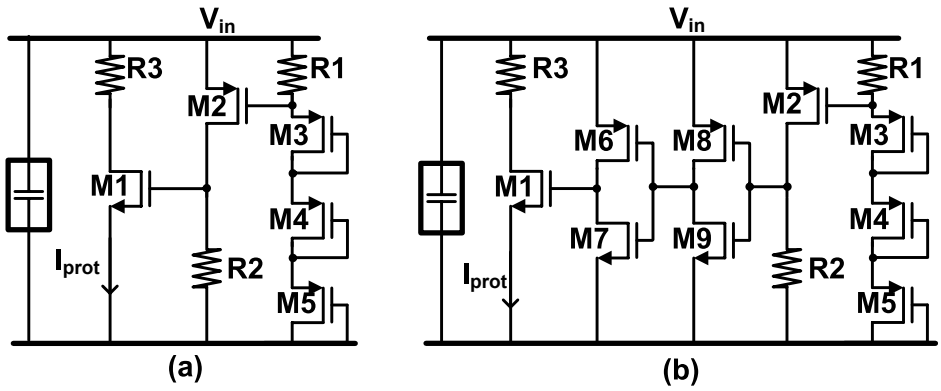

Figure 6.7: Protection circuits: a) without inverters circuit based on [6], and b) with inverters circuit proposed as proposed in this work.

The ideal I–V characteristic of a protection is shown in Figure 6.6. No current is drawn until a threshold is reached, after that the circuit behaves as a short. To approach this characteristic, we used a circuit based on the limiter proposed by [6] (see Figure 6.7.a). As soon as V_{DC} exceeds the sum of all threshold voltages of the transistors M3—M5, current starts to flow through R1. When the voltage drop across R2 reaches the threshold, M2 will switch on and in turn activates M1 which carries the most of the current. Resistor R3 fixes the current to be drawn, when the protection is activated.

A consequence of designing circuits with very low current consumption is a reduction of the switching speed of the transistors. The reason is that the parasitic capacitors of the

transistors are charged and discharged by very low current. In the case of the protection circuit of Figure 6.7.a, this means an increment in the degradation zone (voltage range below the threshold voltage and with a current greater than 100 nA, see Figure 6.10). To reduce the degradation region, two inverters were introduced at the gate of M1 (see Figure 6.7.b). This modification increases the switching speed of M1, since the voltage that drives the M1 gate (see Figure 6.7.b) switches abruptly.

6.3.1 Results

The two protection circuits of Figure 6.7 were implemented in a 0.35μm 2P4M CMOS process from XFAB.

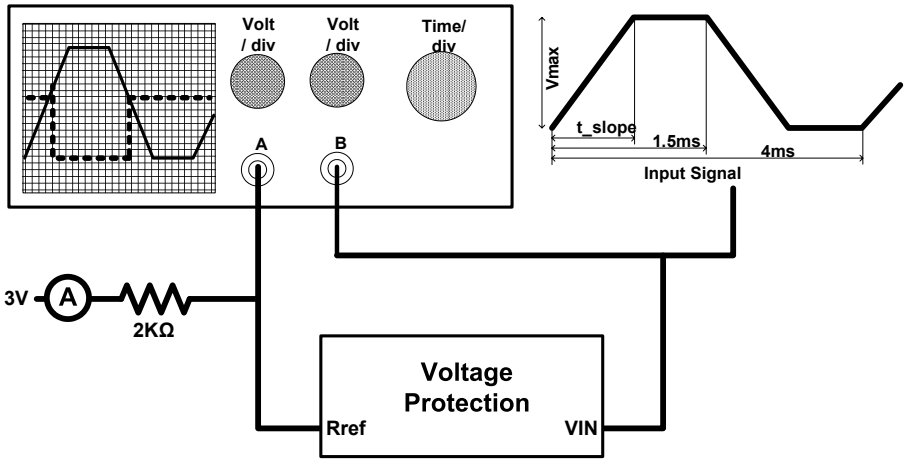

Figure 6.8: Test bench used to measure the switching time of the protection circuit.

Figure 6.8 depicts the test bench used to measure the time required by the circuits to switch once the threshold voltage is reached. The input signal is a pulse with adjustable slope, which models the charge of the supply capacitor by the voltage multiplier. The resistor R3 (see Figure 6.7) is an external element, that adjusts the current to be drawn by the circuit. The transient response to the same input signal of both topologies is showed in Figure 6.9. The time required to switch by the circuit reported in the biblography is around 70 μs, whereas the time required to switch here proposed circuit is around 5 μs. The proposed modification reduces in a 92.9% the response time of the protection circuit.

Figure 6.10 shows the measured I–V characteristic of the both circuits. The degradation region is 0.2 V in the circuit of the state–of–the–art and 0.12 V in the one proposed in this PhD. Work. A reduction of 40% in the degradation region is achieved by inserting the two inverters. As can be apreciated in Figure 6.10 the circuit here proposes is a very accurate approximation of the ideal I–V characteristic of the protection circuit, whereas the circuit proposed in [6] not.

6.4 Conclusions

In passive UHF RFID sensors, Voltage Sensor (VS) and Voltage Protection (VP) are the unique active circuits during the charge of the Supply Capacitor. To optimize this charge the current consumption of VS and VP must be minimized.

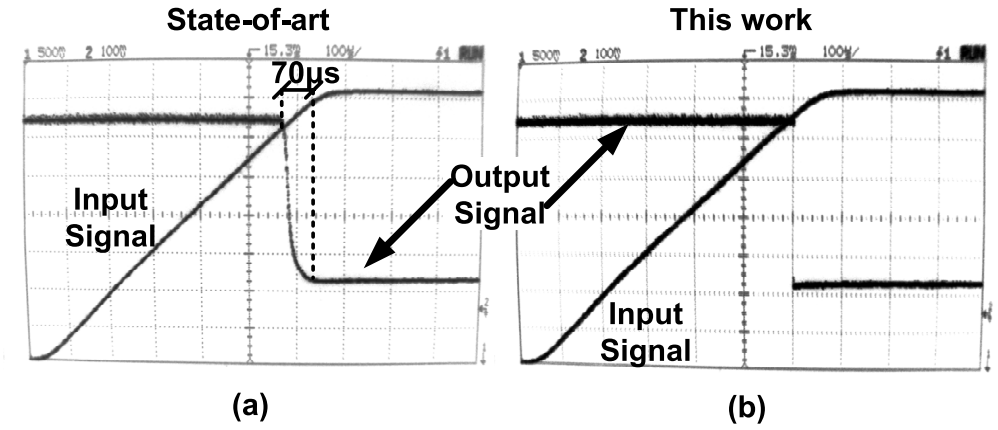

Figure 6.9: Transient response of the protection circuits: (a) without inverters circuit based on [6], and (b) with inverters circuit as proposed in this work.

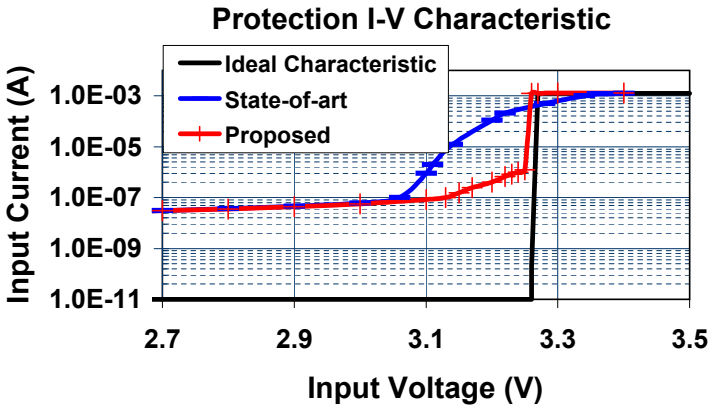

Figure 6.10: Ideal and measured I–V characteristic of the protection circuits.

Two novel VS circuits are proposed and compared with the state–of–the–art alternatives in this chapter. The measured DC current consumption of the two novels structures is 69 nA and 0.2 nA at 3.3 V and implies an improvement of one order of magnitude in terms of current consumption in regard to previous reported results.

This chapter also proposes a modification on the state–of–the–art for VP devices. The measurements have proved that the proposed modification reduces in one order of magnitude the current consumption before the voltage threshold of the circuit is reached.

Chapter 7

Voltage Regulator

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Abstract: The DC voltage generated by the rectifier can not directly used to supply the RFID sensor. A further analog processing is required to adapt this voltage to the supply voltage requirements of the RFID sensor. The circuit that carries out this analog processing is known as Voltage Regulator. This chapter deals

with analysis and design of voltage regulators applied to passive UHF RFID sensors.

The chapter is structured as follows. First, the regulation problem is introduced. Section 7.2 analyzes the different alternatives to implement a voltage regulators in RFID systems and selects the low dropout voltage regulator as the most suitable for the application. Next, the regulator architecture is described and the requirements of the regulation system are specify. Sections 7.7 and 7.5 deal with the particular components of the regulator architecture. In Section 7.6 the design methodology of a low dropout voltage regulator for UHF RFID sensors is presented. To conclude, the proposed methodology is proved by simulations and prototype measurements in Section 7.7.

7.1 Introduction

The supply voltage of any electronic circuit must be inside a security range that assures proper operation. Supply voltages outside this range could causes circuits malfunction or even breakdown of some of their elements.

For the particular case of passive UHF RFID sensors, the supply voltage is generated by the rectifier from a incoming electromagnetic wave. As the power and amplitude of this wave is variable with distance the same occurs with the supply voltage.

On the other hand, current consumption of complex systems, like passive RFID sensor, is variable and present sharp current peaks due to the digital circuits. The changing current consumption would produce severe drops on the supply voltage that could violate the acceptable voltage supply range.

As a final point, it is highly desirable to maintain the supply voltage at the minimum required by the technology to work in ultra low power system. Since this is a way to reduce the power consumption.

In conclusion, the DC voltage generated by the rectifier (V_{rect}) presents a set of problems due to the nature of the energy recovery system of a passive UHF RFID sensor. These problems are: variable V_{rect} due to fluctuation in the input power, undesirable supply voltage drops due to changing current consumption, and non–optimum V_{rect} for ultra–low power consumption.

To solve these issues, an additional block has been included in the supply system. The circuit in charge of generating a defined and stable voltage for proper RFID sensor supplying is known as Regulator.

Figure 7.1 depicts the complete energy recovery system of the passive RFID sensor. The location of the voltage regulator has been highlighted. Its main input is the V_{rect} from the rectifier. An additional input is the enable signal (ES) from the voltage sensor, used to wake up the regulator. Finally, the regulated supply voltage (V_{DD}) is the output of the regulator block.

7.2 Voltage regulation approaches in passive RFID systems

Different approaches have been chosen to face the voltage regulation problem in passive UHF RFID system.

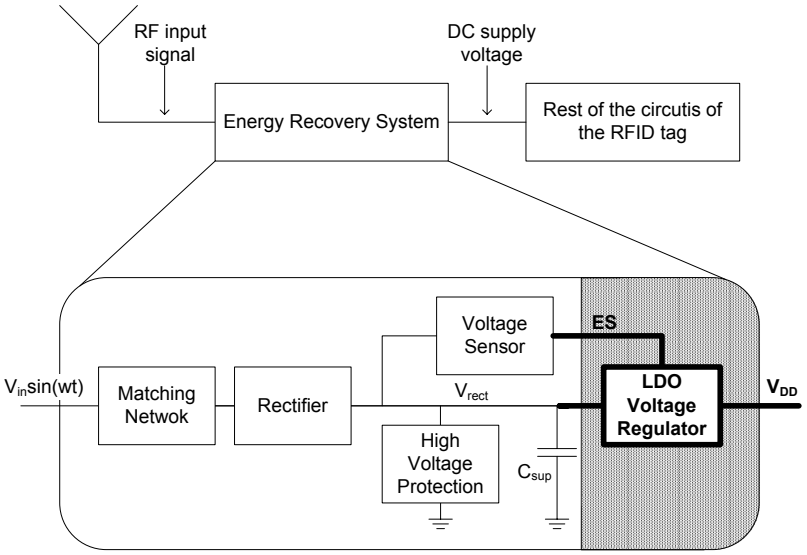

Figure 7.1: Energy recovery system block diagram.

Some authors [1, 4] do not use any regulator circuit. The reason is to reduce as much as possible the power consumption to achieve a longest reading distance. Anyway, it can be possible that the cited authors do not mention the regulators but they make use of them.

Other published systems like [5, 48, 109, 42] use a high voltage protection, also called limiter, similar to the one described in Chapter 6 to avoid breakdown voltages. This approach does not require the use of complicated voltage regulators at the expenses of a very robust design of digital and analog circuits against variation in the supply voltage. Most of the systems that use a simple limiter are pure UHF RFID tags.

The last approach [53, 110, 111] includes a limiter and an additional voltage regulator after the rectifier to assure a stable supply voltage independent of current peaks. The advantage of this approach is a very stable and well controlled V_{DD}. The drawback are higher complexity and extra current consumption.

For the particular case of passive UHF RFID sensors, the reduced breakdown voltage of the supply capacitor obligates the use of at least a High Voltage Protection. Moreover, the introduction of a sensor supposes an extra power consumption regarding to traditional RFID. Thus, the supply voltage of the sensor must be maintain as close as possible to its minimum to reduce the power consumption, and should not fall below it due to current peaks. This functionality can not be achieved by a simple limiter. Additionally, variations in the current consumption are huge due to the additional consumption introduced by the sensor. The same happens with the current peaks of the digital logic. On the other side ,V_{rect} generated by the rectifier fluctuates with the received RF input power. These variations are not accepted by sensors. As a consequence, a stabilization of supply voltage is required. In conclusion, the use of a voltage regulator is mandatory to generate a defined and stable supply voltage against current variation.

7.2.1 Voltage regulators alternatives

There are two main philosophies for building a voltage regulator [112]. On the one hand, Linear Voltage Regulators that are based on devices operating in their linear region. On

the other hand, Switched Voltage Regulators that rapidly switches a series device on and off.

In Linear Voltage Regulators, a transistor is used to control the output voltage, and a feedback circuit compares the output voltage to a reference voltage in order to adjust the input to the transistor, thus keeping the output voltage reasonably constant.

Switched Regulators rapidly switches a power transistor between saturation and cutoff with a variable duty cycle. This rectangular waveform is low–pass filtered with an inductor and capacitor. The main advantage of this method is greater efficiency because the switching transistor dissipates little power in the saturated state and none in the off state.

Switched Regulators are more complex and costly than Linear ones. The formers require a controller with an oscillator, pass elements, inductor, capacitors and diodes. Such a complexity level makes no sense in RFID applications where the price of a Tag is a critical aspect, and should be kept to its minimum. Low cost and simplicity are the reasons of use Linear Voltage Regulators in the Energy Recovery System for RFID sensor.

7.2.2 Linear voltage regulators types

There are three basic types of linear regulator [113]: Standard Regulator, Low Dropout or LDO Regulator and Quasi LDO Regulator.

The single most important difference between these three types is the dropout voltage, which is defined as the minimum voltage drop required across the regulator to maintain output voltage regulation. A critical point to be considered is that, the linear regulator that operates with the smallest voltage across it, dissipates the least internal power and has the highest efficiency. The LDO requires the least voltage across it, while the Standard regulator requires the most.

The second important difference between the regulator types is the ground pin current, or quiescent current, required by the regulator when driving rated load current. The Standard regulator has the lowest quiescent current, while the LDO generally has the highest [113]. Increased quiescent current is undesirable since it is "wasted" current, in other words, it must be supplied by the source but it does not power the load.

For the particular case of passive RFID, some point. First, V_{rect} decays with the distance between reader and tag. And second, it is desirable to maximize the operation range, this is, the system must be operative with the minimal supply voltage. As already discussed, the type of regulator more efficent in terms of voltage is the Low Dropout Regulator. This is the reason because LDO regulators are the more suitable regulator architecture for passive RFID sensors.

7.3 Low Power LDO Regulator

A series low–dropout regulator is a circuit that provides a well specified and stable DC voltage [114] whose input to output voltage difference is low. The term series comes from the fact that a power transistor (pass device) is connected in series between the input and the output terminals of the regulator.

An Error amplifier controls the pass device that drives the charge placed at the V_{out} terminal (see Figure 7.2). The voltage at node V_{out} is then feeded back to an amplifier, which generate the control voltage comparing a reference with the feedback signal. This

type of regulator has two inherent characteristics. First, the magnitude of the input voltage is greater than the respective output and second, the output impedance is low so as to yield good performance [115]. Low dropout (LDO) regulators can be categorized as either low power or high power. Low power LDOs are typically those with a maximum output current of less than 1 A, mostly exhibited by portable applications. On the other hand, high power LDOs can yield currents that are equal to or greater than 1A to the output, which are commonly demanded by many automotive and industrial applications.

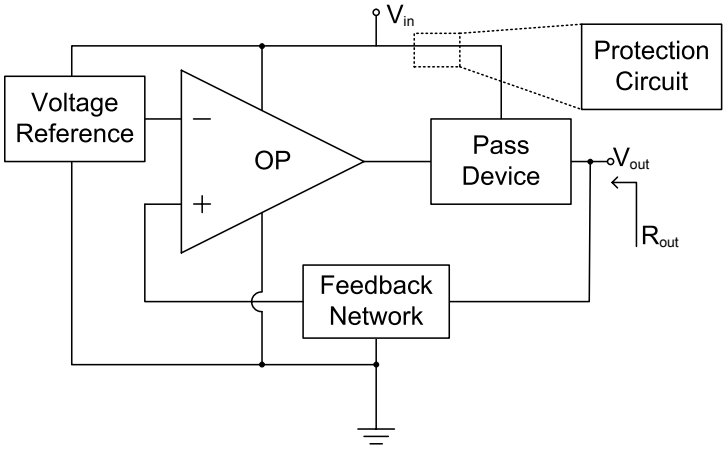

Figure 7.2: Block diagram of a low dropout voltage regulator.

Figure 7.2 illustrates the block level diagram of a generic series LDO regulator. The circuit is composed of a reference, a protection circuit, an error amplifier, a pass element, and a feedback network. The reference provides a stable DC bias voltage with limited current driving capabilities. The protection circuitry ensures that the LDO operates in save stable conditions. The error amplifier, the pass element and the feedback network form the regulation loop. The temperature dependence of the reference and the amplifier input offset voltage define the overall temperature coefficient of the regulator; hence, low drift references and low input offset voltage amplifiers are preferred.

7.3.1 Specifications

The important aspects of the LDO can be summarized into three categories, namely, regulating performance, quiescent current, and operating voltages [116]. Some of the specifications serve as metrics for the LDO include dropout voltage, line regulation, load regulation, tolerance over temperature, output voltage variation resulting from a transient load–current step, output capacitor and ESR range, quiescent current maximum load–current, and input/output voltage range. These performance characteristics often contradict each other giving rise to necessary compromises. The priority of the performance parameters is defined according to the particular application.

In the field of passive UHF RFID sensors the more relevant specifications are dropout, quiescent current and output voltage variations resulting from a transient load current step. Next, the requirements of the energy recovery system will be described in terms of LDO specifications. Finally LDO regulator design guidelines will be presented presented.

Dropout

Dropout voltage can be expressed in terms of switch "on" resistance (R_{on}),

$$V_{drop-out} = I_{Load} R_{on} \tag{7.1}$$

Typical dropout voltages range from 0.1 to 1.5 V [114].

Figure 7.3 shows the minimum V_{rect} required to assure a regulated Supply Voltage for analog and digital circuits, and for EEPROM. As explained in Chapter 6, High Voltage protection limits V_{rect} to 3.3V, avoiding breakdown voltages when reader and tag are too close to each other. Since the DC voltage generated in the rectifier goes down with the distance, the maximal reading range is reached when rectifier generates the minimum V_{rect}. A proper supply voltage can not be assure for longer ranges.

Observing Figure 7.3, Dropout Voltage must be minimized for reducing the minimum V_{rect} and, consequently, for increasing the reading range.

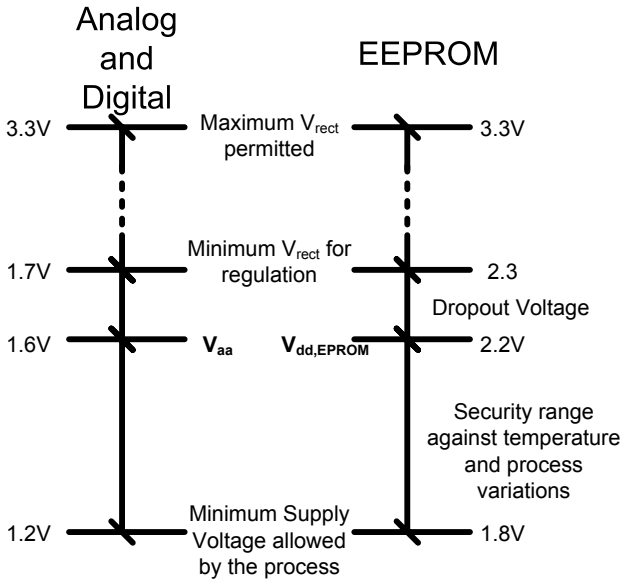

Figure 7.3: Required voltage for proper passive RFID sensor operation.

Quiescent current and LDO power efficiency

The efficiency of the LDO is limited by the quiescent current and the input/output voltages, and is expressed as:

$$Eff_{LDO} = \frac{I_O V_{DC}}{(I_O + I_q) V_{DD}} \tag{7.2}$$

where I_O and V_{DD} correspond to the output current and voltage, voltage and I_q the quiescent current or current consumed by the regulator. In passive RFID systems high efficiency is a priority. The way to maximize the efficiency is reducing as much as possible the quiescent current in the LDO design. This point and its relation with other LDO properties is dealing in the design guidelines.

Load regulation, temperature and transient output voltage variations

Output voltage variations arising from specific changes in input voltage is defined as line regulation. Similarity, load regulation is the change in output voltage for specific changes in load–current [115]. Load regulation is essentially the output impedance of the circuit R_o,

$$R_o = \frac{\Delta V_{LDR}}{\Delta I_o} = \frac{R_{o-pass}}{1 + A_{ol}\beta} \tag{7.3}$$

where ΔV_{LDR} and ΔI_o are the output voltage variation and the load–current changes, respectively. R_{o-pass} is the output impedance of the pass element, A_{ol} is the open–loop gain of the system, and β is the feedback factor [117]. The complete DC power consumption of a RFID sensor is around 25 μA. At supply voltage of V_{DD}=2.3 V, this can be modeled as a load of $R_L = 92\ k\Omega$. To reduce the effect of the load regulation must be assures that $R_o << R_L$. for example a $\Delta V_{LDR} = 0.01R_0 = 0.01R_L = 920\ \Omega$. In conclusion, the output impedance of a LDO operating in a RFID circuit should not be higher than 1kΩ for an acceptable load regulation.

The temperature dependence of the output voltage is a function of the temperature drift of the reference and the temperature dependence of the input offset voltage of the error amplifier. The temperature range in which the RFID sensor is operative, goes from -40°C to 70°C. This range is sufficient for an application in a medical environment as remote interrogable human termometer.

Transient output voltage variations resulting from sudden load–current changes are dominated by the closed–loop bandwidth of the system, output capacitor, and load–current. The worst case situation occurs when the load–current suddenly steps from zero to its maximum specified value. This output voltage variation must be kept low to meet the overall accuracy requirements of the system. Current peaks generated by digital circuits are one order of magnitude higher than the DC current consumption; therefore, this parameter is critical in the design of LDO for RFID sensors.

7.4 Voltage reference for passive RFID sensors.

A voltage reference is a circuit able to generate a constant voltage independent of temperature, supply and process variations. This voltage is used as a reference for other circuits, for example, biasing circuits, comparators, analog–to–digital converters, among others. The reference voltage plays a key role in Voltage regulators, where the output voltage (V_{dd}), throw the feedback–network, is compared with a defined value. The result of this comparison is then used to polarize the pass device. This way the feedback loop is closed, and the voltage regulator is able to regulate itself when changes occur. This regulating process is based on the voltage reference. Therefore, the behavior of the reference versus frequency, supply voltage, temperature and process variation will be extrapolated and exacerbated by (V_{dd}). Consequently, the reference requires an especial meticulous design.

7.4.1 Supply and temperature independent circuits

The objective of a reference generation is to establish a DC voltage or current that is independent of the supply and process and has a well–defined behavior with temperature.

Therefore, the task can be divided into two design problems: supply–independent biasing and definition of the temperature variation [95].

Supply independent biasing. The simplest circuit uses to generates a supply independent current is usually called "bootstrap reference" [95]. The idea is that if I_{out} is to be ultimately independent of V_{dd}, then I_{ref} can be replica of I_{out}. Figure 7.4 illustrates an implementation where M_3 and M_4 copy I_{out}, thereby defining I_{ref}. In essence, I_{ref} is "bootstrapped" to I_{out}. With the sizes chosen here, we have $I_{out} = KI_{ref}$ if channel–length modulation is neglected. Further improvements of here presented crude "bootstrap reference" can be found in [95, 93, 117].

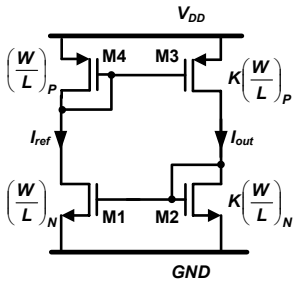

Figure 7.4: Block diagram of a low dropout voltage regulator.

Temperature independent references. The sum with proper weighting of two quantities having opposite temperature coefficients (TKs) results a zero TK. The generation of a voltage or a curren with zero TK is the operation principle of the temperature indepent reference circuits. The most widely used reference circuit is the bandgap reference [116]. Bandgaps combine a PTAT voltage (Proportional To Absolute Temperature) usually the voltage difference between base and emitter of two bipolar transistors operated at unequal current densities and a CTAT voltage (Complementary To Absolute Temperature) traditionally the V_{BE} of a bipolar transistor.

Bandgap references require the use of bipolar transistors, which are not always available in CMOS processes. However full–CMOS voltage references can be also designed, making use of the properties of CMOS transistor operating in sub–threshold region [118].

Based on these fundamentals, there are plenty of papers where the design of voltage reference is faced in different ways. In RFID applications, another design restriction is included, namely ultra–low–power consumption. In the next section, a study in the state of the art in voltage references for low–power consumption is presented.

7.4.2 State–of–the–art references

Table 7.1 presents a comparison of low–power state–of–the–art references.

Followings conclusions can be extracted after reviewing Table 7.1:

- Vita's and Oguey's references present the lowest current consumption, both under 300nA. However its behavior versus temperature and supply is not the best.

Table 7.1: Comparison of low–power state–of–the–art references

Circuit	Supply Voltage(V)	ΔT (ppm/°C)	Power (μW)	V_{ref} (V)	PSRR (1KHz) (dB)	Area (mm^2)	BJT	Res	Process
Jiang 2000 [119]	1.2	100	600	1	-67	1	No	Yes	1.2μm CMOS
Ando2002 [120]	1	50ppm	0.6u	400			No	Yes	CMOS
Fiori(2005) [121]	2.5	28		1.5		0.042	No	Yes	0.35μm CMOS
Cheng05 [122]	1.4	62	6	0.579	-84		No	Yes	0.35μm CMOS
Ripamonti99 [123]	0.9	300	4.5	0.521			Yes	Yes	FLASH pro + BJT parast.
Chen05 [122]	0.85	58.1	23.8	0.238	-30.2	0.019	Yes	Yes	0.25μm CMOS
Vita05 [124]	1.5	25	1.5		-65		Yes	Yes	0.35μmCMOS
Leung03 [125]	1.4		13.58u	0.302		0.055	No	Yes	0.6μmCMOS
Oguey97 [126]	1.2	1nA/C			10%/V	0.06	No	No	2μmCMOS
Hirose03 [127]	1.2	125	1.1	0.727			No	No	0.25μmCMOS
Buck02 [128]	3.7	120	1400	1.112	-45	0.4	No	No	0.5μm CMOS

Table 7.2: Comparison of simulated voltage references

Circuit	V_{ref} (V)	ΔV_{corner} %	Idd nA	PSRR 1kHz (dB)	TK ppm/°C	PW_{sr} (μs)
Oguey [126]	0.305	+/- 61	2.1	-12	2950	249
Vita [124]	0.521	+/- 31	53	-30	1580	362
Cheng [122]	0.466	+/- 29.6	133	-43	1770	457
Fiori [121]	1.5	+/- 21	294	-45	342	283
Bgp	1.21	+/- 1.5	878	-31	105	504

- Chengs reference achieves the highest PSRR [1] at 1 kHz with a moderate power consumption.
- The reference with the lowest temperature coefficient is the one presented by Fiori

7.4.3 Voltage reference selection

A comparison of reference circuits at simulation level has been carried out for a better understanding of the above mentioned best references. Four mentioned current references schematics have been introduced in cadence, using the same technology process. Additionally, a low current consumption bandgap reference has been also compared with the four cited references.

The following magnitudes were evaluated for all the technology corners:

- IDD: Current consumption of the reference.
- V_{ref}: Output reference voltage.
- ΔV_{corner}: Variation of the output reference voltage with the technology corners.
- $PSRR@1kHz$: Defines the relative feed through of the power supply change to the reference voltage change in dB.
- TK: Temperature coefficient (TK) is defined as:

$$TK = \left(\frac{V_{1.8V_{max}} - V_{1.8V_{min}}}{T_{max} - T_{min}} \frac{1}{V_{1.8V_{27C}}} \right) 10^6 [ppm/^\circ C] \tag{7.4}$$

- PW_{SR}: The Power Slew Rate is the Required time by the circuit to produce the reference voltage.

The result of the voltage references comparison is sumarized in Table 7.2. From the results can be inferred that V_{ref} is very unstable with the technology corners in ultra–low power consumption references implemented without bipolar transistors (Oguey [126], Vita [124], Cheng [122] and Fiori [121]). This is because they are implemented with CMOS transistors working in sub–threshold region [129]. Transistors working in this

[1] Power Supply Rejection Ratio.

region present a behaviour with the temperature similar to bipolar transistors. The problem is that the polarization margin is very reduced around 80 mV under the threshold voltage, consequently, transistors in this region are very sensible to changes in the size and geometry. In other words, a stable polarization point can not be assure for all the technology corners.

On the other hand, bandgap references are very stable with technology corners, since they use bipolar transistors. This kind of transistor are generally easier to polarize and very insensible to variations with temperature and technology corners. The drawback of bandgap reference is its higher current consumption, slower response and moderate PSRR regarding to the rest of references.

Oguey's reference presents the lowest current consumption, but an unacceptable variation on V_{ref} with corners and temperature. In addtion, Vita's reference consumes also very low current but the rest of features are still very bad. Cheng and Fiori offer an intermediate solution, since the current consumption is moderate whereas the corner variation and temperature coefficient are better.

Bandgap reference offers a very stable voltage reference, both with the temperature and with the technology corners at the expenses of a higher current consumption. Its behavior in terms of $PSRR$ and PW_{sr} are moderate, but these characteristics are not crucial for passive RFID applications. The rest of references present a lower current consumption but a high sensibility of V_{ref} with temperature and corner variations. As a conclusion, the most appropriate reference for generating a stable supply voltage are Cheng and Fiori from the point of view of current consumption and bandgap in terms of V_{ref} variations with technology corners.

7.5 Previous analysis: LDO design trade–offs

This section describes general LDO design trade–offs applied to the particular characteristics of passive RFID sensors.

7.5.1 Stability analysis

Figure 7.5 shows the elements that determine the stability of the system, namely, the error amplifier, pass element, feedback network, an output load current and associated resistor, an output capacitor and associated electrically series resistance (R_{es}).

Breaking the feedback loop at "A" in Figure 7.5, the open–loop gain ($\frac{V_{ref}}{V_{fb}}$) is:

$$\frac{V_{ref}}{V_{fb}} = |A_v| = \frac{g_{ma} R_{oa} g_{mb} Z}{1 + sR_{oa}C_{par}} \frac{R_1}{R_1 + R_2} \tag{7.5}$$

Where, g_{ma} and g_{mb} refer to the transconductance of the amplifier and the pass element, R_{oa} is the output impedance of the amplifier, C_{par} refers to the parasitic capacitance introduced by the pass element, and Z is the impedance seen at V_{out},

$$Z = R_{o-pass} || (Z_1 + Z_2) || \frac{sC_o R_e s + 1}{sC_o} \tag{7.6}$$

For the majority of load–current range the term $(Z_1 + Z_2)$ in Equation 7.6 can be neglected since $R_{o-pass} << Re(Z_1 + Z_2)$ and $\frac{1}{SC_o} >> Re(Z_1 + Z_2)$. After this

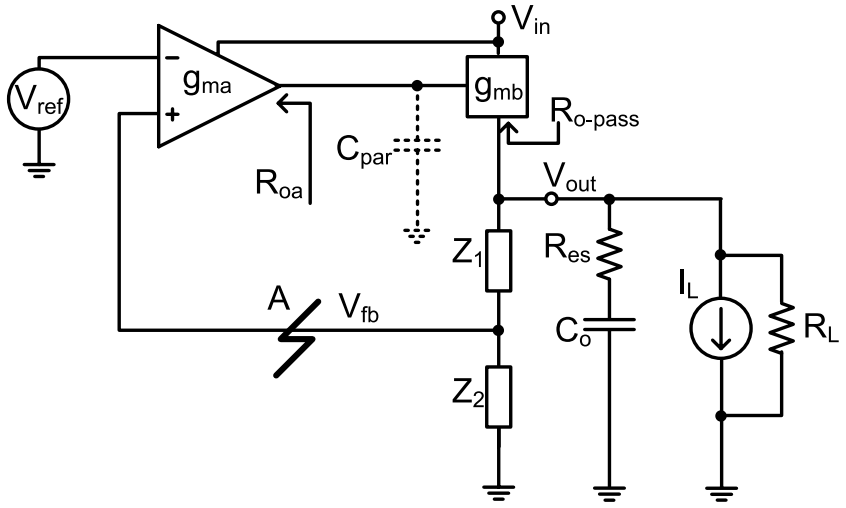

Figure 7.5: Elements that determine the stability of the low dropout regultator.

assumption, the poles and the zeros of the transfer function can be approximated to the following:

$$P_1 = \frac{1}{2\pi C_{oR_{o-pass}}} \tag{7.7}$$

$$P_2 = \frac{1}{2\pi R_{oa} C_{par}} \tag{7.8}$$

$$Z_1 = \frac{1}{2\pi C_o R_{esr}} \tag{7.9}$$

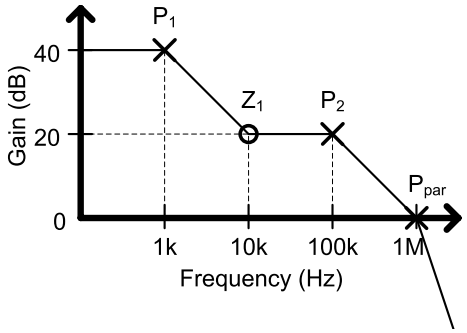

Figure 7.6: Typical frequency response of the low dropout regultator.

Figure 7.6 illustrates the typical frequency response of the system. The regulator yields better load regulation performance as the open–loop gain increases; however, the gain is limited by the close–loop bandwidth of the system, equivalent to the unity gain frequency (UGF). The minimum UGF is bounded by the response time required to yield an allowable output voltage variation during a transient load–current step, which was discussed in the specification section. Furthermore, the maximum UGF is also bounded by the parasitic poles of the system, i.e., poles included by the feedback network and internal poles of the amplifier. If the parasitic poles are assumed to be at higher frequencies than 1 MHz, then the gain at 10 kHz has to be less than 40 – 45 dB depending on

the location of Z_1 and P_2, assuming the conditions illustrated in Figure 7.6. Moreover, the pass element associated input capacitance (error amplifier load capacitance) is significantly large. This places a ceiling on the value of the amplifier output impedance (R_{oa}). The pass element typically needs to be a large device to yield low dropout voltages and high output current characteristics.

7.5.2 Transient analysis

An important specification is the maximum allowable output voltage change for a full range transient load–current step. The application determines how low this value is required to be. For the particular case of RFID sensor, transient load–currents are caused by the peak current of the digital circuits or by the turn on/off of the sensor. It is clear that the minimum voltage reached at the output voltage change can not fall under the minimum supply voltage allowed by the technology.

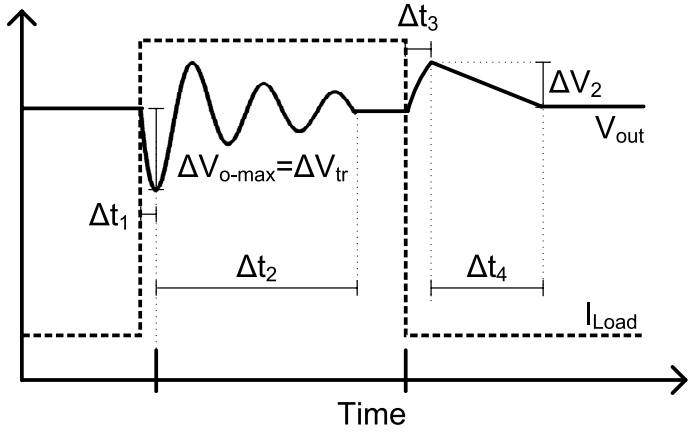

Figure 7.7: Transient response of the low dropout regultator.

Figure 7.7 shows the characteristic nature of the stimulus and the typical respective response. The time required for the loop to respond (Δt_1) (ideally the reciprocal of the closed–loop bandwidth) is specified by the output capacitor, maximum load–current, and maximum allowable output voltage variation. However, in typical implementations the time is prolonged by the internal slew–rate associated with the parasitic capacitance (C_{par}) of the pass element in Figure 7.5. The resulting time can be approximated to

$$\Delta t_1 \approx \frac{1}{BW_{cl}} + t_{sr} = \frac{1}{BW_{cl}} + C_{par}\frac{\Delta V}{I_{sr}} \tag{7.10}$$

where, BW_{cl} is the close loop bandwidth of the system, t_r is the slew–rate time associated with C_{par}, ΔV is the voltage variation at C_{par}, and I_{sr} is the slew–rate limited current. Particularizing for the case of RFID sensors, and assuming that BW_{cl} is 500 kHz, C_{par} is 200 fF, ΔV is 0.5 V, I_{sr} is 5 nA, C_o is 1 nF, and I_{o-max} is 50 μA, then the maximum output voltage variation due to a transient load change is 1.1 V (from Equation 7.10). Notice that if the minimum voltage required by the technology to work is 1.2 V, then the required input voltage to assure that the supply voltage does not fall under this minimum with sharp load transitions is 2.2 V. Therefore, the transient response restriction will dominate the minimum V_{DC} restriction over the dropout voltage. However, ΔV_{tr} can be reduced. If the slew–rate current is large enough, the reciprocal of the close–loop

Table 7.3: Comparison of pass elements structures

	Darlington	NPN	PNP	NMOS	PMOS
I_{o-max}	High	High	High	Medium	Medium
I_q	Medium	Medium	Large	Low	Low
$V_{drop-out}$	$V_{sat}+2V_{be}$	$V_{sat}+V_{be}$	V_{ec-sat}	$V_{sat}+V_{gs}$	V_{sd-sat}
Speed	Fast	Fast	Slow	Medium	Medium

bandwidth starts to dominate Δt_1. This would be at the cost of quiescent current. On the other hand, reducing the size of the pass device reduces value of C_{par}, In this case the price to pay is a reduction in I_{0-max}.

7.5.3 Pass device

There are five basic possible configurations for the pass element, namely NPN Darglington, NPN follower, common emitter lateral PNP, NMOS follower and common source PMOS transistor [114]. The degree of freedom for the choice of topology is dependent on the process technology and the requirements imposed by the RFID sensor.

Table 7.3 shows a comparison between the different pass elements with respect to their applicable LDO performance parameters. Bipolar devices are capable of delivering the highest output currents for a given supply voltage with the faster response time. On the other hand, the output current capabilities per unit area of MOS transistors exhibit limited performance with high dependencies on aspect ratio and gate drive. However, the voltage driven nature of MOS devices is beneficial in minimizing quiescent current. As the bipolar transistors are current driven devices, they will require a relative high base current from the error amplifier, in other words higher quiescent current. For the particular case of RFID sensors, quiescent current is a decisive factor, whereas output current and transient response are not so critical aspects. On the one side, the moderate response time of MOS transistor can be reduced minimizing its size. On the other, the output current required to supply the system is reduced (under 100 μA DC current) and, can be easily driven by small MOS transistors. In conclusion, MOS transistors are better choice than bipolar ones as pass devices.

Lowest dropout voltages are achieved by PMOS (V_{sd-sat}), approximately, 0.1 V. At this point the performance of PMOS is better than NMOS one, since the dropout voltage of the latter is increased by the V_{th} resulting a dropout of around 0.6 V in a 0.35 μm CMOS process. Although the NMOS transistors are faster and capable of deliver higher current than PMOS, the latter are the best overall choice for LDO regulators used in ERS of RFID sensors. They yield a good compromise of dropout voltage, quiescent current, output current, and speed.

7.5.4 Error amplifier

The specifications of the amplifier that are relevant to the LDO are: output impedance, gain, bandwidth, output slew–rate current, output voltage swing, and quiescent current. The output impedance must be low enough so as to place the parasitic pole P_{par} (Figure 7.6) at a frequency greater than the unity gain frequency, thus maintaining stability.

The requirement is not very stringent in RFID sensor applications where the current consumption does not exceed some tens of μAmps. Such a low currents can be delivered by a small pass device which does not introduce a great load capacitance. Load regulation performance is enhanced as the open–loop gain of the system is increased, as shown in Equation 7.3. However the gain is limited by the unity gain frequency. The topology and the biasing current of the amplifier are designed according to the frequency and the transient response requirements of the system. Transient specifications dominate the bias current demands of the amplifier. The choice in topology also reflects the driving requirements of the pass device. For instance, a PMOS pass device requires a high negative voltage swing to yield maximum gate drive and thus produce large output currents and low dropout voltages.

The overall design of the amplifier must be kept as simple as the specifications will allow in order to minimize quiescent currents. The limiting factors for low quiescent current are amplifier bandwidth and slew–rate requirements.

A simple differential pair with MOS loads [95] has been used to implement the error amplifier used in the LDO regulator for ERS of the RFID sensor. Following reasons motivate this choice.

- Simplicity and low power consumption. In comparison with other OP structures (Telescopic, folded cascoded,...), the differential pair is the simplest and the most power saving one [95].
- high voltage swing. This is require to achieve maximum pass device drive.
- simply biasing and high linearity. The differential pair does not require complex biasing circuit due to its simplicity. The high linearity between input and ouput improve the feedback regulation.

7.6 LDO design for passive RFID sensors

This section presents the design procedure to implement voltage regulators used in the ERS of passive RFID sensors. The specifications presented in Chapter 4 and the above described design trade–offs are the starting point.

The specifications introduced in Section 4.5.7 are briefly described below:

1. Dropout $\approx$ 0.1 V. At this point is clear that the only pass device that fulfils this requirement is the PMOS transistor.
2. V_{dd}=1.8 V and V_{aa}=1.2 V. The EEPROM requires a minimum supply voltage(V_{dd}) of 1.8 V, whereas the rest of circuits can work at lower supply voltages (V_{aa}=1.2 V). By setting two different supply voltages two goals are reached. First, the EEPROM can be turned off when not used, and second, a lower supply voltage can be used for the rest of circuits.
3. $I_{consumption} < 2\mu$ A. This is the estimated current consumption of the complete LDO regulator.

From the specification can be inferred that two LDO structures are required to generate two supply voltages (V_{aa} and V_{dd}). For implementing each regulator following elements must be defined according to the corresponding parameters, see Table 7.4.

Table 7.4: Design parameters for LDO regulator elements

LDO regulator Element	Design Parameters
Feedback network	AC behavior, current consumption, V_{out}
C_{out}	AC and transient behavior, area consumption
Pass device	AC behavior, dropout, output current
Amplifier	transient behavior, current consumption

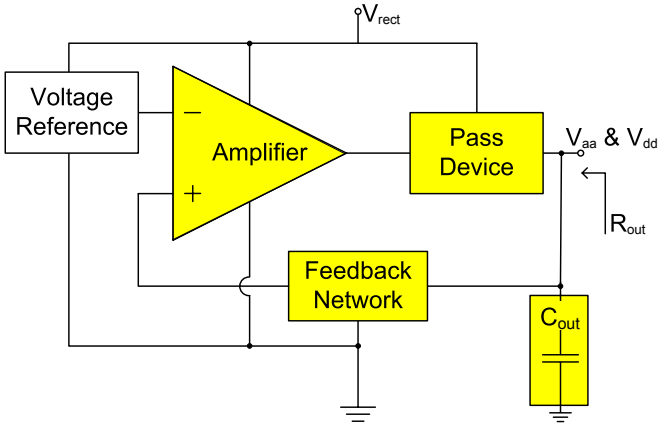

Figure 7.8: Elements to be defined in the design of a LDO regulator.

7.6.1 Feedback network

Feedback network can be implemented with capacitors or with resistances. Resistive feedback networks do not introduce any poles in the system. However, current flow trough the resistances to ground, i. e. quiescent current increases. On the other side, through capacitive feedback networks do not flow any DC current, since capacitors in DC are open circuits. The drawback of capacitors is that AC system behavior degrades. But, as show Figure 7.5, the feedback network is in parallel to the output capacitor (C_{out}). Hence, the effect of the capacitive feedback network can be neglected considering that:

$$C_{out} >> C_{fbn} \tag{7.11}$$

where C_{fbn} is the series equivalent of the two capacitors that form the feedback network. To conclude, since the capacitive feedback network do not increase the quiescent current and do not degrade, excessively, the AC system behaviour, capacitors are used to implement the feedback network.

Assuming the principle of virtual ground of the operational amplifiers, the value of C_1 and C_2 can be easily deduced from Figure 7.9 as:

$$V_{out} = V_{ref}\frac{C_1 + C_2}{C_1} \tag{7.12}$$

where, V_{ref} depends on the voltage reference used, V_{out} is the supply voltage (V_{dd} for the EEPROM and V_{aa} for the rest of the circuits). At this point, it is only needed the value of C_{out}, to calculate C_1 and C_2.

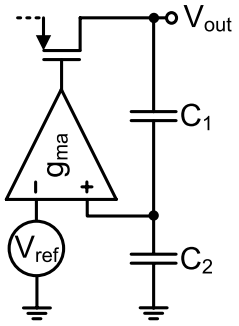

Figure 7.9: Feedback network.

Table 7.5: Paramenters required to calculte C_{out}.

Magnitude	Value
Peak current	400μA
Peak duration	50ns
Max. area of C_{out}	100pF
Min. V_{out}	V_{aa}=1.2V; V_{dd}=1.8V

7.6.2 Output capacitor (C_{out})

The transient requirement imposed by the current peaks of digital circuitry can not be fulfilled by the amplifier, since it is not fast enough. Consequently, an output capacitor (C_{out}) is required. Table 7.5 lists the values required to calculate of C_{out}. The current peak and peak duration were obtained by post–layout simulations of the digital part [130], whereas maximal area and minimum V_{out} are set by the technology process.

The restriction imposed by the maximal capacitor area limits the value of C_{out} to 100 pF. From the capacitor discharge formula [131] V_{out} is calculated and fall around 300 mV with a current peak. Consequently the V_{aa} and V_{dd} must be set at least 300 mV over the minimum supply voltage allowed by the process to work, hence to make the system more robust against to process variations V_{aa}=1.6 V and V_{dd}=2.1 V.

Figure 7.10 shows the behavior of V_{dd} and V_{aa} with current peaks when using different values of C_{out}. A capacitor of around 100 pF is required to maintain V_{dd} above 1.8 V for the generation of V_{dd}. Whereas C_{out} can be reduced to 50 pF for the analog supply voltage.

7.6.3 Pass device

The most suitable pass device for RFID sensor application is the PMOS transistor, as already deduced (see subsection 7.6.3). The reasons are low dropout and low current requirements of the application. The pass device must be able to drive an average DC currents of 50μA and a peak current of 400 μA. Transistor dimensions are calculated from these values.

The regulation limit is defined as the point where $V_{rect} = V_{out} + V_{drop}$, and if V_{rect} goes down the circuit stops regulating, see Figure 7.11.a. The regulation limit is also for

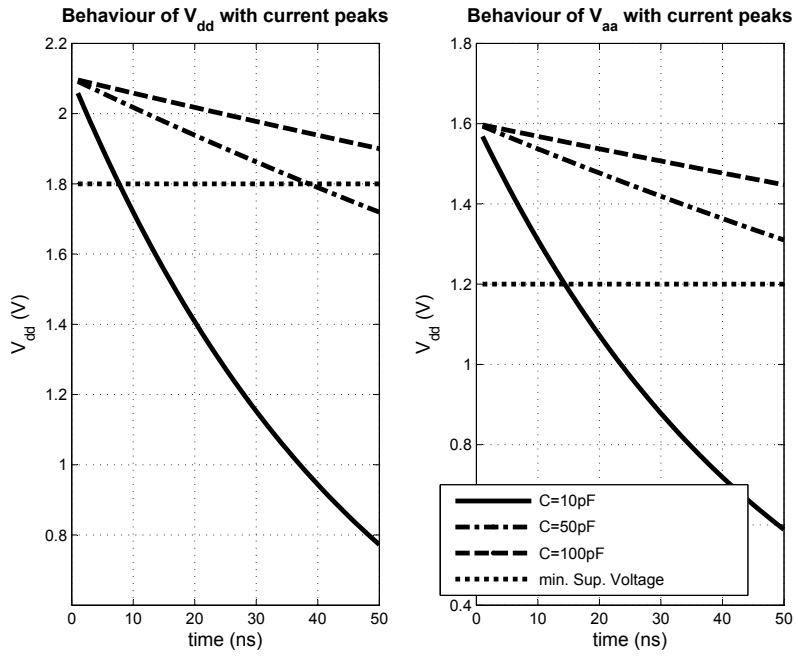

Figure 7.10: Behavior of V_{dd} and V_{aa} with current peaks when using different values of C_{out}.

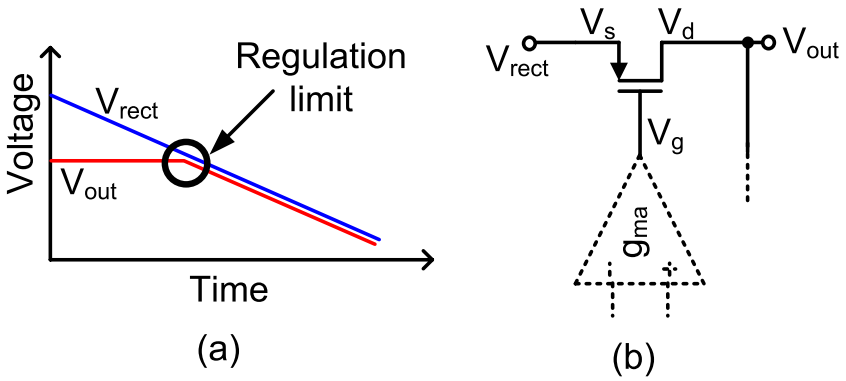

Figure 7.11: (a) Graphical description of the regulation limit, (b) pass device terminals.

the pass device the boundary between saturation and lineal region, notice that at this point V_{ds} is equal to $-V_{drop}$.

In the regulation limit, the pass device must be able to deliver 50 μA. Hence, since the drain current of a PMOS transistor in Saturation region is:

$$I_d = -\frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \tag{7.13}$$

where, μ_p (mobility of holes), C_{ox} (gate oxide capacitance per unit area) and V_{th} (transistor threshold voltage) are specified by the technology process, W and L are transistor width and length respectively. As already deduce, in the limit between saturation and lineal region V_{drop} is:

$$V_{drop} = V_{ds} = V_{gs} - V_{th} \tag{7.14}$$

where V_{ds} is the drop voltage between the drain and source PMOS terminals. Hence the aspect ratio of the pass device is:

$$\frac{W}{L} = \frac{2I_d}{\mu_p C_{ox} V_{drop}^2} \tag{7.15}$$

To minimize the device capacitance, the minimum length of each transistor is chosen, obtaining the corresponding width.

At this point it is necessary to check if, the pass device is able to deliver the peak current without to violate the minimum supply voltage in the regulation limit. From Equation 7.13, the pass device delivers a maximal current of 50 μA in the regulation limit and in Saturation region. But what happen when a current peak occurs? Since the pass device is not able to deliver this current to the load in saturation, the transistor goes in the lineal region and V_{out} decreases.

Now, how much V_{out} has to decrease to allow the pass device to deliver 400 μA? Assuming that I_d of a PMOS transistor in the linear region is:

$$I_d = -\mu_p C_{ox}\frac{W}{L}((V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2) \tag{7.16}$$

and considering $V_{ds} = V_{rect} - V_{out}$ and $V_{out} > 1.2$ V, consequently $V_{ds} < 0.5$ V. Hence, V_{gs} can be found assuming $I_d = 400\mu$A from Equation . Looking to Figure 7.11.b, it is clear that $V_s = V_{rect}$. Finally, If V_g is inside the output swing range of the amplifier then V_{out} will not fall under 1.2 V or 1.8 V, respectively, due to peak currents in the regulation limit.

To sumarize, the dimensioning of Pass Device is split into two steps:

1. Calculate the transistor aspect ratio ($\frac{W}{L}$) from the transistor saturation equation,
2. Check that V_{out} does not fall under the minimum supply voltage under the worst condions, i.e., when the transistor goes into Lineal region.

7.6.4 Amplifier

Figure 7.12 shows the schematic of the error amplifier. As already discussed (see Subsection 7.5.4), the differential pair with active current mirror was the chosen topology to implement the error amplifier. Dimensions of transistors M1–M4 and I_x are the design variables of the circuit.

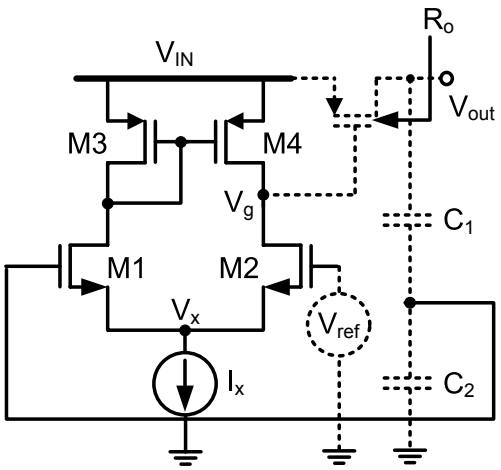

Figure 7.12: Error amplifier schematic.

Two parameters must be considered to set I_x. First, the quiescent current consumption and second the output slew–rate current required to drive the gate capacitance of the pass device in an acceptable time. Figure 7.13 depicts gate voltage of the pass device versus time for different I_x values. The voltage drop in V_g is 1 V and the gate capacitance is 2.5 fF, which is the gate capacitance of a PMOS transistor with aspect ratio W/L=60 and L=0.5 μm. As the graphic shows, I_x=100 nA is not sufficient to drive the transistor in a time lower than 40 ns, which is the maximum time that C_{out} can maintain the output voltage over the limit. The response time is reduced by increasing the I_x, as can be seen by I_x=200 nA and 400 nA. The value of 200 nA will be chosen since it is a trade–off between quiescent current and transient response of pass device.

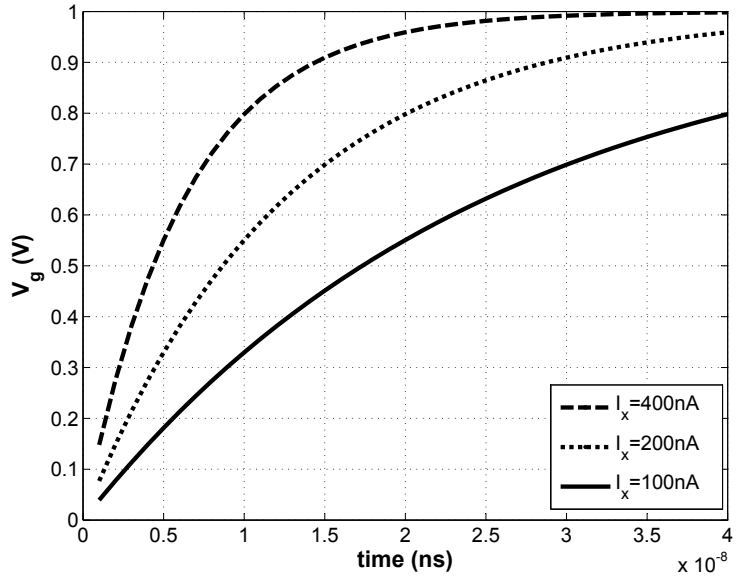

Figure 7.13: Delay in V_g of pass device for different bias currents in the amplifier (C_g=2.5 fF). The voltage drop on the gate of the pass device goes from 0 to 1 V.

The size of the transistors determines the open loop gain (A_{ol}), and will influences

the output resistance of the regulator as illustrate Ec. 7.3:

$$R_o = \frac{R_{o-pass}}{1 + A_{ol}\beta} \tag{7.17}$$

Since RFID sensor supply current (I_o) is in the order of few tens of microamperes, R_o is not a critical parameter. Output resistances up to 1 kΩ would be enough. Consequently, the open loop gain of the amplifier is not a limiting factor, and there are not great restrictions for dimensioning transistors M1–M4. Other parameters are considered for dimensioning transistors; first, M1–M4 will be dimensioned identical to improve the symmetry of the circuit. And second, to minimize the device capacitances, transistor with minimal length will be chosen. Finally the transistor wide is can be defined from R_o. Hence, R_{o-pass} is easily calculated, assuming from [95] that:

$$R_{o-pass} = \frac{1}{\lambda I_o} \tag{7.18}$$

where λ is the channel–length modulation coefficient, whose typical value is 0.5. Hence, $R_{o-pass} = 40\ k\Omega$ assuming $I_o = 50\ \mu$A.

On the other hand, feedback factor was determined in section 7.6.1 as:

$$\beta = \frac{C_1 + C_2}{C_1} = \frac{V_{ref}}{V_{out}} \tag{7.19}$$

Notice that each supply voltage has different feedback factor:

$$\beta_a a = \frac{V_{ref}}{V_{aa}} = \frac{1.2V}{1.6V} = 0.75\ \beta_d d = \frac{V_{ref}}{V_{dd}} = \frac{1.2V}{2.2V} = 0.56 \tag{7.20}$$

The open loop gain of a differential pair with an active current mirror is [95]:

$$A_{ol} = g_{mM2}(r_{OM2}||r_{OM4}) \tag{7.21}$$

where

$$g_{mM2} = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} \tag{7.22}$$

and

$$r_{OM2} = \frac{1}{\lambda I_{DM2}} \tag{7.23}$$

Since $I_{DM2} = 100$ nA and $\mu_n C_{ox} \approx 165\ \mu A/V^2$ for the chosen process, A_{ol} will be 81 if M1–M4 are dimensioned with $\frac{W}{L} = 2$. Notice that, for this A_{ol}, the output impedance of the regulator is 655 Ω. This value of output impedance is sufficient to deliver currents of some tens of microamperes required for the RFID sensor supply.

7.7 Results

Two generations of voltage regulators have been implemented and fabricated in the process XL035 of XFAB following the exposed design guidelines.

The first generation of LDO–Regulators were designed using the voltage reference of Fiori for digital supply (V_{aa}=2.2 V) and the reference of Cheng for analog supply

Table 7.6: Paramenters required to calculte C_{out}

Design	V_{aa} 1st gen.	V_{dd} 1st gen.	V_{aa} $2^n d$ gen.	V_{dd} $2^n d$ gen.
V_{out} (V)	1.6	2.2	1.6	2.2
C_{out} (pF)	50	100	50	100
Pass Device (PMOS)				
PMOS W/L ($\mu m/\mu m$)	5x6/0.5	5x6/0.5	5x6/0.5	5x6/0.5
Reference (V)	0.466(Cheng)	1.5 (Fiori)	1.2 (bandgap)	1.2 (bandgap)
Feedback network				
C_1 (pF)	5	15	14	8
C_2 (pF)	12	7	6	7
Amplifier				
M1 W/L ($\mu m/\mu m$)	1/0.5	1/0.5	1/0.5	1/0.5
M2 W/L ($\mu m/\mu m$)	1/0.5	1/0.5	1/0.5	1/0.5
M3 W/L ($\mu m/\mu m$)	1/0.5	1/0.5	1/0.5	1/0.5
M4 W/L ($\mu m/\mu m$)	1/0.5	1/0.5	1/0.5	1/0.5
I_x (nA)	100	100	200	200

(V_{aa}=1.6 V), see Table 7.2. The Bandgap voltage reference is used as reference for the second generation of Regulators.

Full CMOS voltage reference, i.e., without bipolar transistors, was chosen for the first test chip due to its lower current consumption. The reason of moving to a bandgap reference, in the second generation of regulators, is that EEPROM and Charge Pump require a bandgap reference to works. Consequently, a bandgap circuit must be included in the system to make use of the EEPROM. This reference was not necessary in the first test chip since only the analog front–end was implemented.

Table 7.6 presents the values of the design variables for the two generations of voltage regulators. Figure 7.14 depicts the 1.8 V regulator layout. As can be observed, the capacitors are the biggest devices. Feedback network has been implemented using arrays of poly–poly capacitors introducing some dummy devices, to maximize the symmetry and improve the matching under process deviations. On the other hand, high density capacitors are used as output capacitor to reduce the area consumption. The gate length in Amplifier and Pass Device is 0.15 μm over the minimal allowed by the process, for reduce the effect of corner deviations. Finally, a bias buffer is included in the layout to generate the desired I_x, from a current reference implemented to generate bias voltages for the whole analog front–end.

7.7.1 Simulations

The following magnitudes were evaluated for all the technology corners.

- V_{rect}: Unregulated voltage generated by rectifier. Notice that, from the point of view of the regulator, V_{rect} is at the same time input signal and supply voltage.

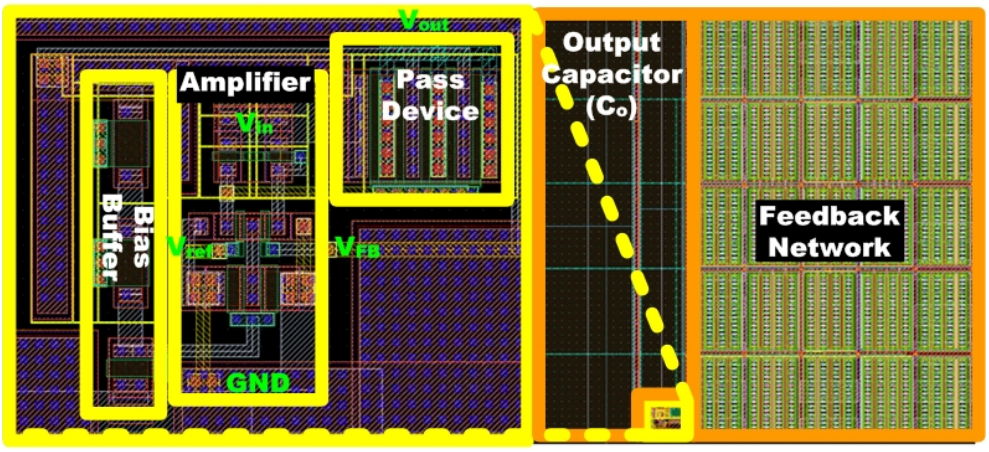

Figure 7.14: Layout of the 1.8 V voltage regulator.

- $I_{consumption}$: Current consumption of the regulator. Current consumption of references were included in the First Generation. However, current consumption of bandgap circuit and current reference were not included in Second Generation regulators, since they are shared by other circuits of the RFID sensor.
- V_{aa} and V_{dd}: Regulated output voltages, see Figure 7.15.
- $\Delta V_{out--Peak}$: Output voltage variation when a current peak of around 300-400 μA with a duration of 5 μs occurs.
- ΔV: Variation of the regulated out voltage when the supply voltage present a ripple of 0.5Vpp and with a frequency of 1 KHz, (see Figure 7.15).
- $PSFTP$[2]$@1KHz$: Defines the relative feed through of the power supply change to the reference voltage change in dB. Can be calculated from:

$$\Delta V_{aa} = V_{aa}x(\frac{\Delta V_{rect}}{\Delta V_{DD}})10^{(}\frac{PSFTP_{1kHz}}{20}) \tag{7.24}$$

- $\Delta V'$: Variation of the regulated out voltage when the temperature varies from -30°C to 120°C.
- TK: Temperature coefficient, defined as:

$$TK = \frac{(V_{aaMAX} - V_{aaMIN})}{(T_{MAX} - T_{MIN})}(\frac{1}{V_{aa}@27C})10^6(ppm) \tag{7.25}$$

- PW_{SR}: Power Slew Rate is the required time by the regulator to produce the regulated voltage. PW_{SR} is mostly dependent of the voltage reference circuit.

Next table illustrates the post–layout simulation results of the regulators. The input signal of the regulator has been simulated as a pulse that switches between cero (supply capacitor discharged) and 2.8 V (supply capacitor charged). The transition between cero and 2.8 V is $500\mu s$. in order to simulate the charge of the supply capacitor. An

[2]Power Supply Feed Through Performance.

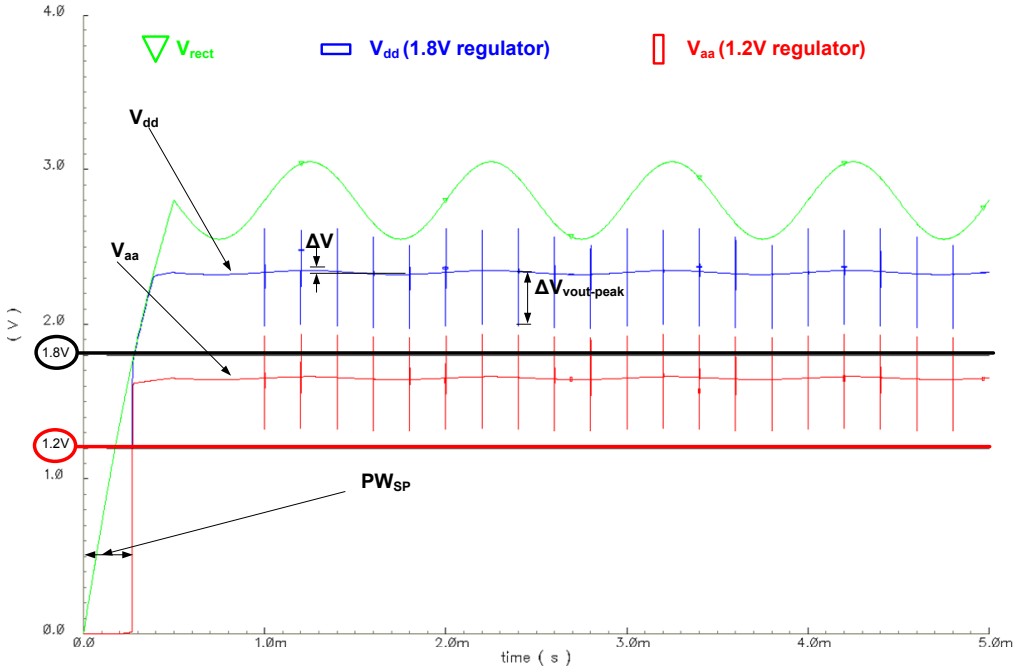

Figure 7.15: Graphical description of the simulated magnitudes to evaluate the Regulator performance.

additional ripple of 500 mV at 1 kHz has been added to V_{rect} for measuring $PSFTP_{1kHz}$ and line regulation. Two resistances load the regulator with $54.7\ k\Omega$. A switch is placed between the resistance and ground for current peaks generation (see Figure 7.16.

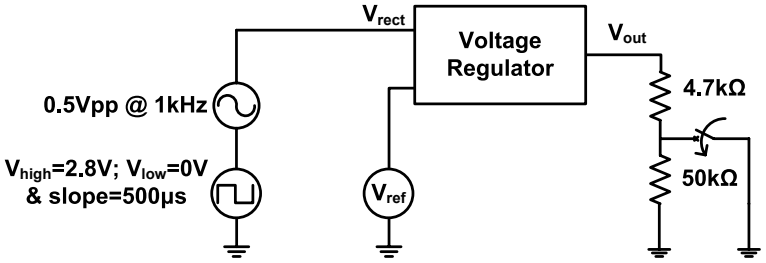

Figure 7.16: Simulation setup for LDO regulator characterization.

1^{st} Generation regulators present a current consumption of 300 nA (1.8 V regulator) and 178 nA (1.2 V regulator), 100 nA correspond to the quiescent current through the amplifier and the rest is the static current consumption of the voltage reference. The current consumption is different, since each regulator uses a kind of reference. 2^{nd} Generation regulators consume 295 nA. 200 nA through the error amplifier and 95 nA through the bias generator for I_x. Current consumption of bandgap reference was not included, the corner dispersion due to temperature and process variations is 100 nA.

V_{out} and $V_{out-Peak}$ values assure that regulated voltages are always above 1.8 V and 1.2 V respectively over all process corners and worst operating conditions. 1^{st} Generation regulators present a higher $V_{out-peak}$ than 2^{nd} generation ones, the reason is the lower

Table 7.7: 1^{st} Generation 1.2 V regulator (Cheng)

Corner	$I_{consumption}$ (nA)	V_{aa} (V)	$\Delta V_{out-peak}$ (V)	ΔV (mV)	PSFTP@1KHz (dB)	ΔV' (mV)	TK (ppm)	PW_{SR} (μs)
Typical	178	1.67	115	9	-30.41	105.5	1174.5	269
Corner dispersion	115	0.5	84		7.00		378	204

Table 7.8: 1^{st} Generation 1.8 V Regulator (Fiori)

Corner	$I_{consumption}$ (nA)	V_{dd} (V)	$\Delta V_{out-peak}$ (V)	ΔV (mV)	PSFTP@1KHz (dB)	ΔV' (mV)	TK (ppm)	PW_{SR} (μs)
Typical	330	2.53	605	10	-33.1	93.7	1580.4	358
Corner dispersion	131	0.5	164		5.00		554	50

Table 7.9: 2^{nd} Generation 1.2 V Regulator (bandgap)

Corner	$I_{consumption}$ (nA)	V_{aa} (V)	$\Delta V_{out-peak}$ (V)	ΔV (mV)	PSFTP@1KHz (dB)	ΔV' (mV)	TK (ppm)	PW_{SR} (μs)
Typical	295	1.65	1.315	19.2	-23.72	22.9	251.9	269
Corner dispersion	205	0.1	0.13		17.00		167	204

Table 7.10: 2^{nd} Generation 1.8 V Regulator (bandgap)

Corner	$I_{consumption}$ (nA)	V_{dd} (V)	$\Delta V_{out-peak}$ (V)	ΔV (mV)	PSFTP@1KHz (dB)	ΔV' (mV)	TK (ppm)	PW_{SR} (μs)
Typical	295	2.34	1.975	27.36	-23.68	32.50	507	269
Corner dispersion	200	0.1	0.164		17.00		284	204

I_x through the amplifier. The consequence is the necessity of higher V_{out} to meet specifications of minimum V_{out}.

The line regulation (ΔV) and $PSFTP_{1kHz}$ is mostly caused by variations of V_{ref} with the input voltage. Notice that regulators reduce in around 7dB the original $PSFTP_{1kHz}$ of the voltage reference (see Table 7.2) as consequence of the body effect of the pass device.

In 2^{nd} Generation, 1.8 V regulator suffers a variation of 32.5 mV when temperature drops from -30 °C to 120 °C. Whereas the variation is 10 mV lower for the same temperature range for the case of 1.2 V regulator. The consequence is higher TK in V_{dd}. The reason is that the pass device drives more current for lower V_{ds}, this is the pass device polarization point is closer to the overdrive voltage ($V_{OD} = V_{gs} - V_{th}$). Consequently, the V_{dd} is more sensible to changes in the pass device's V_{th} due to temperature in degrading the TK.

Finally, the PW_{SR} is the time that the bandgap requires to generate the reference voltage, and is very dependent on the V_{rect}. The Higher V_{rect} is the shorter is PW_{SR}.

7.7.2 Measurements

Figure 7.17 shows the test chip, on the left side are placed the test circuits implemented for this Dissertation. In the middle of the chip is a complete analog front–end and on the right are the rest of the test circuits of the WISEN project that are not dealt on this PhD. Thesis.

Figure 7.17: Test chip microphotograph.

Test chips were bonded to a PCB board to carry out the measurements of the different circuit structures (see Figure 7.18).

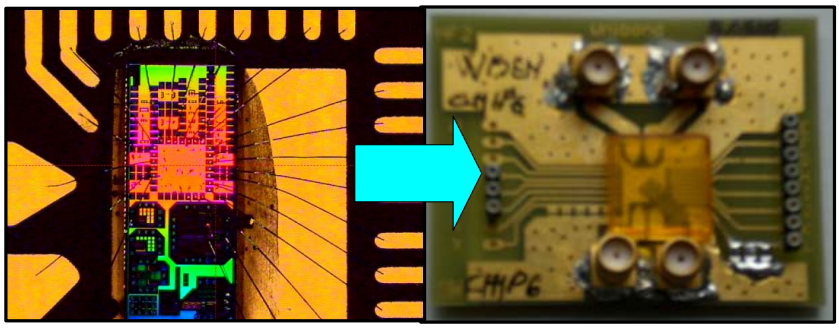

Figure 7.18: Test chip bonded to a PCB for measuring.

The measurement setup to characterize the regulators is showed below. Transient response, dropout, PSFTP and line regulation were measured with the test bench depicted in Figure 7.19.

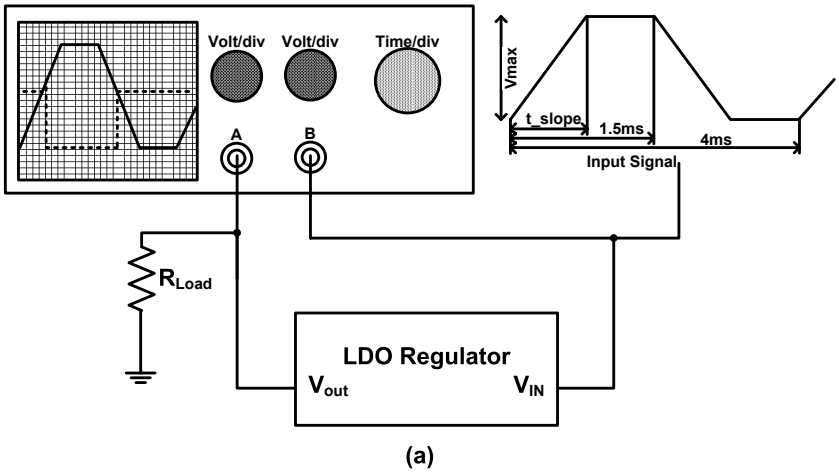

Figure 7.19: Test bench used for chip measurements.

Figure 7.20 shows an example of outputs obtained in the oscilloscope for the different measurements.

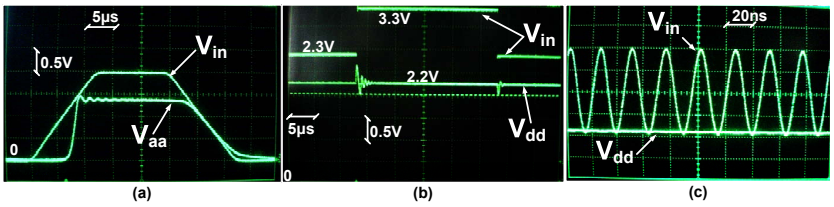

Figure 7.20: Output readed in the osciloscope for measuring: (a)settling time, drop out, (b) line regulation and c)PSFTP.

The static current consumption and regulation by current peaks, as well as regulated voltage were measured as illustrates Figure 7.21. A PMOS transistor driven by a square signal with a drain resistance was used for measuring $V_{out-Peak}$.

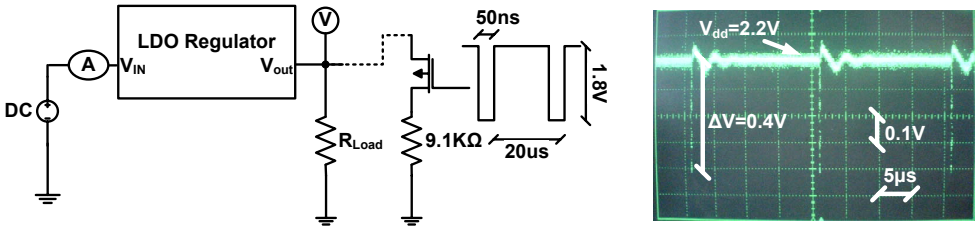

Figure 7.21: Test bench using for $V_{out-peak}$, current consumption and V_{out} measurements.

Figure 7.22 shows the regulated output voltage (V_{aa} and V_{dd}) versus V_{rect}, measured on three chips. Absolute value is 2.25 V with a variation due to technology process

Table 7.11: Measured performance of proposed voltage regulators

Regulator	Analog (1.2V)	Digital (1.8V)
V_{out} (V)	1.73	2.25
ΔV_{out} (mV)	537.5	212.5
$I_{Consumption}$ (nA)	90	240
PSRR@ 1kHz (dB)	-28.9	-30
Dropout (mV)	50	10
Settling time (μs)	5	5

of 60 mV. These measurements are in well agreement with values predicted in corner simulations.

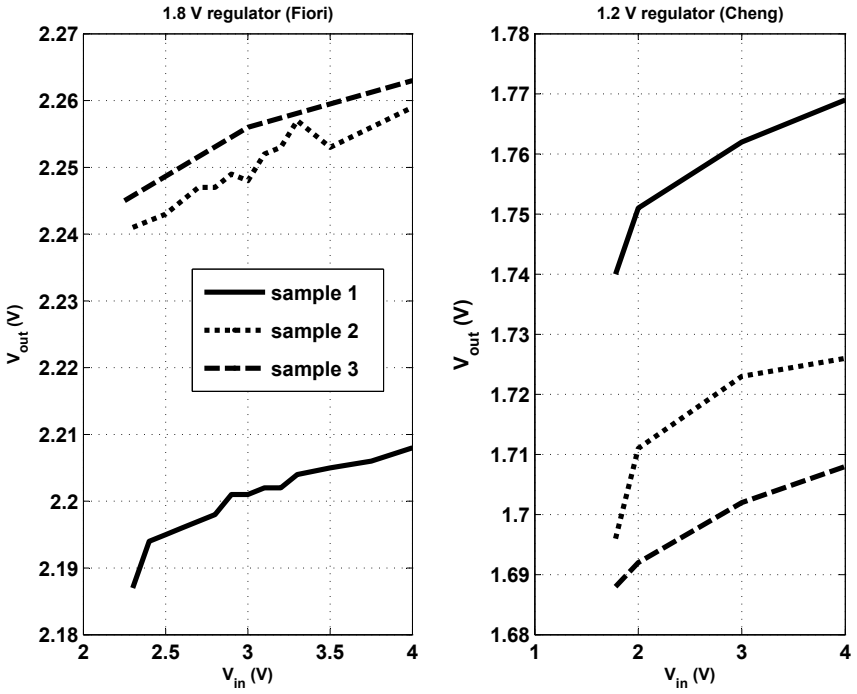

Figure 7.22: Measured regulated output voltage.

Table 7.11 summarizes the measurements of the fabricated regulators. The current consumption of the both regulators include voltage reference consumption. The measured results are inside de margins predicted in simulation. Notice that current consumption of 1.2 V regulator is 90 nA, a value close to a process corner. The consequence is a very low current through the error amplifier that delays the transient response of the regulator. As a result $V_{peak-out}$ increases considerably.

Dropout voltage is 50 mV for Analog and 10 mV for digital regulator. These values are below the maximal value of 100 mV specified in Chapter 4. The rest of measurements are in accordance with the simulated values.

Table 7.12 compares ultra–low power voltage regulators from the state–of–the–art

Table 7.12: Ultra–Low Power Voltage Regulators Comparison

Desing	Barnett [53]	Vita [54]	This Work
process	0.15 μm CMOS	0.35 μm CMOS	0.35 μm CMOS
$I_{Consumption}$ (nA)	110	34	240
Drop Out (mV)	-	30	10 & 50
Settling time (ms)	-	1.5	0.005
V_{out} (V)	1.25	0.605	2.2 & 1.2
Maximun output Current (μA)	-	5	>1000
Line Sensitivity (mV/V)	-	+/-0.8	4
TK(mV/$\circ$C)	-	2	1.5 & 1.1
ΔV_{out} (V)	0.1	-	0.1

with the ones designed in this Dissertation. Current consumption of proposed circuits is in the order of Barnett [53], who uses a technology with lower gate length. Vita [54], who works in 0.35μm reported a quiescent current of 34 nA, however the current consumption of the reference was not included. In terms of dropout, all designs are moving in the same range, from 10 mV to 50 mV. Regulators presented in this work are better than Vita in terms of settling time and maximum output current. From the point of view of ΔV_{out}, all the designs are moving in the same range. To conclude, just a remark, the effect of the current peaks due to digital circuits on the regulated output voltage was not dealt by the rest of authors. In this work, current peaks were a key design parameter since its effect is critical on the sensor supply voltage. Consequently, the critical effect of current peaks in RFID Sensors includes higher grade of difficulty than in the other designs.

7.7.3 Complete energy recovery system results

Figure 7.23 illustrates the microphotograph of the passive RFID analog front–end. The implemented components are the complete energy recovery system, ASK demodulator and Load modulator. The prototype was implemented in collaboration with CEIT, TECNUN and IIS Frauhofer. A complete description of the rest of the blocks inside the analog–front–end can be found in [98].

Figure 7.24 shows the measurements of the protection circuit and regulator together as a function of the voltage on the supply capacitor. The solid line is the supply voltage at the output of the regulator, once the voltage on the supply capacitor exceed the V_{aa} or V_{dd} plus dropout, the regulators begins to regulate. The dashed line depicts the current consumption of the regulator and high voltage protection. Before the protection threshold is reached the current consumption is only due to the regulator, under 400 nA. When voltage on the supply capacitor increases and exceeds the protection threshold, a current higher than 1 mA flows through the protection. The protection circuit switches to ground a resistance that discharges the supply capacitor when the protection threshold is reached. This explains the lineal behavior of the current consumption after threshold.

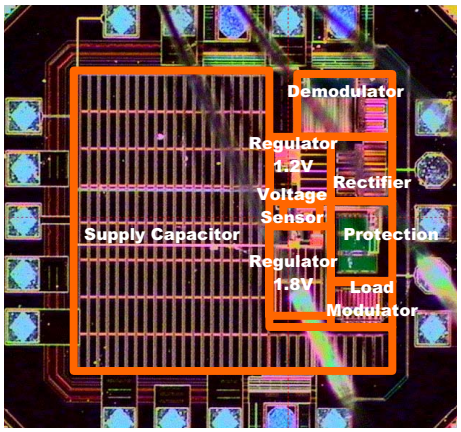

Figure 7.23: Analog Front–End photograph.

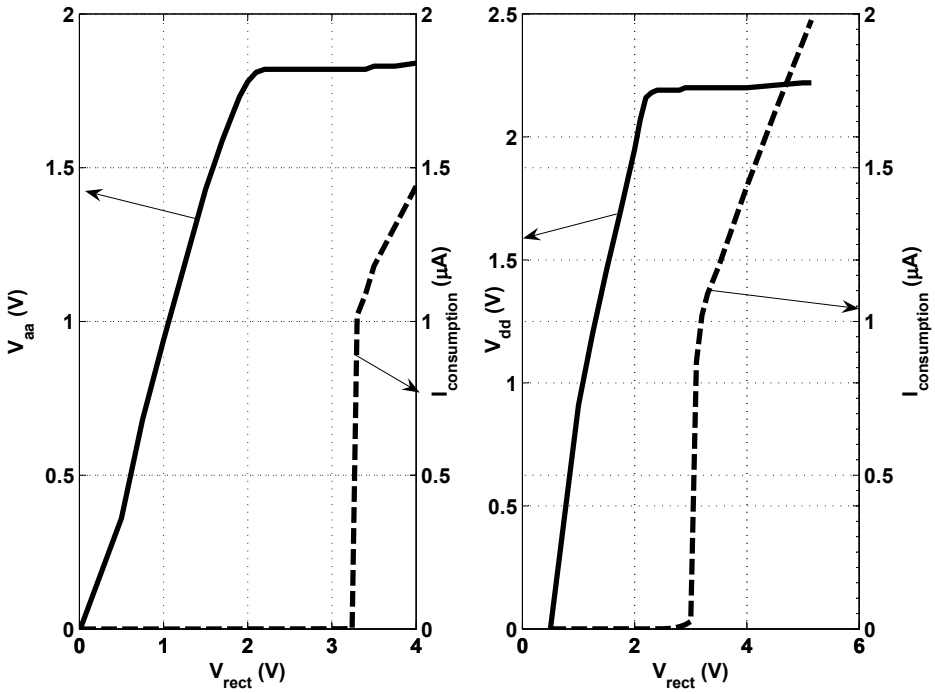

Figure 7.24: Measurements of high voltage protecction and regulators together.

7.8 Conclusions

The state–of–the–art of Supply voltage regulation in passive RFID tags has been analyzed and the reasons of using a voltage regulator in passive RFID sensor were exposed.

LDO regulator has been probed to be optimal regulator architecture for the application. The components of the architecture have been described and design trade–offs analyzed for the particular case of passive RFID sensors.

A detailed study and comparison of ultra low power consumption voltage references were carried out to find out the optimal references for the application.

A set of design rules for Designing LDO regulators for passive RFID sensors was defined.

Results of simulations and measurements on chip of LDO regulators have been presented and compared with the state–of–the–art achieving improvements in terms of stability and current consumption. Additionally, the effect of current peaks on the operation of regulators were analyzed, this key point was not dealt by the state–of–the–art proposed designs.

Finally, two voltage regulators (1.2 V and 1.8 V) have been integrated in the analog–front–end of the passive RFID sensor. Experimental measurements probe proper operation of regulator and the rest of the Energy Recovery System.

Chapter 8

Conclusions and Future Work

Contents

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The WISEN project has analyzed constrains and physical limits of integrating sensors with a full passive Transceiver. The transceiver is based on long range RFID systems and is not only responsible of the wireless communications of the sensor but also for the power recovery and generation. There were investigated plenty of areas in the frame of WISEN project as a result a number of publications [132, 133, 130], PhD. Dissertations [134, 135, 136] and patents of inventions [137, 138] were published.

8.1 Conclusions

This chapter gives a summary of the most relevant conclusions and results extracted from the investigations derived from this PhD. Dissertation.

Energy Recovery System Design Some restrictions and design specifications for the Energy Recovery System (ERS) have been derived from a meticulous analysis of the ERS carried out in this PhD. Dissertation. This specifications and reestrictions are Q factor under 9 to assure adequate input voltage, selection of the backscatter modulation, reasoned selection of technology process and definition of design parameters for the implementation of the circuital units (Rectifier, Voltage sensor, High Voltage protection and Voltage Regulator). The analysis of the input impedance versus the power consumption were published in the 3rd European Workshop on RFID System and Technologies [107].

Rectifier The detailed analysis of the state-of-the-art in rectifiers gave as result that the Dickson topology with Schottky diodes is the best choice to implement the AC into DC energy converter for RFID sensors. A design methodology maximizing to the power efficiency have been also proposed to implement rectifiers with the Dickson topology.

Moreover, it was proposed a mathematical model to characterize the operation of the rectifier in terms of input impedance, and output voltage as a function of the power requirements, technology and input power. The mathematical model was compared with simulations results to prove its feasibility in rectifier design. The average error of the model regarding to the simulations was 7.25% and 1.12% for real and imaginary

part of Zin, respectively, and 1.47% for the Vin. Model and simulation agreed well with experimental results of three rectifiers implemented in a XFAB 0.35μm low power process.

Rectifiers with 4, 6 and 8 stages were implemented and measured in the chosen technology, see Figure 8.1. The experimental results agree well with the theoretical ones.

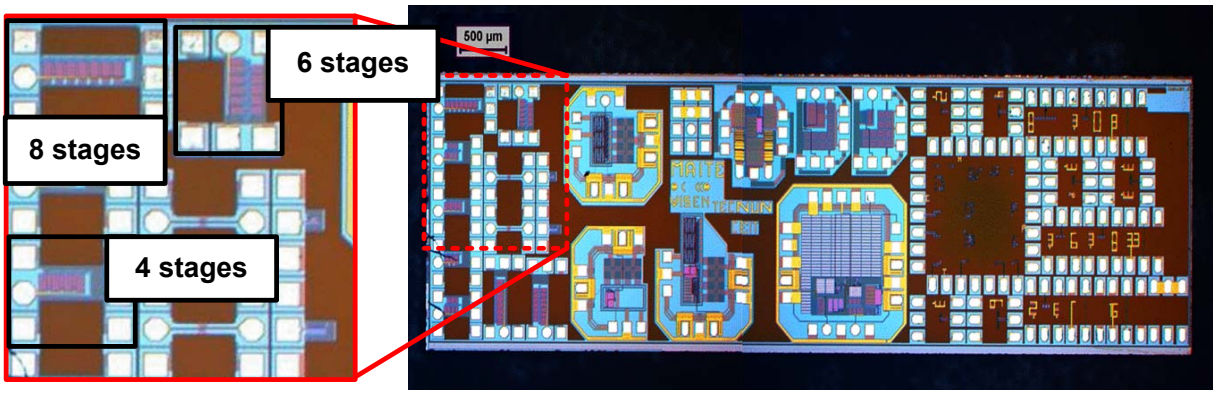

Figure 8.1: Input impedance versus stage number for a $V_{DC} = 2V$ and a load of 90 kΩ.

Voltage Sensor and High Voltage Protection Two novel Voltage Sensor circuits are proposed and its experimental on–chip measurements compared with the state-of-the-art alternatives, Figure 8.2 shows the microphotograph of the Voltage Sensors. The measured DC current consumption of the two novels structures is 69 nA and 0.2 nA at 3.3 V, that means a reduction in terms of current consumption of one order of magnitude in regard to previous reported results. The design of the novel circuits as well as its comparison with the state-of-the-art ones were published in international conferences [139, 140].

A novel Voltage Protection circuit based on [6], reported in the bibliography, have been implemented, fabricated and measured, see Figure 2.29. The on-chip measurements proved that the proposed circuit reduces in one order of magnitude the current consumption before the voltage threshold of the circuit is reached regarding to the state–of–the–art circuit. This analysis were published in the XXII International Conference on Design of Circuits and Integrated Systems [141].

Voltage Regulator LDO regulator has been probed to be the best regulator architecture for the application. Consquently, LDO regulators have been deeply studied as a result set of design rules for LDO regulators for passive RFID sensors have been defined.

Some voltage regulators have been designed, implemented, fabricated and measured (see Figure 2.29). Experimental Results of LDO regulators have been presented and compared with the state-of-the-art circuits, achieving improvements in terms of stability and current consumption. Additionally, the effect of current peaks on the operation of regulators were analyzed, this key point was not dealt by the state-of the-art proposed designs. Part of the results of this research were published in an International conference [142].

Finally, two voltage regulators (1.2 V and 1.8 V) have been integrated in the analogfront-end of the passive RFID sensor. Experimental measurements probe proper operation of

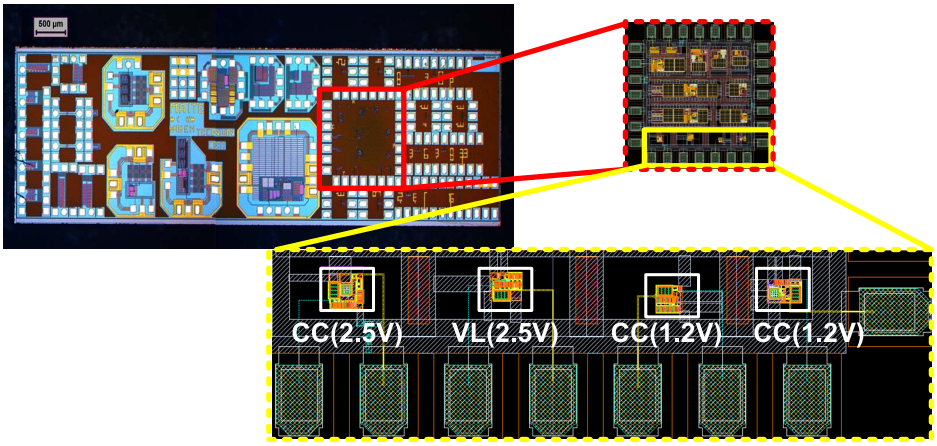

Figure 8.2: Microphotograph of the complete test chip and details of the voltage sensors.

regulator and the rest of the ERS. The complete analog front-end design, where the two voltage regulators are integrated, is the topic of a paper published in the IEEE International Conference on RFID [98].

Figure 8.3: Test chip Microphotograph.

8.2 Future Work

The most interesting parameters to improve in the energy recovery and stabilization system of RFID sensors are the operation range and the power available at the output of the system. In order to achieve this goals the future work can be divide into following points:

- Increase the AC into DC power conversion efficiency. This is, improving the Dickson rectifier. The improvements in the rectifier can be carried out in two directions:

    1. Doing research to improve the technology process in order to: first fabricate Schottky diodes with lower parasitic capacitance (C_D) and lower forward resistance (R_f) but keeping a high reverse resistance (R_r). (see Figure 8.4). And second, improve the process to achieve capacitors with lower parasitic resistance and capacitances.

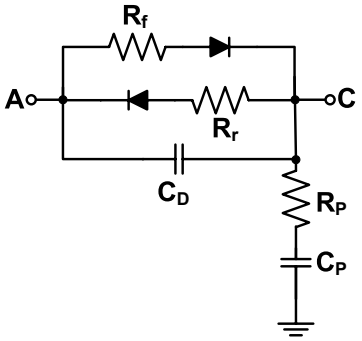

Figure 8.4: RF–model of an integrated Schottky diode[2].

    2. Another research line is to improve the architecture, this is, develop new circuits with higher power conversion efficiency than Dickson topology.

- Reduce the power consumption of the Chip. Working in this research line implies the use of a costly last generation technology process with lower operation voltage, which makes possible the design of lower consumption. An option would be Silicon on Isolator (SOI) processes, where the parasitic loses are dramatically reduced regarding to the typical CMOS processes, this way the consumption can be optimized.

- Another option to increase the operation range of the RFID sensors would be to include an additional power source, like a battery. This voltage source would be used to polarize the switches of the rectifier increasing this way de efficiency of the energy conversion. The batteries could be also used to supply particular circuital blocks of the system like the sensor. The rest of RFID transponder blocks could be further supplied by the RF power.

- The design and implementation of an Analog–Digital Converter (ADC) of ultra low power consumption would be an additional circuit to include in the RFID sensor, which would suppose an additional research line. Including an ADC with moderate resolution and very low consumption in the RFID sensor would make the platform compatible with a long range of sensor types. Since not all the sensor are able to generate a digital output.

- As last future work, it will propose the analysis and improvement of the state–of–art circuits used as a voltage reference of ultra low power consumption. This PhD. Thesis analysed the last bibliography in this field and concluded that the Bandgap reference in terms of stability, however not in terms of power consumption.

Part II

Resumen de la Tesis Doctoral (Español)

Resumen

Los sistemas RFID de largo alcance pasivos abarcan distancias de hasta varios metros trabajando en la banda de ISM (industrial, científica y médica) a 868MHz. Las etiquetas no requieren baterías y los circuitos que las componen se integran en un solo chip, exceptuando la antena. Por lo tanto si se fabrican en masa, el coste de las etiquetas es reducido, alrededor de 10 céntimos por unidad.

El largo alcance, bajo coste y la capacidad de almacenamiento de este tipo de etiquetas RFID hace esta tecnología muy atractiva para construir sensores inalámbricos. Integrar un sensor dentro de un transponder RFID de largo alcance conservando un área de cobertura de algunos metros multiplicaría el campo de aplicaciones actual de las etiquetas RFID. Sin embargo existen barreras técnicas para llevar esta idea a la práctica que aún no han sido superadas. Estas barreras son la eficiencia en la conversión de energía AC en DC y la reducción de consumo de los sensores y en los circuitos de la etiqueta. Hasta lo que se recoge en el estado del arte no existe ningún sensor RFID operativo, aunque existe un gran interés científico en tecnologías RFID UHF pasivas, tanto en lectores como en etiquetas, así como en sensores de muy bajo consumo.

En este trabajo de investigación se realizan aportaciones al diseño del sistema de recuperación y estabilización de energía para sensores inalámbricos pasivos de largo alcance basados en tecnologías RFID UHF pasivas. Con el fin de demostrar las contribuciones de este trabajo de investigación se han diseñado, implementado, fabricado y medido numerosos circuitos microelectrónicos. Esta Tesis abarca los siguientes puntos:

- Análisis del sistema de recuperación y estabilización de energía para sensores inalámbricos pasivos, así como búsqueda de los factores críticos o límites físicos y definición de las especificaciones de cada bloque particular que conforma el sistema de recuperación y estabilización de energía del sensor RFID.

- Análisis de las diferentes arquitecturas y tecnologías utilizadas para diseñar rectificadores (elemento que convierte energía de RF en energía de alimentación) y desarrollo de una metodología óptima para el diseño de sensores inalámbricos.

- Propuesta de un modelo matemático que describe el funcionamiento del rectificador en términos de impedancia de entrada y de amplitud a la entrada, en función de los requisitos de potencia para alimentar el sistema y del proceso tecnológico utilizado.

- Análisis del diseño de sensores de tensión de ultra bajo consumo, que sirvan como Power–On–Reset para sensores inalámbricos pasivos. Fruto de éste análisis se proponen dos nuevas estructuras de ultra bajo consumo adaptadas a sensores RFID.

- Análisis del diseño de circuitos de protección contra tensiones elevadas que puedan dañar la electrónica de la etiqueta RFID. En este apartado se propone un circuito

novedoso que reduce el consumo respecto al estado–del–arte conservando intacta su funcionalidad.

- Análisis del diseño para reguladores de tensión de ultra bajo consumo aptos para sensores inalámbricos de ultra bajo consumo. Como consecuencia de este análisis se presenta una metodología de diseño específica para sensores RFID. A traveés de la fabricación y medida de circuitos, la metodología es probada.

Capítulo 1

Motivación y objetivos de la investigación

Índice General

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Resumen: Este capítulo introduce el tema de esta Tesis Doctoral, define el contexto en el que se ha desarrollado y la línea de investigación donde se encuadra. Finalmente, presenta los objetivos perseguidos.

1.1 Introducción

En esta sección se introducen los sensores inalámbricos pasivos y los sistemas de identificación por radiofrecuencia. La unión de estos dos conceptos es el punto de partida de esta Tesis Doctoral.

1.1.1 Sistemas de identificación por radiofrecuencia pasivos

Los sistemas de identificación por radiofrecuencia (RFID) o etiquetas inteligentes son sistemas de identificación electrónicos e inalámbricos. Estos sistemas se componen básicamente de un dispositivo interrogador o lector y de una o varias etiquetas inteligentes. El dispositivo lector interroga a las diversas etiquetas inteligentes que se encuentre dentro de su radio de cobertura, cada etiqueta transmite cierta información al dispositivo lector. Finalmente el lector procesa la información recibida de las etiquetas y la entrega al usuario. La Figura 1.1 muestra el esquema básico de funcionamiento de un sistema de identificación por radiofrecuencia.

Cada etiqueta dispone de un código de identificación almacenado en su memoria interna. El dispositivo lector después de leer el código identifica a la etiqueta dentro de

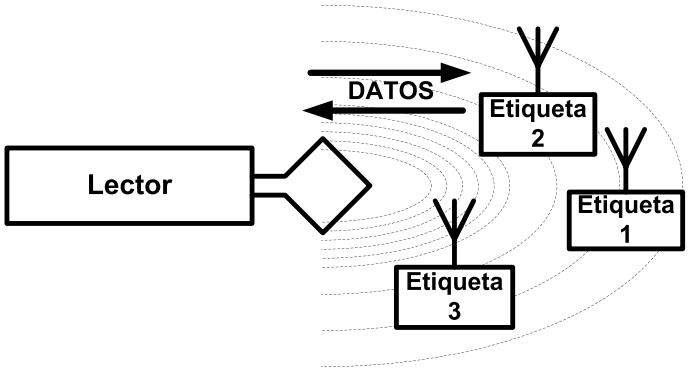

Figura 1.1: Esquema de un sistema de identificación por radiofrecuencia.

su base de datos. Existen multitud de campos en los que este esquema básico encuentra aplicación. Por ejemplo, para realizar control de acceso en edificios, en la identificación de mercancías en almacenes, para la identificación de animales, como sistema para evitar falsificación de productos, en supermercados o tiendas como sustituto de los actuales códigos de barras o como dispositivo antirrobo, entre otros.

1.1.2 Clasificación de sistemas RFID

Los criterios de diferenciación más importante para sistemas RFID son la frecuencia de operación del lector, el método de acoplo físico y el alcance del sistema. El rango de frecuencias a las que un sistema RFID puede operar va desde los 135 KHz hasta los 5.8 GHz. En cuanto al acoplo físico, este puede ser por medio del campo eléctrico, magnético o electromagnético. Finalmente, el alcance de estos sistemas va desde pocos milímetros hasta más de 15 metros.

Los sistemas de alcance muy reducido, hasta 1 cm, se conocen como sistemas de acoplo cerrado (close coupling system). Para que estos sistemas funcionen el transponder tiene que estar insertado dentro del lector o sobre la superficie de este. El acoplo en estos sistemas se realiza usando el campo eléctrico y el magnético y pueden operar a frecuencias entre DC y 30 MHz, ya que el funcionamiento del transponder no depende de los campos radiados. El acoplo cerrado entre la portadora de datos y el lector también facilita la transmisión de grandes cantidades de energía que puede incluso alimentar microprocesadores. Este tipo de sistemas se utilizan principalmente en sistemas que requieren muy altos niveles de seguridad y corto alcance. Por ejemplo controles de acceso o monederos electrónicos. Sin embargo este tipo de sistemas esta cayendo en desuso.

Sistemas con alcances de lectura y escritura de hasta 1 metro se conocen con el término de sistemas de acoplo remoto. Casi todos estos sistemas están basados en acoplo (magnético) inductivo entre lector y etiqueta. Al menos el 90% de todos los sistemas RFID vendidos actualmente son sistemas de acoplo inductivo. Por esta razón existe un gran número de estos sistemas en el mercado. Existen también una serie de estándares que especifican los parámetros técnicos de los transponders y los lectores para varias aplicaciones estándar, como tarjetas inteligentes, identificación de animales o automatización industrial. Se suelen usar frecuencias entre 135 KHz y 13.56 MHz.

Los sistemas RFID con alcances por encima de 1 metro se conocen como sistemas de largo alcance. Todos los sistemas de largo alcance funcionan usando ondas elec-

tromagnéticas en el rango de UHF y microondas. La gran mayoría de estos sistemas son también conocidos como sistemas Backscatter debido a su principio físico de funcionamiento. Además, existen sistemas de largo alcance usando transponders de ondas acústicas superficiales (surface acustic waves, SAW) en el rango de las microondas. Todos estos sistemas operan a frecuencias de UHF 868 MHz en Europa y 915 MHz en EEUU y a frecuencias de microondas 2.5 GHz y 5.8 GHz. Los rangos típicos que se alcanzan usando etiquetas pasivas, es decir sin baterías, es de 8 m mientras que en transponders equipados con baterías, el alcance supera los 20 m.

1.1.3 Sensores RFID UHF (de largo alcance) pasivos

Los sistemas RFID de largo alcance pasivos abarcan distancias de hasta varios metros [16] trabajando en la banda de ISM (industrial, científica y médica) a 868 MHz. Las etiquetas no requieren baterías y los circuitos que las componen se integran en un solo chip, exceptuando la antena. Por lo tanto si se fabrican en masa, el coste de las etiquetas es reducido, alrededor de 10 céntimos por unidad [45].

El largo alcance, bajo coste y la capacidad de almacenamiento de este tipo de etiquetas RFID hace esta tecnología muy atractiva para construir sensores inalámbricos. Integrar un sensor dentro de un transponder RFID de largo alcance conservando un área de cobertura de algunos metros multiplicaría el campo de aplicaciones actual de las etiquetas RFID. Sin embargo existen barreras técnicas para llevar esta idea a la práctica que aún no han sido superadas. Estas barreras son la eficiencia en la conversión de energía AC en DC y la reducción del consumo de potencia en los sensores y en los circuitos de la etiqueta. Hasta ahora en el estado del arte no existe ningún sensor RFID operativo, aunque existe un gran interés científico en tecnologías RFID UHF pasivas, tanto en lectores como en etiquetas, así como en sensores de muy bajo consumo.

Esta Tesis Doctoral se enmarca dentro de un proyecto de investigación internacional cuyo objetivo es diseñar sensores inalámbricos pasivos utilizando como interfaz de radiofrecuencia tecnología RFID de largo alcance pasiva.

1.2 Motivación de la Tesis Doctoral

En esta sección se describe el contexto en el que desarrolla esta Tesis Doctoral y se define la línea de investigación en la que se enmarca.

1.2.1 Contexto de la Tesis Doctoral

La investigación realizada durante esta Tesis Doctoral se enmarca dentro de un proyecto de investigación internacional llamado WISEN (WIreless SENsors). En WISEN están involucrados los siguientes centros: el Instituto Universitario de Microelectrónica Aplicada de la Universidad de Las Palmas de Gran Canaria (IUMA), el Centro de Estudios e Investigaciones Técnicas de Guipúzcoa (CEIT) y el Instituto Fraunhofer de Circuitos Integrados (Fraunhofer IIS). El objetivo principal de este proyecto es investigar en el diseño e implementación de sistemas de sensores inalámbricos pasivos. Este objetivo principal se divide en:

- Diseño e implementación de receptores UHF RFID pasivos optimizados para operar como interfaz de RF en sensores inalámbricos.

- Diseño e implementación de un dispositivo lector de etiquetas UHF RFID pasivas.
- Diseño e implementación de sensores de ultra bajo consumo integrables con el receptor UHF RFID pasivo.
- Estudio y análisis de posibles aplicaciones de la tecnología desarrollada.

1.2.2 Descripción del sistema

En esta sección se describe el esquema de todo el sistema adoptado por WISEN, poniendo un mayor énfasis en la etiqueta. Finalmente se sitúa el lugar que ocupa la investigación de esta Tesis Doctoral dentro del proyecto.

1.2.2.1 Protocolo de comunicación

Como protocolo de comunicación se utiliza el estándar EPC global 2 [31], diseñado específicamente para sistemas RFID UHF pasivos. En este estándar se especifica todos los parámetros y variables envueltos en la comunicación entre lector y etiqueta.

En sistemas RFID UHF pasivos se utilizan dos modulaciones diferentes una para cada sentido de la comunicación. Se usa ASK (modulación en amplitud) para la comunicación lector $\rightarrow$ etiqueta. La razón es facilitar la de–modulación en la etiqueta, reduciendo así el número de circuitos y por tanto el consumo de potencia. Para el sentido etiqueta $\rightarrow$ lector se utiliza un tipo de modulación PSK (modulación en fase) también conocido como modulación Backscattering. Esta modulación consiste en variar la impedancia de entrada de la etiqueta para reflejar o no una señal continua procedente del lector. Este último ha de ser capaz de detectar la onda reflejada.

1.2.2.2 El lector

El dispositivo lector es el componente más caro en sistemas RFID. Algunas de sus características son:

- Incluye la mayor parte de la inteligencia del sistema, para simplificar el diseño y el consumo de las etiquetas.
- Es capaz de transmitir y recibir en la misma frecuencia y al mismo tiempo.
- Un gran rango dinámico. Con la misma antena tiene que transmitir 33dBm hacia las etiquetas y recibir -70dBm de potencia reflejada.
- Ha de ser compatible con uno o varios estándares de comunicación.
- Incluir un sensor en la etiqueta no afecta a la arquitectura del lector.

El lector no entra dentro de los objetivos de esta Tesis Doctoral, con lo que no se entrará en una descripción más detallada.

1.2.2.3 La etiqueta

Las etiquetas UHF RFID pasivas se alimentan de la señal procedente del lector. En la banda ISM a 868 MHz existen limitaciones en la potencia de emisión y de la fórmula de Friis [143] sabemos que la potencia decae con el cuadrado de la distancia. Esto implica que el consumo de las etiqueta ha de ser reducido para tener un mayor alcance. Incluir un sensor en la etiqueta supone un incremento del consumo o lo que es lo mismo una reducción del alcance. Puesto que el consumo es crítico en este tipo de sistemas, las etiquetas han de ser lo más simple posible. En la Figura 1.2 se presenta la arquitectura de una etiqueta UHF RFID pasiva con un sensor incluido.

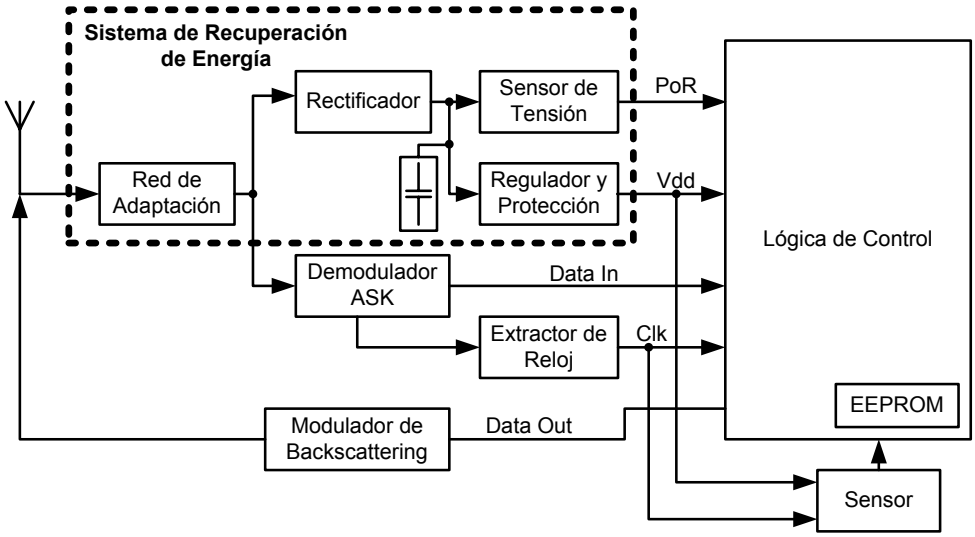

Figura 1.2: Arquitectura de un sensor RFID UHF pasivo.

A continuación se describe cada uno de los bloques que conforma un sensor RFID.

- **Antena y red de adaptación.** El chip se conecta directamente a la antena con lo que ésta ha de estar adaptada a la impedancia de entrada del chip. Elementos externos como bobinas y condensadores se deben evitar para no aumentar el precio de la etiqueta. La solución es integrar la red de adaptación. Si esto no es posible, se diseña la red de adaptación mediante líneas de transmisión unidas a la antena.

- **Rectificador.** El rectificador, también conocido como Multiplicador de Tensión, es el dispositivo encargado de realizar la rectificación de la señal RF capturada por la antena. Este circuito convierte la señal alterna procedente de la antena en una tensión continua a su salida. La eficiencia en esta conversión es clave para determinar el consumo de la etiqueta.

- **Condensador de Alimentación.** A la salida del Rectificador se coloca un condensador con gran capacidad. Este condensador sirve para almacenar cierta carga extra que contrarreste los picos de alimentación y las cortas ausencias de señal de RF consecuencia de la modulación en amplitud.

- **Sensor de Tensión.** El sensor de tensión controla la carga del Condensador de Alimentación. Cuando la tensión en el condensador alcanza un umbral que garantice la correcta alimentación de la etiqueta el sensor de tensión genera la señal PoR (Power on Reset) que activa la etiqueta.

- **Regulador y Protección.** Este bloque se encarga de generar la tensión estable de alimentación (Vdd) para todo el chip y está formado por dos sub–circuitos. El primero de ellos es un protector de tensión para prevenir tensiones muy altas que puedan dañar los componentes. El segundo es un regulador de tensión que mantenga una tensión de alimentación Vdd constante e independiente de la temperatura, picos de consumo y cambios en la tensión del condensador de alimentación

- **De–modulador ASK.** Como su nombre indica, este bloque se encarga de demodular la señal ASK procedente del dispositivo lector. La señal de entrada es una señal modulada en amplitud con dos estados, presencia de señal o nada. Esta modulación también es conocida como OOK (On Off Keying).

- **Recuperador de Reloj.** Este circuito extrae la señal de reloj para la lógica de la señal demodulada. De esta forma no es necesario incluir osciladores adicionales en el sistema para generar el reloj.

- **Modulador de Backscattering.** El modulador consiste básicamente en un interruptor controlado por lógica que conecta un condensador en paralelo con la entrada, para desadaptar la antena y el chip. Con esto se consigue que la señal se refleje si hay desadaptación. El dispositivo lector detecta si hay o no señal reflejada, implementando así una modulación denominada Backscattering.

- **Lógica de Control.** Este bloque constituye la parte digital de la etiqueta. Este bloque es una máquina de estados que implementa el protocolo de comunicación utilizado por el sistema. Además ha de ser capaz de leer datos del sensor y transmitirlos.

- **Sensor.** En principio el sistema está diseñado para poder ser utilizado con cualquier tipo de sensor. Éste, sin embargo, ha de ser optimizado para tener un consumo de potencia mínimo, una sensibilidad aceptable y salida digital.

La investigación a realizar en esta Tesis Doctoral se localiza en la etiqueta UHF pasiva, concretamente en el Sistema de Recuperación de Energía, véase Figura 1.2. Éste incluye los siguientes bloques: Red de Adaptación, Rectificador, Sensor de Tensión, Protección y Regulador. A continuación se presentan los objetivos de la presente Tesis Doctoral.

1.3 Objetivos de la Tesis Doctoral

El objetivo de esta Tesis Doctoral es desarrollar la metodología de diseño de sistemas de recuperación y estabilización de energía para etiquetas UHF RFID pasivas utilizando tecnologías CMOS estándar. Los resultados obtenidos se deben aplicar a la fabricación de los sensores inalámbricos pasivos diseñados dentro del proyecto WISEN.

El objetivo de esta tesis se divide en:

- Análisis del sistema de recuperación y estabilización de energía para sensores inalámbricos pasivos, búsqueda de factores críticos o límites teóricos y definición de las especificaciones de cada bloque particular.

- Análisis de las diferentes arquitecturas y tecnologías utilizadas para diseñar rectificadores, compararlas y definir la metodología óptima para el diseño de sensores inalámbricos.
- Generar pautas de diseño para sensores de tensión de ultra bajo consumo, que sirvan como Power–On–Reset para sensores inalámbricos.
- Generar pautas de diseño para circuitos de protección contra tensiones elevadas que puedan dañar la electrónica de la etiqueta RFID.
- Generar pautas de diseño para reguladores de tensión de ultra bajo consumo aptos para sensores inalámbricos de ultra bajo consumo.

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Resumen: En este apartado se describe la forma en que se ha planteado el trabajo científico realizado, así como, la metodología utilizada en el desarrollo del mismo. Este proceso se puede dividir en cuatro pasos:

1. Análisis del estado del Arte.

2. Identificación y especificación de los parámetros críticos en el diseño del sistema.
3. Implementación de cada uno de los sub–circuitos que conforman el sistema de Recuperación de Energía.
4. Fabricación y Medidas de las características eléctricas de cada bloque así como del sistema completo.

2.1 Estado del arte

Como primer paso se realiza un detallado estudio del estado del arte en sistemas RFID de largo alcance pasivos y de cada uno de los bloques que componen el sistema de recuperación de energía.

2.1.1 Estado del arte: Etiquetas RFID UHF pasivas

El consumo del chip y la eficiencia del sistema de recuperación de energía, especialmente esta última, son los factores que van a limitar el alcance de la etiqueta RFID pasiva. Una etiqueta con mayor alcance tendrá un menor consumo y una mayor eficiencia en la conversión de energía. En el estudio del estado del arte se comparan etiquetas diseñadas por diferentes autores observando su alcance.

En el año 2003 se publicó la primera etiqueta RFID UHF pasiva [1]. Esta etiqueta trabajando a 869 MHz tiene un alcance de lectura de 9.25 m a 4 W de EIRP (potencia radiada isotrópica efectiva). Este artículo aplica la topología presentada por [47] a las etiquetas RFID pasivas, para convertir la señal de RF a DC. Con este método de conversión se alcanzan altas eficiencias [1] de conversión. Sin embargo, del artículo se extrae, que la clave para lograr un mayor alcance no es sólo la topología sino también el uso de una tecnología específicamente optimizada para conseguir una mayor eficiencia. Otro importante punto remarcado es el uso de circuitos de ultra bajo consumo (Ultra–Low–Power). El consumo de la etiqueta sin tener en cuenta el rectificador es de 2.25 μW en modo de lectura y de 3.57 μW en modo de escritura en la EEPROM. Esta etiqueta utiliza modulación PWM para la comunicación Lector→Etiqueta y una modulación Backscatter para el sentido contrario. Finalmente realiza un análisis de optimización del generador de tensión y del modulador teniendo en cuenta el efecto que produce la desadaptación a la entrada del rectificador en la tensión de alimentación.

Dos años después Curty [5] publicó una etiqueta pasiva trabajando a 2.4 GHz y con un alcance de 12 metros, teóricamente a 868 MHz el alcance seria de alrededor de 30 metros. La clave para conseguir este elevado alcance es el uso de una tecnología de SOS (Silicon–On–Sapphire). Esta tecnología incluye transistores con muy baja tensión umbral, además presenta muy bajas capacidades parásitas a las frecuencias de interés. A parte de esto, Curty describe un protocolo de comunicaciones adaptado para ultra bajo consumo, que no es compatible con el estándar EPC Global, protocolo mayormente utilizado en Europa. También incluye modificaciones que simplifican el sistema y reducen las prestaciones para optimizar el consumo.

[1] La eficiencia se define como la división de la potencia DC generada a la salida del multiplicador de tensión entre la potencia AC absorbida a la entrada del multiplicador de tensión.

Tabla 2.1: Alcance de las etiquetas UHF RFID actuales a 900 MHz con una EIRP=4W

Referencia	Tecnología	Batería	Alcance (m)
[1]	CMOS 0.35μm + Schottky modificados	No	9.25
[5]	SOS 0.5μm	No	30
[42]	CMOS 0.35μm + Schottky estándar	Si	24
[48]	CMOS/FeRAM 0.35μm	No	3.51

En 2007, Pillai [42] publica el primer RFID alimentado con baterías. El camino seguido para conseguir un mayor alcance en este es caso es utilizar baterías para polarizar los diodos. Pillai utilizada una tecnología CMOS de 1 μm que dispone de diodos Schottky y EEPROM. El alcance obtenido es de 3.51 metros a 2.4 GHz radiando 4 W de EIRP y de 24 metros a 868 MHz.

Estas dos últimas publicaciones proporcionan una idea de la importancia de la tecnología para lograr un elevado alcance. Pillai utiliza CMOS de 1μm y diodos Schottky e incluso baterías adicionales. Sin embargo su alcance es cuatro veces menor que el de Curty que no utiliza baterías pero su tecnología es SOS con muy bajas capacidades parásitas y tensión umbral. En este punto se puede afirmar que el alcance máximo de la etiqueta lo determina la tecnología utilizada. La razón, por un lado, es que el rectificador aumenta su eficiencia cuando las capacidades parásitas y la tensión umbral son mínimas; por otro, es que la tensión de alimentación requerida se reduce, es decir, los circuitos requieren menos potencia para operar cuando se mejora la tecnología.

Tambin en 2007 [48] se publicó una etiqueta RFID UHF pasiva en una tecnología CMOS/FeRAM de 0.35 μm. La particularidad en esta tecnología es que dispone condensadores ferroeléctricos que tienen una gran permitividad, por lo tanto, reducen el área y los componentes parásitos. La novedad introducida por Nakamoto es utilizar RAM en lugar de EEPROM para el almacenamiento de datos en la etiqueta, esto reduce el tiempo requerido para la escritura. Además emplea condensadores ferroeléctricos para polarizar los transistores en el rectificador y reducir así su V_{th}. El alcance logrado a 868 MHz (3.51 metros), que está muy por debajo de los trabajos antes mencionados, se debe al elevado consumo de la RAM (80 μW). Este trabajo da cierta idea del alcance que se puede lograr para sistemas que consuman 80 μW utilizando una tecnología de 0.35 μm casi estándar. Por lo tanto es una buena referencia para el desarrollo de esta Tesis Doctoral, puesto que el consumo del sensor se estima que sea de unos 60–70 μW, con lo que el consumo final de la etiqueta será de unos 80 μW.

2.1.2 Estado del arte: Sensores de bajo consumo

Existe un gran y variado número de sensores compatibles con los procesos tecnológicos utilizados para fabricar circuitos integrados. Se han desarrollado una gran variedad de dispositivos en tecnologías CMOS estándar; entre otros se pueden destacar los sensores de temperatura, de campo magnético, de huellas digitales o de imagen [55, 7, 56, 57, 58].

Tabla 2.2: Sensores y Conversor Analógico–Digital de muy bajo consumo

sensor	MEMS	Consumo de Potencia	Totalmente pasivo?
Temperatura	No	10μW	Si
Efecto Hall	No	4.2mW	No
Sensor de imagen	No	196μW	No
Huellas digitales	No	250μW	No
Acelerómetro	Si	400μW	No
Giroscopio	Si	15mW	No
Presión	Si	42μW	Si
ADC	No	3.1μW	Si

Por otro lado se puede detectar luz coloreada con dispositivos CMOS, los denominados *metal grating patterns* o uniones PN de profundidad variable como filtro para el color [56, 59]. Paralelamente, los arrays de sensores de imágenes están encontrando aplicación para muy bajo consumo aparte de su uso en cámaras digitales como por ejemplo detección de movimiento en los ratones para ordenador; o toma de imágenes para visualizar controles y luces en entornos industriales donde acompañando al sensor existe un procesado local de imágenes para así sólo transmitir la mínima información.

Las tecnologías MEMS abren el abanico de posibilidades para miniaturizar sensores que procesen magnitudes de diversas naturalezas; aceleración lineal o angular, presión, magnitudes químicas, flujo de fluidos, micrófonos de audio, entre otros. Aunque la mayor parte de estos sensores no son integrables en tecnologías CMOS estándar, éstos ofrecen muchas ventajas como es el bajo consumo, el bajo coste e incluso en ocasiones la posibilidad de ser integrados en el mismo sustrato que los circuitos microelectrónicos que los controlan.

La Tabla 2.2 resume el estudio realizado sobre los diferentes sensores de bajo consumo. En la Tabla se indica el consumo de potencia de cada sensor, si requiere el uso de tecnologías MEMS y si es viable su integración en una etiqueta RFID UHF pasiva de largo alcance. Se asume que como largo alcance una distancia mínima entre lector y etiqueta de 3 metros, esto equivale a una potencia por debajo de 60 μW. Esta restricción hace que los únicos candidatos para ser integrados en nuestro sistema sean los sensores de temperatura y presión cuyo consumo son de 10 y 42 μW, respectivamente. El resto de sensores requieren una potencia de alimentación superior a los 190 μW. Esta cantidad de potencia no puede ser recuperada por una etiqueta RFID UHF pasiva, a partir de la potencia radiada por un lector que respete las regulaciones gubernamentales en términos de potencia radiada y a una distancia de tres metros. La alternativa para estos sensores serían las baterías.

Finalmente remarcar que conversores analógicos digitales (ADCs) de muy bajo consumo también serían integrables en etiquetas pasivas RFID UHF de largo alcance. Como se observa en la Tabla se han desarrollado ADCs con consumos que rondan los 3 μW.

Una vez analizadas las etiquetas RFID UHF pasivas y los sensores de muy bajo consumo aptos para ser integrados con el transponder RFID se procederá a revisar el estado del arte de cada uno de los bloques circuitales que componen el sistema de

recuperación de energía del sensor RFID de largo alcance pasivo. La Figura 2.1 muestra los bloques circuitales objetos de esta Tesis Doctoral.

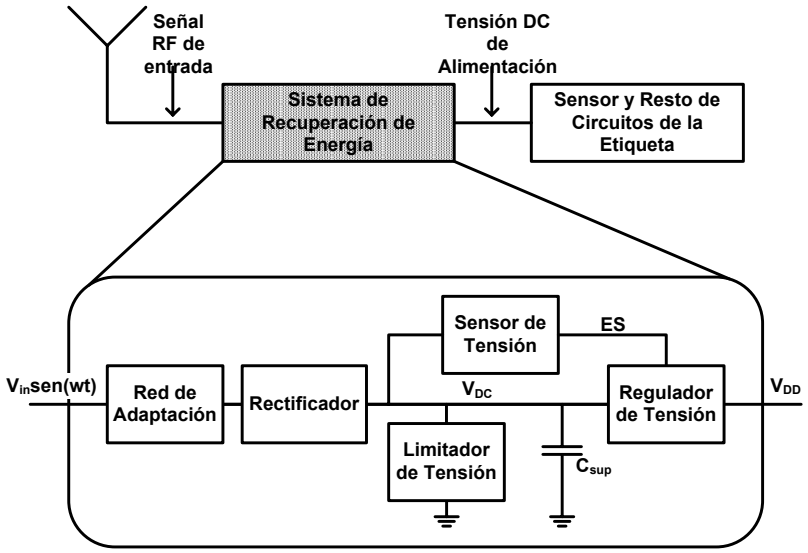

Figura 2.1: Diagrama de de bloques del sistema de recuperación de energía de un sensor RFID pasivo.

2.1.3 Estado del Arte: Rectificador

Un Rectificador o Multiplicador de Tensión (VM– Voltage Multiplier) es una red de condensares y diodos capaz de convertir una tensión alterna de entrada en una tensión continua de salida. Este tipo de circuitos se usa en aplicaciones que requieren alimentación con niveles de tensión más altos que el nivel de tensión de alimentación y en general en cualquier aplicación que requiere conversión alterna a continua. Las memorias no volátiles requieren niveles de tensión elevados (30–40 V), para realizar operaciones de escritura y borrado. Para obtener estas tensiones a partir de una tensión de alimentación de unos 5 V, se utilizan estructuras VM. Más recientemente los circuitos VM han encontrado aplicación como rectificadores en transponders tanto pasivos [2] como activos [3] para aplicaciones de telemetría. En estas aplicaciones la señal de RF recibida por la antena del transponder es rectificada por el VM para obtener a su salida una tensión continua que sirve para iniciar una comunicación entre el transponder y el dispositivo interrogador. Para el caso concreto de etiquetas UHF RFID pasivas, la tensión rectificada por el VM se utiliza también como alimentación en los subsistemas de la etiqueta.

El primer multiplicador de tensión conocido data de 1932 y sus autores fueron los ingleses Cockcrof y Walton [102]. Este circuito era utilizado en el campo de la física nuclear para generar las altas tensiones requeridas para producir iones positivos de alta velocidad. Más recientemente en 1975, Dickson [47] presentó una topología basada en el Multiplicador de Cockcrof y Walton especialmente diseñada para ser integrada en tecnologías CMOS. La primera motivación del multiplicador de Dickson fue la generación de los relativamente altas tensiones necesarias para escribir o borrar información en

[2] Transponders que no requieren baterías para su funcionamiento, son alimentados por acoplo inductivo o potencia de la señal de RF.

[3] Requieren de baterías para su funcionamiento.

memorias no volátiles. Ya en 2003 fue publicado la primera etiqueta RFID UHF pasiva [1], donde el multiplicador de Dickson fue modificado y utilizado por primera vez para generar la tensión continua de alimentación de un chip.

La topología modificada de Dickson y sus variantes son usadas como conversores de AC–DC en todas las etiquetas RFID UHF pasivas y activas publicadas [1, 5, 51, 41, 103, 48, 42]. Esta arquitectura es la elegida para la generación de la tensión de alimentación en esta Tesis Doctoral.

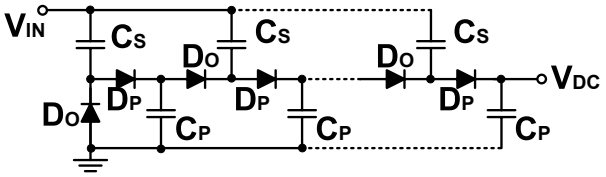

Figura 2.2: Rectificador de Dickson modificado.

En la Figura 2.2, los diodos son conmutados con la tensión AC de entrada (V_{in}), éstos bombean corriente hacia la salida y multiplican la tensión en los condensadores. Nótese que la amplitud de la señal AC de entrada tiene que ser mayor que la tensión umbral de los diodos (V_{th}), para que los diodos puedan conmutar adecuadamente. Entonces en los ciclos negativos de V_{in} los diodos impares (D_O) conducen, los diodos pares (D_P) son circuitos abiertos y los condensadores serie (C_S) se cargan, véase la Figura 2.3.a. Mientras que en los ciclos positivos de V_{in}, los D_Ps conducen, los D_Os están cortados y los condensadores en paralelo C_P se cargan, véase la Figura 2.3.b. Si la capacidad de los condensadores es suficiente, parte de la tensión es mantenida hasta el siguiente ciclo de la señal de entrada, de esta forma la salida puede considerarse una tensión continua. El valor de V_{DC} depende del número de diodos del rectificador de la siguiente forma:

$$V_{DC} = N(V_{in} - V_{th}) \tag{2.1}$$

Las diferentes variantes del multiplicador de Dickson modificado utilizado en etiquetas RFID UHF pueden dividirse en tres grupos diferentes:

- Clásico: Fue introducida en el 2003 [1]. Este enfoque implementa directamente el circuito descrito en la Figura 2.2. Los diodos pueden ser tanto diodos Schottky, cuya tensión umbral es muy reducida, como transistores MOS de bajo umbral conectados como diodos [51, 103].

- Polarizado: Este segundo enfoque utiliza, en lugar de diodos, transistores polarizados de forma que su tensión umbral sea cero. Esto se consigue aplicando una tensión V_{bth} entre los terminales de puerta y drenador del transistor. Como resultado la tensión umbral (V_{th}) se reduce y la equación 2.2 se reescribe como:

  $$V_{DC} = N(V_{in} - V_{th} + V_{bth}) \tag{2.2}$$

  La desventaja de este enfoque es la necesidad de una tensión de polarización. En este punto, algunos autores hacen uso de baterías [41, 42] para generar V_{bth}, por lo tanto las etiquetas dejan de ser pasivas para convertirse en activas o semi–pasivas. Otros autores hacen uso de un circuito interno para cancelar la tensión

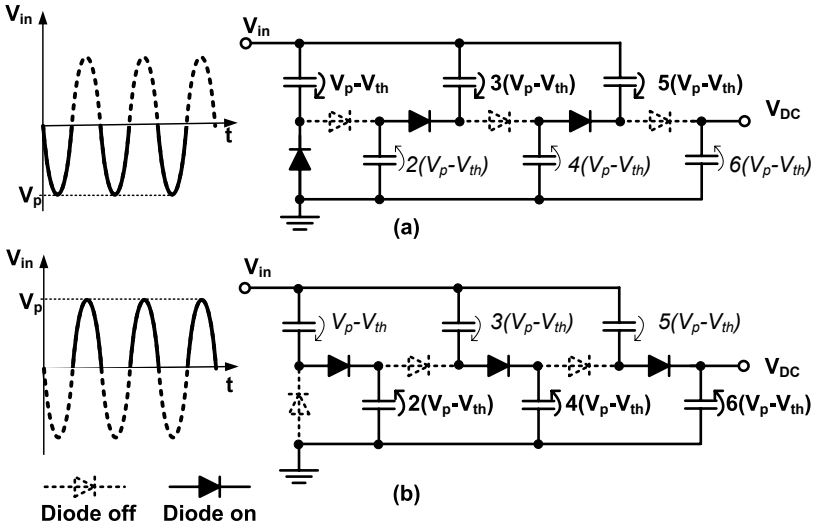

Figura 2.3: Fundamentos de operación del rectificador: (a) para los ciclos negativos de V_{in}, (b) para los ciclos positivos de V_{in}.

umbral basado en condensadores ferroeléctricos. Los condensadores ferroeléctricos requieren un procesado especial que no es contemplado en tecnologías CMOS estándar, con lo cual el precio de fabricación aumenta considerablemente.

- Rectificador de onda completa. En este caso el multiplicador de Dickson es doblado y los condensadores reagrupados de forma que cada diodo sea excitado con la misma amplitud de la señal de entrada [97](véase la Figura 2.4).

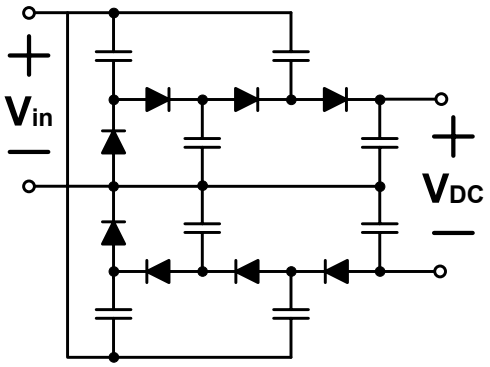

Figura 2.4: Rectificador de onda completa de dos etapas.

La relación entre el número de diodos y la tensión de salida permanece igual que en multiplicador clásico. Los autores de [97] introducen una reducción de la impedancia de entrada, sin embargo esta característica no queda demostrada. Como conclusión, no existe una clara ventaja de este enfoque con respecto al multiplicador clásico, mientras que la complejidad del circuito sí se incrementa. Además, el rectificador de onda completa fue fabricado en una tecnología especial de silicio sobre zafiro (SOS). Se trata de un proceso muy caro que posee transistores de muy bajo umbral así como dispositivos aislados, que presentan muy bajas capacidades parásitas comparadas con los procesos estándar.

Por un lado, los rectificadores polarizados requieren o baterías o costosos procesos tecnológicos. Por otro lado, la rectificación de onda completa sólo ha sido probada en un proceso muy especial y costoso y no hay pruebas que indiquen una mejora del enfoque clásico con tecnologías estándar. Como conclusión el rectificador de onda completa es descartado. En esta Tesis Doctoral se utiliza el rectificador clásico para realizar la conversión de tensión alterna a tensión continua para alimentación del chip ya que esta arquitectura ha sido probada en diversas tecnologías CMOS estándar y ha sido adoptado por la mayoría de los autores.

2.1.4 Estado del arte: Sensor de tensión

El Sensor de Tensión (VS *Voltage Sensor*) detecta la carga del condensador de alimentación y genera la señal de activación (ES–*Enable Signal*) cuando una tensión umbral predefinida se alcanza en bornes del condensador de alimentación.

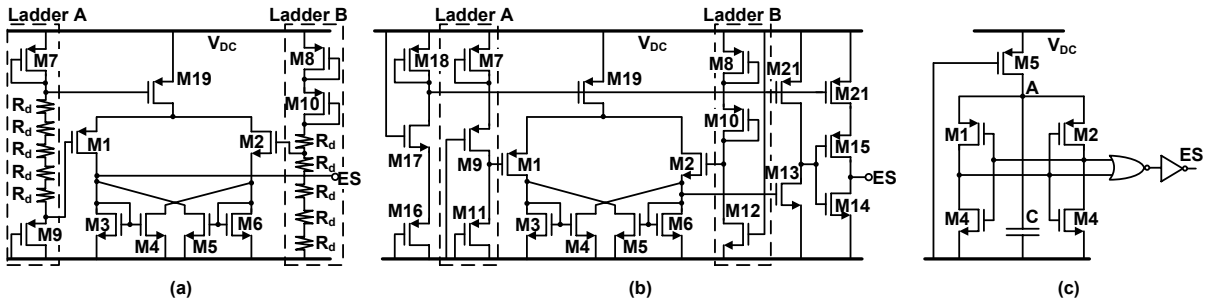

Figura 2.5: Circuitos publicados en la bibliografía: (a) Mode Selector(MS) [3], (b) Modified Mode Selector (MMS) [4], y (c) Power on Reset (POR) [5].

En el estado del arte se presentan tres circuitos, véase Figura 2.5. El *Mode Selector*(MS) [3] se muestra en la Figura 2.5.a. Dos cargas resistivas generan dos tensiones en las puertas de los transistores M1 y M2, estas tensiones son las entradas de un comparador de histéresis formado por los transistores M1–M6. Los puntos débiles de este circuito son dos; por un lado el alto consumo de área de las resistencias integradas y por otro lado la elevada corriente necesaria en las dos cargas resistivas de hasta 5 μA.

Los mismos autores proponen el denominado *Modified Mode Selector* (MMS) [4] véase la Figura 2.5.b. En este circuito las cargas son implementadas mediante transistores en lugar de con resistencias integradas. Con esto se consigue reducir el consumo en área y en corriente, éste último asciende a 900 nA, que es aún excesivo para etiquetas RFID UHF pasivas.

Otra alternativa propuesta en la bibliografía es el *Power–On–Reset* (POR) [5] de la Figura 2.5.c. Cuando una tensión de alimentación (V_{DC}) es aplicada, uno de los dos inversores toma ventaja respecto al otro. La puerta NOR compara la salida de los dos inversores y activa la señal ES. El condensador C fuerza un retraso entre la subida de V_{DC} y ES.

Los circuitos descritos en este apartado servirán como referencia para evaluar las características de los Sensores de Tensión que se van a proponer en esta Tesis Doctoral.

2.1.5 Estado del arte: Regulador de tensión

La tensión de alimentación de cualquier circuito electrónico debe permanecer dentro de unos márgenes de seguridad que asegure un correcto funcionamiento. Salirse de estos márgenes supondría un mal funcionamiento o incluso destrucción de algunos de sus elementos.

En el caso particular de los sensores RFID UHF pasivos, la tensión de alimentación se genera en el rectificador a partir de una onda electromagnética incidente. Ya que la potencia y la amplitud de esta onda varían con la distancia entre lector y etiqueta, lo mismo ocurre con la tensión de alimentación.

Por otro lado el consumo de corriente de sistemas complejos como los sensores RFID pasivos es variable y presenta picos de corriente debido a los circuitos digitales. Las variaciones en el consumo de corriente pueden producir caídas bruscas en la tensión de alimentación llegando incluso a salirse de sus márgenes de seguridad.

Finalmente, en sistemas de muy bajo consumo es deseable mantener la tensión de alimentación al mínimo requerido por la tecnología para trabajar. De esta forma se reduce el consumo de potencia general.

En conclusión, la tensión continua generada por el rectificador presenta una serie de problemas debido a la naturaleza del sistema de recuperación del energía del sensor RFID pasivo. Estos problemas son: V_{rec} variable debido a la fluctuación de la potencia de la señal de entrada, y a las indeseables caídas de tensión causadas por el cambiante consumo de corriente y valor de V_{rec} no óptimo para muy bajo consumo.

Para resolver estos problemas, se ha incluido un bloque circuital adicional. El circuito encargado de generar una tensión definida y estable para la adecuada alimentación del sensor RFID se conoce como Regulador de Tensión.

2.1.5.1 Reguladores de tensión en etiquetas RFID pasivas

Existen diferentes enfoques para solucionar el problema de la regulación de tensión.

Algunos autores [1, 4] no usan ningún tipo de regulador. La razón es reducir el consumo de la etiquetas para conseguir el máximo alcance. En cualquier caso es posible que los autores no hagan mención del regulador pero hagan uso de él.

En la bibliografía también se presentan trabajos [5, 48, 109, 42] donde el único mecanismo de regulación es un limitador de altas tensiones. Este enfoque no requiere complicados circuitos para regular la tensión de alimentación, por el contrario el resto de bloques analógicos y digitales debe diseñarse de forma muy robusta frente a variaciones en la tensión de alimentación. La mayor parte de los sistemas que usan un simple limitador de tensión son etiquetas RFID sin sensor.

Por último existen sistemas que incluyen, después del rectificador, además del limitador un regulador de tensión [53, 110, 111]. La ventaja de estos sistemas es una tensión de alimentación muy estable y bien definida frente a variaciones en el consumo o a la potencia de entrada. Por el contrario este bloque aumenta la complejidad y supone un gasto adicional de corriente.

Para el caso particular de los sensores RFID UHF pasivos, la reducida tensión de ruptura del condensador de alimentación obliga a utilizar un limitador de tensión. Además, la presencia del sensor supone un consumo extra de potencia frente a las etiquetas RFID puras. De esta forma, la tensión de alimentación del sensor debe permanecer tan cerca como sea posible del mínimo requerido por el proceso tecnológico para reducir el consumo

de potencia general, y paralelamente se debe asegurar que los picos de consumo no hagan caer la tensión por debajo del mínimo. Este comportamiento no se puede conseguir con un simple limitador. Puesto que las variaciones en la tensión de alimentación son críticas para el sensor, el uso de un regulador de tensión es indispensable para sensores RFID.

2.1.5.2 Reguladores de tensión

Principalmente existen dos filosofías para construir reguladores de tensión [112]. Por un lado están los Reguladores de Tensión Lineales, que están basados en dispositivos trabajando en la región lineal. Por otro lado están los Reguladores de Tensión conmutados que conmutan rápidamente entre ON y OFF un dispositivo en serie.

En los reguladores de tensión lineales un transistor se usa para controlar una tensión de salida y un circuito de realimentación compara la tensión de salida con una referencia de tensión, el resultado de esta comparación sirve para ajustar el transistor de paso. De esta forma se mantiene una tensión de salida razonablemente constante.

Los reguladores conmutados conmutan rápidamente un transistor de potencia entre saturación y corte con un ciclo de trabajo variable. Esta forma de onda rectangular pasa por un filtro LC paso bajo. La principal ventaja de este método es una gran eficiencia debido a que el transistor conmutado disipa muy poca potencia en saturación y ninguna en corte.

Los reguladores conmutados son más complejos y costosos que los lineales. Los primeros requieren un controlador con un oscilador, un dispositivo de paso, una bobina un condensador y diodos. Este alto grado de complejidad no tiene sentido en aplicaciones RFID donde el precio de una etiqueta es un aspecto crítico y debe ser mantenido al mínimo. El bajo coste y la simplicidad son las razones por las que se utilizan Reguladores Lineales en el sistema de recuperación de energía para Sensores RFID.

2.1.5.3 Tipos de reguladores lineales

Existen tres tipos básicos de reguladores lineales [113]: reguladores estándar, reguladores de baja caída de tensión a la salida, comúnmente conocidos por sus siglas en inglés (LDO–*Low–Drop-Out*) y los reguladores quasi–LDO.

La diferencia más importante entre estos tres tipos de reguladores es la tensión de *dropout*, que se define como la mínima caída de tensión requerida en bornes del transistor regulador para mantener la regulación de tensión a la salida. Un aspecto crítico que ha de ser considerado es que el regulador lineal que opera con la menor tensión entre sus terminales disipe internamente la menor potencia y por lo tanto tenga la mayor eficiencia. Los reguladores LDO requieren la menor tensión entre sus terminales mientras que los reguladores estándar la mayor.

La segunda diferencia más importante entre los diferentes tipos de reguladores es la corriente a tierra o la corriente *Quiescent*, que es la corriente que necesita el regulador para funcionar y por lo tanto no será entregada a la carga a su salida. El regulador estándar tiene la menor corriente a tierra mientras que el regulador LDO presenta la más alta. Corrientes a tierra elevadas no son deseables puesto que es corriente desperdiciada, en otras palabras, es corriente proporcionada por la fuente y que no es entregada a la carga.

Para el caso particular de sensores RFID pasivos, se deben considerar los siguientes aspectos: Primero, V_{rec} decae con la distancia entre lector y etiqueta. Segundo, es

deseable maximizar el rango de operación, esto es, el sistema tiene que ser operativo con la mínima tensión de alimentación. El tipo de regulador más eficiente en términos de tensión es el LDO. Por esta razón los reguladores LDO son los más apropiados para sensores RFID pasivos.

2.2 Especificaciones de diseño del sistema recuperación y estabilización de energía

En esta sección se presenta, primeramente, los fundamentos físicos y límites teóricos del sistema de recuperación y estabilización de energía. A continuación, se introducen parámetros relativos a la comunicación y la tecnología, necesarios para realizar una especificación de cada uno de los bloques circuitales que componen el mencionado sistema. Con éste último punto se concluye la sección.

2.2.1 Fundamentos físicos

La Fórmula de Transmisión de Friis [46] relaciona la potencia transmitida desde una antena emisora a la potencia recibida en la antena receptora en el espacio libre.

$$\frac{P_r}{P_t} = G_r G_t (\frac{\lambda}{4\pi d})^2 \tag{2.3}$$

Donde P_t es la potencia entregada en los terminales de la antena transmisora, P_r es la potencia disponible en los terminales de salida de la antena receptora, G_r y G_t son las ganancias de las antenas receptoras y transmisoras, respectivamente, λ es la longitud de onda y d es la distancia entre las antenas.

Nótese que la fórmula de Friis no debe usarse cuando d es muy pequeña

$$d \geq \frac{2a^2}{\lambda} \tag{2.4}$$

Donde a es la dimensión lineal mayor de cualquiera de las antenas. Para una frecuencia de 868 MHz y a=0.346 m, la distancia entre antenas tiene que ser mayor de 0.7 m para que la fórmula de Friis sea válida.

Por otro lado, la fórmula de Friis es válida sólo para propagación en el espacio libre; esto significa que fenómenos como multipropagación, pérdidas atmosféricas, interferencias, etc. no son considerados. Sería necesario incluir términos adicionales para tener en cuenta estos fenómenos.

Para el caso particular de una etiqueta RFID formada por una antena adherida a un chip, la potencia entregada al chip considerando posibles reflexiones es:

$$P_{in} = (1 - \Gamma) \cdot G_r \cdot EIRP \cdot (\frac{\lambda}{4\pi r})^2 \tag{2.5}$$

Donde, Γ es el coeficiente de reflexión [92] y EIRP es la potencia radiada isotrópica equivalente y se define como:

$$EIRP = P_t \cdot G_t \tag{2.6}$$

la cual queda fijada por organismos de regulación gubernamentales. En Europa la EIRP está limitada a 3.3 W en la banda de 866 a 869 MHz, mientras que estados unidos el límite es 4 W en la banda de 902 a 928 MHz.

De la Ecuación 2.5 se extrae que la única forma de maximizar P_{in} para un rango de frecuencias dado es incrementar la ganancia de la antena y reducir las reflexiones tanto como sea posible. Tanto la ganancia como la impedancia de la antena de la etiqueta RFID son características que varían enormemente con la geometría de la antena, entorno, materiales y localización respecto del lector. El funcionamiento de la antena de la etiqueta depende la impedancia de entrada del chip. Puesto que el tamaño y la frecuencia de operación de la antena imponen limitaciones en la ganancia y el ancho de banda, se debe encontrar un compromiso con la impedancia de entrada y estos factores para obtener una antena óptima [29]. Sin embargo la antena está fuera de los objetivos de esta Tesis Doctoral.

2.2.1.1 Análisis de la tensión de entrada del rectificador (V_{in})

El rendimiento del rectificador está directamente relacionado con la amplitud de la señal de RF a su entrada (V_{in}) de la siguiente manera [1]:

$$V_{DC} = N(V_{in} - V_{th}) \tag{2.7}$$

Donde N es un entero relacionado con la arquitectura del rectificador y V_{th} es definido como la mínima amplitud de la señal de entrada para que el rectificador funcione y depende del proceso utilizado para implementar la etiqueta RFID. De la Ecuación 2.7 se puede concluir que es deseable maximizar V_{in} para conseguir la máxima tensión de salida V_{DC} para alimentar a la etiqueta, y por supuesto con la mínima potencia RF a la entrada.

Para una potencia de entrada dada, la amplitud de la tensión a la entrada del rectificador dependerá de la impedancia de entrada del chip y del grado de adaptación entre la antena y el chip. Así introduciendo la condición de resonancia [93] tenemos que V_{in} viene dada por:

$$V_{in} = \sqrt{2R_p(\frac{4R_{ant}R_{chip}}{(R_{ant}+R_{chip})^2}) \cdot G_r \cdot EIRP \cdot (\frac{\lambda}{4\pi r})^2} \tag{2.8}$$

Donde R_p es el equivalente paralelo de la parte real de la impedancia de entrada del chip (Z_{chip}), R_{chip} es la parte real de la impedancia del chip, R_{ant} es la parte real de la impedancia de la antena. En la Figura 2.6 se muestra la influencia de la impedancia de entrada del chip en V_{in}.

La Figura 2.6 muestra que el máximo en V_{in} se produce cuando R_{ant} y R_{chip} son iguales en la condición de resonancia ($X_{ant} = -X_{chip}$). Como conclusión el máximo se consigue para adaptación conjugada, es decir para máxima transferencia de potencia. Otra interesante característica que puede ser extraída de la Figura 2.6 es que los mayores valores de V_{in} se obtienen para R_{chip} bajas. Nótese que cuanto menor R_{chip} más agudo es el pico de V_{in}. Esto significa que pequeñas desadaptaciones en la entrada causan grandes caídas en V_{in} y por lo tanto en el rendimiento del rectificador. Existe un parámetro para evaluar el grado de la adaptación, es el denominado Factor de Calidad (Q). En el siguiente subapartado se analiza su importancia.

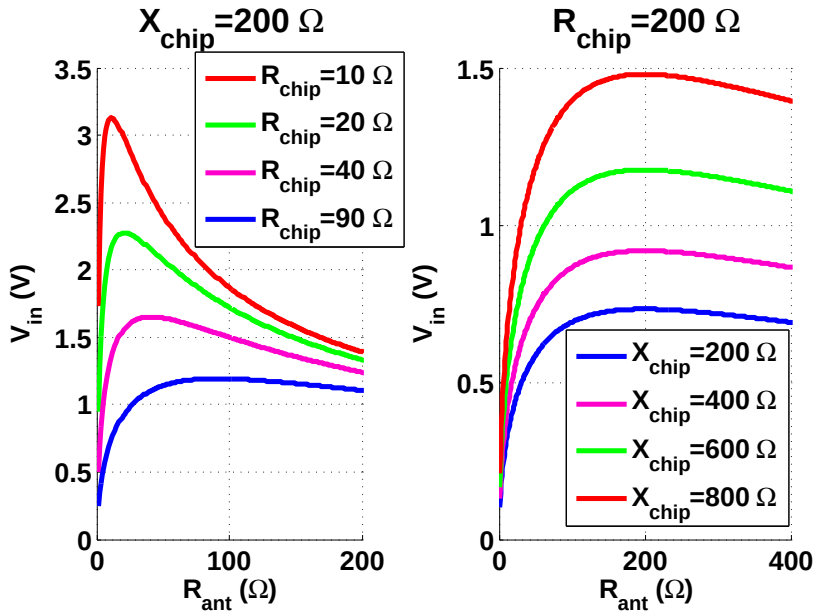

Figura 2.6: R_{ant} vs V_{in} (G_r=-0.5dB, EIRP=4W, r=1m y f=868MHz) a) para diferentes valores de R_{chip}, y b) para diferentes valores de X_{chip}.

2.2.1.2 Restricciones en Z_{in} – Factor de calidad (Q)

El Factor de Calidad es un importante y descriptivo parámetro siempre relacionado con la resonancia. Q puede ser definido como [93]:

$$Q = w_o \frac{\text{energia almacenada}}{\text{potencia media disipada}} \tag{2.9}$$

Donde w_o es la frecuencia de resonancia. Nótese que Q no tiene unidades y que es proporcional a la razón entre la energía almacenada y la energía perdida por unidad de tiempo. El conjunto de las impedancias de la antena y del chip puede verse como un circuito RLC, tal y como se muestra en la Figura 2.7.

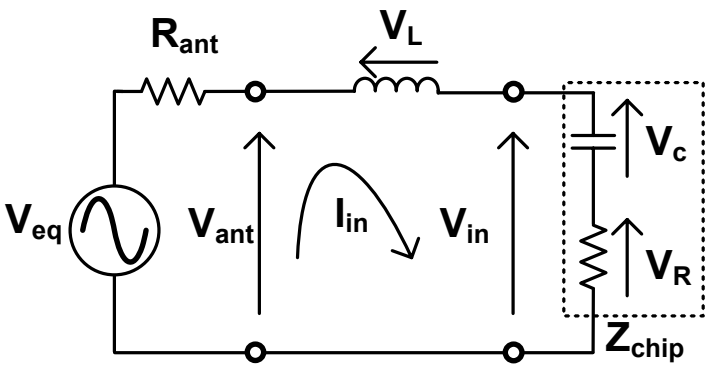

Figura 2.7: Circuito equivalente de la antena y el chip para calcular V_{in} como función de Q.

La respuesta en frecuencia de un circuito serie RLC se describe usando el Factor de

Calidad, puesto que éste se puede expresar como:

$$Q = \frac{f_0}{f_2 - f_1} = \frac{f_0}{BW} \tag{2.10}$$

Donde f_0 es la frecuencia de resonancia, y f_1 y f_2 son las frecuencias donde I_{in} (véase Figura 2.8) cae 3 dB con respecto a su valor en resonancia. El ancho de banda (BW) es definido como $f_1 - f_2$. Como conclusión, la Q de la impedancia de entrada está limitada por el ancho de banda del sistema.

Las frecuencias de interés para una etiqueta RFID de largo alcance pasiva son 868 MHz en Europa (ITU Region 1), 915 MHz en América (ITU Region 2) y 950 MHz en Asia (ITU Region 3). Por lo tanto, una etiqueta RFID compatible con todas las regiones requiere un ancho de bando de unos 100 MHz centrado en 900 MHz. Esta restricción limita el valor de Q a 9, como se muestra en la Figura 2.8.

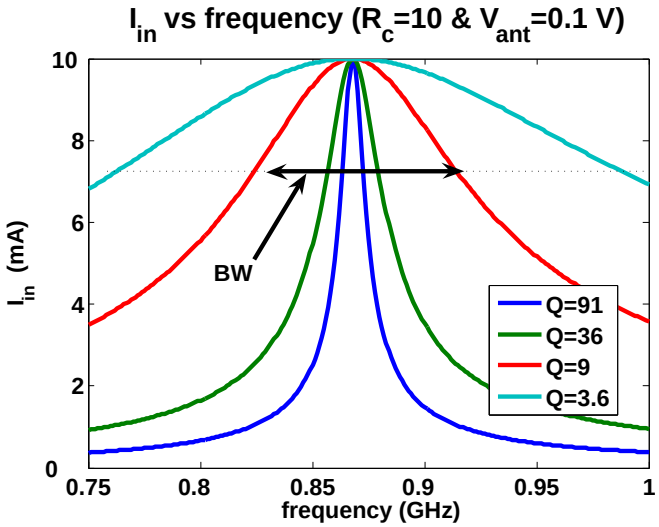

Figura 2.8: Respuesta en frecuencia de I_{in} para diferentes valores de Q.

2.2.2 Restricciones en el sistema de comunicación

La etiqueta RFID es alimentada por una onda de radiofrecuencia desde el lector, la misma onda se usa para la comunicación. El lector y la etiqueta forman un sistema Half–Duplex que proporciona comunicación en las dos direcciones, pero sólo en una dirección en un determinado momento, esto es no simultáneamente.

2.2.2.1 Comunicación lector etiqueta

Un lector se comunica con una o más etiquetas modulando en amplitud la portadora de RF usando ASK (Modulación con desplazamiento de Amplitud, Amplitude–Shift Keying) con PIE (Codificación en intervalos de pulso, Pulse Interval Encoding) [31]. Esta modulación es también conocida como *On–Off Keying* (OOK) y es un tipo de modulación que representa datos digitales con presencias o ausencias de señal portadora.

Una vez introducida la modulación, se procederá al análisis de su influencia en el sistema de recuperación de energía. Como consecuencia de las ausencias de señal RF,

el rectificador se convierte en un circuito abierto y el condensador de alimentación se descarga a través de la resistencia R, que representa el consumo de corriente de la etiqueta, ver Figura 2.9.

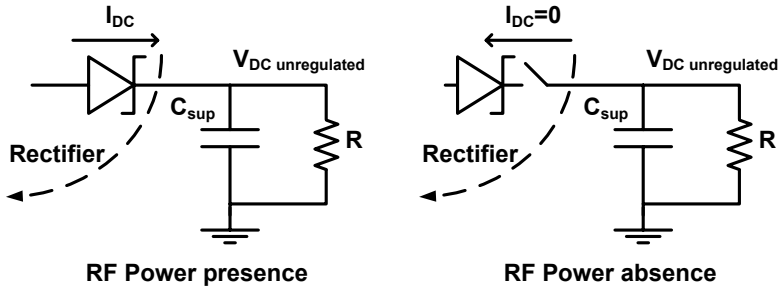

Figura 2.9: Descarga del condensador de alimentación cuand se producen ausencias de señal a la entrada.

El condensador de alimentación (C_{sup}) debe ser dimensionado de forma que la tensión en la resistencia R no caiga por debajo de la tensión mínima de alimentación requerida por la tecnología, en la que se fabrique la Etiqueta RFID, para trabajar (V_{DCmin}). Suponiendo que el condensador está inicialmente cargado a una tensión V_{DC} mayor que V_{DCmin}, entonces:

$$C_{sup} = -\frac{13.125\mu s}{R\ln(\frac{V_{DCmin}}{V_{DC}})} \tag{2.11}$$

Nótese que el condensador de alimentación es un dispositivo integrado, por lo tanto su valor no puede ser arbitrariamente alto, puesto que el consumo de área se convierte en un problema. Se ha de encontrar un compromiso entre tensiones de alimentación, consumo de corriente y área del condensador.

2.2.2.2 Comunicación etiqueta lector

Una etiqueta se comunica con un lector usando modulación Backscatter. Este tipo de modulación consiste en conmutar la impedancia de entrada del chip entre dos estados de acuerdo a los datos que son enviados. Con esto se consigue reflejar de forma determinada la onda de RF enviada por el lector. El lector luego recibe la onda reflejada y extrae la información.

El estándar EPCGlobal establece que la modulación Backscatter de la etiqueta debe usar ASK y/o PSK (modulación por desplazamiento de Fase–Phase Shift Keying). La etiqueta selecciona el formato de modulación y el lector debe ser capaz de demodular los dos tipos.

La modulación PSK se consigue cambiando la parte imaginaria de la impedancia de entrada con la misma cantidad de desadaptación en los dos estados, esto es el coeficiente de reflexión permanece constante. Por otro lado, la modulación ASK requiere cambiar la parte real de la impedancia de entrada. Se ha probado [1] que ASK con coeficiente de reflexión constante en los dos estados es menos eficiente en potencia que PSK. Por lo tanto, sólo será considerado ASK con adaptación conjugada en un estado y desadaptación total en el otro, véase la Figura 2.10.

Existe diversos estudios a cerca de qué modulación es la más eficiente [1, 96, 5]. Todos ellos concluyen que la modulación PSK es más eficiente en potencia que la modulación ASK cuando la etiqueta está la misma cantidad de tiempo en el estado 1 (t_1)

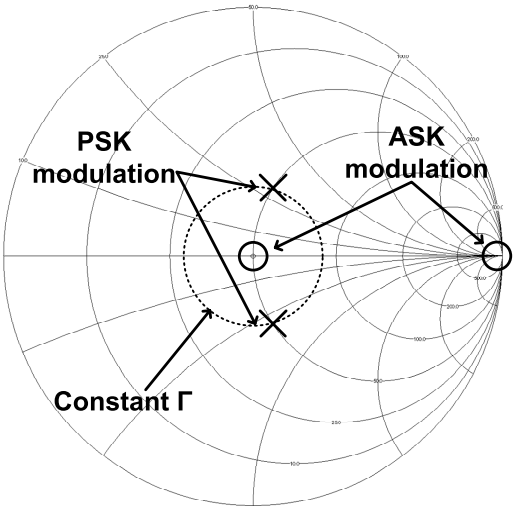

Figura 2.10: Estados de reflexión de la antena para las modulaciones PSK y ASK.

que en el estado 2 (t_2). La razón es que el coeficiente de reflexión y por lo tanto la potencia que entra al chip permanece constante en ambos estados. Por otro lado, en ASK, la potencia que entra al chip es máxima para un estado y nula para el otro. Sin embargo, cuando uno de los dos estados está activo la mayor parte del tiempo, (esto es $t_1 << t_2 \approx 1$) ASK se hace más eficiente en potencia a costa de un mayor ancho de banda. Otra importante ventaja de la modulación ASK sobre PSK es que la primera no necesita ningún elemento reactivo para su implementación. Un simple conmutador CMOS es suficiente. La Figura 2.11 muestra la implementación de los moduladores ASK y PSK. El modulador ASK es más simple que el PSK pues no requiere condensador. Con un diseño óptimo de la antena no es necesaria red de adaptación en el caso de ASK, mientras que para PSK al menos se necesita un elemento reactivo (por ejemplo una bobina). Este elemento reactivo puede ser implementado dentro o fuera del chip. En este último caso se requiere un pad de RF adicional a la entrada del chip.

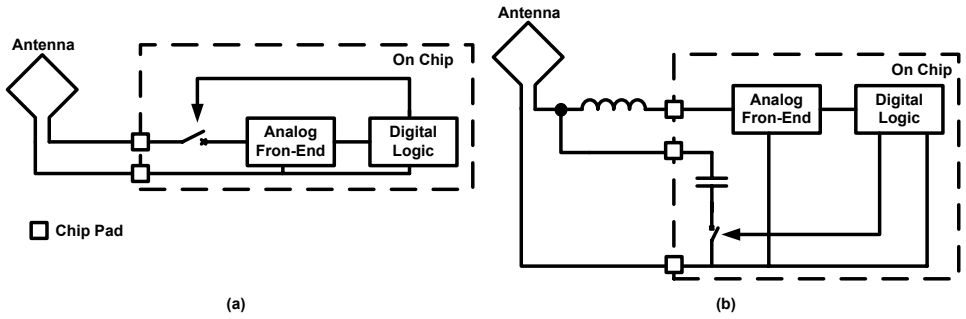

Figura 2.11: Posible implementación del (a) modulador ASK y (b) modulador PSK.

2.2.3 Consideraciones generales y especificación de diseño

Esta sección analiza el comportamiento de la tensión disponible en el condensador de alimentación durante el tiempo de enlace entre lector y etiqueta.

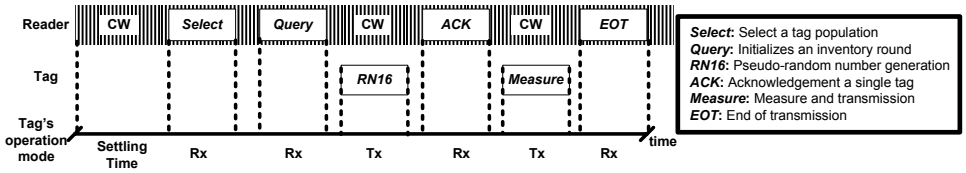

Figura 2.12: Tiempo de enlace entre el lector y la etiqueta como se describe en el estándar EPC global2.

La Figura 2.12 presenta el protocolo de comunicaciones durante el tiempo de enlace de acuerdo con el estándar EPCGlobal. Este protocolo se compone de los siguientes pasos:

1. El lector comienza la comunicación transmitiendo una onda continua (CW–*Continous Wave*) con una duración máxima de 1.5ms. Este periodo se conoce como *settling time* y sirve para cargar el condensador de alimentación y para activar la etiqueta.

2. El lector comienza a mandar comandos modulados en OOK, esto es, el lector comienza a conmutar la CW como consecuencia la potencia que alcanza a la etiqueta comienza a fluctuar.

3. Finalmente el lector espera a la respuesta de la etiqueta mientras transmite la CW. La etiqueta reacciona modulando de vuelta la CW, esto es cambiando la impedancia de entrada. Por lo tanto la potencia que llega al chip también fluctúa cuando la etiqueta responde.

El resultado de estas fluctuaciones de potencia a la entrada del rectificador son caídas en la tensión de alimentación que deben de ser contrarestadas con la carga almacenada en el condensador de alimentación.

Las siguientes ecuaciones definen la potencia (P_{in}) y tensión (V_{in}) de entrada del chip RFID como función del coeficiente de reflexión, distancia y factor de calidad de la impedancia de entrada.

$$P_{in} = (1 - \Gamma) \cdot G_r \cdot EIRP \cdot (\frac{\lambda}{4\pi r})^2 \tag{2.12}$$

y como

$$P_{ant} = \frac{V_{ant}^2}{2R_{ant}} \tag{2.13}$$

entonces

$$V_{in} = V_{ant}(1 + Q) = \sqrt{2P_{in}R_{ant}}(1 + Q) \tag{2.14}$$

Partiendo de V_{in}, la tensión a la salida del rectificador puede ser expresada como:

$$V_{DC} = N(V_{in} - V_{th}) \tag{2.15}$$

Sin embargo esta ecuación no modela el comportamiento del rectificador completamente pues no da idea sobre la carga a la salida. Hay que puntualizar, que la carga a la salida del rectificador influye en la potencia de entrada, la eficiencia y en la tensión V_{DC} de éste [97]. Ahora, sabiendo que la carga a la salida del rectificador modela el consumo del chip. Entonces, cuanto mayor es la potencia de entrada, mayor es la carga a la

Tabla 2.3: Comparación entre diferentes procesos tecnológicos

Característica	XFAB XL035LV	AMIS C5F/N	ATMEL SMOS3EE
Runs por Año	4	11	4
Área mín.(mm^2)	10	5	n.a.
Schottky V_{th} @ 10μA (V)	0.16	0.25	0.235
C densidad ($fF/\mu m^2$)	4.24	0.95	1.25
Tensión mín. de trabajo (V)	1 to 3.3	2.5 to 5	1.8 to 5.5
Tamaño mín. EEPROM (bits)	1	n.a.	256
EEPROM Voltage (V)	1.8 to 3.6	3 to 5.5	1.8 to 5.5
Bipolar	si	no	si
Charge pump	si	no	si

salida. Por otro lado, cuanto mayor es el consumo de corriente del chip, menor es la resistencia de salida. En la bibliografía nadie expresa la impedancia de entrada del multiplicador como función del consumo de corriente del chip. Sin embargo, esto es un aspecto fundamental para automatizar el diseño del rectificador. En el capítulo del rectificador se da un modelo matemático que tiene en cuenta estos factores para modelar la impedancia de entrada del rectificador.

2.2.3.1 Selección de la tecnología

La elección de un proceso tecnológico es un aspecto clave para realizar una especificación del diseño de los circuitos que conforman el sistema de recuperación de energía. La selección de tecnología se basa en factores técnicos, en logísticos y económicos. En el marco del proyecto WISEN se realizó una elección razonada de la tecnología. La Tabla 2.3 resume la comparación entre los diversos procesos posibles.

La Tabla 2.3 compara tres procesos de tres fabricantes diferentes: AMIS, XFAB y ATMEL. El primer fabricante fue elegido pues es ampliamente utilizado en el IIS Fraunhofer, lugar donde se realizó gran parte del trabajo de esta Tesis Doctoral. XFAB fue incluido en la comparación ya que sus procesos ofrecen la posibilidad de integrar MEMS y circuitos CMOS en el mismo sustrato. Finalmente, ATMEL fue incluido ya que en esta tecnología fue fabricada uno de las primeras etiquetas RFID UHF pasivas de largo alcance. Observando las hojas de especificaciones y la información disponible, la mejor opción es XFAB puesto que presenta la menor tensión de alimentación, la menor tensión umbral de los transistores, además dispone de condensadores con la mayor capacidad por área y latches de 1 bit.

2.2.3.2 Especificaciones de diseño

Una vez elegida la tecnología y realizadas las consideraciones de diseño pertinentes se puede proceder a realizar un análisis en detalle para fijar las especificaciones de diseño relativas a cada uno de los bloques que conforman el sistema de recuperación de energía. La Tabla 2.4 resume las especificaciones de diseño relativas a cada elemento circuital,

un desarrollo más detallado de los cálculos se puede encontrar en el apartado 4.5 de la versión en inglés.

Tabla 2.4: Especificación del sistema recuperación de energía

Rectificador	
V_{DC} ($R_{load} = 90K\Omega$)	2.35V (modulación PSK) and 2.8 V (modulación ASK).
Q	< 9
η (r=3m)	20%
Condensador de Alimentación	
C	1.2nF
Sensor de Tensión	
V_{th}	$1.6V$
$I_{consumption}$	$< 100nA$
Limitador de Tensión	
$I_{protection}$	1.17mA @ 3.6V
V_{thHVP}	3.6V
$I_{consumption}$	<100nA
Regulador de Tensión	
drop-out	<0.1V
V_{dd}	1.8V
V_{aa}	1.2V
I_q	$< 2\mu A$

Las especificaciones de diseño están divididas en los diferentes bloques que conforman el sistema de recuperación de energía. El rectificador se especifica en términos de mínima tensión de alimentación (V_{DC}) dependiendo de la modulación, Q de la impedancia de entrada y eficiencia (η). El mejor compromiso entre área consumida y almacenamiento de carga en el condensador de alimentación es 1.2 nF. El consumo de corriente y la tensión umbral del sensor de tensión y del limitador son especificadas, así como la corriente de protección en el limitador para evitar la ruptura del condensador de alimentación. Finalmente, El regulador de tensión se modela con la tensión de drop-out, consumo de corriente y tensiones de alimentación que debe generar; V_{dd} para la EEPROM y V_{aa} para el resto de circuitos del sensor RFID.

2.3 Diseño de los bloques circuitales

En esta sección se describe detalladamente la metodología de diseño empleada para desarrollar los circuitos del sensor RFID involucrados en la recuperación de energía y en la estabilización de la tensión de alimentación.

2.3.1 Diseño del rectificador

Tres son las variables envueltas en el diseño de un rectificador RFID en la banda de UHF:

- El tamaño de los diodos,
- el tamaño de los condensadores series y paralelo y
- el número de etapas del rectificador.

Los parámetros de diseño utilizados para encontrar la mejor combinación de las variables mencionadas arriba son:

- Impedancia de entrada Z_{in}. Necesaria para evaluar Q y diseñar la red de adaptación con la antena.
- Eficiencia (η). La conversión de potencia tienes que ser tan eficiente como sea posible para alcanzar altos rangos de operación. La eficiencia se define como:

$$\eta = \frac{P_{DC}}{P_{in}} 100 = \frac{V_{DC}^2}{P_{in} R_L} 100(\%) \tag{2.16}$$

  Donde P_{in} es la potencia que alcanza el rectificador, P_{DC} es la potencia de salida y R_L la resistencia que modela el consumo de potencia.

- La tensión de salida en condiciones de carga. El rectificador debe generar suficiente tensión para alimentar correctamente el sensor RFID.

En esta sección se presentan los dispositivos es decir los diodos Schottky y los condensadores, a continuación se discuten los diferentes parámetros y la metodología de diseño del rectificador.

2.3.1.1 Diodos Schottky integrados

Los diodos Schottky han sido utilizados desde hace más de 25 años en la industria de la generación de potencia [104]. Sus principales ventajas son muy baja caída de tensión en directa, y bajos tiempos de conmutación, que se acercan a cero, por lo tanto son los dispositivos ideales para etapas de salida en generadores de potencia conmutados. Su alta velocidad de conmutación hace este dispositivo útil en aplicaciones a altas frecuencias, incluyendo procesamiento de señal a muy baja potencia y aplicaciones con tiempos de conmutación por debajo de 100 picosegundos. Estas aplicaciones requieren diodos Schottky pequeños y con bajas capacidades parásitas. Existen diversas limitaciones en el diseño con diodos Schottky con respecto al clásico diodo de unión PN, debido a que las corrientes de pérdidas cuando el diodo está en corto en los primeros son varios órdenes de magnitud mayores que en los segundos. Otra desventaja de los diodos Schottky es que son más sensibles con la temperatura que los de unión PN. La Figura 2.13 muestra el modelo de RF de un diodo Schottky integrado [2]. El diodo ideal sería $R_f = 0$, $R_r = R_P = 0$ y $C_D = C_P = 0$. Sin embargo, los elementos del modelo pueden ser ajustados jugando con las dimensiones de los diodos. La Tabla 2.5 muestra los valores del modelo de tres diodos con diferentes tamaños.

El tamaño de $D3$ es el mínimo permitido por la tecnología, por lo tanto $D3$ presenta la menor capacidad de difusión y menores efectos parásitos. Sin embargo, diodos pequeños

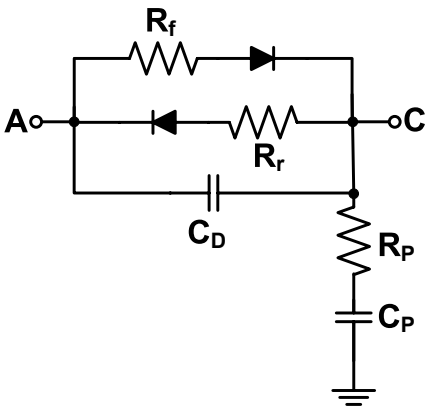

Figura 2.13: Modelo de RF de un diodo Schottky integrado [2].

Tabla 2.5: Características eléctricas de diversos diodos Schottky en XL035–XFAB

	Tamaño del diodo (μm^2)	R_f (Ω)	R_r (Ω)	C_D (fF)	R_P (Ω)	C_P (fF)
D1	16x20	17.5	2.4k	570	6.8k	227
D2	14x2.4	332	55k	30	63.5k	24
D3	7x1.2	665	91k	15	250k	6

tienen una mayor resistencia, puesto que la región P que forma el ánodo del diodo presenta una mayor resistividad por unidad de área. Esta resistividad puede ser reducida introduciendo más contactos y por lo tanto incrementando el área. Nótese que las corrientes de fugas aumentan cuando se incrementa el área.

2.3.1.2 Condensadores integrados

El circuito equivalente de un condensador integrado se muestra en la Figura 2.14.a.

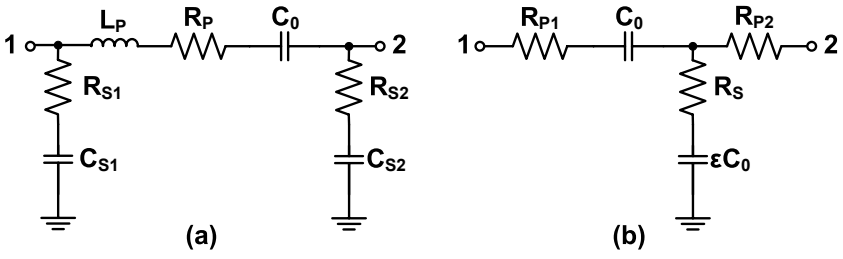

Figura 2.14: Modelo RF de un condensador integrado, (a) modelo general, (b) modelo simplificado de un condensador integrado de placas plano–paralelas.

Donde C_0 es la capacidad ideal entre los nodos 1 y 2, L_P y R_P son las inductancias y resistencias series parásitas respectivamente. El origen de R_P es la resistencia debida al material de la placa, los contactos y las vías. Estos elementos son comunes en todo tipo de condensadores tanto integrados como discretos. Los elementos restantes del modelo

son específicos de los condensadores integrados y comprenden la resistencia del sustrato (R_{S1} y R_{S2}) y la capacidad del sustrato (C_{S1} y C_{S2}). Estos elementos aumentan debido a la proximidad del sustrato del chip, que actúa como un plano de tierra.

En general, el condensador integrado es un dispositivo asimétrico. El tipo de condensador integrado más común es el formado por placas paralelas. Esta estructura es asimétrica puesto que la placa inferior aísla a la placa superior de los efectos del sustrato. Por lo tanto, si el nodo 1 es la placa superior entonces $R_{S1} \approx 0$ y $C_{S1} \approx 0$. De esta forma el modelo de la Figura 2.14.a se simplifica por el de la Figura 2.14.b. Nótese que C_{S2} ha sido renombrada como ϵC_0 para enfatizar que el condensador parásito es proporcional a C_0 y a una constante dependiente del proceso (ϵ).

2.3.1.3 Diseñando un rectificador

Un rectificador se caracteriza definiendo tres variables: El tamaño de los diodos Schottky, el tamaño de los condensadores y el número de etapas del rectificador.

El rectificador óptimo es definido como el que satisface las especificaciones de diseño usando la menor cantidad de potencia de entrada:

- V_{DC} ($R_{load} = 90\ k\Omega$)=2.35 V
- $Q < 9$

En este punto de puede introducir la eficiencia del rectificador como:

$$\eta = \frac{P_{DC}}{P_{in}} \tag{2.17}$$

Donde P_{in} es toda la potencia disipada en el sensor RFID incluido el rectificador y P_{DC} es la potencia disipada en el sensor RFID sin incluir el rectificador. Maximizar el valor de η es el mayor reto en el diseño de rectificadores.

Los pasos que se deben seguir para diseñar un rectificador son los siguientes (véase la Figura 2.15): Primero, definición de los requisitos y de la tecnología en la que se implementará el sistema. Segundo, el tamaño de los diodos es minimizado para maximizar R_p y R_r y para reducir C_D. El siguiente paso es buscar el condensador con las menores pérdidas de potencia y elementos parásitos y dimensionarlo de acuerdo con el tamaño del diodo. Finalmente, se añaden más etapas para alcanzar la V_{DC} deseada.

Figura 2.15: Pasos a seguir para diseñar un rectificador.

Tamaño de los diodos

La Figura 2.16 ilustra un rectificador de una etapa. Está compuesto por un condensador serie C_s un condensador paralelo C_p y por dos diodos con sus respectivas capacidades parásitas C_D. C_s está en el camino de la señal RF por lo tanto, su capacidad y resistencia parásita es crítica. Por el contrario, C_p está paralelo a la tensión continua de salida y su placa inferior está conectada a tierra, esto significa que la capacidad parásita está cortocircuitada y puede ser despreciada.

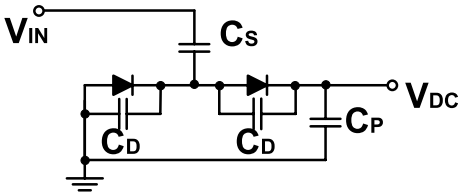

Figura 2.16: Rectificador de una etapa, incluyendo la capacidad de difusión del diodo (C_D).

Existen dos consideraciones de diseño a tener en cuenta para dimensionar los diodos del rectificador:

- La constante de tiempo (τ_c) de los condensadores del rectificador tiene que ser mucho mayor que el periodo de la señal de entrada ($\tau_c >> 1/\mathrm{f}$). Esto es debido a que los condensadores tienen que mantener la carga de un ciclo a otro de la señal de entrada. τ_c se calcula como $\tau_c = RC_{s,p}$ donde R es la resistencia que descarga el condensador. En el rectificador R es calculada de:

$$R = \frac{V_{cap}}{I_L + I_r + I_{par}} \tag{2.18}$$

  donde V_{cap} es la tensión continua en los condensadores, I_L es la corriente de salida del rectificador, I_r es la corriente reversa de fugas del diodo $I_{par} = \frac{V_d}{R_r}$ y I_{par} es la corriente DC que circula a través de la resistencia parásita del diodo al sustrato ($I_{par} = \frac{V_{cathode}}{R_{par}}$). Nótese que R_r y R_{par} requieren una alta capacidad para mantener la carga.

- La capacidad de difusión de los diodos (C_D) mucho menor que la de los condensadores del rectificador ($C_D << C_{s,p}$). Ambos pares de condensadores forman un divisor de tensión, y la tensión que cae en C_D no contribuye a la multiplicación de tensión, por ello debe ser minimizada.

Estas dos consideraciones llevan a una minimización del tamaño de los diodos para aumentar el valor de R_r y R_{par} y reducir C_D. La desventaja de reducir el tamaño de los diodos es que la tensión umbral del rectificador (V_{th}) aumenta y por lo tanto V_{DC} baja. La solución a esto es incrementar el número de etapas. Como conclusión los diodos de menor tamaño son los más eficientes para implementar el rectificador.

Tamaño de los Condensadores

En el rectificador ideal, la tensión en los diodos en estado estacionario es: $(V_p - V_{th} + sen(2\pi f))$. Esto es la señal de entrada más un cierto nivel de continua (véase Figura 2.17). Como resultado una vez que se alcanza la condición de estado estacionario, los diodos están casi todo el tiempo cortados. Nótese que el condensador debe ser lo suficientemente grande para mantener la carga entre dos ciclos sucesivos de la señal RF. En otras palabras, R_r no debe descargar los condensadores. Los condensadores se dimensionan considerando R_r como sigue:

Puesto que el tamaño del diodo es el mínimo permitido por la tecnología (véase D3 en la Tabla 2.5), esto es, R_r=91 $k\Omega$. Con este valor, la capacidad mínima requerida para

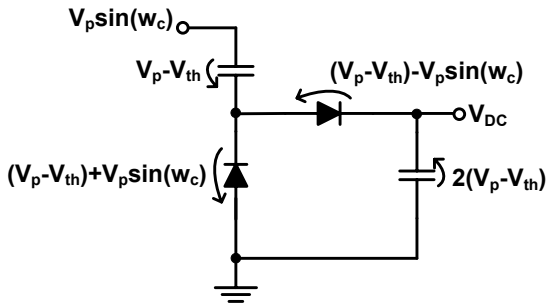

Figura 2.17: Tensión en los diodos y los condensadores del rectificador en régimen estacionario.

mantener el 99% de la carga en el condensador se calcula de la ecuación que describe la descarga de un condensador:

$$V(t) = V_0 e^{-\frac{t}{R_r C}} \tag{2.19}$$

donde V_0 es la condición inicial de carga del condensador, R es la resistencia de descarga y C la capacidad. Así la capacidad mínima es:

$$C \frac{\tau}{0.01 R_r} \approx 1.26pF \tag{2.20}$$

donde τ es la mitad del periodo ($\frac{1}{f}$). Nótese que cuanto mayor sea el condensador, más lenta será la descarga, lo cual es aparentemente mejor para el rendimiento del rectificador. Sin embargo, el área del condensador es directamente proporcional a la capacidad parásita por lo tanto no es conveniente aumentarla demasiado, especialmente en caso de los condensadores serie C_s.

Número de etapas

El número de etapas afecta al rendimiento del rectificador de las siguientes formas:

- Aumenta la razón $\frac{V_{DC}}{V_{in}}$. Puesto que hay más diodos envueltos en la multiplicación, la V_{in} requerida para obtener una determinada V_{DC} se reduce.
- La eficiencia del rectificador cae. Puesto que se aumenta el número de elementos (diodos y condensadores) también aumentan las resistencias parásitas que son las principales causantes de la reducción en la eficiencia. Las resistencias parásitas introducidas por lo diodos son especialmente críticas pues multiplican las pérdidas de corriente DC por N.
- Reducción de la Q de la impedancia de entrada. Las capacidades parásitas introducidas por los condensadores serie C_s aumentan con el número de etapas. La consecuencia es una reducción de la parte imaginaria de la impedancia de entrada. Como resultado Q (definida como $\frac{|X_s|}{R_s}$) cae cuando aumenta N.

2.3.2 Modelo matemático del rectificador

El objetivo de este modelo es describir el comportamiento del rectificador en términos de impedancia de entrada y de tensión de entrada como una función de los parámetros

Tabla 2.6: Expresiónes matemáticas para describir el comportamiento del rectificador

Número de Etapas	Parámetro	Expresión matemática
1	Im(Z_{in})	$X_p = \frac{1}{w(\epsilon C_s + C_{pad})}$
1	Re(Z_{in})	$R_p = \frac{R_L}{2 \cdot 2} \| \frac{R_{reff}}{2} \| R_{par}$
n	Im(Z_{in})	$X_p = \frac{X_{p\ 1st}}{\frac{N}{2}} = \frac{1}{w(C_{pad} + \frac{N}{2}(\epsilon C_s + 2C_D))}$
n	Re(Z_{in})	$R_p = \frac{R_L}{N^2} \| \frac{R_{reff}}{N} \| \frac{R_{par}}{\frac{N}{2}}$
n	V_{in}	$V_{in} = \frac{R_p}{R_s + R_p}(\frac{V_{DC}}{N} + V_{th} + V_{gap})$
n	Q	$Q = \frac{\lvert X_s \rvert}{R_s}$
n	η	$\eta = \frac{P_{DC}}{P_{in}} = \frac{\frac{V_{DC}^2}{R_L}}{\frac{V_{in}^2}{R_p}}$

del proceso, elementos (condensadores y diodos), número de etapas y requerimientos de potencia y tensión.

A modo de resumen se presenta en la Tabla 2.6 los resultados del modelo matemático.

2.3.3 Diseño del sensor de tensión

En esta Tesis Doctoral se proponen dos nuevas estructuras para realizar la función de sensor de tensión. La Figura 2.18.a muestra el circuito basado en niveles de tensión (VL–Voltage Levels). Este circuito considera el nivel de tensión alcanzado en la puerta del transistor M11. Una carga formada por los transistores M1–M10 no conduce corriente hasta que $V_{DC} > 5V_{th}$ (alrededor de 2.5 Voltios en la tecnología CMOS de 0.35μm seleccionada). Sin embargo M11 empieza a conducir una pequeña corriente (i_{sth}) en la región de *Subthreshold* ($V_{GS} < V_{th}$). La corriente i_{sth} descarga el pequeño condensador C y finalmente el inversor genera un flanco de subida. La etapa de salida consume corriente sólo en la transición de ES. El pico de corriente en el transistor depende de la capacidad de C y de las dimensiones de M13 y M14. Antes de la activación del flanco de ES, la carga y M11 están aún cortados y la corriente está por debajo de 1nA.

La Figura 2.18.b muestra el segundo sensor de tensión propuesto en esta Tesis Doctoral basado en la carga de un condensador (CC). La carga formada por los transistores M1–M4 carga el condensador C1. Cuando la carga en el condensador es $2V_{th}$, M5 conmuta y se produce el flaco de subida de la señal ES. M11 descarga C1 cuando la etiqueta se apaga. El circuito CC conduce corriente sólo en el flanco de subida de la señal ES. La carga y la etapa de salida son circuitos abiertos para las corrientes continuas gracias a los condensadores C1 y C2.

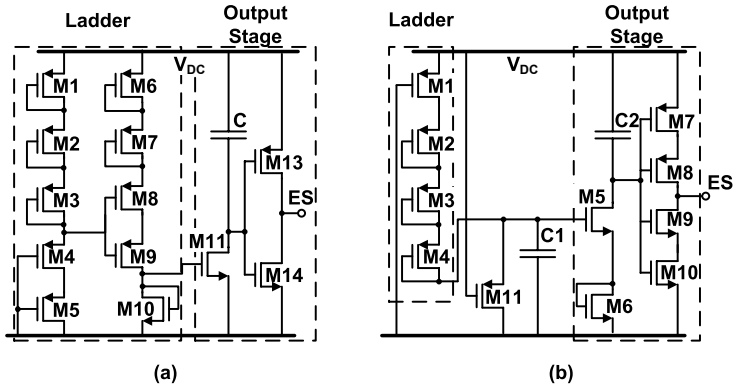

Figura 2.18: Nuevos circuitos propuestos. (a) Basado en niveles de tensión (VL), y (b) basado en la carga de un condensador (CC).

2.3.3.1 Consideraciones de diseño

El rendimiento de los circuitos propuestos es muy dependiente de la tecnología y de la temperatura porque la tensión umbral (V_{th}) de los transistores se usa como única referencia de tensión. Las dimensiones de cada transistor son elegidas de forma que la tensión umbral y el consumo de corriente del circuito estén para todas las esquinas de la tecnología (los peores casos) dentro de las especificaciones de diseño. Nótese que la tensión umbral del sensor de tensión (ES_{th}) ajustado introduciendo o eliminando transistores en las cargas.

2.3.3.2 Simulaciones y comparación

Los circuitos descritos en el apartado de estado del arte y las nuevas estructuras propuestas han sido simulados y comparadas a nivel de esquemático usando la tecnología estándar 2P4M CMOS de 0.35μm de XFAB.

Parámetros para evaluar el rendimiento

La carga del condensador de alimentación depende de la distancia al lector, el rectificador utilizado y de la capacitancia del condensador de alimentación. Puesto que el objetivo es reducir el consumo de potencia y de área para condiciones estándar de funcionamiento. Para comparar las diferentes arquitecturas, todos los circuitos son ajustados para que la señal ES se active para una V_{DC} para todos las esquinas de la tecnología entre 2.5 V y 3.3 V (ES_{th}). Se simularon todas las esquinas. La tensión V_{DC} se genera por una fuente de pulsos con unos niveles de tensión entre 0 V y 3.3 V y tiempo de 50 μs para carga rápida, o 1.5 ms para carga lenta. Los parámetros obtenidos de la simulación fueron:

- Variación de ES_{th} con las esquinas de la tecnología. (ΔES_{thc}) y con el tiempo de carga del condensador de (ΔES_{tht});
- Consumo de corriente continua a 3.3 V ($\bar{I}$) y consumo transitorio de corriente cuando ES conmuta ($\hat{I}$);
- Área activa, que es calculada sumando el tamaño de los dispositivos requeridos

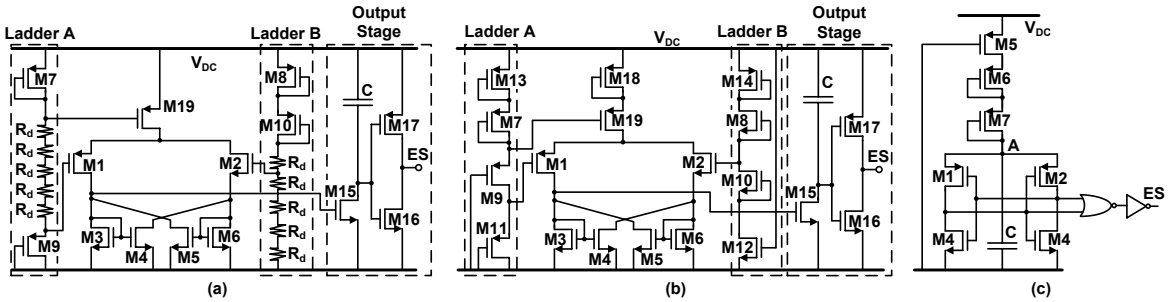

Figura 2.19: Circuitos de la bibliografía modificados. (a) MS', (b) MMS', y (c) POR'.

Tabla 2.7: Resultado de las simulaciones de los diferentes sensores de tensión

$Circuit$	$\bar{I}$ (nA)	$\hat{I}$ (μA)	ΔES_{thc} (V)	ΔES_{tht} (V)	$Area$ (μm^2)	ref.
MS	800	1.87	1.10	0.40	30148	[3]
MMS	57	1.44	0.85	0.50	693	[4]
POR	1350	1.55	1.40	0.20	348	[5]
VL	47	1.65	0.90	0.45	352	Proposed
CC	< 1	0.50	1.10	0.49	590	Proposed

Modificaciones en los circuitos de la bibliografía

El ajuste de ES_{th} a 2.5 V require algunas modificaciones en los circuitos propuesto en la bibliografía. En el circuito MMS (véase Figura 2.5.b), se ha modificado las cargas de transistores A y B, como se muestra en la Figura 2.19.b.

La ES_{th} en el POR original es muy baja (algunos cientos de mV). Para hacer una comparación justa, la tensión umbral del circuito se incrementó a 2.5 V introduciendo los transistores M6 y M7 como se muestra en la Figura 2.19.c.

Finalmente, la etapa de salida usada en VL se introduce en los circuitos MS y MMS para reducir el consumo de corriente como se muestra en la Figura 2.19.b. Los circuitos de la bibliografía modificados se denominan MS', MMS' y POR'.

Resultado de la comparación

La Tabla 2.7 muestra las simulación de los resultados. El consumo de corriente continua es menor que 1 nA para el caso del circuito CC debido a que los condensadores C1 y C2 (véase la Figura 2.18.b) se comportan como circuitos abiertos en continua. La corriente $\bar{I}$ es 47 y 57 nA en VL y MMS', respectivamente. Las cargas son similares pero el circuito MMS' incluye un consumo extra de corriente debido al comparador. El uso de cargas resistivas en MS' incrementa dramáticamente el consumo de corriente debido al valor limitado de las resistencias integradas. Finalmente, el mayor $\bar{I}$ corresponde al circuito POR' que presenta un valor inusual de más de 1 μA. El circuito POR fue diseñado para una ES_{th} de 1 V, y un incremento de este valor incrementa el consumo de corriente continua del circuito.

La corriente de pico es similar en el MS', MMS', POR' y VL debido a que todas las arquitecturas usan el mismo inversor a la salida. $\hat{I}$ en el circuito CC es alrededor

de un 66% menor que los restantes circuitos. Esto es debido a que los transistores del inversor de salida en el circuito CC tienen una relación de aspecto menor que en las otros circuitos.

La variación de ES_{th} debido a las esquinas de la tecnología es de alrededor de 1 V, y la variación debido al tiempo de carga del condensador es de unos 0.4 V. Para bajos tiempos de carga, ES_{th} es mayor que para tiempos largos. La razón es que los transistores usados tienen una relación de aspecto muy baja (W/L$\approx$ 0.09). Esto reduce el consumo de potencia de los circuitos para incrementar el tiempo requerido para conmutar los transistores.

Finalmente, el área activa del circuito MS es dos órdenes de magnitud mayor que los otros circuitos. Esto se debe al uso de resistencias integradas de alto valor para reducir el consumo estático de potencia en las cargas laterales del circuito (véase la Figura 2.19.a).

Resumiendo, MS' y POR' presentan el mayor consumo de corriente; y para el caso de MS' el mayor área activa. El circuito CC muestra el menor consumo de corriente estática. En términos de variación de ES_{th}, VL y MMS' obtienen los mejores resultados. Sin embargo, la corriente continua $\bar{I}$ y el área consumida por MMS' son 2.85 y 1.97 veces mayores que en VL, respectivamente. Finalmente, nótese que los circuitos modificados MMS' y MS' consumen 18 y 6 veces menos corriente que los originales.

Para concluir, los resultados de las simulaciones indican que VL y CC son las mejores estructuras. Estos dos circuitos fueron implementados para verificar los resultados de la Tabla 2.7.

2.3.4 Limitador de tensión

La tensión en el condensador de alimentación aumenta con el nivel de potencia RF a la entrada del Multiplicador de Tensión o Rectificador, cuando el consumo de corriente de la etiqueta permanece constante. El nivel de la potencia RF recibida incrementa de forma cuadrática a medida que la distancia entre Lector y Etiqueta disminuye (véase la Fórmula de Transmisión de Friis [108]). Por otro lado, el proceso CMOS limita la tensión en el condensador de alimentación a 3.6 Voltios. Por lo tanto, el condensador debe ser protegido contra altas tensiones que se puedan producir por la cercanía del lector.

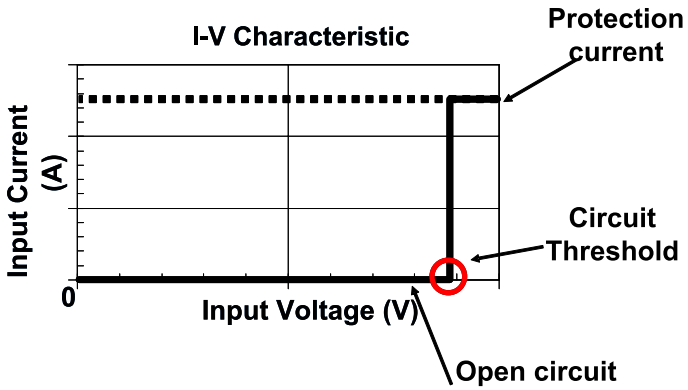

Figura 2.20: Característica (I–V) ideal del circuito limitador de tensión.

La característica Corriente–Tensión (I–V) ideal de un limitador se muestra en la Figura 2.20. El limitador no conduce corriente hasta se alcanza una tensión umbral, después de esto el circuito se comporta como un corto. Para implementar esta

característica, se ha usado circuito basado en el limitador propuesto en [6] (véase la Figura 2.21.a). Tan pronto como la V_{DC} supera la suma de todas las tensiones umbrales de los transistores M3–M5, la corriente empieza a circular por R1. Cuando la caída de tensión en R2 alcanza el umbral, M2 conmuta y activa M1 que es por donde circula la corriente de protección. La resistencia R3 fija el nivel de la corriente a de protección.

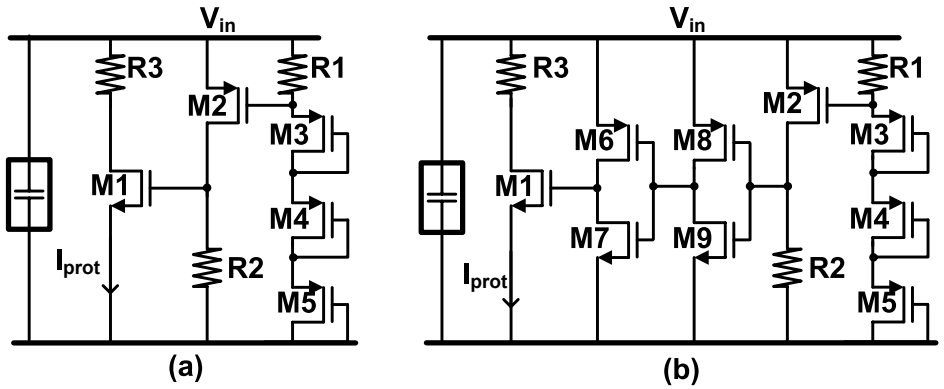

Figura 2.21: Circuitos limitadores: (a) sin inversores basado en [6], y (b) con inversores propuesto por esta Tesis Doctoral.

Una consecuencia del diseño de circuitos de muy bajo consumo es la reducción de la velocidad de conmutación de los transistores. La razón es que los condensadores parásitos en los transistores se cargan y descargan con corrientes muy pequeñas. Para el caso particular del circuito limitador de la Figura 2.21.a, esto significa un incremento en la zona de degradación (rango de tensión por debajo de la tensión umbral y con un consumo de corriente por encima de 100nA). Para reducir la región de degradación se propone el circuito de la Figura 2.21.b. En este circuito se han introducido dos inversores en la puerta de M1. Esta modificación incrementa la velocidad de conmuación de M1 puesto que la tensión que controla la puerta del transistor M1 cambia con los inversores más abruptamente.

2.3.5 Regulador LDO de baja potencia

Un regulador serie de bajo drop-out es un circuito que proporciona una tensión DC bien especificada y estable [114] cuya diferencia de tensión entre la entrada y la salida es baja. El término serie viene de el hecho de que un transistor de potencia (dispositivo de paso) se conecta en serie entre los terminales de entrada y de salida del regulador.

Un comparador controla el dispositivo de paso que suministra potencia a la carga en la salida del regulador (R_{out}). La tensión en el nodo de salida es luego realimentada al comparador, el cuál genera una tensión de control comparando la señal realimentada con una referencia. Este tipo de regulador tiene dos características intrínsecas. Primero, la magnitud de la tensión de entrada es mayor que la de salida. Segundo, la impedancia de salida tiene que ser baja para conseguir un buen rendimiento [115].

La Figura 2.22 ilustra el diagrama de bloques de un regulador LDO genérico. El circuito está compuesto por una referencia de tensión, un comparador, un elemento de paso y una red de realimentación. La referencia de tensión proporciona una tensión continua estable con limitada capacidad de carga. El comparador, el elemento de paso y la red de realimentación forman el bucle de regulación. La dependencia con la temperatura de

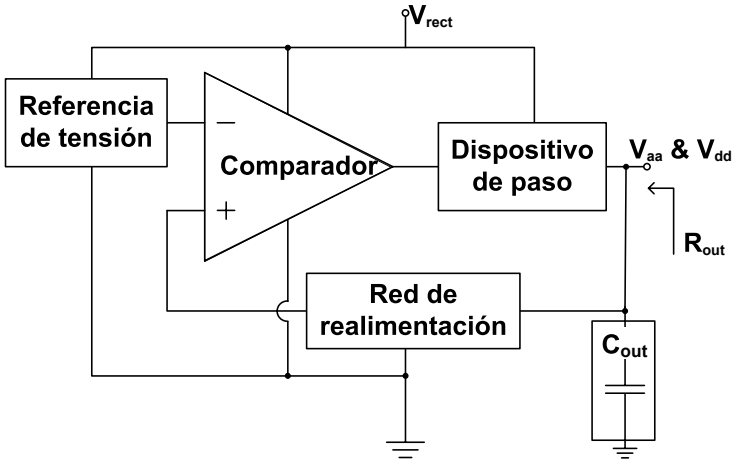

Figura 2.22: Diagrama de bloques de un regulador de bajo dropout.

la referencia y el nivel de continua a la entrada del comparador definen el coeficiente de temperatura de todo el sistema, por lo tanto se prefieren referencias de baja dispersión y comparadores con baja tensión de offset de entrada.

2.3.5.1 Especificaciones

Antes de proceder a relatar las guías de diseño del regulador LDO para el sistema de recuperación de energía del sensor RFID pasivo, es conveniente recordar las especificaciones comentadas en el Capítulo 2.2:

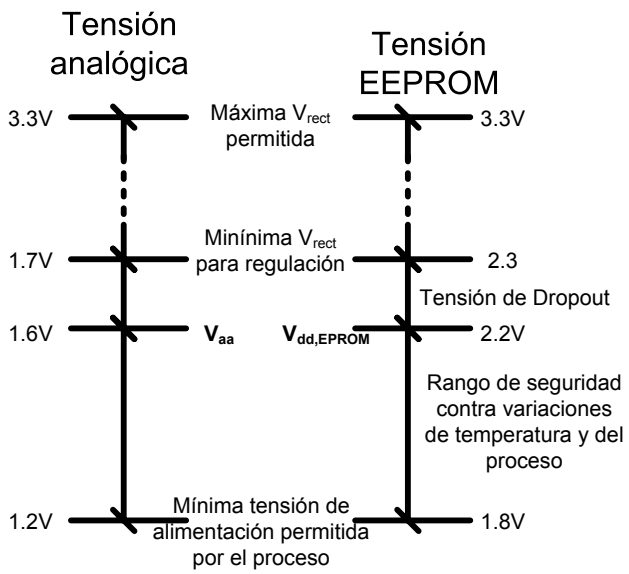

Figura 2.23: Tensión requerida para el correcto funcionamiento del sensor RFID pasivo.

1. Drop-out≈0.1 V. Para tener una idea gráfica de esta especificación obsérvese la Figura 2.23.

2. V_{dd}=1.8 V y V_{aa}=1.2 V. La EEPROM requiere una mínima tensión de alimentación (V_{dd}) de 1.8 V, mientras que el resto de circuitos pueden trabajar con una tensión

Tabla 2.8: Parámetros de diseño para los elementos del regulador LDO

Elemento del regulador LDO	Parámetros de diseño
Red de realimentación	Comportamiento AC,Consumo de corriente, V_{out}
C_{out}	Comportamiento AC y transitorio, área
Dispositivo de paso	Comportamiento AC, dropout, corriente de salida
Comparador–Amplificador	Comportamiento transitorio, consumo de corriente

Tabla 2.9: Comparación de las referencias de tensión a nivel de simulación

Circuit	V_{ref} (V)	ΔV_{corner} %	Idd nA	PSRR 1kHz (dB)	TK ppm/°C	PW_{sr} (μs)
Oguey [126]	0.305	+/- 61	2.1	-12	2950	249
Vita [124]	0.521	+/- 31	53	-30	1580	362
Cheng [122]	0.466	+/- 29.6	133	-43	1770	457
Fiori [121]	1.5	+/- 21	294	-45	342	283
Bgp	1.21	+/- 1.5	878	-31	105	504

de alimentación menor (V_{aa}=1.2 V). Definiendo dos tensiones de alimentaciones conseguimos; primero que la EEPROM pueda ser apagada cuando no se necesite y segundo que una tensión de alimentación pueda ser usada para el resto de circuitos.

3. $I_{consumo}$ <2μA. Esta es la corriente consumida por todo el regulador.

De estas especificaciones se puede extraer que se requieren dos reguladores LDO para generar las dos tensiones de alimentación. La implementación de cada elemento del regulador se debe diseñar de acuerdo a los parámetros descritos en la Tabla 2.8. Para la selección de la referencia se aplica un proceso especial que se describe a continuación.

2.3.5.2 Selección de la referencia de tensión

Se ha realizado una comparativa de las referencias de tensión encontradas en la bibliografía a nivel de simulación. Para ello se han introducido los esquemáticos de 5 referencias de tensión de bajo consumo y se han simulado utilizado la tecnología seleccionada para el desarrollo de esta Tesis Doctoral. La Tabla 2.9 muestra el resultado de esta comparación.

El circuito Bandgap ofrece una referencia de tensión muy estable tanto con la temperatura (TK) como con las esquinas de la tecnología (ΔV_{corner}) a costa de un mayor consumo de corriente. Su comportamiento en términos de PSRR (variación de la referencia cuando varía la tensión de alimentación) y PW_{sr} (tiempo que requiere el circuito para generar la tensión de referencia) es moderado, aunque estas características no son cruciales para sensores RFID. El resto de referencias presentan un menor consumo de corriente pero una mayor sensibilidad de V_{ref} con la tecnología y la temperatura. Como conclusión, los circuitos más apropiados para generar una referencia de tensión estable

de corriente son Cheng y Fiori, si prima el muy bajo consumo, y el Bandgap si prima la estabilidad de V_{ref} con la temperatura y la tecnología.

2.3.5.3 Red de realimentación

La red de realimentación puede ser implementada con resistencias o con condensadores. Las realimentaciones resistivas no introducen polos al sistema. Sin embargo, implican consumo de corriente estática, por lo tanto aumenta el consumo del regulador. La redes de realimentación capacitivas no consumen corriente estática, puesto que los condensadores son circuitos abiertos en continua. Por contra, estas últimas introducen polos al sistema que hacen que el comportamiento en alterna del regulador se degrade. Pero, como muestra la Figura 2.22, la red de realimentación está en paralelo con el condensador de salida (C_{out}). Por lo tanto el efecto de la realimentación capacitiva en AC se puede despreciar frente a C_{out} ya que:

$$C_{out} >> C_{fbn} \tag{2.21}$$

Donde C_{fbn} es el equivalente serie de los dos condensadores que forman la red de realimentación. Para concluir, la red de realimentación es implementada con condensadores puesto que la realimentación capacitiva no consume corriente estática y no degrada, excesivamente, la respuesta AC del sistema.

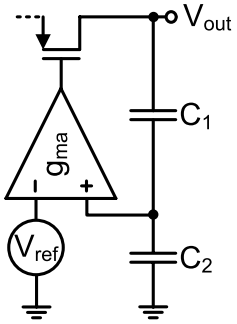

Figura 2.24: Red de realimentación.

Asumiendo el principio de tierra virtual del amplificador operacional, el valor de C_1 y C_2 puede ser fácilmente deducido de la Figura 2.24 como:

$$V_{out} = V_{ref}\frac{C_1 + C_2}{C_1} \tag{2.22}$$

Donde, V_{ref} depende de la tensión de referencia utilizada, V_{out} es la tensión de alimentación (V_{dd} o V_{aa}). En este punto sólo es necesario conocer el valor de C_{out} para calcular C_1 y C_2.

2.3.5.4 Condensador de salida C_{out}

Los requisitos transitorios impuestos por la corriente de pico de la circuitería digital no pueden ser satisfechos por el comparador, puesto que no es suficientemente rápido. Como consecuencia se requiere un condensador de salida (C_{out}). La Tabla 2.10 enumera los parámetros necesarios para calcular C_{out}. La corriente de pico y la duración de los

Tabla 2.10: Parámetros requeridos para calucar C_{out}.

Magnitud	Valor
Pico de corriente	400μA
Durarción del pico	50ns
Área máx. de C_{out}	100pF
Mín. V_{out}	V_{aa}=1.2V; V_{dd}=1.8V

picos fueron obtenidas de las simulaciones post–layout de la parte digital del sensor RFID [130], mientras que el área máxima y la tensión mínima de V_{out} son fijadas por la tecnología.

La restricción impuesta por el área máxima del condensador limita el valor de C_{out} a 100 pF. De la ecuación de descarga del condensador [131] se puede calcular V_{out} para una caída de 300 mV con un pico de corriente. Como consecuencia el valor de V_{aa} y V_{dd} debe ser fijado al menos 300 mV por encima de la tensión de alimentación mínima requerida y permitida por el proceso. Para hacer el sistema más robusto a variaciones del proceso fijamos V_{aa}=1.6 V y V_{dd}=2.1 V.

La Figura 2.25 muestra el comportamiento de V_{aa} y V_{dd} con los picos de corriente cuando usamos diferentes valores V_{out}. Un condensador de 100 pF se requiere para mantener V_{dd} por encima de 1.8 V. Mientras que C_{out} se puede reducir a 50 pF para generar V_{aa}.

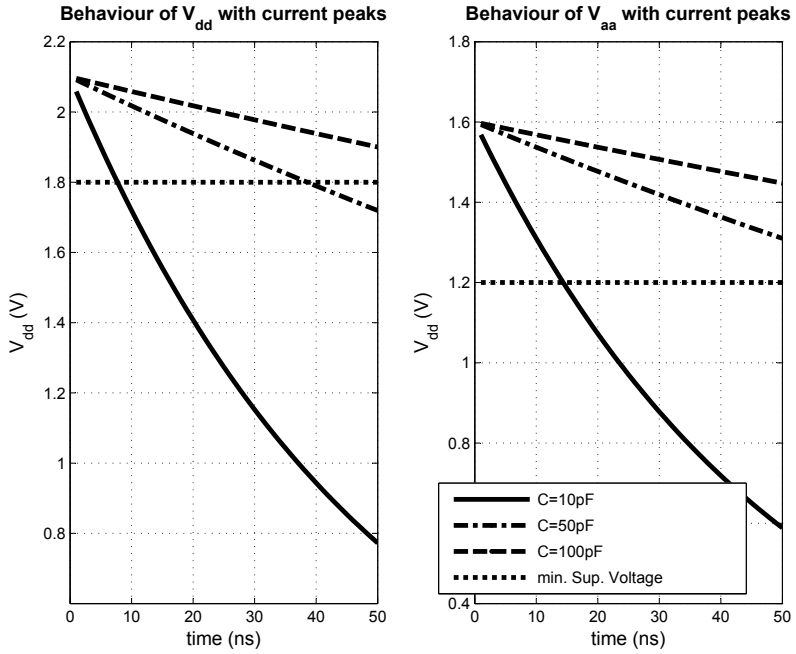

Figura 2.25: Comportamiento de V_{dd} y V_{aa} con los picos de corriente usando diferentes valores de C_{out}.

2.3.5.5 Elemento de paso

El dispositivo más adecuado como elemento de paso para aplicaciones RFID es el transistor PMOS. Ya que con éste se consigue la más baja tensión de drop-out a cambio de bajas corrientes de salida, que de todas formas serán bajas por la naturaleza de ultra bajo consumo de los sensores RIFD pasivos. Para dimensionar correctamente el dispositivo de paso se debe tener en cuenta que ha de suministrar una corriente media de 50 μA con unos picos de 400 μA.

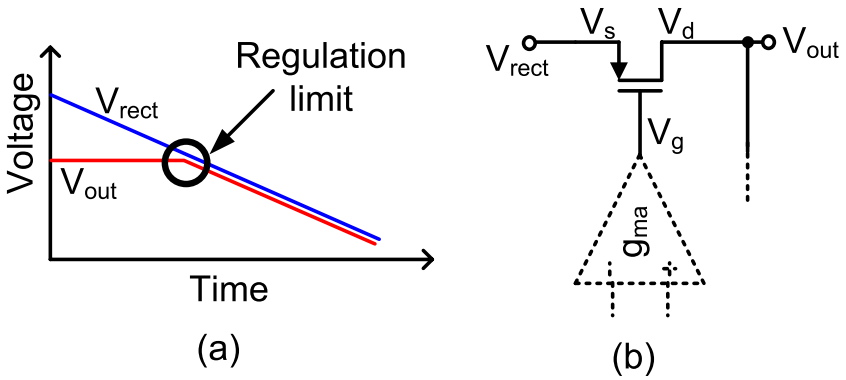

Figura 2.26: (a) Descripción gráfica del límite de regulación, (b) terminales del dispositivo de paso.

El límite de regulación se define como el punto donde $V_{rect} = V_{out} + V_{drop}$ y si V_{rect} cae por debajo de ese valor el circuito deja de regular, véase la Figura 2.26.a. El límite de regulación es también para el dispositivo de paso en la frontera entre la zona de saturación y la zona lineal. Nótese que en ese punto V_{ds} es igual a $-V_{drop}$.

En el límite de regulación, el dispositivo de paso tiene que ser capaz de dar 50 μA. Por lo tanto, puesto que la corriente en saturación de un transistor PMOS es:

$$V_{drop} = V_{ds} = V_{gs} - V_{th} \tag{2.23}$$

donde μ_p (mobilidad de huecos), C_{ox} (capacidad del óxido de puerta por unidad de área) y V_{th} (tensión umbral del transistor) son especificados por el proceso tecnológico. W y L son el ancho y la longitud del transitor. Como ya se ha deducido, en el límite de la zona lineal y saturación V_{drop} es:

$$\frac{W}{L} = \frac{2I_d}{\mu_p C_{ox} V_{drop}^2} \tag{2.24}$$

donde V_{ds} es la caída tensión entre los terminales de drenador y fuente del transistor PMOS. Por lo tanto la relación de aspecto del transistor debe cumplir que:

$$I_d = -\mu_p C_{ox} \frac{W}{L}((V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2) \tag{2.25}$$

Los transistores son dimensionados con la mínima longitud para minimizar la capacidad de puerta, y despejando de la Ecuación 2.24 se obtiene W.

En este punto es necesario comprobar que el dispositivo de paso sea capaz de suministrar la corriente de pico sin violar la condición de mínima tensión de alimentación en el límite de regulación. Para ello se considera la expresión que modela el comportamiento del transistor PMOS en la zona lineal y aplicando las condiciones de tensión se comprueba que I_d no sea superior a 400 μA.

2.3.5.6 Comparador

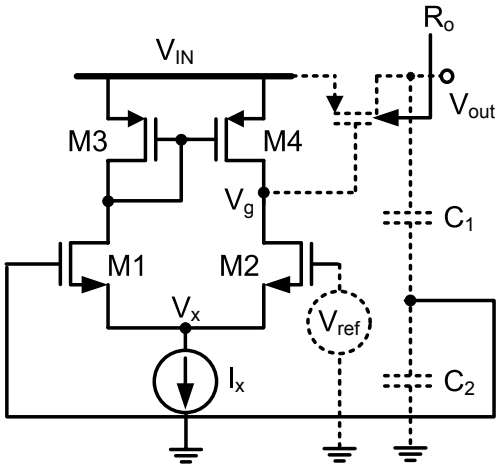

Figura 2.27: Esquemático del amplificador–comparador.

La Figura 2.27 muestra el esquemático del comparador. La estructura más apropiada para implementar es el par diferencial debido a su simplicidad, a su bajo consumo, fácil polarización y alta linealidad. Las dimensiones de los transistores M1–M4 junto con la corriente I_x son las variables de diseño en este circuito.

Para determinar I_x se deben considerar dos aspectos; primero, el consumo de corriente y segundo, el *Slew–Rate* a la salida o corriente necesaria para cargar adecuadamente la capacidad de puerta del elemento de paso en un tiempo aceptable. La Figura 2.28 muestra la tensión de puerta del dispositivo de paso en función del tiempo para diferentes corrientes I_x. La tensión en la puerta es 1 V y la capacidad es de 2.5 fF, que se corresponde con un transistor con W/L=60 y L=0.5 μm. Como se puede apreciar en la gráfica, I_x=100 nA no es sufiente para cargar un transistor en un tiempo por debajo de 40 ns, que es el máximo tiempo en el que C_{out} puede mantener la tensión de salida sobre el límite. El tiempo de respuesta se reduce aumentando el valor de I_x. Un valor de 200 nA es un compromiso aceptable entre tiempo de respuesta y consumo de corriente.

El tamaño de los transistores determina la ganancia en bucle abierto (A_{ol}), que influye en la resistencia de salida del regulador de la siguiente forma:

$$R_o = \frac{R_{o-pass}}{1 + A_{ol}\beta} \tag{2.26}$$

Puesto que la corriente de alimentación de un sensor RFID asciende a unas decenas de microamperios, R_o no es un parámetro crítico. Una resistencia de salida por encima de 1kΩ es suficiente. Consecuentemente, la ganancia en bucle abierto del amplificador no va a ser un factor limitante y no hay grandes restricciones a la hora de dimensionar los transistores M1–M4. Los parámetros utilizados para dimensionar estos transistores son: primero, los cuatro transistores serán dimensionados idénticos para mejorar la simetría del amplificador. Segundo, la longitud es minimizada para reducir al máximo capacidades parásitas. Finalmente, el ancho del transistor puede ser definido de R_o. Así, R_{o-pass} se calcula asumiendo [95] que:

$$R_{o-pass} = \frac{1}{\lambda I_o} \tag{2.27}$$

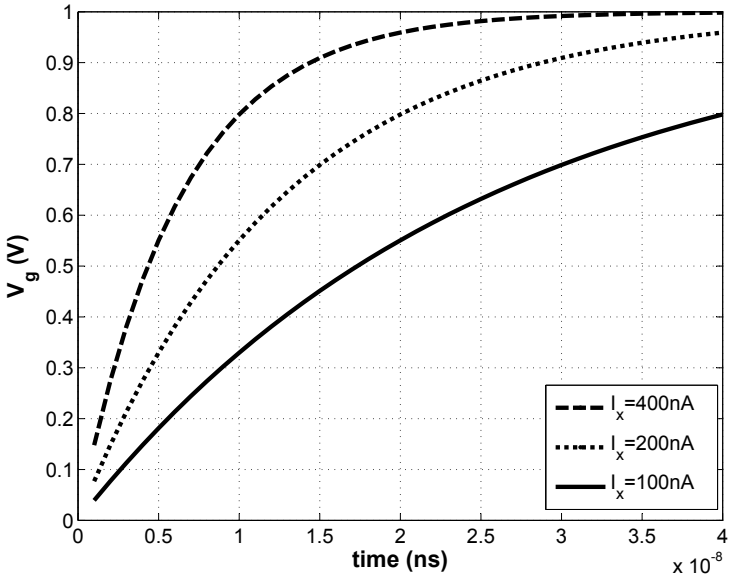

Figura 2.28: Retraso en V_g del dispositivo de paso para diferentes corrientes de polarización en el amplificador (C_g=2.5 fF). La caída de tensión en la puerta del dispositivo de paso es de 0 a 1 V.

donde λ es el coeficiente de modulación de la longitud del canal, cuyo valor normalmente es 0.5. Por lo tanto, R_{o-pass}=40kΩ, asumiendo I_o=50 μA.

Por otro lado, el factor de realimentación es:

$$\beta = \frac{C_1 + C_2}{C_1} = \frac{V_{ref}}{V_{out}} \tag{2.28}$$

Para cada tensión de alimentación es diferente:

$$\beta_a a = \frac{V_{ref}}{V_{aa}} = \frac{1.2V}{1.6V} = 0.75 \beta_d d = \frac{V_{ref}}{V_{dd}} = \frac{1.2V}{2.2V} = 0.56 \tag{2.29}$$

La ganancia en bucle abierto del par diferencial con un espejo de corriente activo es [95]:

$$A_{ol} = g_{mM2}(r_{OM2} || r_{OM4}) \tag{2.30}$$

donde

$$g_{mM2} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} \tag{2.31}$$

y

$$r_{OM2} = \frac{1}{\lambda I_{DM2}} \tag{2.32}$$

Puesto que I_{DM2}=100 nA y $\mu_n C_{ox}$ $\approx$165 $\mu A/V^2$ para el proceso elegido, A_{ol} es 81 si M1–M4 son dimensionados con W/L=2. Nótese que para esta A_{ol}, la impedancia de salida del regulador es 655 Ω. Este valor es suficiente para entregar la corriente de algunas decenas de microamperios requerida para alimentar el sensor RFID.

2.4 Resultados y medidas

Una vez explicadas la metodología utilizada en el desarrollo de esta Tesis Doctoral se procede a resumir los resultados obtenidos después de implementar, fabricar y medir los diferentes bloques que conforman el sistema de recuperación de energía de un Sensor RFID. La Figura 2.29 muestra el chip de Test, fabricado en el proceso de bajo consumo CMOS 0.35μm de XFAB, para probar los circuitos que conforman el sensor RFID del proyecto WISEN, de forma separada y conjunta. En la parte izquierda se encuentran los circuitos diseñados e implementados en el marco de esta Tesis Doctoral. En el centro se encuentran el *Front–End* analógico completo donde se integran el regulador, la protección y el sensor de tensión, desarrollados en esta Tesis Doctoral. En el *Front–End* también se incluye el condensador de alimentación, modulador, demodulador y rectificador, circuitos diseñados e implementados en el CEIT y TECNUN. En la parte derecha se encuentran circuitos de test particulares diseñados en CEIT y TECNUN.

Figura 2.29: Micro–fotografía del chip de test.

2.4.1 Medidas: Rectificador

Tres rectificadores con 4, 6 y 8 etapas han sido implementados y medidos. Para las medidas del rectificador se ha utilizado una estación de puntas directamente conectada a un analizador de redes vectorial (VNA–Vectorial Network Analizer). A la salida del rectificador se conectó directamente una resistencia variable. La potencia de salida del VNA se varió entre -5 y 5 dBm. La impedancia de entrada, la tensión de salida y el coeficiente de reflexión fueron medidos para evaluar cada rectificador. La Figura 2.30 compara las medidas con los resultados teóricos de un rectificador de cuatro etapas cargado con 136 kΩ y 52 kΩ. Tanto la tendencia como el resultado numérico de la impedancia de entrada medida en el rectificador se ajustan bien a los resultados teóricos. Por otro lado, la potencia de entrada medida es algo mayor que la calculada. La razón es que algunas pérdidas óhmicas (resistencia serie del condensador, pads, y otros) no fueron tenidas en cuenta por el modelo. Cuando la corriente de entrada aumenta lo mismo hacen las pérdidas óhmicas.

La Figura 2.31 compara resultados medidos y calculados de tres rectificadores bajo las mismas condiciones de carga. Los rectificadores son de 4, 6 y 8 etapas y están cargados con una resistencia de 1 MΩ. Como en la gráfica anterior, Z_{in} se ajusta bien a las predicciones teóricas. La tendencia de la potencia de entrada medida también sigue los resultados calculados.

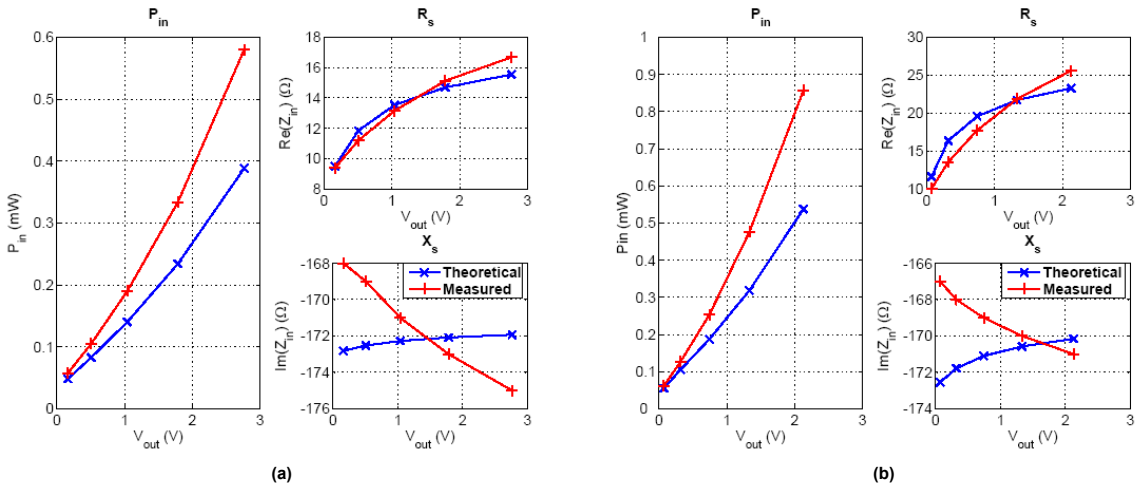

Figura 2.30: Resultados medidos frente a resultados teóricos de un rectificador de cuatro etapas.

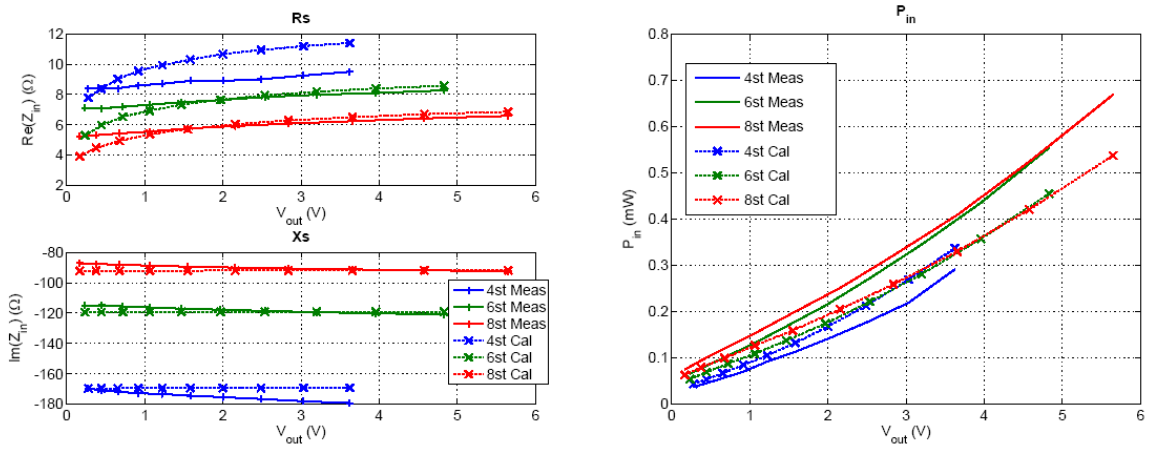

Figura 2.31: Comparación de los resultados medidos frente a los calculados de tres rectificadores bajo las mismas condiciones de carga.(R_L=1 MΩ).

Tabla 2.11: Resultados medidos de los sensores de tensión propuestos en esta Tesis Doctoral

$Circuit$	$\bar{I}$@3.3V (nA)	$\hat{I}$ (μA)	ES_{th}@1ms (V)	ES_{th}@1μs (V)	$Area$ (μm^2)
VL (2.5V)	69	1.79	2	2.5	2584
VL (3.3V)	19	2	3	4.2	3380
CC (2.5V)	0.2	0.75	2	2.8	3762
CC (3.3V)	0.4	1.5	3	4.2	3843

En resumen, el modelo matemático propuesto para modelar el comportamiento del rectificador se ajusta bastante bien a los resultados medidos, especialmente la impedancia de entrada. La tendencia de la potencia de entrada medida también se ajusta a las predicciones. Sin embargo para, los valores absolutos de P_{in} medidos son superan a los calculados para una misma tensión de salida (V_{out}). Para hacer el modelo más preciso se ha de incluir en los cálculos pérdidas adicionales. Como conclusión, los resultados obtenidos prueban que el modelo matemático propuesto se puede usar para diseñar rápida y fácilmente rectificadores a partir de las especificaciones dadas por el proceso tecnológico y los requisitos de consumo de los circuitos de alimentación.

2.4.2 Medidas: Sensor de tensión

Se han implementado, fabricado y medido dos versiones de los sensores de tensión propuestos en esta Tesis Doctoral, VL y CC con diferentes tensiones umbrales (ES_{th}). La Tabla 2.11 muestra los resultados medidos. La corriente DC a 3.3 V del VL y del CC están por debajo de 70 nA y de 1 nA, respectivamente. El pico de corriente en el momento de la conmutación está por debajo de los 2 μA en ambos casos. ES_{th} es 0.5 V menor que los resultados simulados debido a la dispersión de la tecnología.

2.4.3 Medidas: Limitador de tensión

Se han implementado, fabricado y medido dos limitadores, el limitador descrito en la bibliografía y el nuevo circuito propuesto en esta Tesis Doctoral. La respuesta transitoria de los dos circuitos a la misma señal de entrada se muestra en la Figura 2.32. El limitador de la bibliografía requiere alrededor de 70 μs para conmutar, mientras que el tiempo requerido por el limitador propuesto en esta Tesis Doctoral es de 5 μs. Por lo tanto las modificaciones propuestas reduce un 92.9% el tiempo de respuesta del limitador.

La Figura 2.32 muestra la característica I–V de ambos circuitos. La región de degración es de 200 mV en el circuito de la bibliografía y de unos 120 mV en el circuito propuesto, esto supone una mejora del 40%. Además como se aprecia en la Figura 2.33 el circuito propuesto copia casi perfectamente la característica I–V ideal del limitador mientras que el circuito propuesto en la bibliografía se aleja bastante del caso ideal.

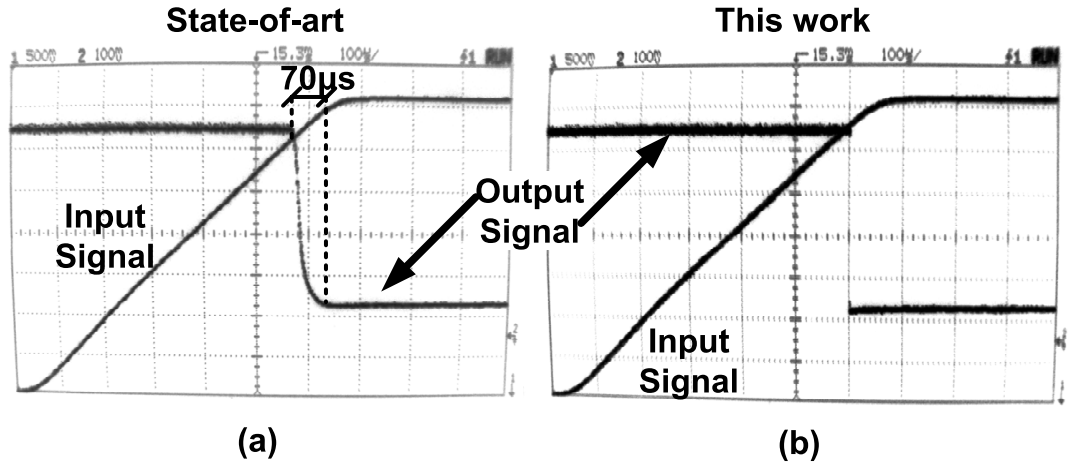

Figura 2.32: Respuesta transitoria de los limitadores de tensión: (a) circuito de la bibliografía [6], y (b) circuito propuesto en esta Tesis Doctoral.

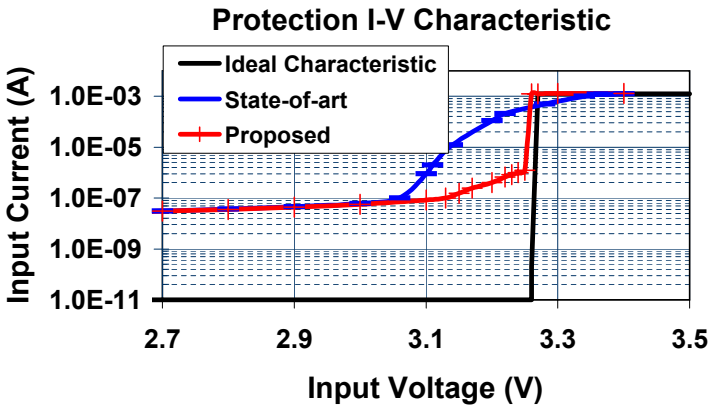

Figura 2.33: Característica I–V ideal frente a la medida en los limitadores fabricados.

Tabla 2.12: Medidas de los parámetros de los reguladores de tensión propuestos

Regulador	Analógico (V_{aa}=1.2V)	EEPROM (V_{dd}=1.8V)
V_{out} (V)	1.73	2.25
ΔV_{out} (mV)	537.5	212.5
$I_{Consumo}$ (nA)	90	240
PSRR@ 1kHz (dB)	-28.9	-30
Drop-out (mV)	50	10
Settling time (us)	5	5

2.4.4 Medidas: Regulador de tensión

Dos reguladores de Tensión fueron implementados, fabricados y medidos. La Figura 2.34 muestra la tensión de salida de los reguladores en función de la tensión de salida el rectificador, medida en tres chips diferentes. La variación debido a la dispersión del proceso es de unos 60 mV.

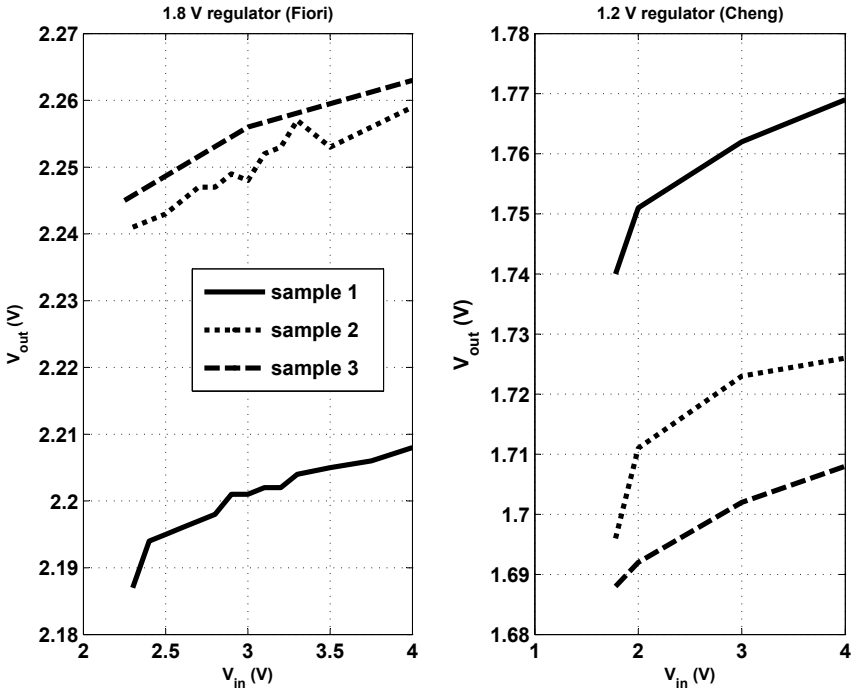

Figura 2.34: Tensión de salida de los reguladores medidos.

La Tabla 2.12 resume las medidas de los reguladores fabricados. El consumo de corriente de los dos reguladores incluye la referencia de tensión. Los resultados están dentro de las predicciones realizadas en simulación. Nótese que la tensión de drop-out medida es de 50 mV para el regulador de V_{aa} y de 10 mV para V_{dd}. Esto valores se encuentran dentro de las especificaciones de diseño.

La Tabla 2.13 compara reguladores de tensión para aplicaciones RFID encontrados

Tabla 2.13: Comparación de reguladores de tensión de ultra–bajo consumo

Diseño	Barnett [53]	Vita [54]	Esta Tesis
Proceso	0.15 μm CMOS	0.35 μm CMOS	0.35 μm CMOS
$I_{Consumo}$ (nA)	110	34	240
Drop-out (mV)	-	30	10 & 50
Settling time (ms)	-	1.5	0.005
V_{out} (V)	1.25	0.605	2.2 & 1.2
Máxima corriente de carga (μA)	-	5	$>$1000
Line Sensitivity (mV/V)	-	$+$/-0.8	4
TK(mV/$\circ$C)	-	2	1.5 & 1.1
ΔV_{out} (V)	0.1	-	0.1

en la bibliografía con los propuestos en esta Tesis Doctoral. La corriente consumida por Barnett [53], que usa una tecnología CMOS de 0.13μm. Vita [54], que trabaja en CMOS 0.35μm presenta un consumo estático de 34 nA, sin embargo el consumo de la referencia de tensión no está incluido. Los reguladores propuesto en esta Tesis Doctoral son mejores que los de Vita en términos de tiempo de respuesta (*settling time*) y máxima corriente de salida. En el resto de parámetros todos los circuitos se mueven en el mismo rango de valores. Para concluir, remarcar que el efecto de los picos de corriente debido a la circuitería digital en la tensión regulada de salida no fue tratada por el resto de autores. En este trabajo, los picos de corriente fueron un parámetro de diseño clave puesto que su efecto es crítico en la alimentación del sensor. Como consecuencia, la consideración de los picos de corriente en sensores RFID añade un grado de dificultad en el diseño de los circuitos propuesto que no fue considerado por el resto de autores.

2.4.5 Medidas: Sistema de recuperación de energía

El sistema de recuperación de energía para el sensor RFID fue implementado, fabricado y medido dentro del *Front–End* analógico. La Figura 2.35 muestra las medidas del limitador y del regulador de tensión como función de la tensión en el condensador de alimentación. La línea azul es la tensión de alimentación a la salida del regulador, una vez que la tensión en el condensador supera V_{aa} o V_{dd} más la tensión de drop-out comienza la regulación. La línea verde ilustra el consumo de corriente del regulador y del limitador. Antes de que el umbral de protección sea alcanzado el consumo de corriente es solo debido al regulador, por debajo de 400 nA. Cuando se alcanza el umbral del limitador el consumo de corriente se dispara por encima de 1 mA. Esta corriente es la llamada corriente de protección que el limitador conmuta a tierra.

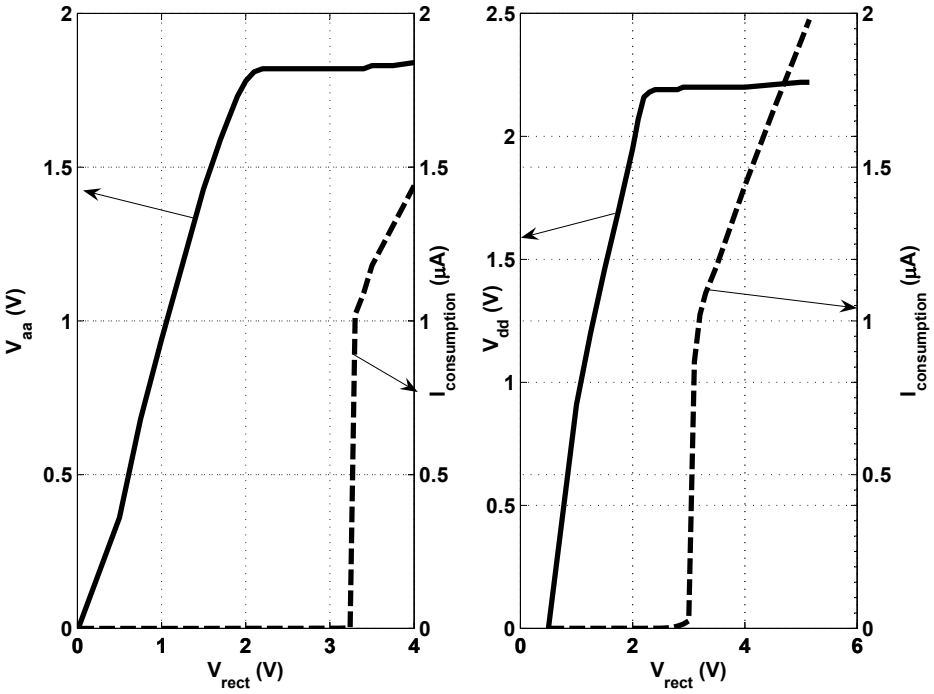

Figura 2.35: Medidas del limitador junto a los reguladores de tesnión en el *Front–End* analógico.

Capítulo 3

Aportaciones científicas de esta tesis doctoral

Índice General

3.1 Aportaciones científicas publicadas 201

3.2 Aportaciones científicas no publicadas 202

Resumen: En este capítulo se enumeran las diversas aportaciones científicas propuesta en esta Tesis Doctoral, algunas de ellas han sido publicada y otras aún no.

3.1 Aportaciones científicas publicadas

A continuación se presenta una lista de los diferentes artículos publicados durante la realización de esta Tesis Doctoral.

Ultra–Low Power Passive UHF RFID for Wireless Sensor Networks. - En este artículo se presenta el sistema de recuperación de energía del sensor RFID. Concretamente se describe el diseño del Sensor de Tensión y del Limitador de Tensión así como su implementación en la tecnología CMOS de 0.35μm y bajo consumo de XFAB y las medidas realizadas y la comparativa con circuitos de la Bibliografía. Además de esto se presenta un el diseño, implementación y medias de un regulador de tensión de muy bajo diseñado para sensores RFID pasivos.

Voltage Protection Circuit for the Supply Capacitor in UHF RFID Sensors. - Este artículo presenta circuitos de protección contra tensiones excesivas de muy bajo consumo para optimizar el consumo de potencia en sensores UHF RFID pasivos. Se analiza el estado del arte y se compara con el circuito propuesto usando un proceso de 0.35μm 2P4M CMOS. El consumo de corriente del circuito te protección de tensión es menor de 60 nA a 3 V y su región de degradación es 0.12 V.

Optimal Impedance Matching in Passive UHF RFID Sensors. - Este artículo propone un método para realizar una adaptación óptima de impedancia entre la antena y un sensor inalámbrico pasivo que utiliza tecnología RFID en la banda de UHF (de 300 MHz a 3 GHz). En sistemas UHF–RFID el circuito denominado Multiplicador de Tensión (MT) es el encargado realizar la conversión de energía RF procedente del dispositivo interrogador a energía DC requerida para alimentar el resto de circuitos del sensor.

El MT es el circuito que determina la impedancia de entrada el sensor RFID, este circuito es estudiado para diferentes condiciones de carga y para diferentes potencias de entrada. Este estudio concluye con un algoritmo diseñado para obtener la impedancia de entrada óptima a la que un determinado MT ha de ser adaptado con el fin de obtener el máximo alcance en la comunicación interrogador–sensor.

Design Criteria for Full Passive Long Range UHF RFID Sensor for Human Body Temperature Monitoring. - Los objetivos de este artículo son: primero, discutir las limitaciones reales de los sistemas RFID pasivos en la banda de UHF y segundo, proporcionar criterios de diseño para optimizar los diferentes bloques para conseguir el mayor alcance. El diseño se ha enfocado a la red de adaptación, el multiplicador de tensión, el demodulador, el modulador y el sensor. Los resultados numéricos se han obtenido usando una tecnología de 0.35μm que incluye diodos Schottky y operando a la frecuencia de 868 MHz.

Adjustable Voltage Sensors for Power Supply Chains in Passive UHF RFID Transponders. - En transponders UHF RFID pasivos, la energía para alimentar los subsistemas del transponder se almacena en un condensador de alimentación. Es conveniente que este condensador se cargue rápidamente y a una tensión apropiada, de ahí la necesidad de un sensor de tensión. Este artículo presenta dos sensores de tensión ajustables con un consumo de potencia muy bajo. Los circuitos propuestos miden la carga almacenada en el condensador de alimentación y activan el resto de sistemas cuando hay carga suficiente. En comparación con los circuitos previamente publicados, el consumo medio corriente de los circuitos propuestos es un orden de magnitud menor. Los circuitos consumen menos de 100 nA@3.3 V.

Voltage Sensors for Supply Capacitor in Passive UHF RFID Transponders. - Este artículo presenta sensores de tensión de muy bajo consumo para el condensador de alimentación en transponders UHF RFID pasivos. Los circuitos propuestos son elementos clave en sensores inalámbricos sin baterías, es decir que se alimentan de la señal de RF transmitida por un sistema interrogador. El sensor de tensión observa la carga del condensador de tensión y activa el resto de circuitos cuando se alcanza un umbral de carga que garantice una correcta alimentación del transponder. En este trabajo se han comparado diferentes circuitos del estado del arte utilizando una misma tecnología (2P3M 0.35μm), además se incluyen dos nuevos circuitos que reducen el consumo de corriente.

3.2 Aportaciones científicas no publicadas

A continuación se presentan las aportaciones científicas propuestas en este trabajo de Tesis Doctoral que aún no han sido publicadas:

- Reglas de diseño para Rectificadores maximizando la eficiencia en la conversión de potencia AC en RF.
- Modelo matemático del Rectificador basado en expresiones teóricas para definir la Impedancia de Entrada así como la amplitud de la señal de entrada en función de

los requisitos de potencia y el proceso tecnológico, para automatizar el diseño de rectificadores.

- Reglas de diseño para los reguladores LDO de ultra bajo consumo para generar una tensión de alimentación bien especificada y estable, considerando los requisitos de alimentación propios de sistemas RFID pasivos.

Capítulo 4

Conclusiones y líneas futuras

Índice General

4.1 Conclusiones 205

4.2 Líneas Futuras 207

El proyecto WISEN ha analizado las restricciones y los límites físicos de integrar sensores con un transceptor completamente pasivo. El transceptor está basado en los sistemas RFID pasivos de largo alcance, y éste no es sólo responsable de las comunicaciones con el dispositivo lector sino también de recuperar la energía y de generar la tensión de alimentación del sensor RFID. En el marco de este proyecto fueron estudiadas infinidad de áreas como resultado se han publicado numerosos artículos científicos [132, 133, 130], Tesis Doctorales [134, 135, 136] y patentes de invención [137, 138].

4.1 Conclusiones

En el caso particular de esta Tesis Docotoral las conclusiones más destacadas se resumen a countinuación.

Diseño del sistema de recuperación de energía. - Se han deducido un conjunto de restricciones y especificaciones para el diseño del sistema de recuperación de energía gracias aun meticuloso análisis. Estas restricciones y especificaciones atañen al Factor de Calidad(Q), selección del tipo de modulaci'on Backscatter, selección de la tecnología y definición de las especificaciones de diseño de cada uno de los elementos circuitales que componen el sistema (Rectificador, Sensor de tensión, Limitador y Regulador de Tensión). El análisis de la impedancia de entrada en función de la potencia consumida fue publicado en el una conferencia Internacional dedicada a tecnologías RFID [107].

Rectificador. - A partir de un detallado análisis del estado del arte se deduce que la topología de Dickson con diodos Schottky es la más óptima para implementar el conversor de energía AC en DC del sensor RFID. También se ha propuesto un metodología de diseño para maximizar la eficiencia en la conversión de potencia.

Por otro lado, en esta Tesis doctoral se propone un modelo matemático para caracterizar la operación del rectificador en términos de impedancia de entrada y de tensión de salida y como función de los requisitos de potencia y tecnología. Resultados obtenidos a partir del modelo matemático se han comparado con resultados simulados a nivel de

esquemático y layout y con medidas *on–chip* para probar el modelo, el resultado de estas comparaciones prueban la efectividad del modelo matemático propuesto.

Rectificadores de 4, 6 y 8 etapas fueron implementados, fabricados y medidos siguiendo las reglas de diseño propuestas. Los resultados obtenidos están de acuerdo con las predicciones teóricas.

Sensor de tensión y limitador. - Se han propuesto dos nuevos sensores de tensión. Estos circuitos se han implementado, fabricado y medido y se han comparado con circuitos del estado del arte, la Figura 4.1 muestra una foto de los sensores de tensión. El consumo estático de corriente de las nuevas estructuras asciende a 69 nA y 0.2 nA a 3.3 V, esto implica una mejora en el estado del arte de un orden de magnitud. Los circuitos propuestos así como la comparación con la bibliografía fue publicada en conferencias internacionales [139, 140].

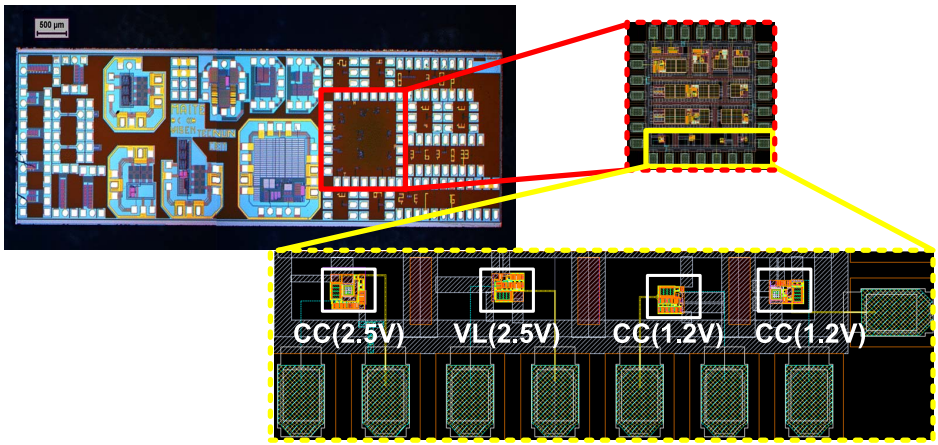

Figura 4.1: Micro–fotografía del chip para test y detalles de los sensores de tensión.

Respecto al limitador de tensión se proponen modificaciones sobre el estado del arte, estos circuitos modificados fueron implementados, fabricados y medidos. Resultados experimentales prueban que las modificaciones propuestas mejoran un orden de magnitud el comportamiento del circuito en términos de consumo de corriente antes alcanzar el umbral de protección. Este análisis fue publicado en una conferencia internacional [141].

Regulador de tensión. - Se ha probado que el regulador de bajo drop-out es la arquitectura más óptima para la aplicación y se han definido un conjunto de reglas de diseño para implementar reguladores LDO para sistemas RFID pasivos.

Se han diseñado, simulado, implementado, fabricado y medido reguladores. Los resultados experimentales de los reguladores implementados en esta Tesis Doctoral se han comparado con la bibliografía, demostrándose mejoras en términos de estabilidad y consumo de corriente. Parte de los resultados de esta investigación fueron publicados en una conferencia internacional [142].

Finalmente, dos reguladores de tensión (1.2 V y 1.8 V) han sido integrados en el *Front–end* analógico de un sensor RFID pasivo. Lo resultados experimentales prueban el correcto funcionamiento del regulador y del resto de circuitos del sistema de recuperación de energía. El diseño de *Front–end* analógico ha sido publicado en una conferencia internacional del IEEE sobre sistemas RFID.

4.2 Líneas Futuras

Los parámetros que más interesa mejorar en el sistema de recuperación y estabilización de energía en sensores RFID son el rango de operación y la cantidad de potencia disponible a la salida. Para ello esta investigación puede continuar en los siguientes líneas:

- Mejorar la eficiencia en la conversión de potencia de alterna en continua. Esto es mejorar el Rectificador de Dickson. Las mejoras del rectificador se pueden llevar a cabo en dos direcciones:

    1. Mejorar el proceso tecnológico para conseguir diodos Schottky con menor capacidad parásita (C_D) y menor resistencia en directa (R_f) conservando una alta resistencia en corte. Mejorar el proceso para obtener condensadores con menores capacidades y resistencias parásitas.
    2. Trabajar en mejorar la arquitectura, es decir, desarrollar nuevos circuitos con mayor eficiencia en la conversión de energía.

- Reducir el consumo del chip. Trabajar en esta línea implicaría utilizar un proceso más moderno o más costoso, que permita una menor tensión de alimentación y que permita diseñar circuitos de menos consumo. Una opción sería utilizar un proceso de silicio sobre aislante (SOI), que reduce las pérdidas parásitas optimizando así la energía generada en el sistema de recuperación de energía.

- Otra línea para incrementar el rango de operación de los sensores RFID sería incluir una fuente de alimentación suplementaria en forma de batería. Esta fuente de tensión se podría utilizar para polarizar los conmutadores en el rectificador o para dar alimentación independiente a determinados bloques del sistema como por ejemplo el sensor. Dejando el resto del transponder RFID que sea alimentado por la energía de RF.

- Un elemento interesante que convendría incluir en el sensor RFID sería un conversor analógico digital de ultra bajo consumo. Una forma interesante de hacer la plataforma compatible con diversos tipos de sensores sería dotándola de un ADC con moderado grado de resolución y con muy bajo consumo, pues no todos los sensores son capaces de generar una salida digital compresible por la lógica.

- Como última línea de investigación futura se propone el análisis y la mejora del estado del are relativo a referencias de tensión de ultra bajo consumo. En el estudio

realizado en esta Tesis Doctoral se ha concluido que la referencia Bandgap es la mejor opción en términos de estabilidad, sin embargo su consumo no es el más óptimo.

Bibliography

[1] U. Karthaus and M. Fischer, "Fully integrated passive uhf rfid transponder ic with 16.7-μw minimum rf input power," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 1602–1608, Oct. 2003.

[2] D. Estreich, "A simulation model for schottky diodes in gaas integrated circuits," *Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on*, vol. 2, pp. 106–111, April 1983.

[3] F. Kocer, P. Walsh, and M. Flynn, "An injection locked, rf powered, telemetry ic in 0.25 μm cmos," *VLSI Circuits, 2004. Digest of Technical Papers. 2004 Symposium on*, pp. 24–27, June 2004.

[4] F. Kocer and M. Flynn, "A new transponder architecture with on-chip adc for long-range telemetry applications," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 1142–1148, May 2006.

[5] J.-P. Curty, N. Joehl, C. Dehollain, and M. Declercq, "Remotely powered addressable uhf rfid integrated system," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 2193–2202, Nov. 2005.

[6] U. Kaiser and W. Steinhagen, "A low-power transponder ic for high-performance identification systems," *Solid-State Circuits, IEEE Journal of*, vol. 30, pp. 306–310, Mar 1995.

[7] J. van der Meer, F. Riedijk, E. van Kampen, K. Makinwa, and J. Huijsing, "A fully integrated cmos hall sensor with a 3.65 μt 3σ offset for compass applications," *Solid-State Circuits Conference, 2005. Digest of Technical Papers. ISSCC. 2005 IEEE International*, pp. 246–247 Vol. 1, Feb. 2005.

[8] A. Wheeler, "Commercial applications of wireless sensor networks using zigbee," *Communications Magazine, IEEE*, vol. 45, pp. 70–77, April 2007.

[9] L. Au, W. Wu, M. Batalin, D. McIntire, and W. Kaiser, "Microleap: Energy-aware wireless sensor platform for biomedical sensing applications," *Biomedical Circuits and Systems Conference, 2007. BIOCAS 2007. IEEE*, pp. 158–162, Nov. 2007.

[10] A.-S. Porret, T. Melly, D. Python, C. Enz, and E. Vittoz, "An ultralow-power uhf transceiver integrated in a standard digital cmos process: architecture and receiver," *Solid-State Circuits, IEEE Journal of*, vol. 36, pp. 452–466, Mar 2001.

[11] D. C. Daly and A. P. Chandrakasan, "An energy-efficient ook transceiver for wireless sensor networks," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 1003–1011, May 2007.

[12] A. Molnar, B. Lu, S. Lanzisera, B. Cook, and K. Pister, "An ultra-low power 900 mhz rf transceiver for wireless sensor networks," *Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004*, pp. 401–404, Oct. 2004.

[13] M. Scott, B. Boser, and K. Pister, "An ultralow-energy adc for smart dust," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 1123–1129, July 2003.

[14] B. Warneke and K. Pister, "An ultra-low energy microcontroller for smart dust wireless sensor networks," *Solid-State Circuits Conference, 2004. Digest of Technical Papers. ISSCC. 2004 IEEE International*, pp. 316–317 Vol.1, Feb. 2004.

[15] M. Philipose, J. Smith, B. Jiang, A. Mamishev, S. Roy, and K. Sundara-Rajan, "Battery-free wireless identification and sensing," *Pervasive Computing, IEEE*, vol. 4, pp. 37–45, Jan.-March 2005.

[16] K. Finkenzeller, *RFID Handbook : Fundamentals and Applications in Contactless Smart Cards and Identification*. John Wiley & Sons, 2nd ed., May 2003. Available on–line:
http://www.amazon.ca/exec/obidos/redirect?tag=citeulike09-20&path=ASIN/0470844027.

[17] K. Stangel, S. Kolnsberg, D. Hammerschmidt, B. Hosticka, H. Trieu, and W. Mokwa, "A programmable intraocular cmos pressure sensor system implant," *Solid-State Circuits, IEEE Journal of*, vol. 36, pp. 1094–1100, Jul 2001.

[18] Q. Huang and M. Oberle, "A 0.5-mw passive telemetry ic for biomedical applications," *Solid-State Circuits, IEEE Journal of*, vol. 33, pp. 937–946, Jul 1998.

[19] O. Chevalerias, T. O'Donnell, D. Power, N. O'Donovan, G. Duffy, G. Grant, and S. O'Mathuna, "Inductive telemetry of multiple sensor modules," *Pervasive Computing, IEEE*, vol. 4, pp. 46–52, Jan.-March 2005.

[20] M. Suster, W. Ko, and D. Young, "An optically powered wireless telemetry module for high-temperature mems sensing and communication," *Microelectromechanical Systems, Journal of*, vol. 13, pp. 536–541, June 2004.

[21] B. Warneke, M. Scott, B. Leibowitz, L. Zhou, C. Bellew, J. Chediak, J. Kahn, B. Boser, and K. Pister, "An autonomous 16 mm3 solar-powered node for distributed wireless sensor networks," *Sensors, 2002. Proceedings of IEEE*, vol. 2, pp. 1510–1515 vol.2, 2002.

[22] A. Graafstra, "Hands on," *Spectrum, IEEE*, vol. 44, pp. 18–23, March 2007.

[23] "Iso 10536: Identification cards contactless integrated circuit(s) cards. contactless smart cards in close coupling technology.." Available on–line:
http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=26737.

[24] "Iso 14443: Identification cards – contactless integrated circuit cards – proximity cards.." Available on–line:
http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=39693.

[25] "Iso 15693: Identification cards – contactless integrated circuit cards – vicinity cards." Available on–line: http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=39695.

[26] A. Polh, "A review of wireless saw sensors," *Ultrasonics, Ferroelectrics and Frequency Control, IEEE Transactions on*, vol. 47, pp. 317–332, Mar 2000.

[27] "European telecommunications standards institute (etsi)." Available on–line: http://www.etsi.org/WebSite/homepage.aspx.

[28] "International telecommunication union - radiocommunication sector (itu-r)." Available on–line: http://www.itu.int/ITU-R/index.asp?category=information&rlink=rhome&lang=en.

[29] K. Rao, P. Nikitin, and S. Lam, "Antenna design for uhf rfid tags: a review and a practical application," *Antennas and Propagation, IEEE Transactions on*, vol. 53, pp. 3870–3876, Dec. 2005.

[30] "Iso 18000: Rfid for item management: Air interface." Available on–line: http://www.iso.org/iso/iso_catalogue/catalogue_tc/catalogue_detail.htm?csnumber=46145.

[31] "Epc tag data standards version 1.1 rev. 1.27." Available on–line: http://www.epcglobalinc.org/standards_technology/specifications.html.

[32] "Atmel rfid-tags product catalog." Available on–line: http://www.atmel.com/dyn/resources/prod_documents/doc4602.pdf.

[33] "Nxp rfid-tags product catalog." Available on–line: http://www.nxp.com/acrobat_download/literature/9397/75016165.pdf.

[34] "Texas intruments rfid-tags product catalog." Available on–line: http://focus.ti.com/paramsearch/docs/parametricsearch.tsp?family=rfid&sectionId=475&tabId=2101&familyId=1351&paramCriteria=no.

[35] "St microelectronics rfid-tags product catalog." Available on–line: http://www.st.com/stonline/products/promlit/pdf/flxrag20206.pdf.

[36] "Epcglobal leads the development of industry-driven standards for the electronic product code (epc) to support the use of radio frequency identification (rfid) in todays fast-moving, information rich, trading networks.." Available on–line: http://www.epcglobalinc.org/home.

[37] "Gs1 is a leading global organisation dedicated to the design and implementation of global standards and solutions to improve the efficiency and visibility of supply and demand chains globally and across sectors.." Available on–line: http://www.gs1.org/.

[38] "860MHz-930MHz Class I Radio Frequency Identification Tag Radio Frequency & Logical Communication Interface Specification." Available on–line: http://www.epcglobalinc.org/standards/specs/860MHz_930_MHz_Class_1_RFID_Tag_Radio_Frequency_Logical_Communication_Interface_Specification.pdf.

[39] "Draft protocol specification for a 900 mhz class 0 radio frequency identification tag." Available on–line: http://www.epcglobalinc.org/standards/specs/900_MHz_Class_0_RFIDTag_Specification.pdf.

[40] J. Haartsen, "The bluetooth radio system," *Personal Communications, IEEE [see also IEEE Wireless Communications]*, vol. 7, pp. 28–36, Feb 2000.

[41] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-mhz rectifier circuit for sensor network tags with 10-m distance," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 35–41, Jan. 2006.

[42] V. Pillai, H. Heinrich, D. Dieska, P. Nikitin, R. Martinez, and K. Rao, "An ultra-low-power long range battery/passive rfid tag for uhf and microwave bands with a current consumption of 700 na at 1.5 v," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, pp. 1500–1512, July 2007.

[43] H. Kitayoshi and K. Sawaya, "Long range passive rfid-tag for sensor networks," *Vehicular Technology Conference, 2005. VTC-2005-Fall. 2005 IEEE 62nd*, vol. 4, pp. 2696–2700, Sept., 2005.

[44] "International telecommunication union – radiocommunication sector (itu–r): Frequently asked questions."

[45] "Uhf rfid tag from atmel (ata5590)." Available on–line: http://www.atmel.com/dyn/resources/press/newuhfdevice_ata5590.html.

[46] H. Friis, "A note on a simple transmission formula," *Proceedings of the IRE*, vol. 34, pp. 254–256, May 1946.

[47] J. Dickson, "On-chip high-voltage generation in mnos integrated circuits using an improved voltage multiplier technique," *Solid-State Circuits, IEEE Journal of*, vol. 11, pp. 374–378, Jun 1976.

[48] H. Nakamoto, D. Yamazaki, T. Yamamoto, H. Kurata, S. Yamada, K. Mukaida, T. Ninomiya, T. Ohkawa, S. Masui, and K. Gotoh, "A passive uhf rf identification cmos tag ic using ferroelectric ram in 0.35-m technology," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 101–110, Jan. 2007.

[49] S. Mandal and R. Sarpeshkar, "Low-power cmos rectifier design for rfid applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, pp. 1177–1188, June 2007.

[50] E. Bergeret, J. Gaubert, P. Pannier, and P. Rizzo, "Power generation system for uhf passive rfid," *Electronics Letters*, vol. 42, pp. 1452–1454, 7 2006.

[51] J. Yi, W.-H. Ki, and C.-Y. Tsui, "Analysis and design strategy of uhf micro-power cmos rectifiers for micro-sensor and rfid applications," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 54, pp. 153–166, Jan. 2007.

[52] S. Chatzandroulis, D. Tsoukalas, and P. Neukomm, "A miniature pressure system with a capacitive sensor and a passive telemetry link for use in implantable applications," *Microelectromechanical Systems, Journal of*, vol. 9, pp. 18–23, Mar 2000.

[53] G. Balachandran and R. Barnett, "A 110 na voltage regulator system with dynamic bandwidth boosting for rfid systems," *Solid-State Circuits, IEEE Journal of*, vol. 41, pp. 2019–2028, Sept. 2006.

[54] G. De Vita and G. Iannaccone, "Ultra-low-power series voltage regulator for passive rfid transponders with subthreshold logic," *Electronics Letters*, vol. 42, pp. 1350–1351, 9 2006.

[55] A. Bakker and J. Huijsing, "Micropower cmos temperature sensor with digital output," *Solid-State Circuits, IEEE Journal of*, vol. 31, pp. 933–937, Jul 1996.

[56] P. Catrysse, B. Wandell, and A. El Gamal, "An integrated color pixel in 0.18μm cmos technology," *Electron Devices Meeting, 2001. IEDM Technical Digest. International*, pp. 24.4.1–24.4.4, 2001.

[57] S.-M. Jung, J.-M. Nam, D.-H. Yang, and M.-K. Lee, "A cmos integrated capacitive fingerprint sensor with 32-bit risc microcontroller," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 1745–1750, Aug. 2005.

[58] O. Schrey, J. Huppertz, G. Filimonovic, A. Bussmann, W. Brockherde, and B. Hosticka, "A 1 k1 k high dynamic range cmos image sensor with on-chip programmable region-of-interest readout," *Solid-State Circuits, IEEE Journal of*, vol. 37, pp. 911–915, Jul 2002.

[59] W.-J. Liu, O.-C. Chen, L.-K. Dai, P.-K. Keng, K.-H. Huang, and F.-W. Jih, "A color image sensor using adaptive color pixels," *Circuits and Systems, 2002. MWSCAS-2002. The 2002 45th Midwest Symposium on*, vol. 2, pp. II–441–II–444 vol.2, Aug. 2002.

[60] A. Bakker, "Cmos smart temperature sensors - an overview," *Sensors, 2002. Proceedings of IEEE*, vol. 2, pp. 1423–1427 vol.2, 2002.

[61] A. Brokaw, "A simple three-terminal ic bandgap reference," *Solid-State Circuits, IEEE Journal of*, vol. 9, pp. 388–393, Dec 1974.

[62] P. Chen, C.-C. Chen, C.-C. Tsai, and W.-F. Lu, "A time-to-digital-converter-based cmos smart temperature sensor," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 1642–1648, Aug. 2005.

[63] M. Tuthill, "A switched-current, switched-capacitor temperature sensor in 0.6-μm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 33, pp. 1117–1122, Jul 1998.

[64] R. Popovic, Z. Randjelovic, and M. D., "Integrated hall-effect magnetic sensors," *Sensors and actuators A: Physical*, vol. 91, pp. 46–50, Jun 2001.

[65] A. Bilotti, G. Monreal, and R. Vig, "Monolithic magnetic hall sensor using dynamic quadrature offset cancellation," *Solid-State Circuits, IEEE Journal of*, vol. 32, pp. 829–836, Jun 1997.

[66] M. Pastre, M. Kayal, and H. Blanchard, "A hall sensor analog front end for current measurement with continuous gain calibration," *Sensors Journal, IEEE*, vol. 7, pp. 860–867, May 2007.

[67] C. Inglis, L. Manchanda, R. Comizzoll, A. Dickinson, E. Martin, S. Mandis, P. Silveman, G. Weber, B. Ackland, and L. O'Gorman, "A robust, 1.8 v 250 μw direct-contact 500 dpi fingerprint sensor," *Solid-State Circuits Conference, 1998. Digest of Technical Papers. 1998 IEEE International*, pp. 284–285, Feb 1998.

[68] S.-M. Jung, J.-M. Nam, D.-H. Yang, and M.-K. Lee, "A cmos integrated capacitive fingerprint sensor with 32-bit risc microcontroller," *Solid-State Circuits, IEEE Journal of*, vol. 40, pp. 1745–1750, Aug. 2005.

[69] R. Hashido, A. Suzuki, A. Iwata, T. Okamoto, Y. Satoh, and M. Inoue, "A capacitive fingerprint sensor chip using low-temperature poly-si tfts on a glass substrate and a novel and unique sensing method," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 274–280, Feb 2003.

[70] M. Tartagni and R. Guerrieri, "A 390 dpi live fingerprint imager based on feedback capacitive sensing scheme," *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International*, pp. 200–201, 456, Feb 1997.

[71] S. Decker, D. McGrath, K. Brehmer, and C. Sodini, "A 256256 cmos imaging array with wide dynamic range pixels and column-parallel digital output," *Solid-State Circuits, IEEE Journal of*, vol. 33, pp. 2081–2091, Dec 1998.

[72] O. Schrey, J. Huppertz, G. Filimonovic, A. Bussmann, W. Brockherde, and B. Hosticka, "A 1 k1 k high dynamic range cmos image sensor with on-chip programmable region-of-interest readout," *Solid-State Circuits, IEEE Journal of*, vol. 37, pp. 911–915, Jul 2002.

[73] D. Stoppa, M. Vatteroni, D. Covi, A. Baschirotto, A. Sartori, and A. Simoni, "A 120-db dynamic range cmos image sensor with programmable power responsivity," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 1555–1563, July 2007.

[74] X. Wang, W. Wong, and R. Hornsey, "A high dynamic range cmos image sensor with inpixel light-to-frequency conversion," *Electron Devices, IEEE Transactions on*, vol. 53, pp. 2988–2992, Dec. 2006.

[75] P. Pieters, "Integrating mems with standard cmos using low temperature poly-sige technology," in *11th Annual International KGD Packaging and Test Workshop*, (Napa, CA), September 2004.

[76] "X-fab silicon foundries- mems technologies." Available on–line: http://www.xfab.com/xfab/frontend/index.php?st_id=2&itid=249.

[77] H. Takao, H. Fukumoto, and M. Ishida, "A cmos integrated three-axis accelerometer fabricated with commercial submicrometer cmos technology and bulk-micromachining," *Electron Devices, IEEE Transactions on*, vol. 48, pp. 1961–1968, Sep 2001.

[78] "Bosch–bma145: Analog, triaxial accelerometer sensor." Available on–line: http://www.bosch-sensortec.com/content/language4/downloads/BMA145_Flyer_Rev.1.0_March2008.pdf.

[79] "Analog devices–adxl323: Small, low power, 2-axis 3g mems accelerometer." Available on–line:
http://www.analog.com/en/mems-and-sensors/imems-accelerometers/adxl323/products/product.html.

[80] "St microelectronics–mems motion sensor 2-axis - 2g/8g smart digital output piccolo accelerometer." Available on–line:
http://www.st.com/stonline/products/literature/ds/13624.pdf.

[81] A. Sharma, M. Zaman, and F. Ayazi, "A 104-db dynamic range transimpedance-based cmos asic for tuning fork microgyroscopes," *Solid-State Circuits, IEEE Journal of*, vol. 42, pp. 1790–1802, Aug. 2007.

[82] A. Sadat, H. Qu, C. Yu, J. Yuan, and H. Xie, "Low-power cmos wireless mems motion sensor for physiological activity monitoring," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, pp. 2539–2551, Dec. 2005.

[83] "Analog devices–adxrs610: 300 deg/sec angular rate sensor." Available on–line:
http://www.analog.com/en/mems-and-sensors/imems-gyroscopes/ADXRS610/products/product.html.

[84] J. Ji, S. Cho, Y. Zhang, K. Najafi, and K. Wise, "An ultraminiature cmos pressure sensor for a multiplexed cardiovascular catheter," *Electron Devices, IEEE Transactions on*, vol. 39, pp. 2260–2267, Oct 1992.

[85] M. Ylimaula, M. Aberg, J. Kiihamaki, and H. Ronkainen, "Monolithic soi-mems capacitive pressure sensor with standard bulk cmos readout circuit," *Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European*, pp. 611–614, Sept. 2003.

[86] M. Scott, B. Boser, and K. Pister, "An ultralow-energy adc for smart dust," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 1123–1129, July 2003.

[87] K. Y. Leung, K. Leung, and D. R. Holberg, "A dual low power $\frac{1}{2}$ lsb nl 16b/1msample/s sar a/d converter with on-chip microcontroller," *Solid-State Circuits Conference, 2006. ASSCC 2006. IEEE Asian*, pp. 51–54, Nov. 2006.

[88] A. Arbat, A. Dieguez, and J. Samitier, "An ultra low power successive approximation adc with selectable resolution in 0.13 m cmos technology," *Electronics, Circuits and Systems, 2006. ICECS '06. 13th IEEE International Conference on*, pp. 415–418, Dec. 2006.

[89] S. Mortezapour and E. Lee, "A 1-v, 8-bit successive approximation adc in standard cmos process," *Solid-State Circuits, IEEE Journal of*, vol. 35, pp. 642–646, Apr 2000.

[90] V. Peluso, P. Vancorenland, A. Marques, M. Steyaert, and W. Sansen, "A 900-mv low-power $\delta\sigma$ a/d converter with 77-db dynamic range," *Solid-State Circuits, IEEE Journal of*, vol. 33, pp. 1887–1897, Dec 1998.

[91] Ceit, "Wissen-project i need a link or a reference to this project," May 2006.

[92] K. Kurokawa, "Power waves and the scattering matrix," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 13, pp. 194–202, Mar 1965.

[93] T. H. Lee, *The Design of CMOS Radio-Frequency Integrated Circuits*. Cambridge University Press, 2nd ed., March 2004. Available on–line: http://www.cambridge.org/uk/catalogue/catalogue.asp?isbn=0521835399.

[94] M. Morn-Araya, *Teora de Circuitos, Tomo I*. Universidad de Las Palmas de Gran Canaria, 1st ed., 2000.

[95] B. Razavi, *Design of Analog CMOS Integrated Circuits*. New York, USA: Mc Graw–Hill Book Co, 2nd ed., August 2000. Available on–line: http://www.amazon.com/Design-Analog-CMOS-Integrated-Circuits/dp/0072380322.

[96] G. De Vita and G. Iannaccone, "Design criteria for the rf section of uhf and microwave passive rfid transponders," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, pp. 2978–2990, Sept. 2005.

[97] J.-P. Curty, N. Joehl, F. Krummenacher, C. Dehollain, and M. Declercq, "A model for μ-power rectifier analysis and design," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 52, pp. 2771–2779, Dec. 2005.

[98] D. Pardo, A. Vaz, S. Gil, J. Gomez, A. Ubarretxena, D. Puente, R. Morales-Ramos, A. Garcia-Alonso, and R. Berenguer, "Design criteria for full passive long range uhf rfid sensor for human body temperature monitoring," *RFID, 2007. IEEE International Conference on*, pp. 141–148, March 2007.

[99] G. Tzanateas, C. Salama, and Y. Tsividis, "A cmos bandgap voltage reference," *Solid-State Circuits, IEEE Journal of*, vol. 14, pp. 655–657, Jun 1979.

[100] P. Nikitin, K. Rao, and S. Lazar, "An overview of near field uhf rfid," *RFID, 2007. IEEE International Conference on*, pp. 167–174, March 2007.

[101] G. Rincon-Mora and P. Allen, "A low-voltage, low quiescent current, low drop-out regulator," *Solid-State Circuits, IEEE Journal of*, vol. 33, pp. 36–44, Jan 1998.

[102] J. Cockcroft and E. Walton, "An overview of near field uhf rfid," *Proceedings of the Royal Society of London. Series A*, vol. 136, pp. 619–630, June 1932.

[103] A. Shameli, A. Safarian, A. Rofougaran, M. Rofougaran, and F. De Flaviis, "Power harvester design for passive uhf rfid tag using a voltage boosting technique," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 55, pp. 1089–1097, June 2007.

[104] H. Henisch, "Metal-semiconductor schottky barrier junctions and their applications," *Proceedings of the IEEE*, vol. 74, pp. 894–894, June 1986.

[105] W. Jeon, J. Melngailis, and R. Newcomb, "Cmos schottky diode microwave power detector fabrication, spice modeling, and applications," *Electronic Design, Test and Applications, 2006. DELTA 2006. Third IEEE International Workshop on*, pp. 6 pp.–, Jan. 2006.

[106] A. Hastings, *The Art of Analog Layout*. Upper Saddle River, New Yersey, U.S.: Prentice–Hall, 2nd ed., 2001. Available on–line: http://www.amazon.com/Art-Analog-Layout-Alan-Hastings/dp/0130870617.

[107] R. Morales-Ramos, D. Puente, H. Milosiu, H. Berenguer, and J. Montiel-Nelson, "Optimal impedance matching in passive uhf rfid sensors," *3rd European Workshop on RFID Systems and Technologies (RFID SysTech)*, June 2007.

[108] R. E. Collin, *Antennas and Radiowave Propagation*. New York, U.S.: McGraw-Hill, 2nd ed., 2003. Available on–line: http://www.amazon.com/Antennas-Radiowave-Propagation-Electrical-Engineering/dp/0070118086.

[109] M. Usami, "An ultra small rfid chip: μ-chip," *Radio Frequency Integrated Circuits (RFIC) Symposium, 2004. Digest of Papers. 2004 IEEE*, pp. 241–244, June 2004.

[110] G. De Vita and G. Iannaccone, "Ultra low power rf section of a passive microwave rfid transponder in 0.35 μm bicmos," *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, pp. 5075–5078 Vol. 5, May 2005.

[111] U. o. A. Auto-ID Laboratory, "Rfid analog front end design tutorial." Available on–line: http://autoidlab.eleceng.adelaide.edu.au/Tutorial.html.

[112] O. Semiconductors^{TM}, "Linear and switching voltage regulators handbook," 2002. Available on–line: Available on–line: http://stef-jon-audio-amps.googlecode.com/files/HB206-D.PDF.

[113] C. Simpson and by National Semiconductor, "Linear and switching voltage regulator fundamentals." Available on–line: http://www.national.com/appinfo/power/files/f4.pdf.

[114] F. Goodenough, "Low dropout linear regulators," *Electronic Design*, pp. 65–77, May 1996.

[115] M. M. Cirovic, *Integrated Circuits: A User's Handbook*. Resto, Virginia, Reston Publishing Company, Inc., 1977.

[116] R. Widlar, "New developments in ic voltage regulators," *Solid-State Circuits, IEEE Journal of*, vol. 6, pp. 2–7, Feb 1971.

[117] P. R. Gray, P. J. Hurst, S. H. Lewis, and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*. New York, USA: John Wiley & Sons, Inc., 4th ed., 2001. Available on–line: http://eu.wiley.com/WileyCDA/WileyTitle/productCd-0471321680.html.

[118] Y. Tsividis, *Operation and modeling of The MOS Transistor*. New York, USA: Oxford University Press, 2nd ed., 1999.

[119] Y. Jiang and E. Lee, "Design of low-voltage bandgap reference using transimpedance amplifier," *Circuits and Systems II: Analog and Digital Signal Processing, IEEE Transactions on*, vol. 47, pp. 552–555, Jun 2000.

[120] H. Watanabe, S. Ando, H. Aota, M. Dainin, Y. Chun, and K. Taniguchi, "Precision and robust cmos voltage reference based on the work function difference of poly si gate," *Solid-State Circuits Conference, 2002. ESSCIRC 2002. Proceedings of the 28th European*, pp. 387–390, Sept. 2002.

[121] F. Fiori and P. Crovetti, "A new compact temperature-compensated cmos current reference," *Circuits and Systems II: Express Briefs, IEEE Transactions on*, vol. 52, pp. 724–728, Nov. 2005.

[122] M.-H. Cheng and Z.-W. Wu, "Low-power low-voltage reference using peaking current mirror circuit," *Electronics Letters*, vol. 41, pp. 572–573, May 2005.

[123] G. Ripamonti, M. Bertolaccini, R. Peritore, and S. Schippers, "Low power-low voltage band gap references for flash-eeprom integrated circuits: design alternatives and experiments," *Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on*, vol. 2, pp. 635–638 vol.2, Sep 1999.

[124] G. De Vita and G. Iannaccone, "An ultra-low-power, temperature compensated voltage reference generator," *Custom Integrated Circuits Conference, 2005. Proceedings of the IEEE 2005*, pp. 751–754, Sept. 2005.

[125] K. N. Leung and P. Mok, "A cmos voltage reference based on weighted v_{GS} for cmos low-dropout linear regulators," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 146–150, Jan 2003.

[126] H. Oguey and D. Aebischer, "Cmos current reference without resistance," *Solid-State Circuits, IEEE Journal of*, vol. 32, pp. 1132–1135, Jul 1997.

[127] T. Hirose, T. Matsuoka, K. Taniguchi, T. Asai, and Y. Amemiya, "Ultra-low-power current reference circuit with low temperature dependence," *IEICE Trans. Electron.*, vol. E88-C, pp. 1142–1147, June 2005.

[128] A. Buck, C. McDonald, S. Lewis, and T. Viswanathan, "A cmos bandgap reference without resistors," *Solid-State Circuits, IEEE Journal of*, vol. 37, pp. 81–83, Jan 2002.

[129] E. Vittoz and J. Fellrath, "Cmos analog integrated circuits based on weak inversion operations," *Solid-State Circuits, IEEE Journal of*, vol. 12, pp. 224–231, Jun 1977.

[130] I. Zalbide, G. Nanclares, A. Vaz, D. Pardo, J. Sevillano, and I. V'elez, "Reducing the power consumption of the digital part of a gen2 rfid sensor tag," *Conference on Design of Circuits and Integrated Systems DCIS07*, November 2007.

[131] J. Bird, *Electrical Circuit Theory and Technology*. Oxford, UK: Elsevier, 2nd ed., 1999.

[132] A. Vaz, A. Ubarretxena, D. Pardo, I. Sancho, and H. Berenguer, "Design metodology of a voltage multiplier for full passive long range uhf rfid," *3rd European Workshop on RFID Systems and Technologies (RFID SysTech)*, June 2007.

[133] I. Mayordomo, A. Vaz, D. Pardo, I. Gutiérrez, A. García-Alónso, and R. Berenguer, "Design considerations for long range passive rfid readers," *XXII Conference on Design of Circuits and Integrated Systems, DCIS 2007*, Nov. 2007.

[134] A. Vaz Serrano, *Design and Optimization of an Analog Front End for a Long Range Full Passive RFID Sensor*. PhD thesis, TECNUN, Universidad de Navarra, December 2008.

[135] D. Pardo Sanchez, *Design and Implementation of a Long Range Full Passive RFID Sensing System*. PhD thesis, TECNUN, Universidad de Navarra, October 2008.

[136] I. Mayordomo Lastra, *Design, Analysis and Implementation of a Long Range RFID Reader for Passive Wireless Sensors*. PhD thesis, TECNUN, Universidad de Navarra, July 2008.

[137] A. Vaz, R. Berenguer, D. Pardo, I. Medizabal, I. Zalbide, and I. Mayordomo, "Demodulador de bajo consumo," 2008.

[138] R. Berenguer, A. Vaz, A. Ubarretxena, I. Ayerdi, J. Sevillano, and A. García-Alónso, "Convertidor capacidad–frequencia con la capacidad variable como fuente de alimentacin del oscilador," 2008.

[139] R. Morales-Ramos, J. Montiel-Nelson, H. Milosiu, R. Berenguer, and A. Garcia-Alonso, "Adjustable voltage sensors for power supply chains in passive uhf rfid transponders," *Emerging Technologies and Factory Automation, 2006. ETFA '06. IEEE Conference on*, pp. 286–291, Sept. 2006.

[140] R. Morales-Ramos, J. Montiel-Nelson, R. Berenguer, and A. Garcia-Alonso, "Voltage sensors for supply capacitor in passive uhf rfid transponders," *Digital System Design: Architectures, Methods and Tools, 2006. DSD 2006. 9th EUROMICRO Conference on*, pp. 625–629, 0-0 2006.

[141] R. Morales-Ramos, R. Berenguer, and J. Montiel-Nelson, "Voltage protection circuit for the supply capacitor in passive uhf rfid sensors," *XXII Conference on Design of Circuits and Integrated Systems, DCIS 2007*, Nov. 2007.

[142] R. Morales-Ramos, A. Vaz, D. Pardo, and R. Berenguer, "Ultra-low power passive uhf rfid for wireless sensor networks," *Digital System Design Architectures, Methods and Tools, 2008. DSD '08. 11th EUROMICRO Conference on*, pp. 671–675, Sept. 2008.

[143] D. M. Pozar, *Microwave Engeeniering*. John Wiley & Sons, 2nd ed., May 1998.

Capítulo A

Publications

Voltage Sensors for Supply Capacitor in Passive UHF RFID Transponders

*R. Morales–Ramos**, Juan A. Montiel–Nelson**, R. Berenguer*†, A. García–Alonso*†
*Institute for Applied Microelectronics University of Las Palmas de G.C. Las Palmas de G.C., Spain
†Centro de Estudios e Investigaciones Técnicas de Guipúzcoa (C.E.I.T.), San Sebastian, Spain
Email: ricmorales@iuma.ulpgc.es

***Abstract*— This paper presents two very low–power consumption voltage–sensor circuits for the supply capacitor in passive UHF RFID transponders. The proposed circuits are key points in a battery–life–free RFID tag, by sensing the charge stored in a supply capacitor, and enabling the rest of the system when enough charge is available. In comparison to previous published circuits, the average current of our circuits is one order of magnitude lower. The average current consumption for our solutions is below 100 nA, for a supply voltage between 2.5 V and 3.3 V.**

In addition, we have proposed some modifications to the best published results; and diminished the power consumption one order of magnitude.

I. Introduction

Sensor networks to realize ubiquitous computing require not only a small, simple, and low–cost RF terminal with sensing device, but also a very low–power consumption and a long–distance communication range. Radio frequency identification (RFID) systems are one of the most appropriate RF terminals for sensor networks, satisfying previous requirements. In recent years, RFID tags have become very popular in many applications such as manufacturing, product distribution, sales, security and surveillance. They have a number of additional advantages over the traditional barcode labels namely, larger storage capacity, write capability and larger distance range, among others. Passive RFID systems working in the UHF band will probably be the next generation of RFID systems. Battery–life–less operation, reading distance of few meters and international standards availability, are some of their features [1].

Power consumption is the key issue in passive UHF transponders. The DC power is obtained from the incident RF signal by means of a voltage multiplier [2], which feeds a charge capacitor. This capacitor serves as DC power storage to supply the rest of the system. At this point, there are two ways to manage the charge of the capacitor.

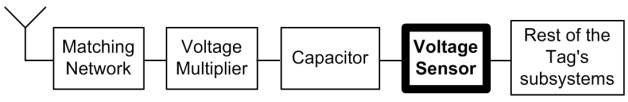

Fig. 1. Simplified block diagram of passive RFID system.

Some authors [2]–[4] connect the terminals of the capacitor directly to the system supply signal. Therefore, if the charge speed is lower than the discharge speed, the system can suffer unwanted supply interruptions caused by short absence of the RF signal. This limitation reduces the operation range of this kind of systems.

In order to extend the operation range, as much as possible, some other authors [5], [6] use a specific circuit, the voltage sensor (VS). This subsystem avoids malfunctions of the system caused by short absences of RF signal (see Fig. 1). This circuit senses the stored voltage in the capacitor, and turns on the complete system only when enough charge is available. The current consumption of the voltage sensor must be very low to allow a fast charge. On the other hand, the "EPC RFID generation2" protocol [7] promotes the use of this circuit. The standard fixes a settling time of 1.5 ms at the beginning of the communication between reader and transponder. This time is very suitable to charge the capacitor and to initialize the rest of the system.

We have chosen a 0.35–μm complementary metal–oxide–semiconductor (CMOS) technology from XFAB (XL035), due to the high integration density, and the availability of schottky diode and EEPROM macrocells, which are fundamental components to fabricate a RFID system. All the results presented in this paper are obtained using this technology.

Two different voltage sensors architectures has been published up to nowadays. The first one is based on a differential stage, and it is referenced as Mode Selector (MS) [5]. The second one is based on the charging time of a capacitor, and it is termed as Power On Reset (POR) [6].

This paper is organized as follows. Section II introduces three circuits from the state of the art, MS, POR, and a modified version of MS (MMS) [8]. In addition, we propose two novel circuits, and the low power versions of MMS and POR. Section III describes, in detail, the experimental setup for obtaining results and providing a fair comparison between circuit structures. The results and comparisons are presented in Section IV. Finally, the main conclusions of this work are presented in Section V.

II. Circuit Structures

This section introduces those referenced circuits, namely MS and POR, from the state of the art in voltage–sensor circuits. A modified version of MS, termed MMS, is also analyzed in detail. We describe the operation of these voltage sensors. Two novel circuits are proposed and analyzed. In addition, we propose some modifications of MMS and POR for

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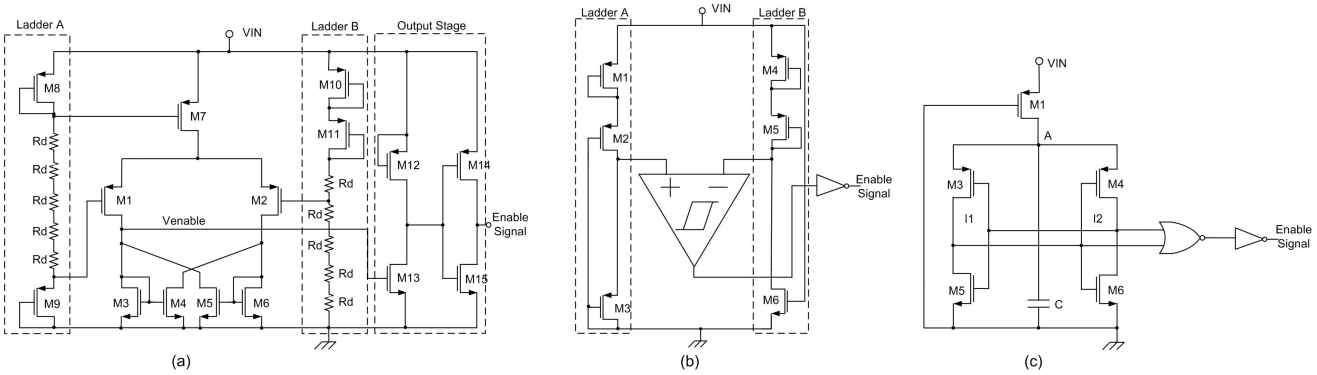

Fig. 2. Schematic circuits from state of art: (a) Mode Selector (MS), (b) Modified Mode Selector (MMS), and (c) Power On Reset (POR).

very low–power consumption, and providing a fair comparison among solutions.

A. State of the Art

In passive UHF RFID transponders, the power supply capacitor is charged during the settling time, at the beginning of the communication stage. Then, an activation signal (Enable Signal) turns on the rest of the circuit. At the end of the communication stage, the RF signal is no more present, and the complete system is turned off — due to lack of supply.

As we mentioned before, there are three published circuit–structures, MS, POR and MMS. The MS schematic is illustrated in Fig. 2(a). The two lateral branches (ladder A and B) fix the voltage at the gate of transistors M1 and M2. Depending on the gate voltage, either M1 or M2 will be in saturation. Transistor M2 conducts for small values of VIN. When VIN exceeds a threshold voltage level, M1 conducts and Enable Signal is activated. The cross coupled transistors M3, M4, M5 and M6 fix the VIN voltage required to activate (deactivate) the Enable Signal. When VIN voltage is equal or higher than an upper threshold voltage (Vup), Enable Signal is turned on. If VIN is equal or lower than a lower threshold voltage (Vdown), Enable Signal turns off. For comparison against the POR circuit, we will only consider the upper threshold voltage level Vup.

Some results from the state of the art is as follows. In the standby mode, the current consumption of the MS circuit is 5 μA. The same authors [8] proposed a modification of this circuit (see Fig. 2(b)), termed MMS, where the resistors were replaced by active loads. The current consumption in the modified version is about 900 nA.

The other alternative is the POR circuit (see Fig. 2(c)). When the circuit powers up, one of the two inverters I1 and I2 takes advantage over the other. The NOR gate compares the output of two inverters, and activates Enable Signal. The capacitor C forces a delay between the rise of the voltage supply signal and Enable Signal, so Vup depends on the value of C, as well.

B. Novel architectures

We propose two additional circuits; the first one is based on voltage levels, termed VL (Voltage Level). The second one is based on the charging time of a capacitor, it is known as Charge Capacitor (CC).

The VL circuit is presented in Fig. 3(a). The MOS resistive ladder (M1–M10) turns on the transistor M12, when VIN achieves the upper threshold voltage level (Vup). At this point, the Enable Signal is activated. The circuit is implemented entirely with MOS devices. The dimensions of all devices are optimized for ultra low–power consumption.

Fig. 3(b) shows the CC circuit. The capacitor C delays the activation of Enable Signal. The output stage, formed by M6–M12 network, turns on Enable Signal when the transistor M7 is switched on. It occurs when the capacitor C is charged enough. Because C is charged via transistors M1–M4, the dimensions of this transistors determine the charging time and Vup rise time. Finally, when VIN goes down Vup, C is discharged quickly by M5. Therefore, we have reduced the minimum required time between two consecutive Enable Signals.

III. Experimental Setup

We used Cadence v5.1.41 as CAD tool for both schematic and layout entry and simulation. The technology is from XFAB, in particular the XL035 process. We have done both a pre– and post–layout simulation for measuring comparison–performance.

A. Performance Parameters

The capacitor, which feeds up the RFID tag, is charged quickly or slowly depending on the reader distance, the used voltage multiplier circuit, and the capacitance. We are interested in power consumption and area of each structure, for standard operational conditions. In order to compare the different alternatives, all the circuits were adjusted to activate the Enable Signal when Vup is between 2.5 V and 3.3 V. All the eight simulation corners, as specified in the technology process, were tested. VIN is generated by a pulse source with

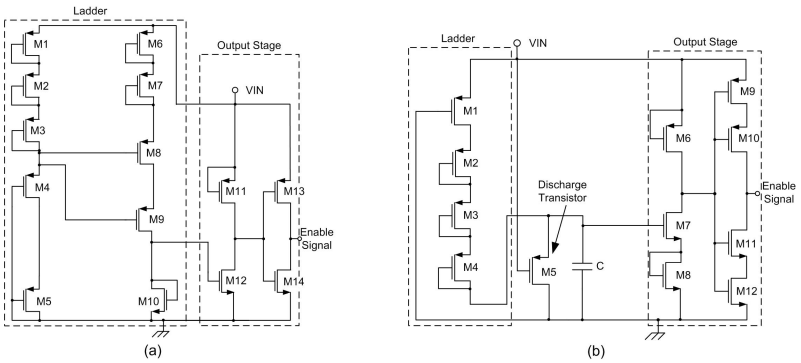

Fig. 3. Novel schematic circuits: (a) Voltage Levels (VL), and (b) Charge Capacitor (CC).

voltage levels between 0 V and 3.3 V; and a rise time of 250 μs for quick charging time; or 1.5 ms for slow charging time.

The measured parameters obtained from the simulations were:

- Vup variation due to corner simulations (ΔVup_c), and due to charging time of the capacitor (ΔVup_t);
- average ($\bar{I}$) and peak ($\hat{I}$) current consumption; and
- active area, which is calculated though the size of the required devices according with the technology.

B. Vup Adjusting

Adjusting Vup to 2.5 V, requires some modifications on the MMS and POR circuits. In MMS circuit (see Fig. 2(b)), we have modified the MOS resistive ladders A and B, as is illustrated in Fig. 4(a). The presence of several transistors as diodes with high aspect ratio (Width=0.5/Length=6) reduces, considerably, the current and, therefore, power consumption.

The original POR circuit produces very low Vup (some hundreds of mV), when it is implemented using XL035 process. In order to provide a fair comparison, the threshold voltage Vup was increased to 2.5 V, by introducing two transistors, M7 and M8, connected as diodes, as shown in Fig. 4(b).

IV. RESULTS

Firstly, we will introduce some comparisons between MMS, POR, VL and CC structures, in terms of current consumption and area. In addition, the details about post–layout simulations of the novel circuits are discussed at the end of this section.

A. Comparison

We implemented and simulated the circuit structures MS, VL, CC and the modified versions MMS and POR. Table I provides the performance for the five circuits. Column one is the name of the circuit. Columns two and three are the average ($\bar{I}$) and peak current ($\hat{I}$), respectively. Columns four and five represent the maximum variation of the upper threshold voltage level Vup ($\Delta Vup_{c,t}$), because of the process corner and capacitor charging time, respectively. Column six is the active area of each circuit. Finally, column seven and eight are performance compositions as Figures of Merits; where Γ_1 is the product of average current $\bar{I}$ and active area (columns two and six), and Γ_2 is the peak current $\hat{I}$ per active area (columns three and six). Γ_1 provides some inside about the product power consumption and area on average, i.e. the lower Γ_1, the better is the circuit–structure. Γ_2 is related with the power dissipation feature; e.g. as Γ_2 is decreased, the peak current per area unit is reduced.

Results of Table I show that the average current consumption of MMS, VL and CC circuits is one order of magnitude lower than the MS and POR circuits. The use of resistors in MS circuit increases the power consumption, dramatically. For the POR circuit, the input stage to the NOR gate is responsible of the high current consumption. In addition, our modified version of the MMS circuit consumes one order of magnitude less than the original MMS [8].

Because the output stage is similar in all the circuits, the peak current is similar (see column three in Table I). Our CC circuit reduces the peak current more than 1 μA. This is because the inverter at the output stage formed by our transistors with high aspect ratio.

The dispersion of Vup due to technology corners is around 1 V; and the dispersion due to the charging time of the capacitor is about 0.4 V, except for the POR circuit that has better buffering stage.

Finally, the active area of the MS circuit is two orders of magnitude bigger than the other circuits, because of the use of high value integrated resistors.

To sum up, MS and POR present the biggest current consumption; and, in the case of MS, the highest active area. Although, VL circuit is based on MMS, the performance of the former is better. Both CC and VL have similar performance, in terms of $\bar{I}$, $\hat{I}$, ΔVup_c and ΔVup_t. Peak current of CC is lower than that of VL. However, active area of VL is lower than that of CC. Figures of Merits Γ_1 and Γ_2 indicate that CC has some advantages against VL.

Although all the performance in pre–layout measurements indicates that CC is the best circuit–structure, a further physical implementation of this two circuits should be done, in order to know more about which principle is the most suitable for our passive UHF RFID transponders (charge of a capacitor or on voltage levels).

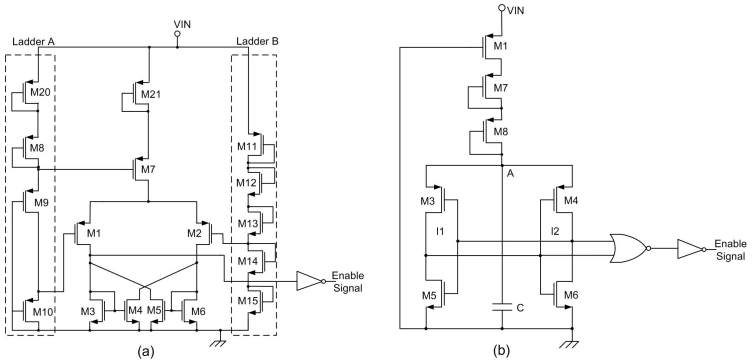

Fig. 4. Modified versions of: (a) MMS circuit, and (b) POR circuit.

TABLE I

PERFORMANCE COMPARISON BETWEEN VOLTAGE SENSOR CIRCUIT–STRUCTURES

$Circuit$	$\bar{I}$ (nA)	$\hat{I}$ (μA)	ΔVup_c (V)	ΔVup_t (V)	$Area$ (μm^2)	Γ_1 (nA$\times\mu m^2$)	Γ_2 (μA/μm^2)$\times 10^{-5}$
MS	800	1.87	1.10	0.40	30148	24118400	6
MMS	57	1.44	0.85	0.50	693	39501	207
POR	1350	1.55	1.40	0.20	348	469800	445
VL	47	1.65	0.90	0.45	352	16544	468
CC	$<$ **1**	**0.50**	1.10	0.49	590	$<$ **590**	**85**

TABLE II

POST–LAYOUT PERFORMANCE FOR VL AND CC CIRCUIT–STRUCTURES

$Circuit$	$\bar{I}$ (nA)	$\hat{I}$ (μA)	ΔVup_c (V)	ΔVup_t (V)	$Area$ (μm^2)	Γ_1 (nA$\times\mu m^2$)	Γ_2 (μA/μm^2)$\times 10^{-5}$
VL	85	1.63	0.9	0.45	2870	**24950**	56
CC	33	0.50	1.1	0.49	4672	154176	**10**

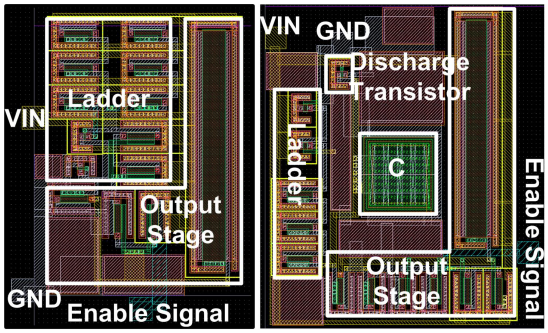

Fig. 5. Layouts in silicon chip for: (a) VL circuit, and (b) CC circuit.

B. Post–layout simulations

The layout of the CC and VL circuits were done, parasitic extracted and simulated. Table II shows the obtained post–layout results. Comparisons between Table I and Table II, for average current consumption, indicates this is increased by a factor of two. This increment is because the capacitive and resistive parasitic, in the post–layout implementation. Peak current and Vup dispersions do not undergo remarkable changes with respect to pre–layout simulations. Now, column six in Table II represents the chip area of both circuits. This area includes extra area for placement and routing, guard rings, and input/output pins. Figures of Merits, Γ_1 and Γ_2, do not provide the best candidate. Both circuits were implemented in silicon to obtain measurements from the chip. Fig. 5(a) and (b)

illustrated the layouts for the VL and CC circuits, respectively.

V. Conclusions

We have proposed two novel voltage–sensor circuits, namely VL and CC, for battery–life–free passive UHF RFID systems. Although the main aim of these systems is a long distance communication range, the power consumption is the most important design variable. By optimizing each subsystem of the RFID transponder, in terms of power consumption, we achieve the longest range of operation.

In a battery–life–free RFID system, our novel circuits, VL and CL, enable the tag, when enough charge is available in the supply capacitor using a very low power consumption. The average current consumption for both solutions are under 100 nA, for a supply voltage between 2.5 V and 3.3 V. In comparisons to previous published work [5], [6], [8], the average current of our circuits is one order of magnitude lower. We use a 0.35–μm CMOS process from XFAB. Because the output stage is similar in all the analyzed structures, the peak current is similar.

In addition, we have proposed some modifications of the best published results [8] and [6]. Our modified version of MMS has a power consumption of one order of magnitude less than the original MMS [8], when is implemented in XFAB technology.

In post–layout simulations, Figures of Merits — average current–area product (Γ_1), and peak current per unit of area (Γ_2) — of VL and CC illustrate a tradeoff between both solutions.

Acknowledgment

This work was supported by the Spanish Ministry of Science and Technology under Grant TEC2005–08138–C02–01 (ENDIVIA Project), and by Telefonica S.A. under contract EU–14/01–66043. In addition, the authors would like to thank to the Institute for Applied Microelectronics of the University of Las Palmas de Gran Canaria.

References

[1] K. Finkenzeller, *RFID Handbook, Radio–Frequency Identifications Fundamentals and applications,* 2nd ed. New York: Wiley, 2003.

[2] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponders IC with 16.7-μW minimun RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pages 1602–1608, Oct. 2003.

[3] G. De Vita and G. Iannaccone, "Ultra Low Power RF Section of a Passive Microwave RFID Transponderin 0.35 μm BiCMOS," in *IEEE Int. Symp. Circuits Systems (ISCAS 2005)*, Kobe, Japan, May 2005.

[4] U. Kaiser and W Steinhagen "A Low–Power Transponder IC for High-Performance Identification Systems," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pages 306–310, Mar. 1995.

[5] F. Kocer, P. M. Walsh and M. P. Flynn, "Wireless remotely powered telemetry in 0.25 μm CMOS," in *IEEE Radio Frequency Integrated Circuits(RFIC) Symp.*, pages 339–342, Jun. 2004.

[6] J.-P. Curty, N. Joehl, C. Dehollain and M. J. Declercq, "Remotely Powered Addressable UHF RFID Integrated System," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pages 2193–2202, Nov. 2005.

[7] EPC Tag Data Standards Version 1.1 Rev. 1.27, (2005, May), [Online] Avalible: http://www.epcglobalinc.org/standards_technology/specifications.html.

[8] F. Kocer and M. P. Flynn, "A Long-Range RFID IC with On–chip ADC in 0.25 μm CMOS," in *IEEE Radio Frequency Integrated Circuits(RFIC) Symp.*, pages 361–364, Jun. 2005.

Adjustable Voltage Sensors for Power Supply Chains in Passive UHF RFID Transponders

R. Morales–Ramos[1], *Juan A. Montiel–Nelson*[1], *H. Milosiu*[2], *R. Berenguer*[3], *A. García–Alonso*[3]
[1]Institute for Applied Microelectronics University of Las Palmas de G.C., Las Palmas de G.C., Spain
[2]Fraunhofer Institute for Integrated Circuits, Erlangen, Germany
[3]Centro de Estudios e Investigaciones Técnicas de Guipúzcoa (C.E.I.T.), San Sebastian, Spain
Email: ricmorales@iuma.ulpgc.es

***Abstract*— In passive UHF RFID transponders, a storage capacitor is used to supply the tag's subsystems. A quick charge of the storage capacitor and a sufficient supply voltage for the subsystems are intended for proper operation, thus using a voltage sensor.**

This paper presents two adjustable very low power consumption voltage sensor circuits for the supply capacitor in passive UHF RFID transponders. The proposed circuits sense the charge stored in a supply capacitor and enable the rest of the system when enough charge is available. In comparison to previous published circuits, the average current of our circuits is one order of magnitude lower. The average current consumption for our two solutions is below 100 nA, for a supply voltage between 2.5 V and 3.3 V.

I. Introduction

Sensor networks realizing ubiquitous computing require not only a small, simple and low cost RF terminal with sensing device, but also a very low power consumption and a long distance communication range. Radio frequency identification (RFID) systems are one of the most appropriate RF terminals for sensor networks, satisfying previous requirements. In recent years, RFID tags have become very popular in many applications such as manufacturing, product distribution, sales, security and surveillance. They have a number of additional advantages over the traditional barcode labels namely larger data capacity, rewrite capability and larger distance range, among others. Passive RFID systems working in the UHF band will probably be the next generation of RFID systems. This kind of RFID tags does not use batteries and can be read from a distance of a few meters [1].

Power consumption is the key issue in passive UHF transponders. The DC power is obtained from the received RF signal. A voltage multiplier converts RF in to DC power [2]. Then, the DC signal of the voltage multiplier charges a capacitor serving as DC power storage to supply the rest of the system. At this point, there are two ways to manage the charge of the capacitor.

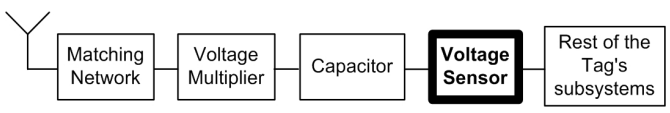

Fig. 1. Simplified block diagram of passive RFID system.

One way [2]–[4] is to connect the terminals of the capacitor directly to the system supply voltage. In this case, the supply of the system can be interrupted by short absences of the RF signal. This limits the operation range[1] of this kind of systems.

In order to extend the operation range as much as possible, a second way [5], [6] is to use a voltage sensor (VS). This subsystem avoids malfunctions of the system caused by short absences of the RF signal (see Fig. 1). This circuit senses the stored voltage in the capacitor, and turns on the complete system only when a minimum charge is available. The current consumption of the voltage sensor must be very low to allow a fast charge. On the other hand, the "EPC RFID generation2" protocol [7] promotes the use of this circuit. The standard fixes a settling time of 1.5 ms at the beginning of the communication between reader and transponder. During the settling time the capacitor is charged and the rest of the system is initialized.

Two different voltage sensors architectures have been published till now. The first one is based on a differential stage, and it is referenced as Mode Selector (MS) [5]. The second one is based on the charging time of a capacitor, and it is termed as Power On Reset (POR) [6].

We have chosen a 0.35 μm complementary metal oxide semiconductor (CMOS) technology from XFAB (XL035), due to the high integration density, the availability of schottky diode and EEPROM macrocells, which are fundamental components to fabricate a RFID system.

This paper is organized as follows. Section II introduces three circuits from the state of the art, MS, POR, and a modified version of MS (MMS) [8]. In addition, we propose two novel circuits. Section III describes in detail, the experimental setup for obtaining results and providing a fair comparison between circuit structures. The results and comparisons are presented in Section IV. Finally, the main conclusions of this work are presented in Section V.

II. Circuit Structures

Firstly, this section introduces the state of the art in voltage sensors for passive RFID tags. Next, two novel circuits are proposed and analyzed.

[1]minimum distance between reader and tag for proper operation.

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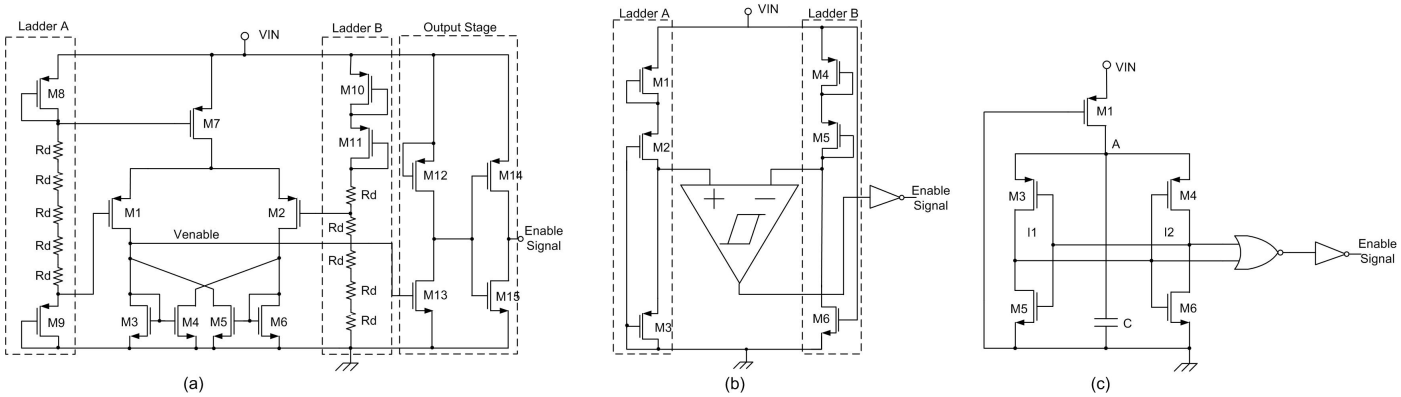

Fig. 2. Schematic circuits from state of art: (a) Mode Selector (MS), (b) Modified Mode Selector (MMS), and (c) Power On Reset (POR).

A. State of the Art

In passive UHF RFID transponders, the power supply capacitor is charged during the settling time, at the beginning of the communication between reader and tag. Then, an activation signal (Enable Signal) turns on the rest of the circuit. At the end of the communication, the reader stops the transmission of the RF signal, and the complete system is turned off due to lack of supply.

As we mentioned before, there are three published circuit structures, MS, POR and MMS. The MS schematic is shown in Fig. 2(a). The two lateral branches (ladder A and B) bias the transistors M1 and M2. Depending on the gate voltage, either M1 or M2 will be in saturation. Transistor M2 conducts for small values of VIN. When VIN exceeds a threshold voltage level, M1 conducts and the Enable Signal is set to HIGH[2]. The cross coupled transistors M3, M4, M5 and M6 adjust the VIN voltage required to set to HIGH or to LOW[3] the Enable Signal. When VIN voltage is equal or higher than an upper threshold voltage (Vup), the Enable Signal is set to HIGH. If VIN is equal or lower than a lower threshold voltage (Vdown), the Enable Signal is set to LOW. To compare with the POR circuit, we will only consider the upper threshold voltage level Vup.

Before the activation of the Enable Signal, the current consumption of the MS circuit is 5 μA [5]. A modification of this circuit (MMS) is proposed in [8] (see Fig. 2(b)). In this case, the resistors are replaced by active loads. The current consumption in the modified version is about 900 nA.

The other alternative is the POR circuit (see Fig. 2(c)). When a supply voltage is applied to VIN, one of the two inverters I1 and I2 takes advantage over the other. The NOR gate compares the output of the two inverters, and activates the Enable Signal. The capacitor C forces a delay between the rise of the voltage supply signal and the Enable Signal, so Vup depends on the value of C, as well.

[2]The Enable Signal is equal to VIN.
[3]The Enable Signal is equal to 0 V.

B. Novel architectures

We propose two additional circuits; the first one is based on voltage levels (VL). The second one is based on the charging time of a capacitor (CC).

The VL circuit is shown in Fig. 3(a). The ladder (M1–M10) biases the transistor M12. When VIN achieves the upper threshold voltage level (Vup), M12 conducts and the Enable Signal is set to HIGH. The circuit is implemented entirely with MOS devices. The dimensions of all devices are optimized for ultra low power consumption, see Table I.

Fig. 3(b) shows the CC circuit. The capacitor C delays the activation of the Enable Signal. The output stage, formed by M6–M12, sets to HIGH the Enable Signal when the transistor M7 is switched on. M7 conducts only when capacitor C is charged enough. Because C is charged via transistors M1–M4, the dimensions of these transistors determine the charging time and Vup rise time. Finally, when the voltage in VIN decreases, C is discharged through M5. In this way, the minimum required time between two consecutive Enable Signals is reduced.

Notice that the Vup can be adjusted in both architectures by changing the number of diode transistors in the ladders. The more transistors are in the ladder, the higher is Vup.

III. Experimental Setup

We used Cadence v5.1.41 as CAD tool for schematic and layout entry and simulation. We have done both a pre– and postlayout simulation. The obtained results for each architecture were compared.

A. Performance Parameters

The charge of the supply capacitor depends on the reader distance, the used Voltage Multiplier and the capacitance of the supply capacitor. We are interested in power consumption and area of each structure, for standard operational conditions. To compare the different architectures, all the circuits were adjusted to set to HIGH the Enable Signal when Vup is, for all the corners, between 2.5 V and 3.3 V. All the eight simulation corners, as specified in the technology process, were tested. VIN is generated by a pulse source with voltage levels between

TABLE I

SIZE OF THE TRANSISTORS OF THE NOVEL ARCHITECTURES

VL		CC	
Device	W/L (μm^2)	Device	W/L (μm^2)
M1..M8	0.5 / 6	M1	1 / 2
M9, M10	0.9 / 0.35	M2..M4	0.5 / 6
M11	50 / 5	M5	0.9 / 0.35
M12..M14	0.5 / 6	M7..M12	0.5 / 6

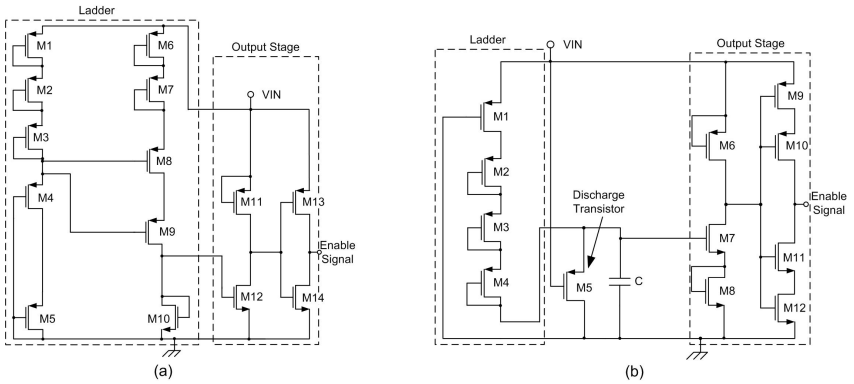

Fig. 3. Novel schematic circuits: (a) Voltage Levels (VL), and (b) Charge Capacitor (CC).

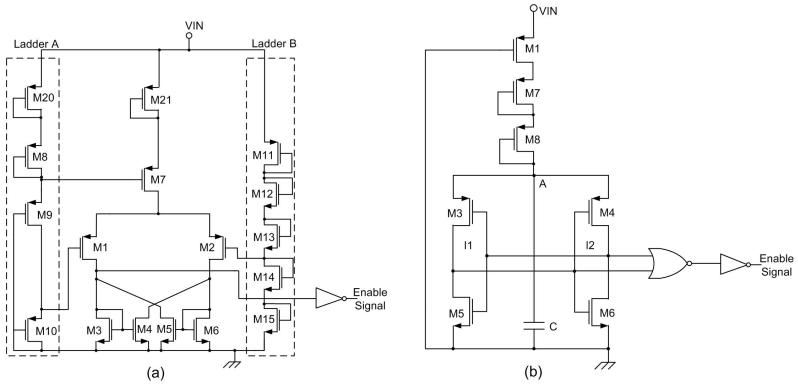

Fig. 4. Modified versions of: (a) MMS circuit, and (b) POR circuit.

0 V and 3.3 V, and a rise time of 250 μs for quick charging time, or 1.5 ms for slow charging time.

The parameters obtained from the simulations were:

- Vup variation due to corner simulations (ΔVup_c) and due to charging time of the capacitor (ΔVup_t);
- average ($\bar{I}$) and peak ($\hat{I}$) current consumption
- active area, which is calculated by adding the size of the required devices.

B. Modifications on MMS and POR structures

Adjusting Vup to 2.5 V requires some modifications on the MMS and POR circuits. In the MMS circuit (see Fig. 2(b)), we have modified the MOS resistive ladders A and B, as can be seen in Fig. 4(a). The presence of several transistors in the Ladder A and B with low aspect ratio (Width=0.5 μm/Length=6 μm) reduces considerably the current and therefore power consumption.

The Vup in the original POR circuit is very low (some hundreds of mV), when it is implemented. In order to provide a fair comparison, the threshold voltage Vup was increased to 2.5 V by introducing two transistors, M7 and M8 as shown in Fig. 4(b).

IV. RESULTS

Firstly, we will show some comparisons between MMS, POR, VL and CC structures, in terms of current consumption and area. Secondly, the results obtained from the postlayout simulations of the novel circuits are discussed. At the end of this section, we describe some postlayout simulation results, which verify the adjustability of Vup in the CC and VL structures.

TABLE II
SIMULATION RESULTS OF VOLTAGE SENSOR CIRCUIT–STRUCTURES

$Circuit$	$\bar{I}$ (nA)	$\hat{I}$ (μA)	ΔVup_c (V)	ΔVup_t (V)	$Area$ (μm^2)	reference
MS	800	1.87	1.10	0.40	30148	[5]
MMS	57	1.44	0.85	0.50	693	[8]
POR	1350	1.55	1.40	0.20	348	[6]
VL	80	1.65	0.90	0.45	352	this paper
CC	$< \mathbf{1}$	**0.50**	1.10	0.49	590	this paper

TABLE III
POSTLAYOUT SIMULATION RESULTS OF VL AND CC CIRCUIT–STRUCTURES

$Circuit$	$\bar{I}$ (nA)	$\hat{I}$ (μA)	ΔVup_c (V)	ΔVup_t (V)	$Area$ (μm^2)
VL	85	1.63	0.9	0.45	2870
CC	< 1	0.50	1.1	0.49	4672

A. Comparison

We simulated and implemented the circuit structures MS, VL, CC and the modified versions MMS and POR (see Fig. 4). Table II shows the simulation results for the five circuits. We simulated the average ($\bar{I}$) and peak ($\hat{I}$) current and the maximum variation of the upper threshold voltage level Vup with respect to process corners (ΔVup_c), and to the capacitor charging time (ΔVup_t). In addition, we estimated the area of each structure.

Table II shows that the average current consumption of the MMS, VL and CC circuits is one order of magnitude lower than of the MS and of the POR circuits. The use of resistors in the MS circuit increases the power consumption dramatically. For the POR circuit, the input stage to the NOR gate is the cause of the high current consumption. In addition, our modified version of the MMS circuit consumes one order of magnitude less than the MMS in [8].

The peak current is similar in the MS, MMS, POR and VL circuits (see Table II) because all these architectures use the same inverter at the output. The peak current of the CC circuit is one order of magnitude less than the above mentioned architectures. This is due to the transistors of the output inverter in the CC circuit have lower aspect ratio than in the other architectures.

The variation of Vup due to technology corners is around 1 V, and the variation due to the charging time of the capacitor is about 0.4 V. For short charging times Vup is higher than for long ones. The reason is that the used transistors have low aspect ration (W/L$\simeq$0.09). This reduces the power consumption of the structures, but increaese the time reqired by the transistors to swicht.

Finally, the active area of the MS circuit is two orders of magnitude bigger than the other circuits, because this circuit require high value integrated resistors (Rd in Fig. 2(a)) to reduce the current through the ladders A and B.

To sum up, MS and POR have the highest current consumption; and in the case of MS also the largest active area. The simulation results of the circuits VL and MMS are similar, the MMS structure has lower current consumption but larger active area. Both CC and VL have similar Vup variation results (ΔVup_c and ΔVup_t). The average and peak current of CC are lower than that of VL. However, the active area of VL is lower than that of CC.

The simulation results indicate that VL and CC circuits are the best structures. However, a further physical implementation of this two circuits should be done, to verify the results of Table II

B. Postlayout simulations

The layout of the CC and VL circuits were done, the parasitic capacitance extracted and simulated. Fig. 5 depicts the VIN, the Enable Signal and the current consumption versus time for the extracted CC and VL structures. VIN simulates the charge of the supply capacitor. When VIN exceeds Vup, the Enable Signal turns on. Both circuits present a current peak of about 1 μA, caused by the inverter of the output stage when the enable signal is activated. Notice that the current consumption before the activation is very low ($<$5nA). The rest of the current produced by the voltage multiplier is used to charge the supply capacitor until the activation.

Table III shows the obtained postlayout results. Comparisons between Table II and Table III for average current consumption indicate that this is increased about 10%. This increment is because the capacitive and resistive parasitics in the postlayout simulation. Peak current and Vup variation do not undergo remarkable changes compared to prelayout simulations. Column six in Table III represents the chip area of both circuits. This value includes extra area for placement and routing, guard rings, and input/output pins. Both circuits were implemented in silicon to obtain measurements from the chip. Fig. 6(a) and (b) shows the layouts for the VL and CC circuits, respectively.

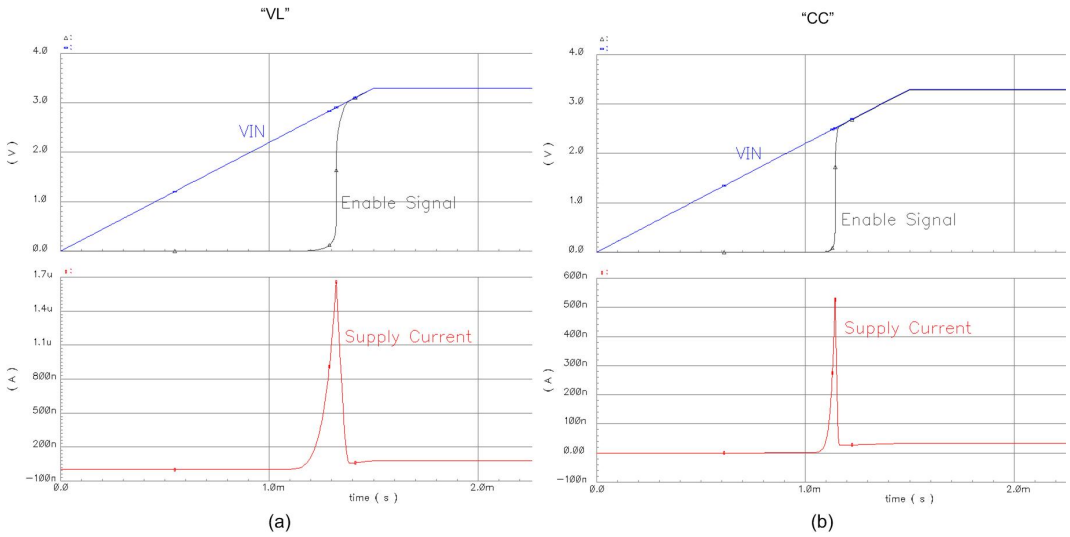

Fig. 5. VIN, Enable Signal and Current consumption versus time after post–layout simulations. (a) VL structure, and (b) CC structure.

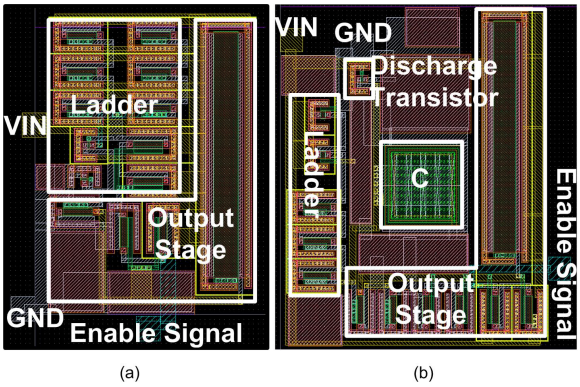

Fig. 6. Layouts in silicon chip for: (a) VL circuit, and (b) CC circuit.

C. *Vup Adjusting*

The Vup can be easily adjusted in the VL and CC structures. To verify that, some modifications were made in the VL and CC circuits to adjust Vup to 3.3 V. As a result, two new circuits, VL_33 and CC_33 were done, parasitic capacitance extracted and simulated. These new circuits only include modifications in the ladder compared to the VL and CC structures, as shown in Fig. 7.

Fig. 8 depicts the VIN, the Enable Signal and the current consumption versus time for the extracted CC, CC_33, VL and VL_33 structures. An increment of 1 Volt in Vup is achieved both in the CC_33 structure in relation to the CC structure, and in the VL_33 structure regarding to the VL structure. This increment is obtained by inserting two transistors in the ladders of the original CC and VL circuits. The peak current is higher in the CC_33 and VL_33 circuits, the reason is that the inverter switches at higher VIN (3.3 Volts instead of the 2.5 Volts of the CC and VL circuits). The structure VL_33 presents a higher current consumption than VL after the Enable Signal is set to HIGH. This is due to the ladder behaves as a resistance after the activation, therefore the consumed current increases linearly with VIN. On the other hand, the current consumption after the activation of the Enable Signal in CC and CC_33 is the same, because only the branch of M7 (Fig. 7(b)) draws current, which is the same in both structures.

V. Conclusions

We have proposed two novel adjustable voltage sensor circuits, namely VL (based on voltage levels) and CC (based on the charging time of a capacitor), for battery free passive UHF RFID systems. The main goal of these systems is the longest distance communication range. Since a RF signal supplies the RFID tag, the received power decreases with the distance. By optimizing each subsystem of the RFID transponder in terms of power consumption, we achieve a longer range of operation.

Our novel circuits are designed to operate in battery less RFID systems. Both the VL structure and the CC structure enable the tag, when a minimum charge is available in the supply capacitor. The average current consumption for both solutions is below 100 nA, for a supply voltage between 2.5 V and 3.3 V. In comparisons to previous published works [5],

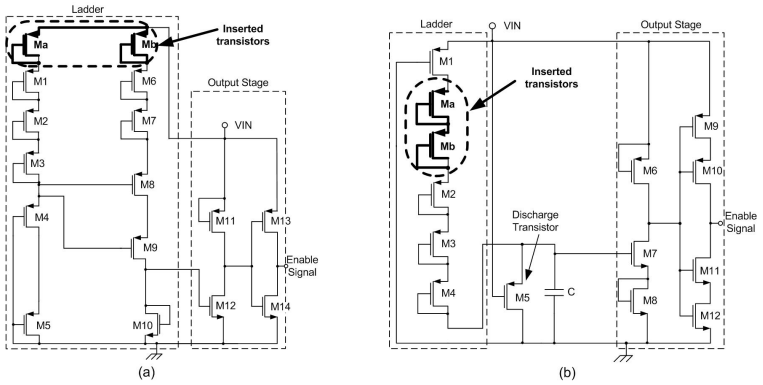

Fig. 7. New version with Vup adjusted at 3.3Volts: (a) VL_33 structure, and (b) CC_3 structure.

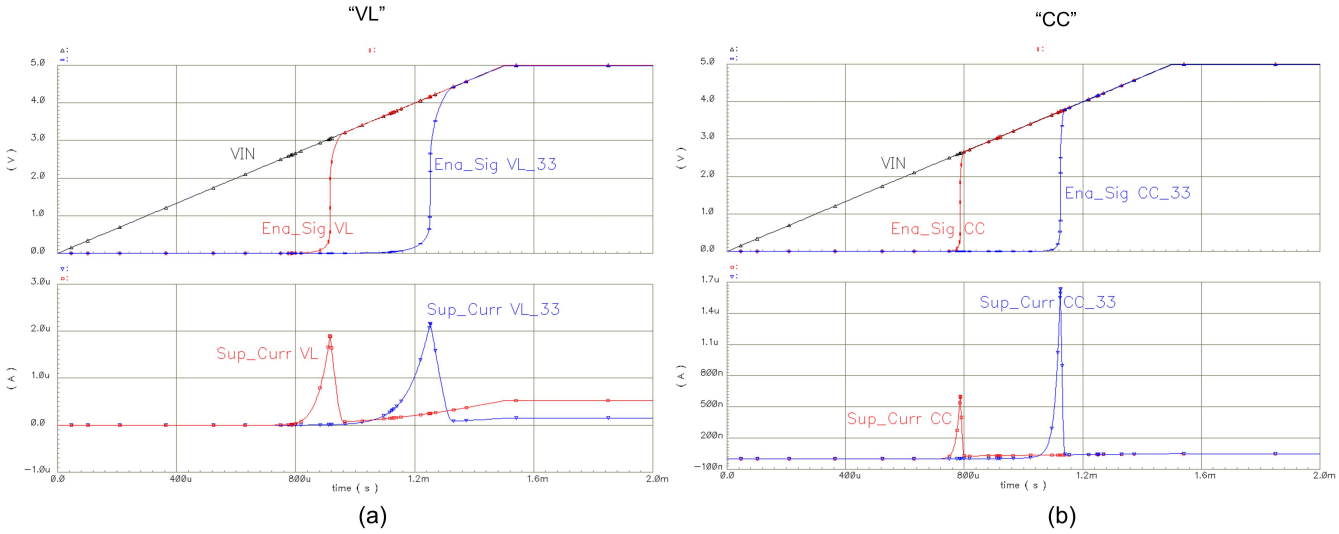

Fig. 8. VIN, Enable Signal and Current consumption versus time after post–layout simulations. (a) VL and VL_33 structures, and (b) CC and CC_33 structures.

[6], [8], the average current of our circuits is one order of magnitude lower. We used a 0.35 μm CMOS process from XFAB. The peak current is lower than 2 μA.

In addition, we have proposed some modifications of the best published results [8] and [6]. Our modified version of MMS has a power consumption of one order of magnitude less than the original MMS [8], implemented in XFAB technology.

Finally, the adjustability of the proposed voltage-sensor circuits was verified in postlayout simulations.

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REFERENCES

[1] K. Finkenzeller, *RFID Handbook, Radio–Frequency Identifications Fundamentals and applications,* 2nd ed. New York: Wiley, 2003.

[2] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponders IC with 16.7-μW minimun RF input power," *IEEE J. Solid-State Circuits*, vol. 38, no. 10, pages 1602–1608, Oct. 2003.

[3] G. De Vita and G. Iannaccone, "Ultra Low Power RF Section of a Passive Microwave RFID Transponderin 0.35 μm BiCMOS," in *IEEE Int. Symp. Circuits Systems (ISCAS 2005)*, Kobe, Japan, May 2005.

[4] U. Kaiser and W Steinhagen "A Low–Power Transponder IC for High-Performance Identification Systems," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pages 306–310, Mar. 1995.

[5] F. Kocer, P. M. Walsh and M. P. Flynn, "Wireless remotely powered telemetry in 0.25 μm CMOS," in *IEEE Radio Frequency Integrated Circuits(RFIC) Symp.*, pages 339–342, Jun. 2004.

[6] J.-P. Curty, N. Joehl, C. Dehollain and M. J. Declercq, "Remotely Powered Addressable UHF RFID Integrated System," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pages 2193–2202, Nov. 2005.

[7] EPC Tag Data Standards Version 1.1 Rev. 1.27, (2005, May), [Online] Avalible: http://www.epcglobalinc.org/standards_technology/specifications.html.

[8] F. Kocer and M. P. Flynn, "A Long-Range RFID IC with On–chip ADC in 0.25 μm CMOS," in *IEEE Radio Frequency Integrated Circuits(RFIC) Symp.*, pages 361–364, Jun. 2005.

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Design Criteria for Full Passive Long Range UHF RFID Sensor for Human Body Temperature Monitoring

Daniel Pardo, Alexander Vaz, Santiago Gil[1], Josean Gómez, Aritz Ubarretxena, David Puente[1]
Ricardo Morales-Ramos[2], Andrés García-Alonso *Member IEEE*, Roc Berenguer, *Member IEEE*

***Abstract*—Although the insertion of a sensor in a full passive UHF RFID tag for long range is a challenge itself, the main goals of this paper are discussing the real constraints of RFID tags and providing the design criteria to optimize the different blocks in order to achieve long distances. The design has been focused on the matching network, the voltage multiplier, the ASK demodulator, the load modulator and the temperature sensor. The numerical results have been obtained using 0.35μm technology from XFAB (XL035) and operating at the 868MHz ISM Europe band.**

I. Introduction

Radio Frequency Identification (RFID) is a widespread used technology that allows wireless communication between a reader and a tag [1]. Although the reader is an active component, the tag can be active, semiactive or passive. In a full passive tag, the RF signal transmitted by the reader is not only used to establish communication between both terminals, but also to supply the energy that the tag requires.

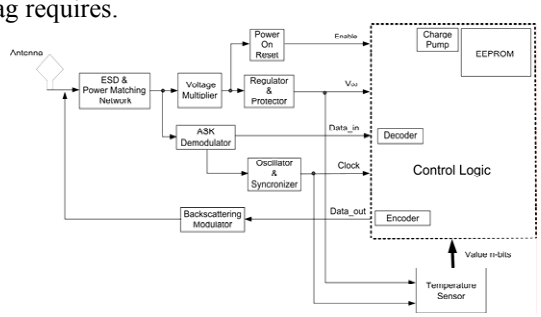

Fig. 1. Block diagram of a full passive RFID tag with a temperature sensor incorporated.

As Fig. 1 shows, the wave sent by the reader is captured by the tag antenna, which is a bent dipole. A matching network is implemented after the antenna in order to provide maximum power transference and to increase the peak voltage of the incoming signal. The voltage multiplier is in charge of rectifying the incoming signal and of raising the voltage level. In order to minimize the power consumption, a voltage sensor is implemented. The rest of the analog blocks are not switched on until the supply capacitor reaches a minimum voltage. The last one provides the necessary energy for the operation of the whole tag. Once the *enable* signal is active, the digital logic may process the data given by the ASK demodulator. As the whole tag, especially the digital logic and the sensor, performs better with a stable supply signal, a voltage regulator has also been implemented.

Furthermore, the sensor sends the temperature value to the digital logic, where it is processed and sent to the load modulator. This is the block in charge of backscattering information from tag to reader. EPCGlobal Gen2 is the chosen standard for the communication between the reader and the tag [2].

Long range tags have been reported previously [3], [4]. That information has been used as a reference for the development of the present work. Despite of this, current RFID sensors have not achieved communication distances higher than few cm [5], [6]. This paper encloses the challenge of including a low power temperature sensor in a passive long range UHF RFID tag.

In section II, the main constraints of the system will be described. Sections III and IV will explain the design of the analog blocks and the temperature sensor according to the system constraints. Section V will show the Layout of the chip and finally, Section VI and VII will show the achieved results and conclusions.

II. System Constraints

In the present section, three main limitations involving maximum communication distance between tag and reader are presented. Two limitations are given for the reader-to-tag link and another one for the tag-to-reader link.

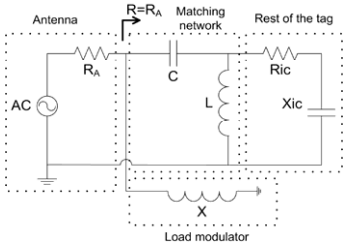

Fig. 2. Equivalent circuit for the whole RFID tag.

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The authors are with the Radio Frequency Integrated Circuits Group, Department of Electronics and Communications, Centro de Estudios e Investigaciones Técnicas de Gipuzkoa (CEIT) and Technological Campus, University of Navarra (Tecnun), 20018 San Sebastián, Spain.

[1] S. Gil and D. Puente are with TECNUN(University of Navarra), Spain.

[2] R. Morales is with Institute for Applied Microelectronics (University of Las Palmas de Gran Canaria), Spain

A. Previous definitions

1) Power available at the input of the tag antenna

$$P_{AV} = SA_{ef} = \frac{P_{EIRP}}{4\pi r^2}\frac{\lambda^2}{4\pi}G \quad (1)$$

Where G is the tag antenna gain, r is the distance between the reader and the tag, λ is the wavelength and P_{EIRP} is the Effective Isotropic Radiated Power.

2) Input power [4]

$$P_{RFin} = P_{AV}\left(1-|\rho|^2\right) = P_{AV}\frac{4X^2}{R_A^2+4X^2} \quad (2)$$

Where ρ is the reflection coefficient, R_A is the impedance of the antenna and X is the reactance introduced by the load modulator as Fig. 2 shows.

3) Backscattered power [4]

$$P_{BS} = P_{AV}\frac{4\left(R_A^2+X^2\right)}{R_A^2+4X^2} \quad (3)$$

4) Quality factor

$$Q = \frac{X_{IC}}{R_{IC}} \quad (4)$$

Where R_{IC} and X_{IC} are the components of the complex impedance of the whole integrated (Fig. 2).

B. Forward link constraints (Reader → Tag)

1) Minimum input power

The reader feeds the tag with a continuous wave. The incident power must be enough to afford the whole power consumption of all the analog and digital blocks of the tag. Equation (5) provides a relation between power consumption and maximum range [4].

$$P_{AV}\frac{4X^2}{R_A^2+4X^2} \geq \frac{1}{\eta}\left(P_{ANA}+P_{DIG}\right) \quad (5)$$

Where P_{ANA} and P_{DIG} are the power consumption of the analog and digital blocks respectively; and η is the efficiency of the rectifier circuit.

From (5), and considering free space power losses, the communication range is given by:

$$r_P \leq \sqrt{\frac{P_{EIRP}\lambda^2 G X^2 \eta}{4\pi^2\left(R_A^2+4X^2\right)\left(P_{ANA}+P_{DIG}\right)}} \quad (6)$$

From (6), for a given P_{AV}, an increment on the efficiency implies an increment on the communication range. This fact should be taken into account on the design of the voltage multiplier, which is the most influent block in the efficiency. Besides, also from (6), if (P_{ANA}+P_{DIG}) increases, r_p decreases. So the minimization of the power consumption of the analog and digital blocks is mandatory in order to achieve longer communication distances.

2) Minimum voltage at the input of the voltage multiplier

Not only a minimum input power is necessary at the tag antenna. It is also necessary a minimum voltage swing at the input of the voltage multiplier. This will allow to perform properly, with good efficiency and be able to achieve the required supply voltage both for analog and digital circuits at its output.

The circuit shown in Fig. 3 is obtained from the one shown in Fig. 2, where:

$$R_P = R_{IC}\left(Q^2+1\right) \quad (7)$$

The quality factor of the matching network (Fig. 3) is defined as:

$$Q_{mn} = \sqrt{\frac{R_P}{R_A}-1} \quad (8)$$

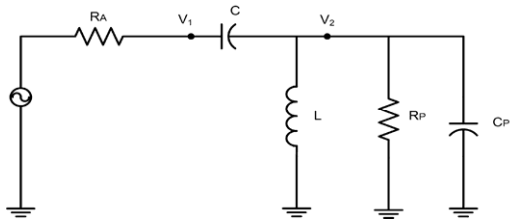

Fig. 3. Serial to parallel transformation of the input impedance of the tag (without the matching network).

From Fig. 3, (9) can be deduced:

$$\frac{V_2}{V_1} = \frac{1}{1-\frac{j}{R_P C\omega}-\frac{1}{LC\omega^2}+\frac{C_P}{C}} \quad (9)$$

Where V_1 and V_2 are respectively the voltage at the input and the output of the matching network.

In Fig. 3, R_P and C_P are the equivalent parallel values of R_{IC} and X_{IC} of Fig. 2. L and C are the values of components of the matching network.

As Fig. 3 shows, the whole tag can be simplified as a voltage source and a real impedance (antenna) followed by a complex impedance (rest of the tag). A matching network has been implemented in order to provide maximum power transference which implies an increase of the circuit efficiency. Additionally, an increment of the voltage is also produced. The voltage is multiplied by the quality factor of the matching network as (10) shows.

$$\frac{V_2}{V_1} \cong 0.7xQ_{mn} \quad (10)$$

Equation (10) is valid whenever R_P is much bigger than R_A. Anyway, it is quite a restrictive simplification. Besides, it is multiplied by 0.7 in order to make it more restrictive.

If a matching condition is achieved ($R=R_A$), then:

$$V_1 = \sqrt{P_{AV}R_A} \quad (11)$$

From (1), (2) and (11), the range can be calculated as:

$$r_V = \frac{0.7Q_{mn}\lambda\sqrt{P_{eirp}GR_A}}{4\pi V_{\min}} \quad (12)$$

Equation (12) provides the relation between the necessary voltage at the output of the voltage multiplier ($V_2 > V_{min}$) and the distance between tag and reader. An increment of V_{min} implies a reduction of the communication range. So a

minimum V_{min} is desired. But this parameter depends on the used technology.

This constraint is not usually included in the system analysis of the RFID bibliography, although it could be the limitation of the maximum achievable distance.

C. Backward link constraint (Tag → Reader)

1) Maximum Probability of error at the input of the reader

The backward link is performed using a BPSK (Binary Phase Shift Keying modulation). For a BPSK receiver architecture, the probability of error can be calculated from the analysis of its constellation (Fig. 4) as:

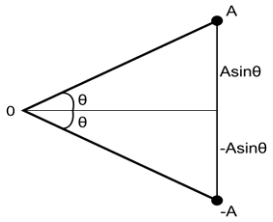

Fig. 4. BPSK constellation.

$$Pe = Q(\frac{d}{2\sigma}) = Q(\frac{2A\sin(\theta)}{2\sigma}) = \frac{1}{2}erfc(\frac{A\sin\theta}{\sqrt{2}\sigma})$$

$$P_e = \frac{1}{2}\left\{erfc\left[\frac{A\sin(\theta)}{\sqrt{2\sigma}}\right]\right\} \quad (13)$$

Where σ is the standard deviation of the noise, A is the amplitude of the backscattered signal and θ is the phase of the signal.

Equation (13) does not accurately represent the real value of the probability of error because it does not take into account neither the phase noise nor the thermal noise. Equation (14) gives a more accurate value for the probability of error [4]:

$$P_e = \frac{1}{2}\left\{erf\left(\frac{A\sin(\theta)(2\cos(\varphi)-1)}{2\sigma}\right)erf\left(\frac{A\sin(\theta)}{2\sigma}\right)\right\} \le 10^{-3} \quad (14)$$

Where φ is the phase noise related term.

The value of 10^{-3} is considered enough to achieve an appropriate communication.

The following section will show the design of the main analog blocks of the tag.

III. Analog Block Design

A. Matching Network and Voltage Multiplier

The goal of the voltage multiplier (VM) circuit is to charge the supply capacitor with an output voltage determined by the technology. This capacitor will supply the necessary energy to the rest of the tag. As it has been mentioned in Section II, high efficiency and Q are desired in order to achieve higher distances. See (6) and (12).

Modified Dickson Topology (Fig. 5) has been selected because high multiplication factors can be reached with high substrate capacitance, typical of integrated circuits. While other topologies are too complex for RFID systems and its multiplication factors are smaller [7].

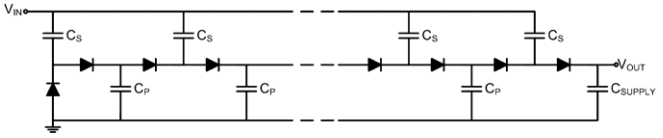

Fig. 5. N-stage Modified Dickson Topology with the supply capacitor connected.

Using the modified Dickson Topology, the output voltage can be obtained with the following formula:

$$V_{OUT} = K_N N (V_{IN} - V_{fwr}) \quad (15)$$

Where V_{OUT} is the output voltage, V_{fwr} is the voltage drop on the diodes, V_{IN} is the voltage at the input of the multiplier, N is the number of stages and K_N is a constant dependant on the number of stages ($K_N \approx 2$).

A low V_{fwr} value is desired in order to obtain a high value of V_{OUT} with minimum V_{IN}. This can be implemented using Schottky diodes in the voltage multiplier design [3].

For RFID human body temperature monitoring, usually, long reading distances are required, so the whole tag has to be optimized in order to achieve the maximum communication range as explained in Section II. Although both the voltage multiplier and the ASK demodulator are connected directly to the matching network output, the voltage multiplier impedance is much smaller than the ASK demodulator. So, as explained in Section II, input impedance of voltage multiplier is critical. Therefore, the voltage multiplier is decisive in order to achieve longer distances.

The limitations that depend on the voltage multiplier are given by (6) and (12). The optimization of the voltage multiplier depends on the most critical of both constraints. In the voltage multiplier design, different parameters will be optimized depending on which constraint is the real limitation. In some cases, higher r_p will be required and in others r_v is the real limitation that has to be increased. So a classification based on the different constraints can be made:

1) If the Power constraint is critical ($r_p < r_v$)

Two alternatives are given in order to obtain higher r_p. The first one is obtaining lower power consumption of the analog and digital blocks. This is a task to be performed by digital and analog designers [4].

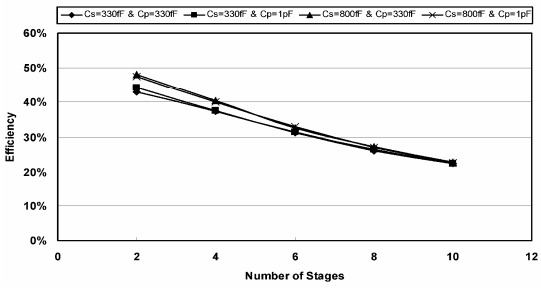

Fig. 6. Efficiency of the matching network and the voltage multiplier versus the number of stages for different C_S and C_P.

The second choice deals with the design of the voltage

multiplier itself. It consists on increasing conversion efficiency. As Fig. 6 shows, in order to obtain higher efficiency, a minimum number of stages is desired.

The main reason of this increase is that the Q of the input impedance is also increased (see Fig. 10 and Fig. 11), and so Q_{MN}. Therefore, a matching network with higher Q_{MN} entails higher V_2. With higher input voltage at the voltage multiplier, the diode performs better and so, its efficiency is much higher.

Furthermore, to obtain the maximum efficiency, it is important to use the optimum diode area. Higher area means lower forward voltage (and higher V_{OUT}). But on the other hand higher losses to substrate are obtained. Thus, a compromise to obtain the optimum diode area should be achieved.

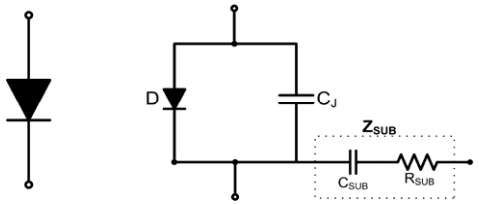

Fig. 7. Equivalent circuit of the Schottky diode.

2) If the Voltage constraint is critical ($r_v<r_p$)

From (10) and (11), the output voltage of the matching network can be defined as:

$$V_2 \cong 0{,}7 Q_{MN} \sqrt{P_{AV} R_A} \tag{13}$$

So, using (8) in (13):

$$V_2 \cong 0.7 \sqrt{P_{AV} \left(R_P - R_A\right)} \tag{14}$$

As it has been mentioned before, higher input voltage at the voltage multiplier (V_2) is desired. To achieve this goal, (14) shows that the antenna impedance has to be minimized and R_P maximized (7). Therefore, both R_{IC} and Q have to be maximized.

As Fig. 8 and Fig. 9 show, a minimum number of stages and a low C_S value are required to maximize R_{IC}. Each stage is connected in parallel so the input impedance decreases when a new stage is added. High C_S values mean lower impedance and so, as C_S capacitors are connected in parallel, the input impedance is also reduced.

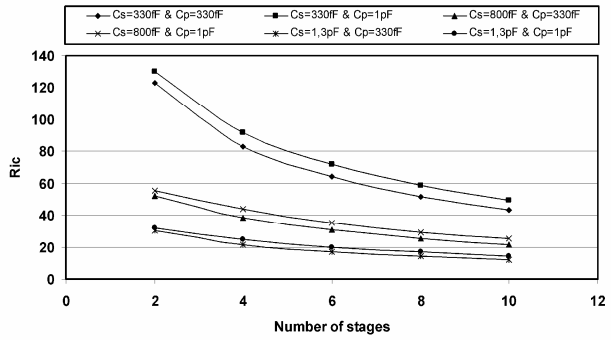

Fig. 8. R_{IC} Vs the number of stages for different C_S and C_P.

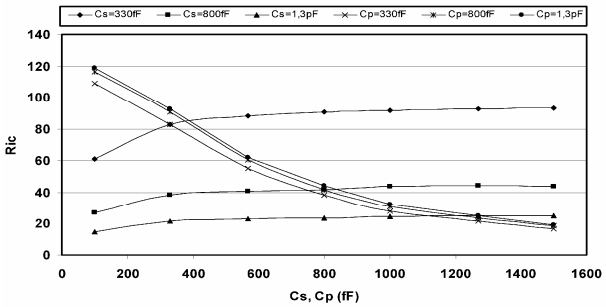

Fig. 9. Variation of R_{IC} for different C_S and C_P in a 4 stage VM.

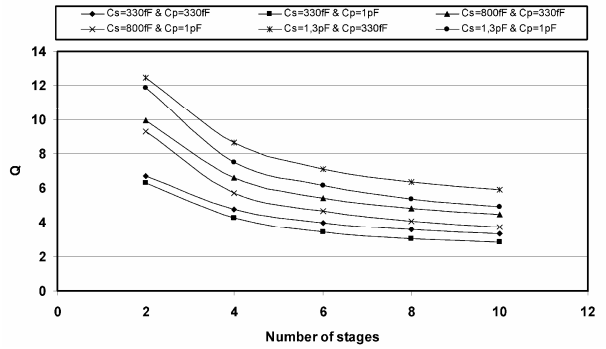

Fig. 10. Q Vs the number of stages for different C_S and C_P.

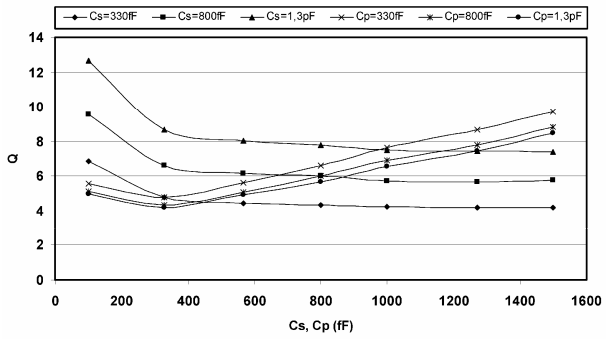

Fig. 11. Variation of Q for different C_S and C_P in a 4 stage VM.

Fig. 10 and Fig. 11 show that a minimum number of stages, high C_S value and low C_P value are required to obtain a higher Q. In consequence, R_P is maximized if the minimum of stages and low C_P value are used. So, a trade off between high and low C_S in order to achieve higher Q or R_{IC} is requested (see Fig. 9 and Fig. 11).

Besides, the input impedance of the matching network varies with the input power: diodes perform worse (the efficiency decreases) and the input impedance varies slightly. As the matching network assures the maximum power transference at a fixed load, if the load suffers a variation on its impedance, a mismatch between both blocks is generated and so power losses are obtained. Therefore, lower efficiency is achieved.

In order to obtain the optimum power transference, the following steps have to be followed:

- Determine the minimum input voltage (V_{min}) necessary for the correct performance of the tag without the

matching network.

- Calculate the input impedance.
- Calculate the matching network to obtain the maximum power transference between the antenna and the tag.

This methodology guarantees the correct performance of the tag for the maximum distance. Shorter distances entail higher input power at the tag, which produces a variation of the input impedance of the tag. Therefore, a mismatching between the antenna and the tag is obtained. But power losses are widely compensated with the increase of the input power.

Both constraints demand to use a minimum number of stages, but they have to be set taking into account the input power (that the matching network transforms in input voltage) and the output voltage that is necessary to be achieved (as (15) and Fig. 12 show). Besides, there is a minimum value for Cp and Cs in order to guarantee the power transference between stages.

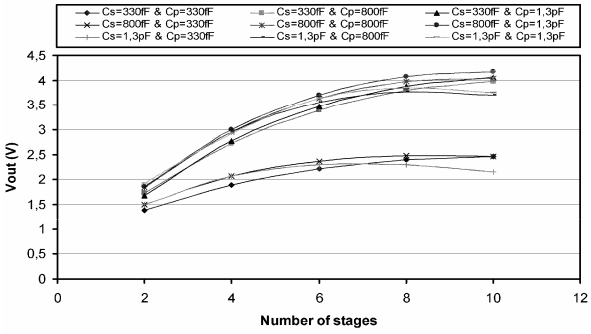

Fig. 12. V_{OUT} Vs the number of stages for different C_S and C_P.

So, depending on which one is the constraint, r_v or r_p, C_S and C_P have to be determined. Also, the number of stages has to be established in order to achieve the determined voltage, taking into account that a minimum number of stages is desired.

B. ASK Demodulator

The demodulator is an important block of a RFID tag. It demodulates the information of the ASK modulated incoming signal and delivers the data to the digital part. The presented demodulator has been optimized for minimum power consumption and to work at both, short and long distances. The architecture of the ASK demodulator is shown in Fig. 13.

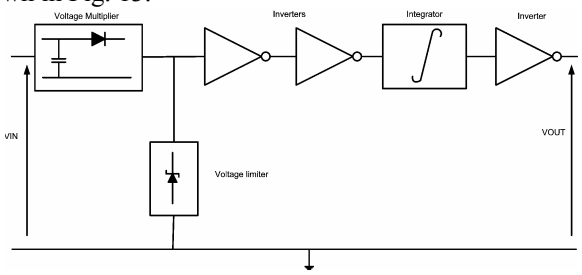

Fig. 13. Architecture of the ASK demodulator.

The voltage multiplier provides multiplication and rectification of the incoming signal. It is based on a modified Dickson topology which performs the multiplication and rectification operations.

Two inverters obtain a rectangular signal. This signal is integrated by a very simple integrator architecture which is based on a resistor and a capacitor. The result is finally compared by an inverter.

The integrator circuit is shown in Fig. 14. The resistor will limit the current charging the capacitor and will set the time constant for the integration operation, which is performed by the capacitor. The NMOS transistor and the inverter reset the circuit for every arriving bit. When a pulse is received, it is integrated while the NMOS transistor remains under cut-off conditions. When the integration ends, the switch is closed and connects the capacitor to ground resetting the integrator.

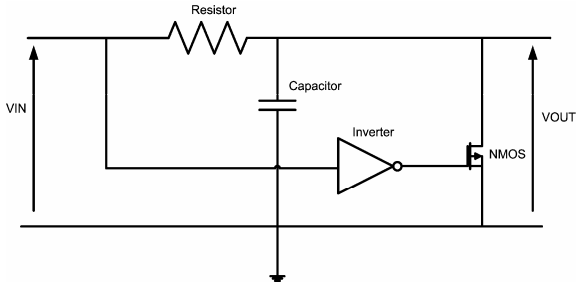

Fig. 14. Architecture of the Integrator.

A voltage limiter has been added. It allows short and long distance operation. The main function is to protect the circuit against high voltages that could exceed limit operation voltages. This happens when the tag and the reader are close. The voltage is limited to 4.5V.

The outputs provided by the demodulator are the demodulated bit stream and the clock. The output bit stream presents transitions from '1' to '0' when bit '1' is transmitted and remains constant when bit '0' is detected. The demodulator also provides an asynchronous clock signal where each arising edge denotes the arrival of a new bit. Every arising edge of the clock signal denotes the arrival of a new bit. This signal is also used to reset the integrator.

The performance of the demodulator as a part of the full analog block of a RFID tag is shown from Fig. 18 to Fig. 20.

C. Load modulator

There are two modulation alternatives allowed by EPC Global Gen2 standard for RFID backscattering communication [2]:

- Amplitude Shift Keying (ASK)
- Phase Shift Keying (PSK)

Both ASK and PSK modulate the load complex value, but in a different way. For ASK the real part of the input impedance is changed, so the backscattered wave amplitude is modulated. In PSK cases the phase of the backscattering wave is modulated changing the imaginary part of the input

impedance.

As it is demonstrated in [3] and [4], PSK modulation is more efficient than ASK. Thus, it is the modulation used for the load modulator.

In PSK modulation the imaginary part of the reflection coefficient must change in the same magnitude and opposite signs. According to this requirement, only phase changes and no amplitude variations between states should occur.

As it is shown in Fig. 1 and Fig. 15, the load modulator is located between the tag antenna and the rest of the analog system. The antenna is simulated as a sinusoidal source, which represents the power captured by the antenna, and a resistor, which represents its impedance.

In the tag, the PSK modulator receives the data from the digital logic and has to convert these bits into phase variations which are sent to the antenna at a frequency of 868MHz. A matching inductor will be used to centre both impedances in the Smith chart. In this way, the imaginary part changes symmetrically at the chart, when the states from the digital logic change. Thus, the phase will also change symmetrically (±φ) and no amplitude variations will be generated.

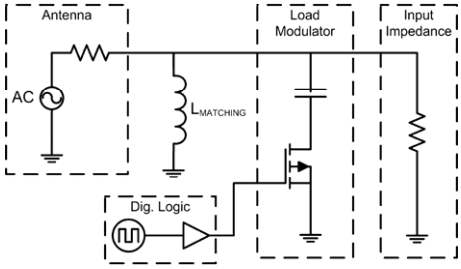

Fig. 15. Location and architecture of the load modulator.

This topology is composed by a switch which connects and disconnects a capacitor. Thus, the imaginary impedance of the system is changed and a phase difference is achieved. In order to maintain the real input impedance constant, the switch must have a low parasitic resistance when its state is on. This is achieved using a transistor with a large channel width.

If higher phase difference is required, the capacitor has to be increased. But this causes higher power and area consumption. Besides, the channel width of the switch has to be also increased, because the parasite capacitance is connected in series with the capacitor. So a trade off between the phase difference and consumption is necessary. In fact, a very low power consumption can be easily achieved.

IV. Temperature Sensor

A temperature sensor has been implemented in the RFID tag. As the chosen application is the human body temperature monitoring, the sensor works in the range of 30º to 50ºC, although it can work with higher temperatures. The architecture is shown in Fig. 16. It is composed by a Proportional To Absolute Temperature (PTAT) circuit which provides a voltage slope (V_{PTAT}) given by a capacitor, charged by a constant current source (I_{DC}). A voltage reference circuit has been added in order to provide a constant voltage (V_{CP}) for a certain temperature.

The voltage achieved in the capacitor (V_{CP}) is compared with V_{PTAT}. The output signal of the comparator is multiplied by the clock signal in order to obtain a proportional number of pulses according to the temperature. This data is transmitted to digital logic where the pulses are counted.

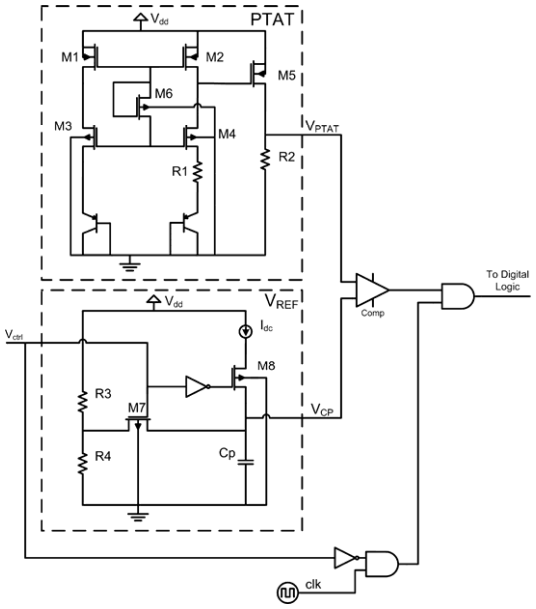

Fig. 16. Architecture of the temperature sensor.

The PTAT circuit consists of a current mirror connected to two bipolar transistors, which cause the dependence with the temperature. The voltage reference is obtained with the charge of a capacitor. A control signal (V_{ctrl}) has been included in order to reset the voltage of the capacitor. Instead of charging the capacitor from 0V every time is reset, a voltage divider is added so V_{CP} is reset at a certain voltage in order to minimize the power consumption. This is the function of R3 and R4 (high value resistors), M7, M8 and the inverter.

Besides, in order to achieve less power consumption, the clock signal turns on only when V_{ctrl} is activated.

V. Layout

As it has been mentioned in the abstract, XL035 is the technology used for this design. Fig. 17 shows the front-end of a full passive long range RFID tag with pads.

The different blocks that can be appreciated in the figure are the ASK demodulator, the voltage multiplier (VM), the power on reset (POR), the voltage regulators, the voltage limiter (it is too small to appreciate in the figure), the load modulator and the supply capacitor.

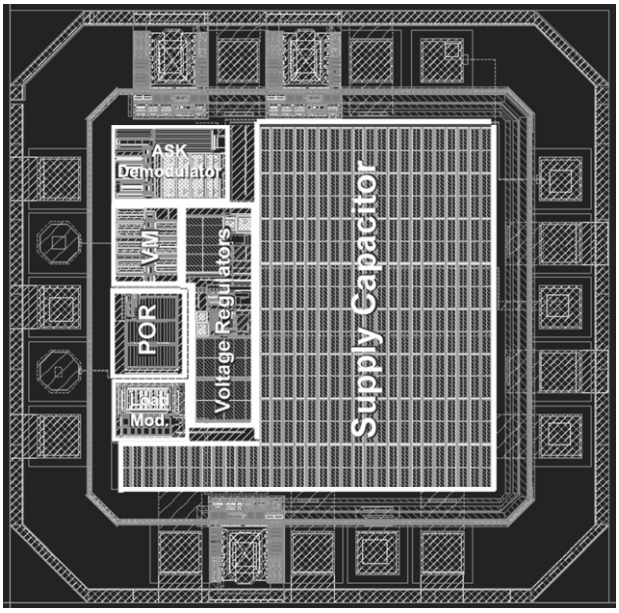

Fig. 17. Layout of the RFID tag front-end with pads.

Notice that most of the area of this chip is occupied by the supply capacitor. The value of this capacitor (C=1.2nF) needs to be high in order to support the consumption of the rest of the tag, including the EEPROM.

VI. RESULTS

A four stage voltage multiplier has been implemented with C_S=800fF and C_P=1pF. The optimum size of the Schottky diode is 8pm^2 for this particular design. These values have been chosen because the main limitation of the system is the voltage constraint (r_v<r_p).

The optimum values of the load modulator for the present design are:

- Capacitor: 2.125pF
- Switch: W=665µm and L=0.35µm
- $L_{MATCHING}$=16.5nH

These parameters have been chosen in order to obtain the highest phase difference (in degrees) and the lowest power consumption. The area occupied by the components has also been considered.

Fig. 18 to Fig. 20 show the results that have been achieved for the different blocks of the tag. Notice that in Fig. 18 the supply capacitor achieves the determined voltage in less time than the charging time specification of the EPC standard (80µs versus 1.5ms). Lower input power entails higher charging time. It is interesting to point out the reduction of the supply voltage due to a low state of each bit of the ASK modulated signal is received by the tag (the incoming energy is smaller than the consumption of the whole tag). Although in this case the voltage supply is increased rapidly, for higher distances this effect could be a problem. Thus, a higher value for C_{SUPPLY} is needed. A higher value of the capacitor will cause longer charging time. So a trade off between C_{SUPPLY}, the area occupied and the charging time (that has to be lower than 1.5ms) is required.

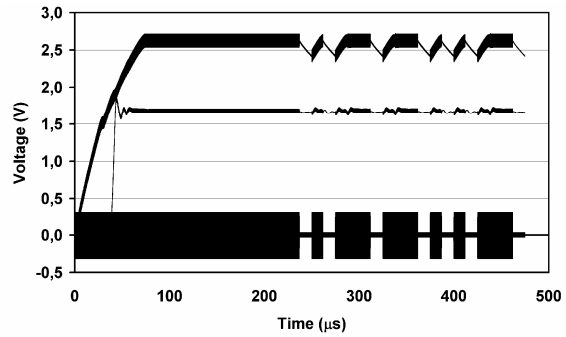

Fig. 18. Results of the charge capacitor, the voltage regulator and the input voltage.

The POR circuit activates the rest of the tag when the supply voltage reaches a determined value. Then, the voltage regulators supplies two different stable voltage: for the digital logic, the sensor and the rest of the front-end blocks.

As Fig. 19 and Fig. 20 show, the ASK demodulator performs correctly, as it has been explained in Section III. B.

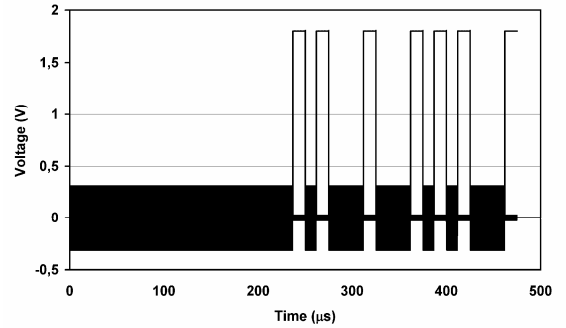

Fig. 19. RF_{IN} and Clock signal extracted by the ASK demodulator.

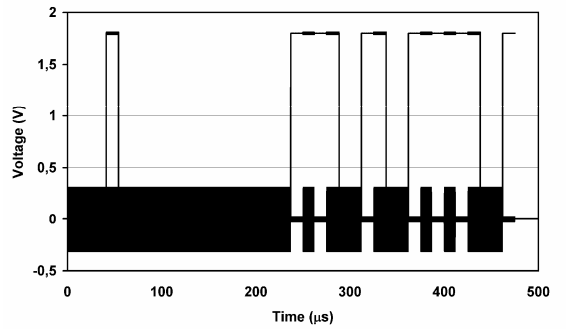

Fig. 20. RF_{IN} and demodulator output signal. Notice that the first pulse is due to the activation of the voltage regulator and so the ASK demodulator. The digital logic ignores this pulse because the clock signals remains in 0V.

Results are presented leading to a demodulator which operates at 868MHz and consumes less than 0.6µA, as it is shown in Table I. This low current consumption makes the use of this demodulator very suitable for RFID tags.

The S_{11} variation is shown in the Fig. 21.

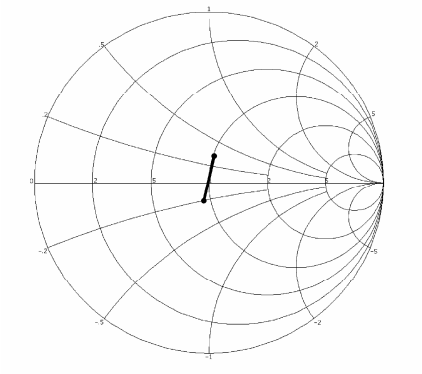

Fig. 21. Smith Chart of the S_{11}.

Finally, the results achieved in the temperature sensor are shown in Fig. 22. This results are a very low power consumption (0.22µW for 10 samples per second) and a linear relation between the number of pulses and the temperature (as show in Fig. 18, R^2=0.9993). This temperature sensor has been designed for a resolution of 0.1ºC. So it is verified that this tag performs correctly for human body temperature monitoring.

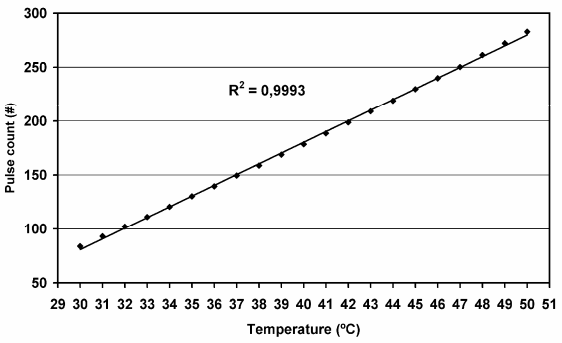

Fig. 22. Behaviour of the temperature sensor.

The results of the full chip are summarized in table I.

TABLE I
UHF RFID TAG RESULTS

Parameter	Value
C_{SUPPLY}	1.2nF
T_{CHARGE}	80µs
Voltage Regulators	1.6V and 2.2V
Phase difference	15º
Open state impedance	46.7+14j
Closed state impedance	44.4-14j
Temperature range	30º to 50ºC
Temperature resolution	0.1ºC
Linearity (R^2)	0.9993
ASK demodulator consumption	0.6µA
Load Modulator consumption	0.27µA
Power consumption (P_{ANA}+P_{DIG})	25µW
Temperature sensor consumption (10 samples/sec)	0.22µW

VII. CONCLUSION

This paper has presented a full passive long range UHF RFID sensor for human body temperature monitoring. With the results showed in Section VI, the achieved communication range is higher than 3 meters for 868MHz European ISM band (which allows 2W of power transmission).

It should be mentioned that the real limitation has been the voltage constraint whereas previous publications have focused on the power and probability of error constraints.

ACKNOWLEDGMENT

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REFERENCES

[1] K. Finkenzeller, *RFID Handbook: Fundamentals and Applications in Contactless Smart Cards and Identification*, 2nd ed. New York: Wiley, 1999, pp. 7-9, 29-53, 117-126, 182-185

[2] Specification for RFID air interface. EPC Global Class-1 Gen-2 UHF RFID Version 1.0.9. Available: http://www.epcglobalinc.org/standards/Class_1_Generation_2_UHF_Air_Interface_Protocol_Standard_Version_1.0.9.pdf

[3] U. Karthaus and M. Fischer, "Fully integrated passive UHF RFID transponder IC with 16.7-µm minimum RF input power" IEEE J. Solid-State Circuits, vol. 38, no. 10, pp. 1602-1608, Oct. 2003.

[4] G. De Vita and G. Iannaccone, "Design criteria for the RF section of UHF and microwave passive RFID transponders" IEEE Trans. Microw. Theory Tech., vol. 53, no. 9, pp. 2985-2989, Sep. 2005

[5] Opasjumruskit, K.; Thanthipwan, T.; Sathusen, O.; Sirinamarattana, P.; Gadmanee, P.; Pootarapan, E.; Wongkomet, N.; Thanachayanont, A.; Thamsirianunt, M., "Self-powered wireless temperature sensors exploit RFID technology", Pervasive Computing, IEEE,Vol. 5, Issue 1, pp. 54–61, Jan.-March 2006

[6] F. Kocer, M.P.Flynn, "A new transponder architecture for long-range telemetry applications", vol. 2, pp.177-180 European Conf. Circuit Theory and Design (ECCTD), 2005. Aug.-Sept. 2005

[7] Dickson, J.F. "On-chip high-voltage generation in NMOS integrated circuits using an improved voltage multiplier technique", Solid-State Circuits, IEEE Journal. Vol. 11, Issue 3, pp. 374-378, Jun. 1976

[8] B. Jamali, D. C. Ranasinghe, P. H. Cole. "Analysis of a UHF RFID CMOS rectifier structure and input impedance characteristics" School of Electrical & Electronic Engineering, Univ. of Adelaide, Aus. Dec. 2005

[9] Z. Zhu, B. Jamali, P.H. Cole, "Brief comparison of different rectifier structures for RFID transponders" Auto-ID Labs Adelaide report, 2004.

Optimal Impedance Matching in Passive UHF RFID Sensors

Ricardo Morales–Ramos, IUMA (University of Las Palmas de G.C.), Las Palmas de G.C., Spain
David Puente, TECNUN (University of Navarra), San Sebastian, Spain
Heinrich Milosiu, Fraunhofer Institute for Integrated Circuits, Erlangen, Germany
Roc Berenguer, Centro de Estudios e Investigaciones Técnicas de Guipúzcoa (C.E.I.T.), San Sebastian, Spain
Juan Antonio Montiel–Nelson, IUMA (University of Las Palmas de G.C.), Las Palmas de G.C., Spain

Abstract

This paper proposes a method for optimal impedance matching in passive UHF RFID Sensors. The voltage multiplier (VM) is a key subsystem in power recovery circuits. Both its impedance and operation range are optimized. The proposed method evaluates each VM under the same load conditions, thus it can be also used as a comparison tool for different VM structures.

1 Introduction

UHF RFID passive wireless sensors do not require extra supply batteries to operate, they are fed up by the same RF–wave used for communications purposes. In addition, the RFID transponder is integrated into the same chip as the sensor, thus reducing the dimension and cost of the wireless sensor.
Fig. 1 shows the typical architecture of a passive UHF RFID sensor architecture, and remarks the location of the power recovery system.

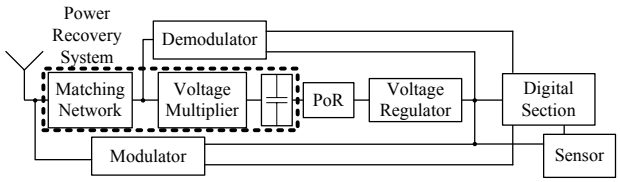

Figure 1 Power recovery system inside the passive UHF RFID sensor architecture.

The power recovery system of a UHF passive RFID is composed by the antenna, the matching network, the supply capacitor and the Voltage Multiplier (VM), as shown in Fig. 1. The interrogator (also called reader) transmits the RF signal at the resonant frequency of the tag antenna. The input power in the tag antenna is transferred to the VM using a matching network for maximum power transfer. The VM converts RF into DC power to supply the chip. The DC voltage at the output of the VM charges a high value integrated capacitor (around 1 nF). The supply capacitor stores energy for maintaining the supply voltage of the system, when short absences of the RF input power are produced, or when a high value current peak is required for the system.

As the radiated RF power decreases with the distance, the power recovery system must be as efficient as possible, in order to achieve the largest range. Here are two aims: the meticulous design of the VM [2, 1] and the reduction of the mismatching reflections. This paper includes the analysis of the VM behaviour (RF and DC) to obtain the its input impedance. An algorithm is proposed to find the optimal input impedance to match and the maximal range of the UHF RFID passive wireless sensor, for a given VM.
Section 2 introduces the RF and DC behaviour of the VM and the influence on each other. The proposed algorithm is presented in Section 3. Finally, results and conclusions are described in Sections 4 and 5, respectively.

2 Power recovery system overview

The Voltage Multiplier (VM) converts the received RF signal into a DC voltage for the power supply of the transponder. So the VM is studied from both sides, RF and DC.

2.1 VM as a DC source

The VM and the supply capacitor consitute a DC voltage source. This voltage source must meet the power requirements of the wireless sensor during the whole link time between reader and tag. This time is defined in the standard EPCglobal2 [4], which also defines the communication protocol adopted in the system. Fig. 2 shows the link timing between reader and tag adapted to the wireless sensor.
Table 1 shows the power requirements (based on a 0.35μm 2P4M CMOS process) of each operation mode, which must be fulfilled by the supply chain. The chip operates in three different modes, the first mode is the *power up* of the RFID transponder. During it, the current consumption is minimal to speed up the charge of the supply capacitor. The power up ends when the voltage on the capacitor achieves the minimal voltage required for a proper chip operation. A voltage sensor [5] senses the charge of the capacitor and generates the Power-On-Reset signal, which activates the analog and digital circuits (*Active* mode). When the transponder receives the order of measure, the operation mode is switched to *Measure*. In this mode, the current

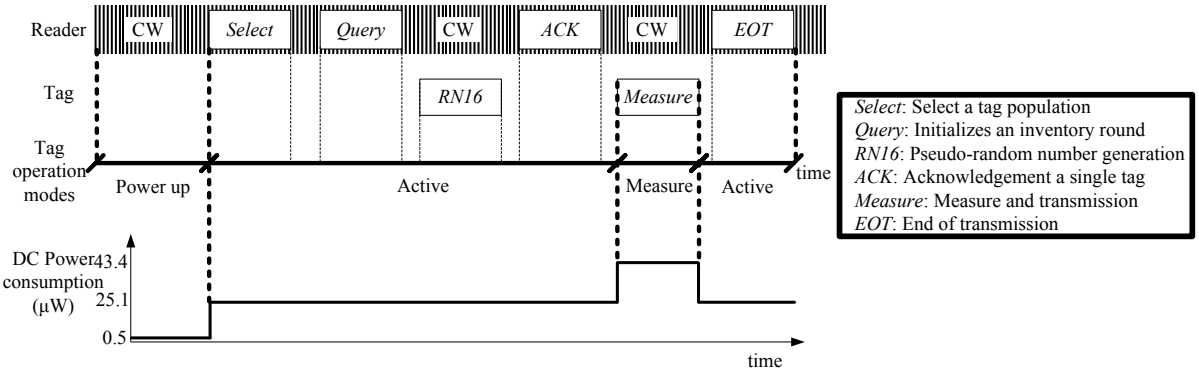

Figure 2 Link timing between reader and interrogator as described in the standard EPC global2.

Table 1 RFID sensor chip power requirements

Operation Mode	*Active Blocks*	*DC Power Requirements*	*Current Peaks*	*time* (ms)
Power up	*Voltage S.*	200 nA @ 2.5 V		1.5
Active	*Analog and Digital*	3 μA @ 1.2 V 12 μA @ 1.8 V	200 μA	2.1
Measure	*Analog, Digital and Sensor*	3 μA @ 1.2 V 12 μA @ 1.8 V 12.1 μA @ 1.8 V	200 μA 35 μA	0.65

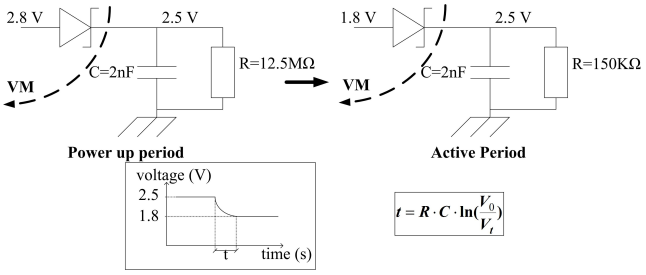

Figure 3 Discharge of the supply capacitor by mode transition

consumption is the higher because every block is active, namely, digital, analog and sensor.
The supply capacitor reduces the effect of the current peaks and the shorts absences of RF signal on the supply voltage. However the supply capacitor is not able to hold the required supply voltage for the average DC power requirements. Fig. 3 illustrates the functionality in transition mode, from *Power up* to *Active*, of the VM. The discharge time is 100μs so the DC power requirements are not fulfilled after 100μs. A higher value capacitor can be used to increase the discharge time, but the area consumption becomes a problem.
When a mode transition is produced, the drop on the supply voltage depends on the design of the voltage multiplier, the input RF wave and the DC power requirements. This paper deal with the two last aspects, but the design of the voltage multiplier is not here discussed.

2.2 VM as a load for the antenna

Assuming unobstructed free space propagation conditions and correctly aligned and polarized antennas, the available power at the receive antenna terminals is calculated using the Friis transmission equation:

$$P_a = G_r \cdot G_t \cdot P_t(\frac{\lambda}{4\pi r})^2 \quad (1)$$

where G_r and G_t are the antenna gain of the transmitting and receiving antennas, respectively, P_t is the power delivered to the transmit antenna in Watts, λ is the wavelength and r is the distance between the tag and the reader. P_a will be fully delivered to the VM only if the VM is impedance matched to the antenna.
The VM and the rest of the blocks (modulator and demodulator are here included [1]) can be modelled as complex impedance when they are seen from its input. A matching network is required to achieve maximum power transfer from the antenna to the VM, see Fig. 4.

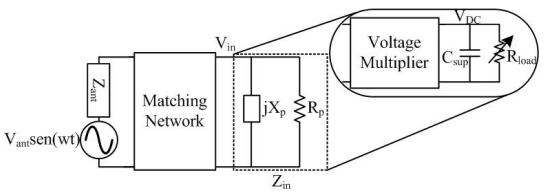

Figure 4 Chip equivalent impedance, matching network and antenna equivalent circuit.

The dissipated power in the charge is expressed as:

$$P_{diss} = \frac{V_{in}^2}{2R_p} \quad (2)$$

where V_{in} is the amplitude of the voltage across the VM. The maximum value of P_{diss} is obtained when the antenna and the VM are impedance matched and is equal to P_a. Hence, the maximal input voltage amplitude across the

VM is:

$$V_{in,max} = \sqrt{2 \cdot G_r \cdot G_t \cdot P_t \cdot R_p \cdot (\frac{\lambda}{4\pi r})^2} \qquad (3)$$

it is desirable to maximize the $V_{in,max}$ for a given range [3]. The product $P_t \cdot G_t$ (EIRP) is fixed by government regulations, λ is set by the frequency of application and the G_r is limited to a maximum of 2 dBi. So the R_p must be maximized in the design of the VM.

The matching network for a VM design is not a trivial issue, because the input impedance of the VM is not constant. There are tree factors which have influence in the input impedance of the VM:

- The first one is the design of the VM and those issues related with technology of fabrication, architecture, number of stages and size of its components.
- The distance between reader and tag reduces the amplitude of the input voltage. The VM is a non-linear circuit, its behaviour and therefore its input impedance depends on the input voltage.
- Finally, the load at the output of the VM has an influence on its input impedance.

For the design of the matching network, it is supposed that the VM is already designed, so the first factor is eliminated. Regarding to the second factor, it is desirable to achieve the longest range of operation, so the matching network must be designed to maximize the distance between reader and tag in which all the power requirements are fulfilled. As the output load change during the link time, the input impedance also changes and the reflections can not be avoided using a passive matching network. Reflections mean a reduction in the V_{in}, which also changes the input impedance and the supply voltage, so the power requirements can be violated.

3 Algorithm

An analytical solution to calculate the input impedance in function of the output load is a complex expression due to the mentioned non-linearity of the diodes and the influence of the amplitude of the input voltage. Besides, an analytical solution is very dependent on the architecture and the technology. In order to obtain a general solution, independent of the technology and the architecture, the input impedance of VM and the supply voltage (V_{DC}) is found by measurements for a range of amplitude input voltages and for every load requirements, as shown Fig. 5. The impedance table takes into account all the factors which have influence in the input impedance of the voltage multiplier: Distance (V_{in}) Power requeriments (V_{DC} and R_{load}) and VM design Z_{in} and V_{DC}.

We propose an algorithm to process the Impedance Table and obtain the optimal matching network. The idea is to test iteratively a number of matching networks for a given Impedance Table, selecting the network, which fullfils all the power requirements for a larger range. Fig. 6 shows the

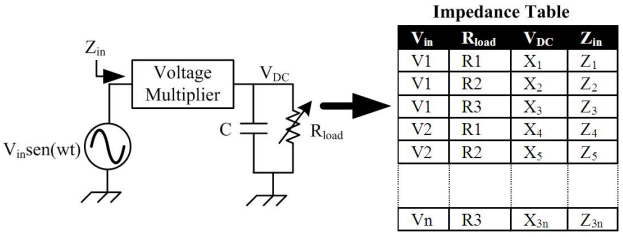

Figure 5 Voltage Multiplier characterization.

flow diagram of the algorithm.

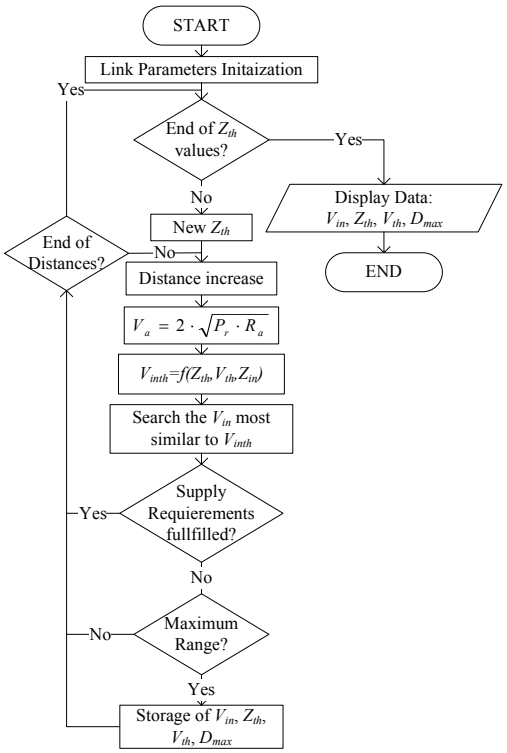

Figure 6 Flow diagram of the the algorithm for optimal matching.

The inputs of the algorithm are the impedance table and the link parameters. The outputs are the Thevenin Equivalent Circuit of the matching network and the antenna and the maximal range. First of all the link parameters are initialized; frequency, antennas gain and radiated power, among others. After that, a range of Thevenin Impedances (Z_{th}) are tested, each one for different distances (from 0.5 m until 30 m in steps of 0.1 m). For each value of Z_{th} and distance, V_{th} is calculated using the Friis formula. Next, V_{inth} is calculated for each row of the impedance table using the formula of the voltage divider. Then, the impedance table is run through looking for the row with the lowest absolute error between V_{in} and V_{inth}. If the found row meets the power requirements, then the distance is increased; if not then the saved range and the actual range are compared

Table 2 Algorithm Results of four Voltage Multipliers

$VM\ architecture$	Range (m)	Re(Z_{th}) (Ω)	Im(Z_{th}) (Ω)
2 stages	4.3	600	1780
3 stages	3.6	420	1100
4 stages	3.4	360	800
6 stages	3.8	140	580

and the Z_{th}, D, V_{in} and R_{load} are saved in case the actual range is shorter. After that, next values of Z_{th} and distance are processed. Once all the values of Z_{th} and distance are processed, the saved distance is the maximal range of the tested VM, and from the Thevenin Equivalent Circuit the matching network can be calculated.

4 Results

Four VM with different number of stages has been simulated using Cadence v5.0.33 as CAD tool for schematic and layout entry and simulations. The 0.35μm 2P3M CMOS technology with Schottky diodes availability of XFAB has been used. Both pre- and post-layout simulations have been done to obtain the impedance table. Fig. 7 shows the behaviour of the Z_{in} and V_{DC} for different R_{load}, V_{in} and VM structure.

Each operation mode presents a different Z_{in} which also varies with V_{in}, as can be seen in Fig. 7.a Therefore the matching for one mode and V_{in} implies a mismatching in the other modes and input voltages, which produces a descend in V_{in}. The Fig. 7.c shows the variation of V_{DC} with the V_{in} for the three operation modes. The highest values of V_{DC} are obtained for the *Power up* mode. The current consumption in this mode is around 100 times lower than in the other modes, thus almost the whole current is used to charge the supply capacitor. On the other hand, Fig. 7.b and d show the behaviour of V_{DC} and Z_{in} of four VM, which differ in the number of stages. High values of Z_{in} are obtained for lower stage number, which implies lower input power for the same V_{in}, this fact increase the efficiency ($\frac{P_{out}}{P_{in}}$). Higher values of V_{DC} are achieved by VM with higher stages number. A tradeoff between efficiency and V_{DC} must be found.

In order to find out the VM, that works properly in a wider range, the proposed algorithm has been applied to the four VM structures. The proposed algorithm calculates the maximal range of each circuit under the optimal matching conditions to fulfil the power requirements described in Table 1. This comparison is fair because it takes into account all the factors involved in the performance of a VM under the same load conditions. Table 2 shows the obtained results.

The VM with the longest range is the 2 stages one. The Z_{th} is the impedance that must be viewed from the input of the VM to achieve the obtained range.

5 Conclusion

An algorithm to calculate the optimal input impedance to match and the maximal achievable operation range in passive UHF wireless sensors has been presented in this paper. The proposed method is independent of the architecture and technology used to implement the Voltage Multiplier (VM). This method is therefore a fair tool to compare the performance of different implementations of a VM.

6 References

[1] G. De Vita and G. Iannaccone, "Design Criteria for the RF section of UHF and Microwave Passive RFID Transponders," in *IEEE Trans. Microw. Theory Tech.*, Vol. 53, no. 9, pages 2978–2990, Sep. 2005.

[2] J.-P. Curty, N. Joehl, F. Krummenacher, C. Dehollain and M. J. Declercq, "A Model for μ–Power Rectifier Analysis and Design," *IEEE Trans. Circuit and Systems I*, vol. 52, no. 12, pages 2771–2779, Dec. 2005.

[3] S. Mandal, "Far Field RF Power Extraction Circuits and Systems," Master's Thesis, MIT, D. of Electrical Engineering and Computer Science. Jun. 2004.

[4] EPC Tag Data Standards Version 1.1 Rev. 1.27, (2005, May), [Online] Avalible: http://www.epcglobalinc.org/standards_technology/specifications.html.

[5] R. Morales–Ramos, J. A. Montiel–Nelson, H. Milosiu, R. Berenger and A. García–Alonso, "Adjustable Voltage Sensors for Power Supply Chains in Passive UHF RFID Transponders," in *11th Int. Conf. on Emerging Technologies and Factory Automation(ETFA)*,pages 286–291, Sep. 2006.

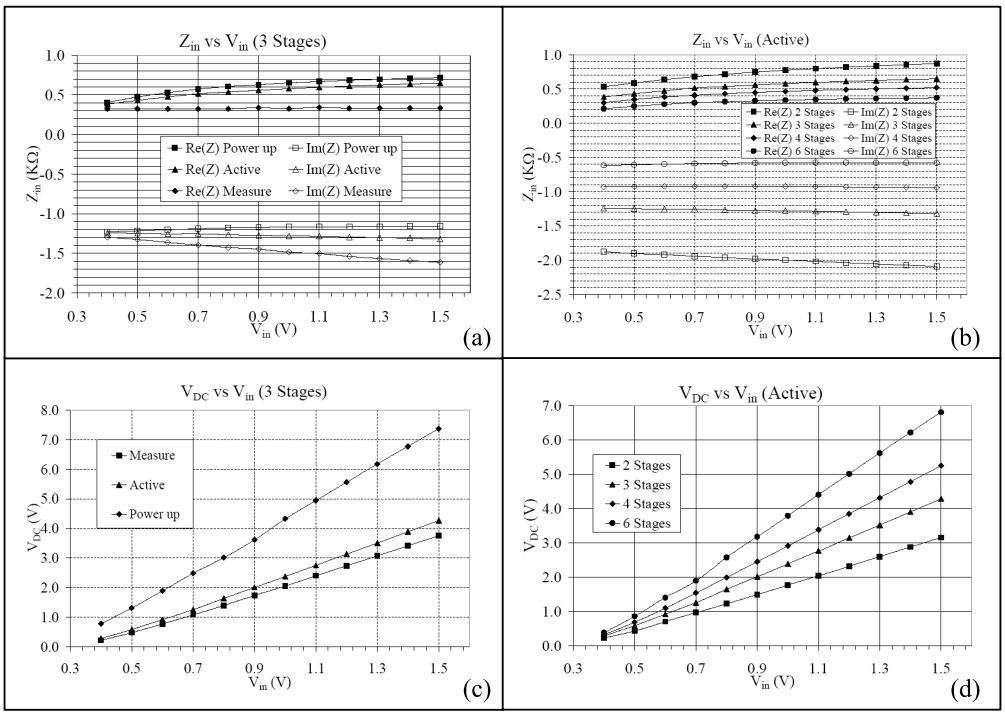

Figure 7 Behaviour of the input impedance and the output DC supply voltage versus input amplitude voltage, operation mode and VM architecture.

Voltage Protection Circuit for the Supply Capacitor in Passive UHF RFID Sensors

R. Morales–Ramos[1], *R. Berenguer*[2], *J.A. Montiel–Nelson*[1]
[1]Institute for Applied Microelectronics, University of Las Palmas de G.C., Las Palmas de G.C., Spain
[2]Centro de Estudios e Investigaciones Técnicas de Guipuzkoa (C.E.I.T.), San Sebastian, Spain
Email: ricmorales@iuma.ulpgc.es

***Abstract*— This paper presents a ultra–low–power voltage protection circuit to optimize the power consumption in passive UHF RFID sensors. The state-of-the-art in the field is analyzed and compared with the proposed circuit using a 0.35 μm 2P4M CMOS process. The measured current consumption of proposed Voltage Protection circuit is less than 60 nA at 3 V and its degradation region is 0.12 V.**

I. Introduction

Passive RFID technology is becoming the most suitable RF interface for Passive Wireless Sensors. The RFID tag is supplied by an EM wave transmitted from an interrogator [1], thus no batteries are required. Low power inductive coupling, widely used in RFID near field tags, has been already proved as an interface for wireless sensors, but in a reduced range (<50cm) [2]. In order to increase the operation range to some meters, Far Field RFID Tags working in UHF Band are required.

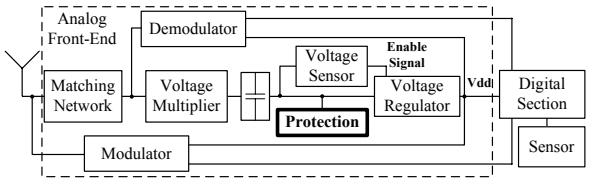

Fig. 1. Architecture of the passive UHF RFID sensor.

Fig. 1 shows the block diagram of the passive UHF RFID sensor. The RF input power is captured by the antenna, which is matched for maximizing power transfer. The Voltage Multiplier (VM), also called rectifier, converts RF into DC power. The DC power produced by the VM charges the supply capacitor. This capacitor maintains the supply voltage when short absences of RF power or consumption current peaks occur. To assure a proper supply voltage, the tag is powered up only after the capacitor is properly charged. To handle the charging of the supply capacitor, two circuits are required: a Voltage Sensor and a Voltage Protection. The first one senses the charge of the capacitor and generates the Enable Signal. This signal turns on the Voltage Regulator, which generates the V_{dd} for the rest of the subsystems of the transponder. High RF power on the antenna produces high voltages on the capacitor [3], that could damage the electronics. The voltage protection circuit protects the supply capacitor and the complete chip subsystems against breakdown voltage.

The bottleneck, to achieve the longest range in UHF passive RFID tags, is the RF into DC power conversion. This is because the input power decreases quadratically with the distance (see Friis Transmision Formula [4]) and the efficiency of the conversion is limited. A way to increases the range is reducing the power consumption of the different blocks of the system. To do this, firstly the supply voltage is reduced. In second place, the circuits are designed for minimal current consumption.

The power consumption of an RFID sensor is not constant along the time. There are three different operation modes with different power requirements [5]:

- **Power–Up**, Supply Capacitor is charged (below 1μW),
- **Active**, Analog and Digital active (24μW), and
- **Measure**, the Sensor is operative (50μW).

A consequence of the different power consumtion is that the input impedance changes with the operation mode. Therefore an optimal matching is not possible for all the operation modes. A solution is to match for the worst case (highest power consumption) and reduce the power consumption in the rest of operation modes.

This paper propose a modification in the state–of–the–art voltage protection circuit to reduce the current consumption when the protection is not active. The state–of–the–art circuit and the proposed one were implemented and measured in a 0.35 μm 2P4M CMOS process.

Section II presents the state-of-the-art voltage protection and introduces the proposed circuit. The measured results of both circuits are compared in Section III. Finally, the main conclusions are summarized in Section IV.

II. Voltage Protection

The voltage on the supply capacitor increases with the level of RF power at the input of the Voltage Multiplier (see Fig. 1), when the current consumption of the tag remains constant. The level of the received RF power increases quadratically as the distance between reader and tag decreases (see Friis Transmission Formula [4]). On the other side, the CMOS process limits the voltage on the supply capacitor to 3.6 Volts. Therefore, the supply capacitor must be protected against high voltages produced when the Reader is close to the tag.

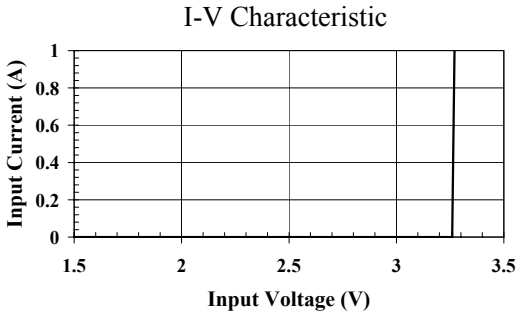

Fig. 2. Ideal characteristic of the protection circuits.

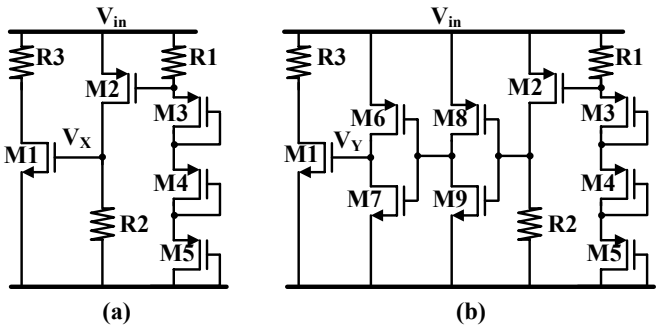

Fig. 3. Protection circuits, (a) Without Inverters circuit based on [6], and (b) With Inverters circuit proposed in this paper.

The ideal I-V characteristic of a protection is shown in Fig. 2. No current is drawn until a threshold is reached, after that the circuit behaves as a short. To approach this characteristic, we used a circuit based on the limiter proposed by [6] (see Fig. 3.a). As soon as V_{in} exceeds the sum of all threshold voltages of the transistors M3—M5 current start to flow through R1. When the voltage drop across R2 reaches the threshold, M2 will switch on and in turn activates M1 which carries the most of the current. Resistor R3 fix the current to be drawn, when the protection is activated.

A consequence of designing circuits with very low current consumption is a reduction of the switching speed of the transistors. The reason is that the parasitic capacitors of the transistors are charged and discharged by very low current. In the case of the protection circuit of Fig. 3.a, this means an increment in the degradation zone (voltage range below the threshold voltage and with a current greater than 100nA, see Fig. 7). To reduce the degradation region, two inverters were introduced at the gate of M1 (see Fig. 3.b). This modification increases the switching speed of M1, since the voltage V_X (Fig. 3.b) switches more abruptly from 0 to Vin than V_Y.

III. Results

The two protection circuits of Fig. 3 were implemented in a 0.35μm 2P4M CMOS process. Fig. 4 shows the place of the protecction circuit inside the Analog Front-End of a passive UHF RFID Transponder.

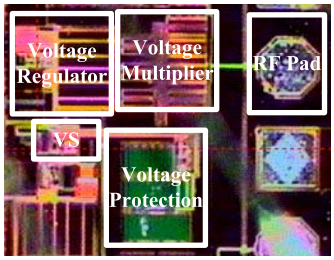

Fig. 4. Photograph of the test chip.

Fig. 5 depicts the test bench used to measure the time required by the circuits to switch once the threshold voltage is reached. The input signal is a pulse with adjustable slope, which models the charge of the supply capacitor by the voltage multiplier. The resistor R3 (Fig. 3) is an external element, that adjusts the current to be drawn by the circuit. The transient response to the same input signal of both topologies is showed in Fig. 6. The time required to switch by the circuit without inverters is around 70 μs, whereas the time required to switch with inverters is around 5 μs. The proposed modification reduces in a 92.9% the response time of the protection circuit.

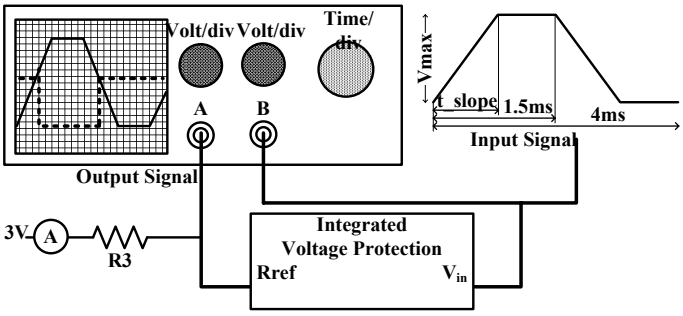

Fig. 5. Test bench used to measure the switching time of the protection circuit.

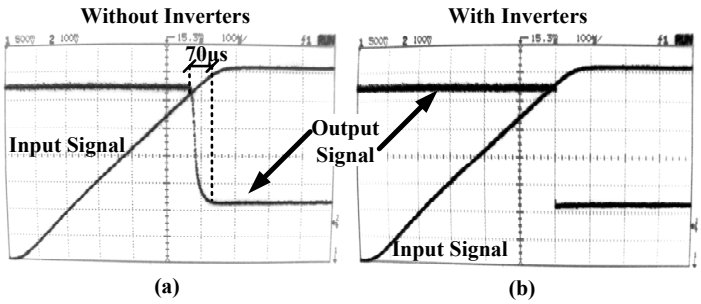

Fig. 6. Transient response of the protection circuits. (a) Without Inverters circuit based on [6], and (b) With Inverters circuit proposed in this paper.

Fig. 7 shows the measured I-V characteristic of the both circuits; with and without inverters. The degradation region is 0.2 V in the circuit with inverters and 0.12V in the one without inverters. A reduction of 40% in the degradation region is achieved by inserting the two inverters. The measured current consumption for a V_{in} of 3 V is 57 nA with and 61 nA without inverters. But if we increase V_{in} to 3.1 V the current consumption is 1 μA with and 100 nA without inverters.

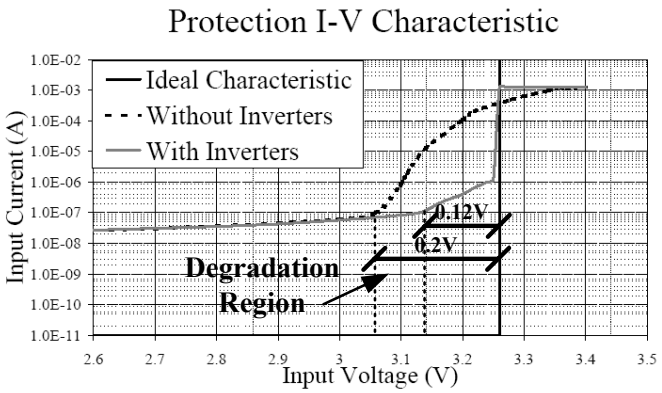

Fig. 7. Ideal and measured I-V characteristic of the protection circuits.

IV. Conclusion

In passive UHF RFID sensors, Voltage Sensor and Voltage Protection are the unique active circuits during the charge of the Supply Capacitor. To optimize this charge the current consumption must be minimized. This paper propose a modification on the state-of-the-art voltage protection, which reduce considerably the current consumption before the voltage threshold of the circuit is reached. As a result, the I-V characteristic of the proposed topology is closer to the ideal protection circuit. Measured waveforms and I-V characteristic of the protection circuits implemented in a 0.35μm CMOS process are given.

References

[1] K. Finkenzeller, *RFID Handbook, Radio–Frequency Identifications Fundamentals and Applications in Contactless Smart Cards and Identification,* 2nd ed. West Sussex, U.K.: Wiley, 2003.

[2] R. R. Harrison, P. T. Watkins, R. J. Kier, R. O. Lovejoy, D. J. Black, B. Greger, and F. Solzbacher, "A Low–Power Integrated Circuit for a Wireless 100–Electrode Neural Recording System," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pp. 123–133, Jan. 2007.

[3] F. Kocer and M. P. Flynn,, "A New Transponder Architecture With On–Chip ADC for Long–Range Telemetry Applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pages 1142–1148, May. 2006.

[4] R. E. Collins, *Antennas and Radiowave Propagation,* New York, U.S.: McGraw-Hill, 2003.

[5] R. Morales–Ramos, D. Puente, H. Milosiu, R. Berenguer, and J.A. Montiel–Nelson "Optimal Impedance Matching in Passive UHF RFID Sensors," in *3rd European Workshop on RFID Systems and Technologies (RFID SysTech)*, accepted, Jun. 2007.

[6] U. Kaiser and W Steinhagen, "A Low–Power Transponder IC for High-Performance Identification Systems," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pages 306–310, Mar. 1995.

Ultra-Low Power Passive UHF RFID for Wireless Sensor Networks

R. Morales–Ramos[1], *A. Vaz*[2], *D. Pardo*[2] *and R. Berenguer*[2]
[1]Institute for Applied Microelectronics, University of Las Palmas de G.C., Las Palmas de G.C., Spain
[2]Centro de Estudios e Investigaciones Técnicas de Guipúzcoa (C.E.I.T.), San Sebastian, Spain
Email: ricmorales@iuma.ulpgc.es

***Abstract*— This paper presents two ultra-low-power voltage sensors and a voltage protection, to optimize the charge of the Supply Capacitor in passive UHF RFID sensors. The state-of-the-art in the field is analyzed and compared with the proposed circuits using a 0.35 μm 2P4M CMOS process. The measured current consumption of the Voltage Sensors are 70 nA and 0.2 nA at 3.3 V. The Voltage Protection circuit consumes less than 60 nA at 3 V. Additionally, a low power consumption voltage regulator is presented. Experimental results prove its proper operation.**

I. Introduction

Passive RFID technology is becoming the most suitable RF interface for Passive Wireless Sensors. The RFID tag is supplied by an EM wave transmitted from an interrogator [1], thus no batteries are required. Low power inductive coupling, widely used in RFID near field tags, has been already probed as an interface for wireless sensors, but in a reduced range (<50cm) [2]. In order to increase the operation range to some meters, Far Field RFID Tags working in UHF Band are required.

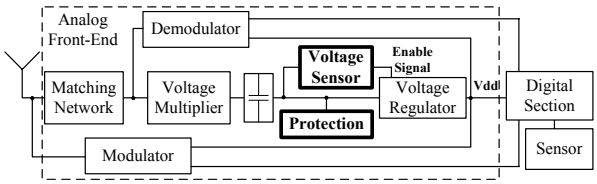

Fig. 1. Architecture of the passive UHF RFID sensor.

Fig. 1 shows the block diagram of the passive UHF RFID sensor. The RF input power is captured by the antenna, which is matched for maximizing power transfer. The Voltage Multiplier (VM) converts RF into DC power. The DC power produced by the VM charges the supply capacitor. This capacitor maintains the supply voltage when sort absences of RF power or consumption current peaks are produced. In order to assure a proper supply voltage, the tag is powered up only after the charge of the capacitor. To handle the charge of the supply capacitor, two circuits are required: a Voltage Sensor (VS) and a Voltage Protection (VP). The first one senses the charge of the capacitor and generates the Enable Signal (ES). ES turns on the Voltage Regulators, which generate the V_{dd} for the rest of the subsystems of the transponder and the suplly voltage of the EEPROM memory, where all the informationi of the tag will be stored. High RF power on the antenna produces high voltages on the capacitor [3], that could produce damages in the electronic. VP protects the supply capacitor and the complete chip subsystems against breakdown voltage.

The bottleneck, to achieve the longest range in UHF passive RFID tags, is the RF into DC power conversion. This is because the input power decreases quadratically with the distance (see Friis Transmision Formula [4]) and the efficiency of the conversion is limited. A way to increase the range is reducing the power consumption of the different blocks of the system. To do this, firstly the supply voltage is reduced until its minimum, established by the technology. Secondly, the circuits are designed for minimal current consumption.

The power consumption of a RFID sensor is not constant along the time. There are three different operation modes with different power requirements:

- **Power–Up**, Supply Capacitor is charged (below 1μW),
- **Active**, Analog and Digital active (24μW), and
- **Measure**, the Sensor is operative (50μW).

A consequence of the different power consumptions is that the input impedance changes with the operation mode. Therefore an optimal matching is not possible for all the operation modes. A solution is to match for the worst case (highest power consumption) and reduce the power consumption in the rest of operation modes.

This paper propose ultra–low–power voltage sensor circuits and a voltage protection circuit to reduce the power consumption during the Power–Up operation mode. Moreover, two low–power voltage regulators will be proposed, implemented and measured

Section II presents the state-of-the-art in Voltage Sensor and introduces two novel circuits. Different architectures of Voltage Sensors are compared, fabricated and test chips measured. Results are introduced in Section III. The Voltage Protection is discussed in Section IV. The implemented voltage regulators are presented in Section V. Finally, the main conclusions are summarized in Section VI.

II. Voltage Sensor

The Voltage Sensor (VS) senses the charge of the supply capacitor and generates the Enable Signal (ES) when a specified voltage threshold (ES_{th}) is reached on the capacitor.

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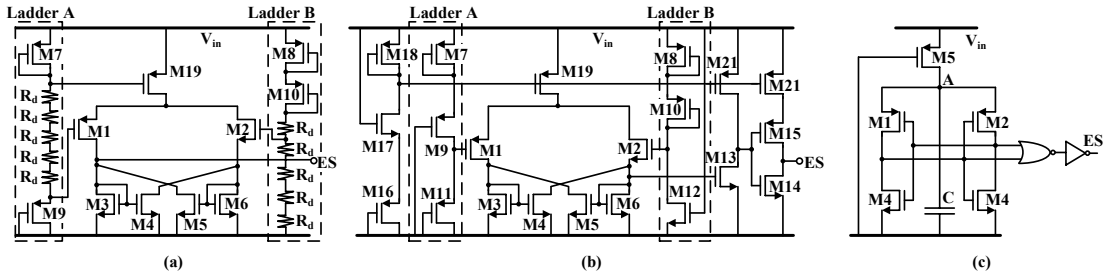

Fig. 2. Circuits reported in the bibliography, (a) Mode Selector(MS) [5], (b) Modified Mode Selector (MMS) [3], and (c) Power on Reset (POR) [6].

A. State-of-the-art

The Mode Selector (MS) circuit [5] is shown in Fig. 2.a. Two trip voltages are generated by two resistive ladders and compared by a hysteresis comparator formed with transistor M1-M6. The integrated resistances increase the area consumption dramatically and also the current consumption (reported as 5μA).

The same authors propose the Modified Mode Selector (MMS) [3], see Fig. 2.b. In this circuit, the ladders are implemented with transistor instead of integrated resistances reducing so the active area. The current consumption is also reduced to 900nA, which is still excessive for passive UHF RFID systems in the Power–Up mode.

Other alternative is the POR circuit [6] of Fig. 2.c. When a supply voltage is applied to V_{in}, one of the two inverters takes advantage over the other. The NOR gate compares the output of the two inverters, and activates the ES. The capacitor C forces a delay between the rise of the V_{in} and the ES.

B. Novel structures

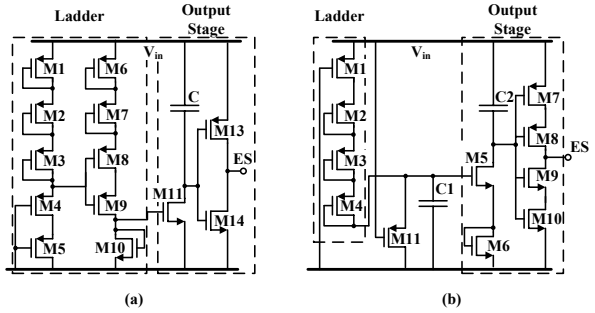

Fig. 3. Proposed Novel Circuits. (a) Based on Voltage Levels (VL), and (b) based on the charge of a capacitor (CC).

Two novel structures are presented. Fig. 3.a shows the Voltage Levels (VL) circuit. It is based on the voltage level reached at the gate of M11. The ladder composed of the transistors M1-M10 does not draw current until $V_{in} > 5 \cdot V_{th}$ (around 2.5 Volts in 0.35 μm CMOS technology). However M11 begins to conduct a small current (i_{sth}) in Subthreshold Region ($V_{GS} < V_{th}$). The current i_{sth} discharges the small capacitor C and finally the inverter generates a rising edge. The Output Stage consumes current only in the transitions of the ES. The current peak on the transition depends on the capacity of C and on the dimensions of M13 and M14. Before the edge of ES (Power up operation mode), Ladder and M11 are still OFF and the current is below 1nA.

Fig.3.b shows the second novel circuit based on the charge of a capacitor (CC). The ladder made up of M1-M4 charges the capacitor C1. When the charge on the capacitor is $2 \cdot V_{th}$ M5 turns on and the rising edge of the ES is produced. M11 discharges C1 when the tag is turned off. CC circuit draws current only in the rising edge of the enable signal. Ladder and Output Stages are open circuits for the DC current thanks to C1 and C2.

C. Design Considerations

The performance of the proposed circuits is very dependent on the technology and temperature because the V_{th} of the transistors is used as unique voltage reference. This is taken into account in the design. The dimension of each transistor is chosen so that, the threshold voltage and the current consumption of the circuit are for all technology corners (worse cases) as constant as possible.

Notice that the ES_{th} of the proposed circuits can be increased/decreased by inserting/removing diode–connected transistors in the ladders.

III. Comparison and measurements

Circuits of the state-of-the-art and novel structures have been simulated and compared at schematic level using a standard 0.35μm 2P4M CMOS process, then the circuits with the best features has been implemented and measured.

A. Performance Parameters

The charge of the supply capacitor depends on the reader distance, the used Voltage Multiplier and the capacitance of the supply capacitor. We are interested in reducing power consumption and area of each structure, for standard operational conditions. To compare the different architectures, all the circuits were adjusted to set to HIGH the ES when V_{in} is, for all the corners, between 2.5 V and 3.3 V (ES_{th}). All the eight simulation corners, as specified in the technology process, were simulated. V_{in} is generated by a pulse source with voltage levels between 0 V and 3.3 V, and a rise time of

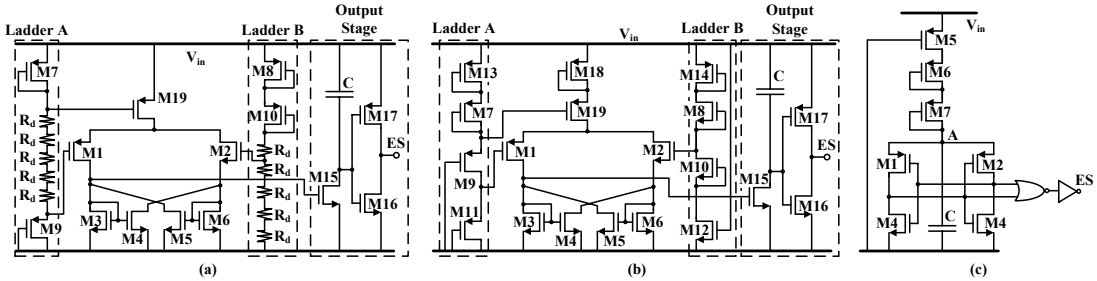

Fig. 4. Modifications in state-of-the-art circuits. (a) MS', (b) MMS', and (c) POR'.

TABLE I
SIMULATION RESULTS OF VOLTAGE SENSOR CIRCUIT–STRUCTURES

$Circuit$	$\bar{I}$ (nA)	$\hat{I}$ (μA)	ΔES_{thc} (V)	ΔES_{tht} (V)	$Area$ (μm^2)	ref.
MS	800	1.87	1.10	0.40	30148	[5]
MMS	57	1.44	0.85	0.50	693	[3]
POR	1350	1.55	1.40	0.20	348	[6]
VL	47	1.65	0.90	0.45	352	this paper
CC	< 1	0.50	1.10	0.49	590	this paper

50 μs for quick charging time, or 1.5 ms for slow charging time. The parameters obtained from the simulations were:

- ES_{th} variation due to corner simulations (ΔES_{thc}) and due to charging time of the capacitor (ΔES_{tht});
- DC current consumption at 3.3V ($\bar{I}$) and transient current consumption when the ES is set to HIGH ($\hat{I}$) i.e. when the output inverter switches;
- active area, which is calculated by adding the size of the required devices.

B. Modifications on MMS and POR structures

Adjusting ES_{th} to 2.5 V requires some modifications on the state-of-the-art circuits. In the MMS circuit (see Fig. 2.b), we have modified the MOS resistive ladders A and B, as can be seen in Fig. 4.b.

The ES_{th} in the original POR circuit is very low (some hundreds of mV), when it is implemented. In order to provide a fair comparison, the threshold voltage ES_{th} was increased to 2.5 V by introducing two transistors, M6 and M7 as shown in Fig. 4.c.

In addition, the output stage used in VL is introduced in the MS and MMS circuits to reduce the DC current consumption, as can be seen in Fig. 4.b. The modified state-of-the-art circuits are termed MS', MMS' and POR'.

C. Comparison Results

Table I shows the simulation results. The DC current consumption is lower than 1nA in the CC circuit because the capacitors C1 and C2 (Fig. 3.b) behave as open circuits in DC. ($\bar{I}$) is 47 and 57 nA in VL and MMS' respectively. The ladders are similar but the MMS' includes an extra current consumption due to the comparator. The use of resistive ladders in MS' increase the $\bar{I}$ because of the limited value of the integrated resistances. Finally, the highest $\bar{I}$ correspond to the POR' which presents an unusual value, more than 1 μA. The POR circuit was designed for a ES_{th} of 1 V, an increment on this voltage increases the DC current consumption on the NOR gate.

The peak current is similar in the MS', MMS', POR' and VL circuits (see Table I) because all these architectures use the same inverter at the output. The peak current of the CC circuit is around 66% less than the above mentioned architectures. This is due to the transistors of the output inverter in the CC circuit have lower aspect ratio than in the other architectures.

The variation of ES_{th} due to technology corners is around 1 V, and the variation due to the charging time of the capacitor is about 0.4 V. For short charging times ES_{th} is higher than for long ones. The reason is that the used transistors have low aspect ration (W/L$\simeq$0.09). This reduces the power consumption of the structures, but increase the time required by the transistors to switch.

Finally, the active area of the MS circuit is two orders of magnitude bigger than the other circuits. This is because this circuit requires high value integrated resistors (Rd in Fig. 2.a) to reduce the current through the ladders A and B.

To sum up, MS' and POR' have the highest current consumption; and in the case of MS' the largest active area. The CC circuit presents the lowest current consumption. In terms of ES_{th} variation, VL and MMS' are the best circuits. However, $\bar{I}$ and area consumption of MMS' circuit are 2.85 and 1.97 times higher than in VL circuit. Finally, notice that the modified estate–of–the–art circuits, MMS' and MS' consume 18 and 6 times less current than the original ones.

The simulation results indicate that VL and CC circuits are the best structures. This two circuits were implemented, to verify the results of Table I.

D. Measurements Results

Fig. 5.a is the photograph of the test chip, for implementing the VS circuits. Two versions of VL and CC circuits with different ES_{th} (2.5V and 3.3V) have been fabricated and measured. Table II shows the measured results. The DC current consumption at 3.3 Volts of VL and CC circuits are below 70 nA and below 1nA, respectively. The Current peak is below 2 μA in all cases. The ES_{th} is about 0.5 V lower regarding to

TABLE II
MEASURED RESULTS OF VL AND CC CIRCUIT–STRUCTURES

$Circuit$	$\bar{I}$@3.3V (nA)	$\hat{I}$ (μA)	ES_{th}@1ms (V)	ES_{th}@1μs (V)	$Area$ (μm^2)
VL (2.5V)	69	1.79	2	2.5	2584
VL (3.3V)	19	2	3	4.2	3380
CC (2.5V)	0.2	0.75	2	2.8	3762
CC (3.3V)	0.4	1.5	3	4.2	3843

the simulated results. The dispersion of ES_{th} with the slope of V_{in} is between 0.5 and 1 volt. Fig. 5.b is the photograph of the complete supply generation chain of the Passive UHF RFID sensor without the supply capacitor.

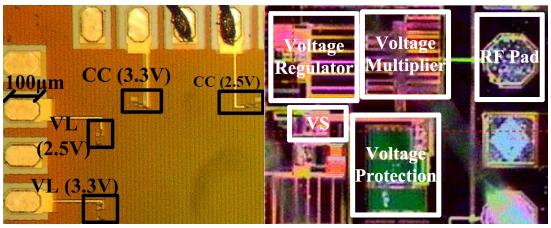

Fig. 5. Photograph of the test chip.

IV. VOLTAGE PROTECTION

The voltage on the supply capacitor increases with the level of RF power at the input of the Voltage Multiplier (see Fig. 1), when the current consumption of the tag remains constant. The level of the received RF power increases quadratically as the distance between reader and tag decreases (see Friis Transmission Formula [4]). On the other side, the 0.35 μm CMOS process limits the voltage on the supply capacitor to 3.6 Volts. Therefore, the supply capacitor must be protected against high voltages produced when the Reader is close to the tag.

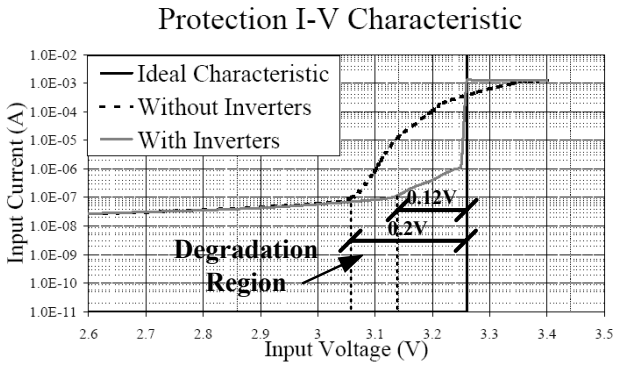

Fig. 6. Ideal characteristic and measured results of the protection circuits.

The ideal I-V characteristic of a protection is shown in Fig. 6. No current is drawn until a threshold is reached, after that the circuit behaves as a short. To approach this characteristic, we used a circuit based on the limiter circuit proposed by [7] (see Fig. 7.a). As soon as V_{in} exceeds the sum of all threshold voltages of the transistors M3—M5 current start to flow through R1. When the voltage drop across R2 reaches the threshold, M2 will switch on and in turn activates M1 which carries the most of the current.

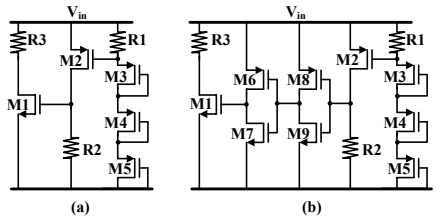

Fig. 7. Protection circuits, (a) without inverters circuit based on [7], and (b) with inverters circuit proposed in this paper.

A consequence of designing circuits with very low current consumption is a reduction of the switching speed of the transistors. The reason is that the parasitic capacitors of the transistors are charged and discharged by very low current. In the case of the protection circuit of Fig. 7.a, this means an increment in the degradation zone (voltage range below the threshold voltage and with a current greater than 100nA, see Fig. 6). To reduce the degradation region, two inverters were introduced at the gate of M1 (see Fig. 7.b). This modification increases the switching speed of M1. Fig. 6 shows the measured result of the both circuits; with and without inverters. The degradation region were reduced 40% by inserting the two inverters. The measured current consumption is 57nA at 3V.

V. VOLTAGE REGULATORS

Two voltage regulators have been implemented in the present design. The need of two regulators comes from the purpose of minimizing the power consumption. The first regulator is established to provide a regulated output voltage of 1.8 V, which is necessary for the proper working of the EEPROM memory, where all the data will be stored in the tag.

The second regulator is the one that provides the supply voltage to the rest of the circuits of the system. This supply voltage has been minimized down to the technological limit in order to reduce the power consumption. The rest of the system must be able to operate properly with this supply voltage; otherwise, the inclusion of a sensor would be impossible.

The power requirements for both regulators limit to 2 μA the total current consumption of these blocks.

The architecture implemented is based on a low power Low Dropout (LDO) regulator. This is a circuit that provides a well specified and stable dc voltage whose input to output voltage difference is low. The operation of the circuit is based on the feeding back of an amplified error signal used to control the output current flow of the power transistor driving the

load. The circuit is composed by a voltage reference, an error amplifier, a pass element and a feedback network as is shown in Fig. 8

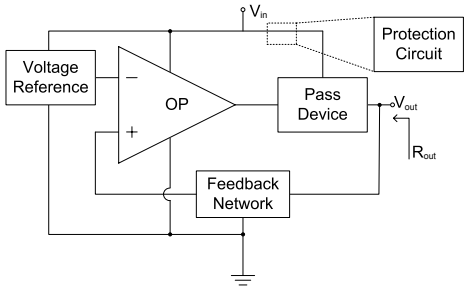

Fig. 8. Architecture of the voltage regulator.

The final implementation of the voltage regulators is shown in Fig. 9. In order reduce current consumption it is interesting to keep as simple as posible, thus the Error amplifier was implemented with an differential pair. A subthreshold reference circuit was used to generate V_{ref}, this reference circuit reduce the current consumption as the expense of reference stability. A PMOS transistor was used as pass element. Finally, the V_{out} can be adjusted with the values of the capacitive feedback network. We used capacitors instead or resistances to reduce the static current through the feedback network.

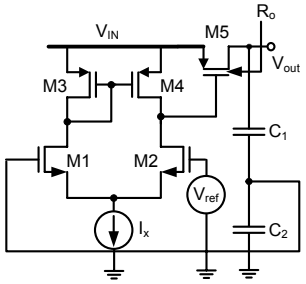

Fig. 9. Schematic of the voltage regulator.

In Fig. 10 the measurements of the fabricated voltage regulators may be observed. Although the regulated voltages are supposed to be 1.2 V and 1.8 V respectively, the measured voltages are 1.6 V and 2.2 V. This is not due to an error, but to the process dispersion. They have been to be designed taking into account the possible dispersions in the process, simulating all the corners provided by the foundry. Taking this into account, the minimum output voltage is settled for the worst case of the corner simulations. This way, the operation of the circuits is assured, although the typical case output will be higher than the specified. This must be done in order to avoid obtaining a regulator that, due to process dispersion, provides a voltage lower than the minimum supply voltage, what would cause the blocks of the tag not to switch on.

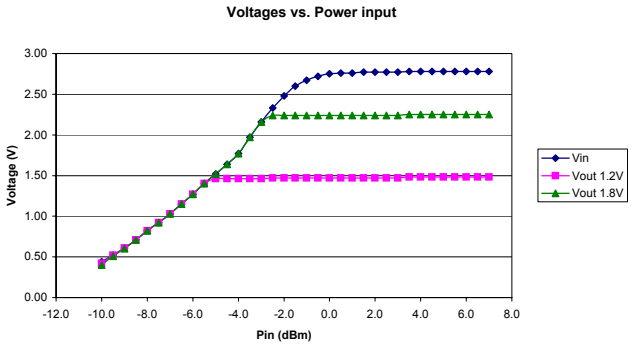

Fig. 10. Measures of the voltage regulator performance.

VI. Conclusion

In passive UHF RFID sensors, Voltage Sensor (VS) and Voltage Protection (VP) are the unique active circuits during the charge of the Supply Capacitor, to optimize this charge the current consumption of VS and VP must be minimized. Two novel VS circuits are proposed and compared with the state-of-the-art alternatives. The measured DC current consumption of the two novels structures is 69 nA and 0.2 nA at 3.3V and implies a improvement of one order of magnitude in terms of current consumption in regard to previous reported results. This paper also propose a modification on the state-of-the-art VP, which reduce considerably the current consumption before the voltage threshold of the circuit is reached.

Finally, two voltage regulators have been designed and implemented. Measurements show proper operation of the designed regulators.

References

[1] K. Finkenzeller, *RFID Handbook, Radio–Frequency Identifications Fundamentals and Applications in Contactless Smart Cards and Identification,* 2nd ed. West Sussex, U.K.: Wiley, 2003.

[2] R. R. Harrison et al., "A Low–Power Integrated Circuit for a Wireless 100–Electrode Neural Recording System," *IEEE J. Solid-State Circuits*, vol. 42, no. 1, pages 123–133, Jan. 2007.

[3] F. Kocer et al., "A New Transponder Architecture With On–Chip ADC for Long–Range Telemetry Applications," *IEEE J. Solid-State Circuits*, vol. 41, no. 5, pages 1142–1148, May. 2006.

[4] R. E. Collins, *Antennas and Radiowave Propagation,* New York, U.S.: McGraw-Hill, 2003.

[5] F. Kocer et al., "An injection locked, RF powered, telemetry IC in 0.25 μm CMOS," in *Symp. VLSI Circuits Dig. Tech. Papers*, pages 24–27, Jun. 2004.

[6] J.-P. Curty et al., "Remotely Powered Addressable UHF RFID Integrated System," *IEEE J. Solid-State Circuits*, vol. 40, no. 11, pages 2193–2202, Nov. 2005.

[7] U. Kaiser et al., "A Low–Power Transponder IC for High-Performance Identification Systems," *IEEE J. Solid-State Circuits*, vol. 30, no. 3, pages 306–310, Mar. 1995.