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Conductivity-Based DC Model for OECTs

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***Abstract*—In this paper, a new model of the DC drain current in organic electrochemical transistors (OECTs) is developed based on the channel conductivity. For this purpose, a thick-film PEDOT-based OECT was manufactured on a standard FR4 PCB substrate. By making use of the channel capacitance extracted from the AC characteristics, the expected sigmoid function of the gate voltage for the free carrier density is obtained. A bell-shaped dependence on the gate voltage for the carrier mobility is also extracted, with the transistor operating in the linear region and through the Y function method. Both dependencies combines to give the conductivity, which is obtained from DC measurements and modeled. The drain current is then evaluated using the gradual channel approximation. Channel length modulation effect is incorporated into the model. Good agreement is achieved between the measured and modeled output characteristics of the transistor. In addition, the proposed model predicts the peak in the transconductance and the forward–backward hysteresis curves typically observed in OECTs. The model can be easily implemented in circuit simulators, with the continuity of the transconductance and output conductance between the linear and saturation regions being ensured through a threshold voltage defined as the gate voltage for which the channel conductivity becomes null.**

***Index Terms*—compact model, DC characterization, AC characterization, mobility, OECT, PEDOT:PSS.**

I. Introduction

An organic electrochemical transistor (OECT) is a type of organic thin-film transistor (OTFT) that consists of a metallic source, drain and gate electrodes, and a polymer semiconductor channel between the source and the drain. The conducting polymer film, which is typically p-type conductive poly(3,4-ethylenedioxythiophene) doped with poly(styrene sulfonate) (PEDOT:PSS), is in contact with an electrolyte, in which the gate electrode is immersed. Typical applications of OECTs include biological sensing for medical diagnostics and therapeutic devices [1], [2], [3], digital logic [4], and neuromorphic engineering, including neuromorphic computing units and monitoring tasks in medicine and agriculture [5], [6].

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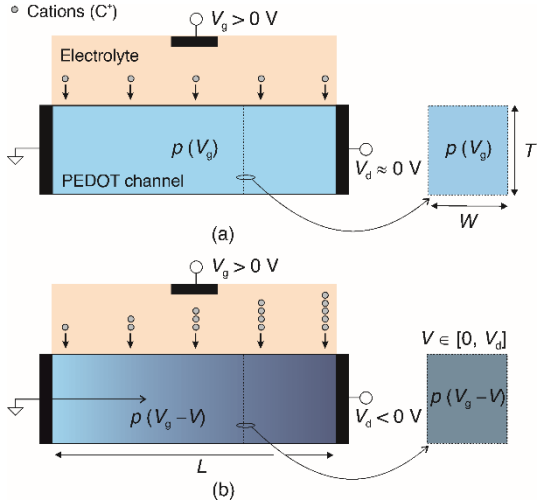

Fig. 1. Schematic diagrams showing the distribution of cations in the electrolyte injected into the PEDOT and the resulting hole concentration in the channel for (a) $V_d \approx 0$ V and (b) $V_d < 0$ V, with $V_g > 0$ V.

When a source-to-drain voltage, V_d, is applied, a drain current, I_d, flows through the channel. The current in the channel is controlled by the gate-to-source voltage, V_g. Upon application of a positive gate voltage, the cations in the electrolyte are injected into the PEDOT:PSS channel, which leads to a decrease in the hole concentration, p, and a reduction in the conductivity of PEDOT, σ. This will deplete the number of available carriers, meaning that the drain-source current decreases. Figs. 1 (a) and (b) show schemes for the distribution of the cations injected from the electrolyte into the PEDOT and the resulting hole concentration in the channel when $V_g > 0$ V, for $V_d \approx 0$ V and $V_d < 0$ V, where L, W, and T are the channel length, width, and thickness, respectively. Cations can also move along the channel, under the influence of V_d, which impacts the steady-state of OECTs [7]. When diffused cations do not go back to the electrolyte once the gate-to-channel voltage varies, hysteresis is observed in OECT testing [8].

The electrical response of an OECT is therefore determined by the interaction between the ionic and electronic charge carriers. Since the conducting polymer used as the channel for the device is amorphous, the drift-diffusion transport

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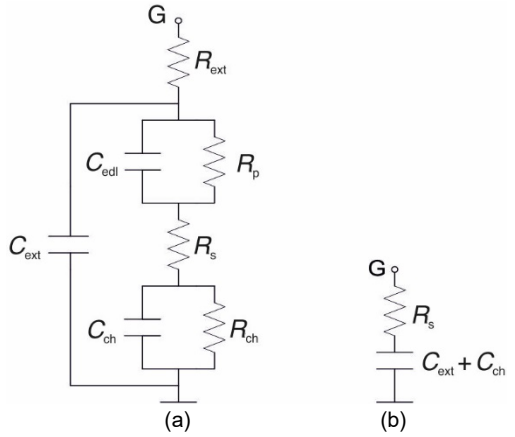

Fig. 2. (a) Small-signal equivalent circuit for OECTs for a drain-to-source short-circuit configuration (V_d = 0 V). (b) Simplified equivalent circuit.

mechanism in OECTs is conditioned by hopping [9], a thermally-assisted quantum mechanical tunneling process that is much slower than transport through organic crystals [10], [11]. This gives rise to a bell-shaped dependence on the gate voltage for the carrier mobility, μ, and transconductance, g_m. Accurate modeling of transconductance is crucial in OECT-based biosensors, as the amplitude of the detected signal is directly proportional to this quantity.

When the OTFT mobility is extracted by a conventional method based on saturation transfer characteristics [12], an underestimated value can be obtained [13]. A more reliable method, in which the transistor operates in the linear region, is known as the Y function method (YFM) [14]. In this case, the extracted OTFT mobility is contact-independent [13].

The capacitance of the device basically consists of two capacitors in series: the capacitance at the channel and the gate interfaces offered by electrical double layers, and the space-charge capacitance. In some applications the former is much higher and can be neglected, leaving only the latter type of device capacitance to be modeled [15]. Due to the low printing resolution of existing techniques, extrinsic parasitic capacitances must also be considered [16].

For simplicity, the DC characteristics of OECTs are approximated assuming behavior similar to that of a metal-oxide-semiconductor field-effect transistor (MOSFET) [17]. The DC current of OECTs is usually modeled based on the assumption of a constant value or a monotonic dependence on the gate voltage for the carrier mobility of PEDOT [17], [18], [19], [20], [21]. Under these conditions, the bell-shaped transconductance observed for OECTs cannot be predicted, as in [20], where a sigmoid function of the gate voltage for the free carrier density is even considered. The bell-shaped transconductance was predicted in [22] using an empirical model. As far as we know, no physical model for PEDOT-based OECTs exists in the literature that can predict this dependence [17], [18], [19], [20], [21], at least if diffusion transport is not involved [23] (see Fig. 6 in [22] for an example).

In the present work, we aim to predict the evolution of the DC current at the voltage terminals in OECTs, including hysteresis phenomena, for circuit simulators. To achieve this, we develop a new method based on the dependence on the gate voltage of the conductivity of PEDOT. Expressions for the free charge density, hole mobility and conductivity, and a derivation of the model for the drain current are described in Section II. The device under test considered here is described in Section III, together with the experimental setup used for the DC and AC measurements. The measured and modeled results are given and analyzed in Section IV. Finally, the conclusions are presented in Section V.

II. Procedure

A. Free charge density

In this work, we consider a channel made of PEDOT:PSS polymer. When a positive gate voltage is applied to an OECT, the cations in the electrolyte are uniformly injected over the entire thickness of the channel; this scenario is usually assumed for modeling purposes [15], [17], [20], and has also been demonstrated through numerical simulations in [7]. This leads to a uniform PEDOT hole concentration, p, as indicated in Fig. 1(a), which decreases with the gate voltage by de-doping.

The de-doping process is described by the following equation:

$$\mathrm{PEDOT^+{:}PSS^- + C^+ + e^- \leftrightarrow PEDOT^0 + PSS^-C^+} \tag{1}$$

where C^+ is a cation injected from the electrolyte and $PEDOT^+$ and $PEDOT^0$ are the oxidized and reduced forms of the polymer, respectively. Similarly to [20] and [24], we propose to apply the Nerst equation to OECTs, with the potential referred to the source electrode, to derive the free charge density in the PEDOT layer as follows:

$$V_g = V_o - V_T \ln \frac{[\mathrm{PEDOT^+}]}{[\mathrm{PEDOT^0}]} \tag{2}$$

where V_o is the equilibrium voltage, V_T = 25.69 mV is the thermal voltage at room temperature (25 °C), and [$PEDOT^+$] and [$PEDOT^0$] are the oxidized and reduced concentrations of the polymer, respectively. [$PEDOT^+$] represents the hole concentration, [$PEDOT^+$] = p, and the sum of [$PEDOT^+$] and [$PEDOT^0$] remains constant (p_o), therefore [$PEDOT^0$] = $p_o - p$. By solving (2), the free charge density in the PEDOT layer, $Q = qp$, where q is the elementary charge, can be expressed as follows:

$$Q = \frac{qp_o}{1 + e^{\xi\left(\frac{V_g - V_o}{V_T}\right)}} \tag{3}$$

where ξ is an empirical parameter used to take into account the effect of deep traps [20]. A sigmoid function is therefore predicted for the dependence of Q on the gate voltage, which is consistent with [7], [23].

To extract Q, we consider the small-signal equivalent circuit for OECTs shown in Fig. 2(a), for a drain-to-source short-circuit configuration (V_d = 0 V) [16]. In this circuit, C_{ext} and R_{ext} are the extrinsic gate-terminal capacitance and resistance, respectively, due to interconnections. The intrinsic gate impedance is modeled using the simplified Randles model [25].

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Thus, C_{edl} is the capacitance at the channel and gate interfaces offered by electrical double layers, and R_p is the electrolyte resistance associated with the polarization resistance or charge transfer resistance. The solution resistance between the gate electrode and the channel is modeled as the resistance R_s. Finally, C_{ch} and R_{ch} are the space-charge (channel) capacitance and resistance in the PEDOT layer, respectively.

The elements of the equivalent circuit were extracted using a MATLAB code, in which the operation frequency and gate voltage were varied, and the gate voltage dependence of the channel capacitance, $C_{ch}(V_g)$, was then obtained. At high frequencies (e.g., 50 kHz) the measured reactance from the gate is approximately the same as the gate capacitance, $C_g \approx 1/[2\pi f \cdot \mathrm{Im}(Z)] \approx C_{ext} + C_{ch}C_{edl}/(C_{ch}+C_{edl})$, where Z is the measured impedance. If additionally, as in many applications of interest, $C_{edl} \gg C_{ch}$, the simplified equivalent circuit shown in Fig. 2(b) can be used [15], [16], for which $C_g \approx C_{ext} + C_{ch}$.

When the gate voltage dependence of the channel capacitance has been determined, the free charge density in the PEDOT layer can be extracted as described in [17], [19]:

$$Q = \frac{C_{ch}(V_g)}{WTL}(V_{th} - V_g) \tag{4}$$

B. Hole Mobility and Conductivity

As previously indicated, to prevent an underestimation of the mobility induced by contact resistances, the gate voltage dependence of the mobility, $\mu(V_g)$, is extracted for the transistor operating in the linear region and through the YFM [13], [14], in which

$$\mu = -\frac{L^2}{V_d C_{ch}(V_g)} \cdot \left[\frac{\partial\left(\frac{I_d}{\sqrt{g_m}}\right)}{\partial V_g}\right]^2 \tag{5}$$

where $g_m = \partial I_d/\partial V_g$ is the transconductance. The YFM was originally used in MOSFETs, for which the capacitance is constant, $C_{ch} = C_{ox}$ (the oxide capacitance), and there is a monotonic dependence of the mobility on the gate voltage: $\mu \propto [1+\theta \cdot (V_g - V_{th})]^{-1}$, with θ as a fitting parameter. In case of PEDOT-based OECTs, a bell-shaped dependence on the gate voltage for both C_{ch} and μ is expected, and the YFM is therefore only applicable if C_{ch} and μ do not vary significantly.

In the literature on hopping conduction in an electric field, the mobility of PEDOT along the channel length has been expressed as $\mu \times \exp(0.17d \cdot E_{\|}/V_T)$, where $d = 30$ nm is the characteristic PEDOT hopping length at room temperature and $E_{\|}$ is the longitudinal electric field [26], [27]. Since $0.17d \cdot E_{\|}/V_T \le 0.17d \cdot (V_{th} - V_g)/(LV_T) << 1$ in an OECT, the weak-field regime of hopping conduction is maintained, and the PEDOT hole mobility (5) is valid for any region of operation. For the carrier mobility, a bell-shaped dependence on gate voltage is expected, similar to the dependence on hole concentration observed in [15], [28].

Finally, by combining (4) and (5), the carrier conductivity of PEDOT, $\sigma = Q\mu$, can be obtained as follows:

$$\sigma = \frac{L}{WT} \cdot \frac{V_g - V_{th}}{V_d} \cdot \left[\frac{\partial\left(\frac{I_d}{\sqrt{g_m}}\right)}{\partial V_g}\right]^2 \tag{6}$$

In this case, the dependence of the channel capacitance on the gate voltage has no influence.

C. Current Equation

When a negative drain voltage is applied, the number of available carriers diminishes from the source to drain terminals, staying constant in any cross-section over the channel length [7]. Fig. 1(b) shows a scheme for the distribution of cations injected from the electrolyte into the PEDOT and the resulting hole concentration in the channel when $V_g > 0$ V, for $V_d < 0$ V.

Thus, for a given quiescent operating point (V_g, V_d), the PEDOT hole concentration depends only on the position along the channel length, $x \in [0, L]$, where x represents the distance from the source terminal. This dependence can be extended to that of the hole mobility and conductivity of PEDOT, since Q and μ are co-dependent [15], [28].

To evaluate the drain current in an OECT, methods based on charge-based compact modeling are commonly used, in which a constant hole mobility is assumed [20]. In this case, in view of the sigmoid function for the dependence of Q on the gate voltage (3), the bell-shaped transconductance observed for OECTs is not predicted.

The dependence of the hole mobility on the gate voltage observed in the transistor (see Fig. 4(b), left axis) suggests the use of a conductivity-based compact model, rather than a charge-based compact one. As described in Section IV, a bell-shaped function is obtained for the dependence of the conductivity on the gate voltage, which is modeled as the derivative of a sigmoid function as follows:

$$\sigma = \gamma + (\sigma_{max} - \gamma)\frac{4 \cdot e^{\frac{V_g - V_{go}}{\alpha \Delta V_{go}}}}{\left(1 + e^{\frac{V_g - V_{go}}{\alpha \Delta V_{go}}}\right)^2} \tag{7}$$

where α is set to 0.567 so that $\sigma/(\sigma_{max} + \gamma) = 0.5$ for $V_g = V_{go} + \Delta V_{go}$; ΔV_{go} accounts for the conductivity deviation; σ_{max} is the maximum conductivity; and γ is a parameter related to the threshold voltage, V_{th}, which is defined as the gate voltage for which the conductivity is zero and is expressed as follows:

$$V_{th} = V_{go} + \alpha \Delta V_{go} \ln\left(\frac{\gamma - 2\sigma_{max} - 2\sqrt{\sigma_{max}(\sigma_{max} - \gamma)}}{\gamma}\right) \tag{8}$$

Ion accumulation close to the drain contact creates some screening of the channel's electric field, which can lead to diffusion transport [7], [23]. For simplicity, to account for this effect, the conductivity of PEDOT is assumed to vary along the channel length of the transistor as $\sigma(V_g - V/\beta)$, with the channel voltage, V, ranging from zero to V_d, and β as a fitting parameter that modulates the drain-to-source voltage for which the channel pinches off, $V_{d,sat} = \beta(V_g - V_{th})$ [22]. Using the gradual channel approximation, the current density is evaluated as $j = \sigma \cdot dV/dx$. Then, by integrating along the channel length, the drain current is as follows:

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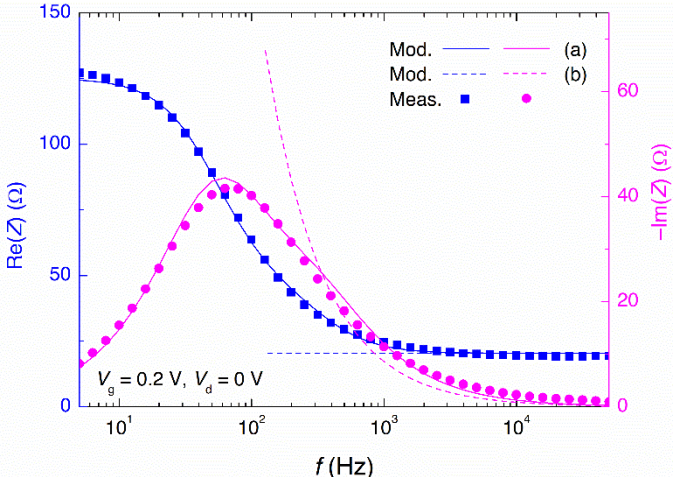

Fig. 3. Comparison between the measured impedance and that modeled with the small-signal equivalent circuit (solid line) and the simplified equivalent circuit (dashed line): real part (left axis) and imaginary part (right axis); V_g = 0.2 V, V_d = 0 V.

$$I_d = \frac{WT}{L}\int_0^{V_d} \sigma dV =$$

$$= \frac{WT}{L}\int_0^{V_d}\left[\gamma + (\sigma_{max}-\gamma)\frac{4\cdot e^{\frac{V_g - V/\beta - V_{go}}{\alpha\Delta V_{go}}}}{\left(1+e^{\frac{V_g - V/\beta - V_{go}}{\alpha\Delta V_{go}}}\right)^2}\right]dV \quad (9)$$

Taking into account the pinched-off channel when $V_{d,sat} = \beta(V_g - V_{th})$ and solving (9) gives the result:

$$\frac{I_d}{1-\lambda V_d} = \frac{WT}{L}\times$$

$$\times\begin{cases}\gamma V_d + F(V_g,V_d) - F(V_g,0) & \text{for } V_d \geq V_{d,sat}\\ \gamma\beta(V_g - V_{th}) + F(V_{th},0) - F(V_g,0) & \text{for } V_d < V_{d,sat}\end{cases} \quad (10)$$

where

$$F(V_g,V_d) = \frac{4\alpha\beta\Delta V_{go}(\sigma_{max}-\gamma)}{1+e^{\frac{V_g - V_{go} - V_d/\beta}{\alpha\Delta V_{go}}}} \quad (11)$$

and λ is a parameter that reflects when the channel-length modulation effect takes place [19]. In case of OECTs, this effect may be associated with effects arising from fringing capacitances at the surface of the channel [29].

The use of the threshold voltage in (8) ensures continuity between the linear and saturation regions of not only the drain current but also the transconductance and output conductance of the transistor (see the Appendix).

Finally, by making use of the transconductance in the saturation region, $g_{m,sat}$, a parameter commonly used in biological sensing applications of OECTs, the conductivity of PEDOT is obtained as follows:

$$\sigma = \frac{L}{WT}\frac{g_{m,sat}}{\beta(1-\lambda V_d)} \quad (12)$$

III. Experimental Setup

A thick-film OECT with PEDOT:PSS as the channel material and (Au/Ni) electrodes has been used in this study. The width, thickness, and length of the channel were 5 mm, 25.5 µm, and 0.5 mm, respectively, and the electrolyte used consisted of a 0.1 M PBS (0.1 M KCl in case of hysteresis phenomena). More details about its fabrication and the rest of the dimensions of the transistor can be found in [22].

Output characteristics were obtained for gate voltages ranging from 0.15 to 1 V, in steps of 0.05 V, and drain voltages from –0.6 to 0 V, in steps of 0.06 V, using a multimeter (Agilent 34401A). A power source (Keysight EDU36311A) was used for biasing of the transistor and data were acquired via instruments controlled by USB.

The gate capacitance, C_g, was experimentally characterized at room temperature by means of impedance measurement using an electrochemical impedance analyzer (PalmSens4, PalmSens B.V., the Netherlands), whose internal potentiostat was used to bias the transistor. The gate electrode was connected to the working terminal, and the source and drain electrodes were connected to the reference voltage and counter. The DC voltage V_g was sweept from 0.1 to 1 V, in steps of 0.1 V, with an AC signal superimposed in the frequency range of 5 Hz–50 kHz and with an amplitude of 10 mV.

IV. Results

By making use of a drain-to-source short-circuit configuration, the frequency response of the real and imaginary parts of the gate impedance was measured. This is shown by the symbols in Fig. 3 for V_g = 0.2 V, as an example, where the results using the small-signal equivalent circuit and the simplified equivalent circuit are represented by solid and dashed lines, respectively, with the real parts shown on the left axis and the imaginary parts on the right axis. Good agreement between the measured data and the results from the small-signal equivalent circuit is achieved, which is also the case with the simplified equivalent circuit at high frequencies. The resulting dependence on the gate voltage of the channel capacitance, with $C_{ext} \approx 4.9$ µF, is shown by the symbols in Fig. 4(a) (right axis); the corresponding trend is also indicated by a dotted line.

The measured output characteristics of the OECT are shown in Fig. 5(a) by closed symbols. The corresponding ideal characteristics (with zero output conductance in the saturation region) are obtained from dividing the measured drain current by $1 - \lambda V_d$, with the value for λ indicated in Table I (with PBS solution), and are shown in Fig. 5(b) by open symbols.

From the ideal characteristics, the threshold voltage (V_{th} = 0.8 V) was determined in the vicinity of the cut-off region from the gate voltage axis intercept of the $(-I_d)^{0.5}$–V_g linear regression in the saturation region of the transistor (not shown) [30]. The Q–V_g characteristic was then obtained by applying (4), and is represented by symbols in Fig. 4(a) (left axis). As expected, the sigmoid function (3) predicts this dependence with values of $p_o = 8.5\times10^{17}$ cm^{-3}, V_o = 0.48 V, and ξ = 0.28, as represented by the line.

The symbols in Fig. 4(b) (right axis) indicate similar bell-shaped dependences on the gate voltage for measured conductivities in the linear and saturation regions, with (6) and

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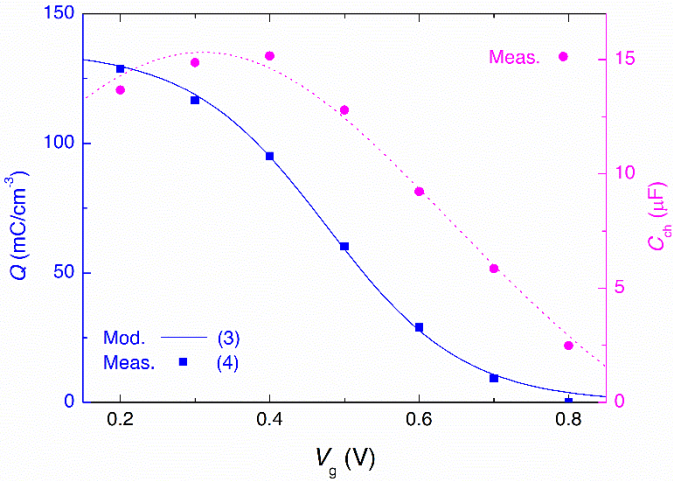

Fig. 4. (a) Extracted channel capacitance (right axis) and free carrier density (left axis) vs. gate voltage (shown as symbols), and the dependence of the modeled free carrier density (shown as a solid line); (b) extracted conductivity (right axis) and hole mobility (left axis) vs. gate voltage (symbols), and the corresponding dependence of modeling results (lines). Inset: dependence of the transconductance in the saturation region on the gate voltage. Measured and modeled results are represented by symbols and a dashed line, respectively; V_d = –0.6 V.

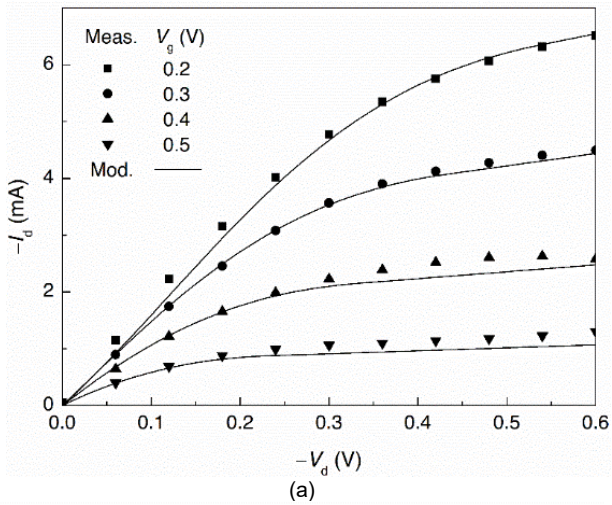

Fig. 5. (a) Output characteristics and (b) corresponding ideal characteristics. Measured and modeled results are represented by lines and symbols, respectively.

Table I. Parameters of the DC Model

Solution	λ (V^{-1})	γ (mS/cm)	σ_{max} (mS/cm)	V_{go} (mV)	ΔV_{go} (mV)	β -
PBS	0.70	–80	600	290	–230	1.0
KCl	0.30	–0.50	195	360	–127	1.8

(12), respectively. From the measured data in the linear region (with a null conductivity in the cut-off region clearly satisfied), the modeled conductivity obtained with (7) can be adjusted with the least squares method. This is represented in Fig. 4(b) (right axis) by a dashed line, and shows good agreement with the measured conductivities. The values for γ, σ_{max}, V_{go}, ΔV_{go}, and β are listed in Table I (with PEDOT solution). The value of V_{th} = 0.74 V obtained from (8) is close to that obtained from the $(-I_d)^{0.5}$–V_g linear regression in the saturation region.

The channel capacitance [see Fig. 4(a) (right axis)] shows a maximum deviation of 6.3% for a gate voltage up to 0.5 V. In this case, the hole mobility determined by the YFM, with V_d = –0.06, is nearly constant, as shown in Fig. 4(b) (left axis) by closed squares, with a maximum deviation of 6.4%. A good agreement with the hole mobility extracted in the saturation region as (12)/(4), which is shown by open squares, is achieved. For gate voltages higher than 0.5 V, near the cut-off region, alternative methods to extract the hole mobility are required [31]. In this case, since few carriers populate the low density of states and hopping between carrier sites is unlikely, a reduction of hole mobility is expected [15], as that modeled as the relation between the conductivity (7) and the free charge density (3) suggests, which is shown in Fig. 4(b) (left axis) by a solid line.

The bell-shaped curve for $\mu(V_g)$ gives rise to the peak in the conductivity and, through (12), to the peak in the transconductance typically observed in OECTs. The inset to Fig. 4(b) shows the measured bell-shaped transconductance in the saturation region (with symbols), with V_d = –0.6 V, which is correctly reproduced by the modeled results (shown as a dashed line), evaluated as $g_{m,sat} = (WT/L)\cdot\sigma$.

The modeled results for the ideal current are shown in Fig. 5(b) by dashed lines. The final modeled output characteristics are shown in Fig. 5(a) by solid lines. In both cases, the measured and modeled results show good agreement.

The validity of our model relies on the observation that the OECT is not operating in the high ion density regime. In this

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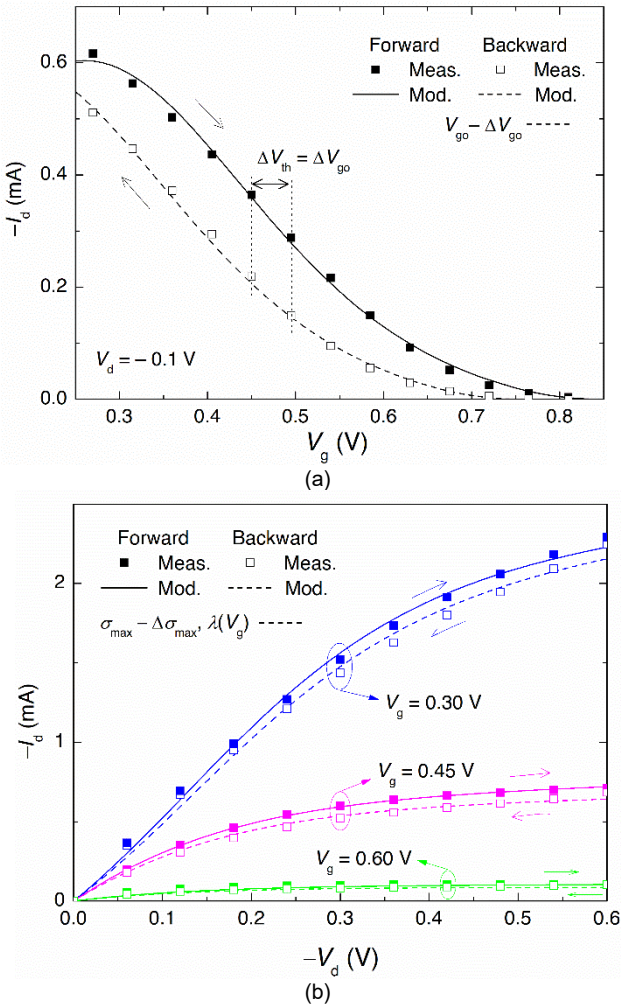

Fig. 6. Hysteresis in (a) transfer characteristics with $V_d = -0.1$ V and (b) output characteristics with $V_g = 0.30$, 0.45, and 0.60 V. Measured forward/backward curves are represented by closed/open symbols and the corresponding modeled results by solid/dashed lines.

regime, the electric field is suppressed and the current in the channel is diffusion-dominated [23]. OECTs based on doped semiconductor are switched off by injecting cations that compensate the dopants, bringing the material to its undoped state. Thus, the hole concentration when the channel is depleted of cations and the cation density when the channel is fully de-doped coincide. Using (3), their values are ~10^{18} cm^{-3} (< 10^{19} cm^{-3}), which is indicative that the OECT does not operate at the high ion density regime and the drift current therefore dominates [23].

Finally, hysteresis was clearly manifested in the OECT when the electrolyte used consisted of a KCl solution, as clockwise and counterclockwise loops in transfer and output characteristics, respectively. Measured forward/backward curves are represented by closed/open symbols in Fig. 6, with the corresponding modeled results shown by solid/dashed lines (the parameters of the model with KCl solution are listed in Table I). As Fig. 6(a) shows, the hysteresis in the transfer characteristics with $V_d = -0.1$ V is modeled by a reduction of the threshold voltage, ΔV_{th}, of 45 mV (the same as that of the gate voltage for the maximum conductivity, ΔV_{go}). Concerning the hysteresis in the output characteristics shown in Fig. 6(b), it can be modeled assuming a reduction of the maximum conductivity, $\Delta\sigma_{max}$, of 70 mS/cm and $\lambda = (V_{th} - V_g)^{1.7}$, which maintains continuity between the linear and saturation regions of the transconductance and output conductance.

Note that the hysteresis induced by ion doping is conditioned by ionic and electronic transit time constants [8]. Therefore, an in-depth analysis of the hysteresis response of PEDOT-based OECTs involves the use of a dynamic model, which will be the object of future work.

V. Conclusion

A conductivity-based compact model for PEDOT-based OECTs has been presented, in which the dependencies of the mobility and free charge density on the gate voltage are considered based on that of the conductivity of PEDOT, which is determined to predict the peak in transconductance typically observed in OECTs. Extraction of the necessary parameters from DC characteristics ensures continuity between the linear and saturation regions of the drain current, and the transconductance and output conductance of the transistor. The model, including hysteresis phenomena, can easily be incorporated into circuit simulators and will be useful in future work involving bio-sensing applications.

Appendix

Equation (8) can be rewritten as follows:

$$\gamma = -\frac{4(\sigma_{max}-\gamma)e^{\frac{V_{th}-V_{go}}{\alpha\Delta V_{go}}}}{\left(1+e^{\frac{V_{th}-V_{go}}{\alpha\Delta V_{go}}}\right)^2} \tag{13}$$

Let us first assume that there is no channel length modulation effect (this is the ideal case, with $\lambda = 0$). Then, when the channel pinches off for a drain-to-source voltage of $V_{d,sat} = \beta(V_g - V_{th})$, the transconductances in the linear and saturation regions ($g_{m,lin}$ and $g_{m,sat}$, respectively) coincide as follows:

$$g_{m,lin} = g_{m,sat} - \frac{4(\sigma_{max}-\gamma)e^{\frac{V_{th}-V_{go}}{\alpha\Delta V_{go}}}}{\left(1+e^{\frac{V_{th}-V_{go}}{\alpha\Delta V_{go}}}\right)^2}\beta - \gamma\beta = g_{m,sat} \tag{14}$$

In addition, the output conductance in the linear and saturation regions ($g_{d,lin}$ and $g_{d,sat}$, respectively) is zero:

$$g_{d,lin} = \gamma + \frac{4(\sigma_{max}-\gamma)e^{\frac{V_{th}-V_{go}}{\alpha\Delta V_{go}}}}{\left(1+e^{\frac{V_{th}-V_{go}}{\alpha\Delta V_{go}}}\right)^2} = 0 = g_{d,sat} \tag{15}$$

If the channel length modulation effect is considered and the channel pinches off, taking into account the continuity of the ideal transconductances and output conductances, $g_{m,lin} = g_{m,sat}$ and $g_{d,lin} = g_{d,sat}$ are again satisfied, these being $(WT/L)(1-\lambda V_{d,sat})\beta\sigma$ and $-I_{d,sat}\lambda/(1-\lambda V_{d,sat})$, respectively, where σ is given by (7) and $I_{d,sat}$ is the drain current in the saturation region.

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