Micro-credentials as an environment for teaching the RISC-V ecosystem

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***Abstract*—This paper presents a training programme based on micro-credentials (short courses) for the RISC-V hardware-software ecosystem. Micro-credentials are a way, proposed by the European Union and adopted by the member countries, to meet the needs for lifelong re-qualification of working people. We propose a training programme around this ecosystem based on the needs (knowledge and skills) of job seekers related to Systems on Chip (SoC) design.**

***Index Terms*—RISC-V, micro-credentials, job re-skilling, SoC, chip design, technology sovereignty**

I. Introduction

Micro-credentials are learning experiences that complement traditional qualifications. They are short courses of between one and fifteen ECTS (European Credit Transfer and Accumulation System) credits, as outlined in the ECTS guide [1]. These courses allow learners to gain specific competencies and skills that are aligned with the needs of society and the labour market, as outlined in the European Commission's 2024 strategy [2].

This initiative of the European Commission has the objective of establishing a standard at the European level that will allow the learning outcomes of these educational experiences to be recognised and understood by employers, learners and education and training institutions. This represents a key component for the European Education Area. In this way, last June 2023, the Ministry of Universities presented the Microcredentials Plan (Microcreds), with an economic endowment for its development in the period 2024-2026 of 56 million euros [3].

In Spain, a group of universities has created the Spanish Open Hardware Alliance (SOHA), based on the paradigm of education, research and innovation. SOHA's goal is to expand the use of open hardware, and its strategy for success is based on the use of RISC-V architecture and Linux.

RISC-V represents a development opportunity in processor architecture because its instruction set (ISA) does not require the payment of licensing fees or royalties. This provides us with the mechanisms to ensure collaborative and efficient development, whether on a national or European level.

In addition, SOHA promotes the UN Sustainable Development Goals (SDGs) related to its area of activity, such as improving energy efficiency, reducing carbon footprint, increasing economic productivity, equal opportunities, increasing access to information and communication technologies (ICTs), and collaborative evolution based on the complicity of the three basic pillars mentioned above [4].

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RISC-V is a specification for an open RISC-type processor architecture with a defined, standardised but open and extensible instruction set architecture (ISA) and an open hardware/software (HW/SW) platform, originally developed in 2010 at the University of California at Berkeley [5].

This feature lays the foundation for the entire ecosystem around RISC-V, which includes: Open source software, commercial software, open source intellectual property (IP) block, commercial IP, and design and verification tools. In this context, micro-credentials - without prejudice to the fact that this technology is being introduced in Spanish vocational training (FP), university degrees and master's degrees - is a fast and effective way to acquire skills and competences in the RISC-V ecosystem.

This work presents an open proposal of different short courses around the RISC-V ecosystem, organised in three levels: basic courses, intermediate courses and advanced courses. The proposed structure allows students to link them appropriately for their training in the design of System-on-Chip (SoC) based on the RISC-V specification and platform. The specific content of these courses is strongly linked to the RISC-V architecture (e.g. 32-bit or 64-bit), the final application, the design of extensions (e.g. vector extension), the simulation of the architecture or the use of electronic design automation (EDA) tools.

Students can choose to specialise in different areas, either in intensive hardware design for different implementation goals, such as the Internet of Things (IoT) and low power, or in complex systems for high-performance computing. This is exemplified by the work being developed in the EPI (European Processor Initiative) [6], which brings together the main technology providers and users.

In the hardware domain, several specialisations can be distinguished, depending on the technology used to implement the SoC, either FPGA programmable devices or ASIC technologies. The design problems are different for each of these technologies, so a tailored approach is required for each use case. Both types of implementation require a basic understanding of digital design, the principles of processor architectures and electronic design based on description languages, as well as synthesis from register transfer level (RTL) specifications.

If the student needs training in software development for the RISC-V architecture, it will be essential to create a training program using flexible programming environments. This includes using compilers that are adapted and optimised for the architecture in order to develop optimised algorithms and applications.

II. Micro-credentials

Technological progress, the transition to more sustainable practices, and demographic challenges are reshaping both economic activities and jobs, as well as other important dimensions of people's lives. The threat of automation is affecting many workers, meaning that their knowledge, skills, and competencies could become obsolete long before retirement.

At the same time, these same processes are generating quality job opportunities that require new skills, which are still scarce in the workforce. This discrepancy between the skills required and those currently available demonstrates the need for a decisive increase in lifelong learning, with the objective of assisting citizens, productive sectors, public administrations and social entities in successfully navigating this transition phase.

A. Re-skilling needs

According to the Organization for Economic Cooperation and Development (OECD), it is estimated that 22% of Spanish jobs are redundant and at high risk of automation, while 30% are at significant risk [7].

On the other hand, the adult population in Spain (15-64 years of age) exhibits the lowest levels of competencies and skills, including reading comprehension, mathematical abilities, knowledge of foreign languages, digital competencies, and soft skills, when compared to the EU and the OECD. Only 4.8% of this adult population demonstrates a high level of reading comprehension, while 4.1% exhibits a high level of mathematical skills.

According to the OECD study, this is attributed to two main components. Firstly, the Spanish adult population aged between 25 and 64 who do not have post-compulsory education is double than the European average. Secondly, for each educational level, the level of competence is significantly lower than that of its European counterparts.

The combination of accelerated technological change and skills shortages generates mismatches in the labour market such that unemployed workers coexist with unfilled jobs.

Fig. 1 shows the increase in vacancies by sector and defined as the proportion of vacant jobs over the total number of salaried persons. In the case of the Professional, Technical Sciences and Information and Communications sectors, there were 15,000 vacancies in 2021. Furthermore, according to this study, 8% of Spanish companies in industry, 12% in construction and 11% in services reported difficulties in finding qualified labour.

According to the report on the socio-economic and labour situation in Spain, the cumulative forecast of employment demand for the period 2018-2030 will have generated 1.8 million jobs due to new activities and 12 million jobs due to replacement needs. Moreover, these data coincide with the progressive ageing of the active population and an increase in the retirement age (67 years). If in 2002 25.4% of the population aged 20-64 was over 50, in 2021 this figure will be 35.2% and in 2031 it is expected to reach 38.2%, according to the Spanish National Statistics Institute (INE). These mismatches in the Spanish labour market and the growth of economic activities driven by the digital and green transition require greater re-skilling needs.

Despite the clear need for re-skilling, the use of lifelong learning in Spain is significantly lower than in other European countries. When we consider the European indicator that defines the percentage of adults aged 25 to 64 who have participated in some training action in the twelve months before the survey, Spain (43%) is far from leading countries such as the Netherlands (64.1%), Sweden (63.8%) or Austria (59.9%). The target for 2025, as outlined in the European Framework for Cooperation in Education of 2021, is 47%, while the Action Plan of the Pillar of Social Rights, approved in Oporto in 2021, sets the target for the year 2030 at 60% (Fig. 2). In conclusion, Spain is situated in a quadrant with the lowest competencies and skills in adulthood and the lowest use of lifelong learning, which would facilitate the alleviation of these deficiencies.

B. Action Plan

In this context, an innovative type of non-conventional educational certification, especially suitable for adult education, has emerged prominently at the international level: micro-credentials.

The European Commission, in its report "Recommendation on a European approach to micro-credentials for lifelong learning and employability" [8], defines them as the record of learning achievements obtained by a learner after a short period of training. In other words, certifications derived from short training courses focused on the acquisition of specific knowledge, skills or competencies, aligned with the needs of the productive sectors.

These credentials are associated with programmes that are flexible and adaptable to the various needs and constraints of adult learners, including through virtual modalities. With a modular structure, each training module makes sense independently and can be accumulated to be combined into broader credentials, such as bachelor's or master's degrees, in customised learning pathways. Institutions with the capacity to generate micro-credential-based programmes include universities, as well as vocational training providers, employment agencies, non-conventional educational providers, private companies and public administrations.

The reconciliation of technological change with employment presents a multitude of challenges. In this context, micro-credentials can be employed as a means of preventing the epochal change from giving rise to a process of polarisation and social fracture. This occurs when a section of the population is unable to comprehend and keep pace with technological, economic and social change, thereby preventing them from fully exercising their social and citizenship rights.

Furthermore, micro-credentials can facilitate the broadening and democratisation of access to higher education. In essence, the flexible access criteria, which incorporate the recognition of professional experience, facilitate the transition from micro-credentials to bachelor's or master's degree studies. Adults who obtain a certain number and type of micro-credentials are guaranteed access to specific higher education programmes, analogous to the current tests for those over 25, 40 or 45 years of age. Finally, micro-credentials, when created with the specific intention of serving vulnerable population groups, such as refugees or immigrants, with the purpose of facilitating the acquisition of relevant competencies and skills to enter the labour market, can become an instrument to promote social inclusion.

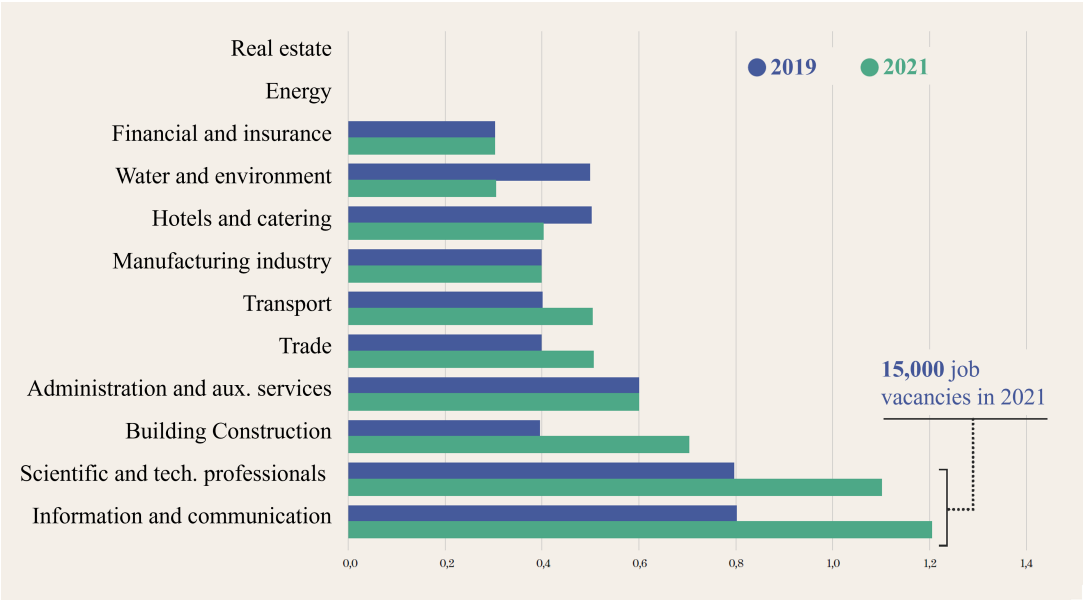

Figure 1: Vacancy rate by sector of activity in Spain (Source: Report on the socio-economic and labour situation 2021, Economic and Social Council, prepared based on Eurostat and Spanish National Statistics Institute (INE) data).

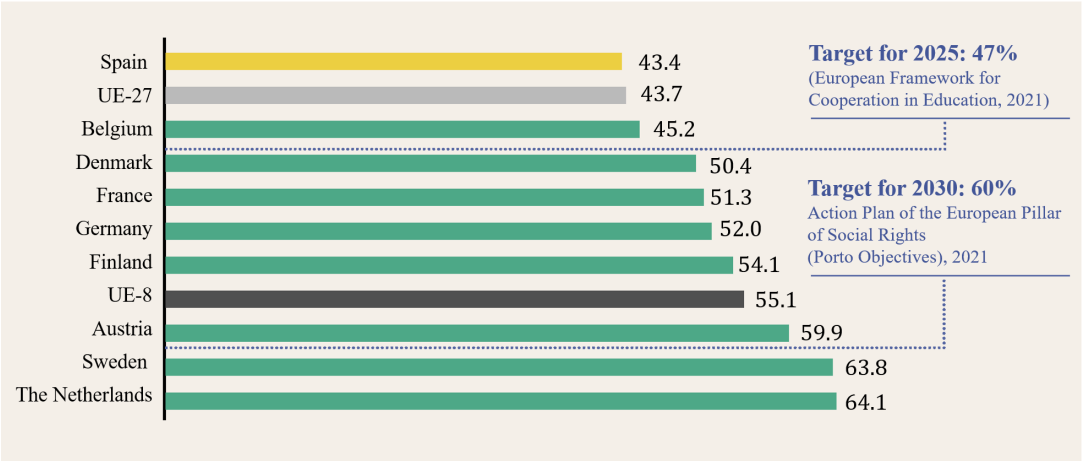

Figure 2: Adults aged 25 to 64 who have participated in some training action in the twelve months prior to the survey (Source: 2019, Eurostat Labour Force Survey).

In this context, the Ministries of Economic Affairs and Digital Transformation; Labour and Social Economy; Inclusion, Social Security and Migration; and Science have developed an action plan based on the concept of micro-credentials. This is aligned with the approach set out in the 2023 report by the Ministry of Science, Innovation and Universities. As previously stated, the approach is limited to the development of university micro-credentials, without prejudice to the actions to be undertaken at other educational levels and in other ministries to establish a plural micro-credential ecosystem that serves the needs of all citizens.

III. RISC-V TECHNOLOGY MICRO-COURSES

As previously stated, micro-credentials represent a potential avenue for teaching the hardware/software ecosystem around RISC-V. If designed appropriately, they could serve as a means of differentiating a population of graduates of engineering careers, graduates, and master's students in the field of information and communication technologies (ICT).

A. Demand from the labour market for RISC-V

Recent data on the evolution of RISC-V in the market indicate that this architecture is experiencing spectacular growth driven by artificial intelligence [9]. Specifically, according to this analysis, the use of RISC-V-based components will grow at a compound annual growth rate of 40%, reaching 16 billion units by 2030, according to RISC-V International CEO Calista Redmond.

Furthermore, a study by ABI Research [10] indicates that the utilisation of RISC-V in artificial intelligence (AI) applications for edge processing in the Internet of Things (IoT) networks (edge AI RISC-V) is in its initial stages. Market penetration will remain stable throughout the remainder of the decade, with an estimated 129 million units sold by

2030 (Fig. 3). The primary technology driving this growth is artificial intelligence platforms, which are predominantly utilised in consumer applications involving home sensors, as well as in manufacturing plants.

These expectations will result in a growing and short-term labour demand for experts in the ecosystem of RISC-V related technologies. In this context, countries such as China, the United States, and India are already investing a significant amount of effort in the development of open-source software applications and hardware platforms. This is done in order to maintain their competitiveness and preserve their sovereignty in key sectors where security is a growing concern.

Similarly, to maintain its technological sovereignty, Europe must respond by creating a critical mass for the development of both open-source software and open-source hardware. The development of a strong European open-source ecosystem should also boost competitiveness, as it enables greater and more agile innovation at lower costs.

To achieve this, however, it is necessary to align and coordinate activities so that the key European players in the sector create the right synergies [11]. In other words, the realisation of such an ecosystem requires a radical change in the work at all levels, with the leadership and contribution of key European industrial and research players and other players in the value chain. A comparable approach is required to that of the European Processor Initiative (EPI) [6], which brings together the principal suppliers and users of technology in the supply chain to produce open-source intellectual property (IP).

B. SoC expertise demanded by companies

SoC design engineers must have a wide range of skills to succeed in this demanding job market. Due to the complexity of the problem to be solved, it should be noted that the process and responsibility for developing an SoC typically falls to a highly structured and specialised team of experts. including product engineers, software engineers, hardware engineers and chip design engineers. Key skills and expertise include the following:

- Logic design with expertise in hardware description languages;
- Processor architecture and its application to SoC design;
- Digital signal processing, image processing, AI architectures, and their integration into a SoC;
- Methodologies, e.g. Universal Verification Methodology (UVM) and verification languages, e.g. SystemVerilog;
- Analogue design and mixed-signal for analogue IPs;
- SoC communication and high-speed interfaces;
- SoC-level synchronisation, clock tree and reset network design;
- Power Management;
- FPGA design and prototyping;
- Programming (C/C++, Python, Assembler);
- RTL synthesis and design for test (DFT), timing analysis;
- Physical design, placement, and routing;
- Post-silicon lab bring-up, evaluation, debugging and test;
- Project management, communication and problem solving.

C. RISC-V software/hardware Ecosystem

The RISC-V initiative requires a complete hardware/software ecosystem to be successful. With this in mind, international institutions, companies, and organisations are focusing their efforts on accelerating the growth and adoption of this technology worldwide. RISC-V International [12], a global non-profit organisation, serves as the epicentre of the open RISC-V Instruction Set Architecture (ISA) standard, as well as its associated specifications and stakeholder community.

By adopting RISC-V, the community can collaborate on shared technical investments, contribute to future strategic development, accelerate the design process, benefit from design freedom, and achieve significant reductions in the costs associated with innovation. In addition, the RISC-V Software Ecosystem (RISE) initiative, established at The Linux Foundation [13], aims to bring together collaborative efforts, led by industry leaders to accelerate the development of open source software tools for the RISC-V architecture.

The software components of the RISC-V ecosystem are diverse and span all layers, from low-level firmware, device drivers, and bootloaders to a fully functional operating system kernel, applications, and design and verification tools. Numerous community efforts address the needs of specific application classes, including ultra-low power computing for IoT, the broad range of embedded systems, and even exascale supercomputing platforms.

Application development requires the availability of drivers and an API that communicates directly with the underlying hardware platform. This low-level software must be implemented using emulators and simulators before the real hardware becomes available. For example, when RISC-V International introduces completely new features into the instruction set, developers face the challenge of waiting two or three years for the system-on-a-chip with the new feature to become available for testing and writing the application software. This highlights the importance of simulation and emulation tools, as well as verification tools, in the design process.

A brief overview of the software ecosystem surrounding RISC-V technology is presented in [14]. This extensive ecosystem includes a wide range of software tools, including simulators, compilers and libraries; debugging tools; boot loaders and monitoring tools; operating systems and kernels; real-time operating systems; development environments; and verification tools.

On the other hand, there are currently over 100 RISC-V cores, 40 RISC-V based SoCs, and numerous SoC platforms available and growing ([15], [16]). While the RISC-V Foundation protects the standard and promotes the free and open architecture of the RISC-V instruction set and its ecosystem of hardware and software for use in all computing devices, many other organisations are building different parts of the RISC-V ecosystem. As an example of these community efforts, a guide to the RISC-V architecture, applications, software and hardware libraries, and ecosystem tools can be found at [17].

IV. Micro-credentialed training structure for the RISC-V ecosystem

Organising education in the RISC-V ecosystem on the basis of micro-credentials implies the need to integrate a complex structure of knowledge into collaborative programmes between institutions and companies. This integration must be done in a way that does not compromise the potential of each

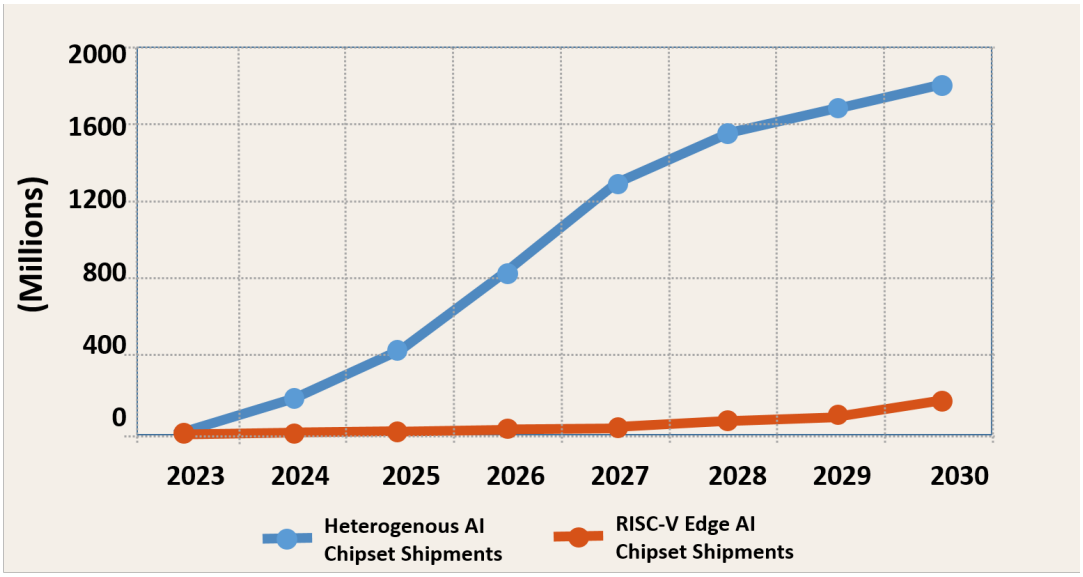

Figure 3: The use of heterogeneous chip-sets for AI is projected to reach over 1.8 billion by 2030. Additionally, by 2030, 129 million RISC-V-based edge AI acceleration systems will be in use (Source: ABI Research Group 2024 Report [10]).

university, while enriching the programme from a global point of view.

It is important, on the one hand, that the training is conditioned by the demand for skills and competences required by employers in the SoC sector and, on the other hand, that the student can choose his or her curricular path within this training, certainly with an interdisciplinary profile that will be enhanced as an expert in different fields.

For the design of a RISC-V based SoC micro-credentialing programme, as it is not covered by a formal programme and allows access to students with heterogeneous starting knowledge, it is necessary that the programme considers and covers the path that the student wants to take to achieve their educational goals and that it has different entry points depending on the student's initial background and interest.

For the sake of simplicity, and if the student (for example, a student with an existing degree in electrical engineering or computer science in Spain) lacks the specific knowledge required to train in the SoC ecosystem based on RISC-V, it is necessary to define a minimum set of knowledge that the student can acquire within the micro-credential programme itself. Furthermore, after the initial phase, the training structure must offer independent courses that allow the student to specialise in some of the skills required by the job market.

As mentioned above, the knowledge and skills required by companies in the sector will influence the structure of SoC training based on micro-credentials for the RISC-V ecosystem. However, it is important to recognise that in order to find an effective solution to this problem, factors such as motivation (labour demand or student enthusiasm for the ecosystem), human resources (experts and support staff), appropriate materials, collaboration between public and private institutions and funding will significantly influence the success of this training.

In this context, the need for collaboration between different institutions is an important factor. This collaboration can facilitate the sharing of resources, such as jointly developed materials that are accessible to students. This contributes significantly to the achievement of the learning objectives. It should be noted that this type of course requires a significant amount of practical training.

The development of practical material involves considerable costs for the institution, both in terms of material resources and development time. By sharing these costs through joint development, a multiplier benefit can be generated in terms of the impact achieved. This is one of the basic principles of the RISC-V community: the sharing of projects developed on GitHub or similar platforms.

Consequently, the availability of both theoretical and practical training material appears to be a solved problem. It has been shown that a considerable amount of effort is required to select the potential practical material and to integrate it into the planned training courses in a productive way.

The lack of documentation of design methods and design processes, a task that is typically supported by minimal information (commercial companies dedicate entire departments to this costly task), does not facilitate the teacher's work. In our view, the teacher's role is to define the starting point, the route to be taken in the micro-credential programme, to select the necessary material and to develop what may not be available. The involvement of interdisciplinary teams will facilitate the achievement of significant results in this task.

The potential heterogeneity of the student population seeking micro-credential-based training has been discussed above. The ability to work independently is a fundamental aspect of this type of programme. In addition to encouraging students to engage in interdisciplinary learning, the creative design process needs to motivate students to engage in their studies, which requires faculty to work intensively with students and apply their expertise to the practical aspects of the training.

In order to promote independent learning, it is beneficial for the micro-credential programme to include lectures, ac-

tivities, experiments, blended learning techniques, internships and workshops or related activities. It is of interest that students publish their significant results obtained as a result of the development of their work, for which the necessary infrastructure should be identified or created. This will add value to the results obtained.

Taking into account the skills required by companies in the chip and SoC design and manufacturing sector, as well as the heterogeneous aspects of the potential student body, we propose a stack structure of micro-courses grouped into three training levels: basic, intermediate and advanced. Each of these levels, organised in modules, allows the acquisition of individualised qualifications.

The modules form a RISC-V training pathway. Each of these modules is organised into 12 credits, with the duration of each course adapted to the level of difficulty. All courses include both theoretical and practical training, with a combination of virtual training for the theoretical aspects and face-to-face training for the practical laboratory training. Fig. 4 shows the general organisation, including the organisation by modules, the duration of the modules and courses, and the titles of the proposed courses developed in this section. It has been assumed that one ECTS credit corresponds to 25 hours of student work, including 10 hours of student-teacher interaction and 15 hours of individual work.

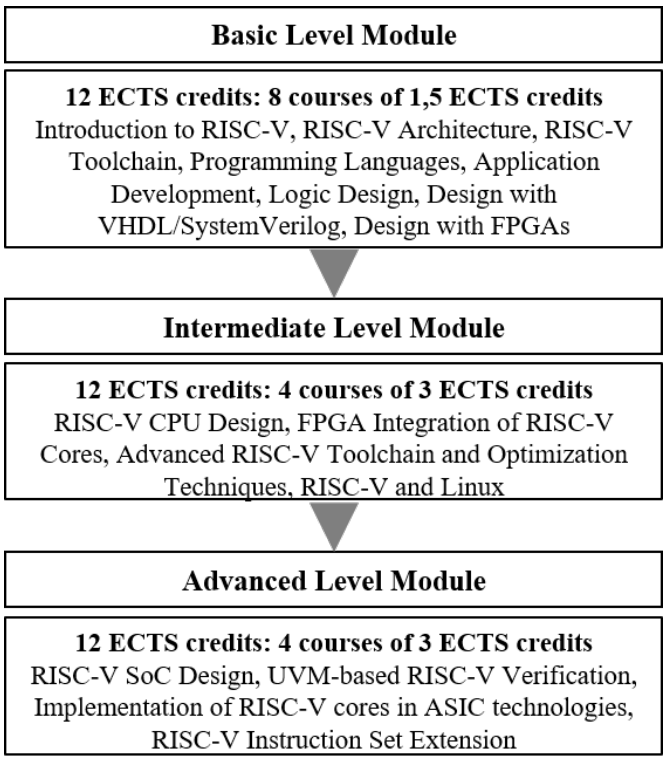

Figure 4: Structure of the proposed micro-credential programme.

A. Basic Level Module.

This module is designed for engineering students and 16+ VET students who wish to gain an understanding of the fundamental concepts of the RISC-V ecosystem. It also covers the skills required to design logic circuits, register transfer level (RTL) circuits and a brief introduction to field programmable gate array (FPGA)-based design. The module is worth 12 ECTS credits. Each course is worth 1.5 ECTS credits.

The following courses are included in this basic module:

- **BM1: Introduction to RISC-V.** This course introduces the RISC-V architecture, the RISC-V ecosystem, and the RISC-V.org community organisation.
- **BM2: RISC-V Architecture.** This course covers the theoretical aspects of the RISC-V ISA architecture: instruction formats, registers, and instruction sets for the different types of architectures.
- **BM3: RISC-V Toolchain.** This course covers hands-on compilation tools, assemblers, and emulation tools, among others, for the RISC-V architecture.
- **BM4: Programming Languages C/C++, Python.** This basic course is aimed at students with no background in the C/C++ and Python programming languages. It also covers the use of Linux-based development tools such as compilers, makefiles, scripts, etc.
- **BM5: Application Development.** The aim is to develop complete applications on existing emulators and platforms using RISC-V based processors using either baremetal or FreeRTOS approaches, for example.
- **BM6: Logic Design.** This course introduces the basics of logic design, covering combinational design, aspects of data representation, arithmetic circuits, state machines, and finite state machines with data path (FSMD).
- **BM7: Design with VHDL/SystemVerilog.** This introductory course covers the principles of design with hardware description languages using either VHDL or SystemVerilog and their use in simulation environments.
- **BM8: Introduction to FPGA Design.** This course covers the application of the concepts of logic design and design with HDL for the implementation in FPGA devices of various blocks designed at the RTL level.

B. Intermediate Level Module.

Intermediate level courses are worth 3 ECTS credits and require the student to demonstrate that he/she has achieved the basic level learning outcomes. The module is worth 12 ECTS credits.

The courses included in this module are the following:

- **IM1: Designing a RISC-V CPU.** This course explains the process of designing a basic CPU to execute a subset of instructions for integer data types. The course includes a simulation of the designed functional units in HDL and their control.
- **IM2: FPGA Integration of RISC-V Cores.** An existing RISC-V core will be integrated into an FPGA board capable of running a RISC-V or FreeRTOS based application.
- **IM3: Advanced RISC-V Toolchain and Optimisation Techniques.** This course covers various advanced tools from the RISC-V ecosystem and introduces various code optimisation techniques and their incorporation into the compiler.
- **IM4: RISC-V and Linux.** The course covers the selection of Linux-OS supported cores, their integration into an FPGA SoC, the compilation of the boot environment, the configuration of the kernel and the applications included in the **rootfs**.

C. Advanced Level Module.

The advanced level courses are also 3 ECTS credits and require the student to have achieved the learning outcomes of the intermediate level. The module also involves a workload of 12 ECTS credits.

The following courses are included in this advanced module:

- **AM1: RISC-V SoC Design.** This is an advanced course where system-level aspects such as bus architecture, memory hierarchy, interrupts or traps, operating modes, etc. are considered. The resulting architecture is simulated and performance is measured using benchmarks.
- **AM2: Verification of RISC-V based on UVM.** The basic concepts of the UVM (Universal Verification Methodology) and its application to the verification of RISC-V based CPUs are explained.
- **AM3: Implementation of RISC-V Cores in ASIC Technologies.** This advanced course aims to introduce the student to the design-oriented design methodology for ASIC technologies, including RTL synthesis, optimisation, DFT, physical implementation and sign-off processes. Post silicon lab bring-up, evaluation, debug and test.
- **AM4: Extending the RISC-V Instruction Set.** This course proposes the definition and implementation of new specialised instructions to support application acceleration, including matrix operations, machine learning, etc.). Also includes the development of software support for the new instructions: compiler, libraries, drivers for Operating System (e.g. Linux), etc.

V. Conclusions

Micro-credentials, unlike regulated studies (bachelor's and master's degrees), can, according to their definition and objectives, be an effective and rapid educational tool for updating the labour profile of active people throughout their working life. That is to say, a means of continuous re-qualification of the workforce. In this sense, we have designed a training proposal around the RISC-V ecosystem to meet the labour demand and re-qualify the active population interested in SoC training.

This training proposal, based on micro-credentials, has been structured in three modules: basic, intermediate and advanced, of 120 hours (12 credits) each. Each module is organised in a series of courses with corresponding exercises in such a way as to achieve the objectives of the training applicant. The ultimate goal is to meet the needs and training interests of the (changing) job market around the RISC-V ecosystem.

The fundamental premise of this training is that its success is contingent upon the principles of collaboration – a cornerstone of the RISC-V community. This implies the coordinated efforts of diverse research and educational institutions, as well as the business sector, to deliver this training in a unified manner, sharing both material and human resources.

In addition, and no less important for collaboration, given the strategic positioning of micro-credential-based training as presented above, there must be permanent funding for the development of this training, and the teaching effort invested should and must be recognised as teaching merit that can be consolidated in the activity of the teaching staff.

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