The demanding requirements arising from electronic device users as well as next-generation Wireless Sensor Networks (WSNs), 5G technologies and Internet of Things (IoT) applications force integrated circuits designers to explore alternative topologies, techniques, and design procedures to be able to meet stringent latency, data rate, power consumption, gain, noise and area specifications. The thesis addresses these issues for radiofrequency (RF) and mmWave circuits in CMOS, SOI and III-V compound technologies. Major contributions are focused on Low Noise Amplifier (LNA) performance metrics and area reduction techniques both in RF and microwave (MW) frequencies.

The work in RF frequencies, centered in LNAs for WSN nodes, resulted in the design and measurement of a wideband Second-Generation Controlled Current Conveyor (CCII) based RF-VGA (RF-Variable Gain Amplifier) in a low-cost SiGe BiCMOS process. With this technique a wideband behavior in an inductor-less circuit is obtained, reporting the lowest die footprint of all the solutions available in the literature, to the best of the author's knowledge. Moreover, the higher the gain, the lower the power consumption drawn by the circuit, due to the nature of the CCIIs employed. The Noise Canceling (NC) technique is exploited in a second version of the amplifier to further reduce the Noise Figure (NF) of the circuit by more than 1.5 dB and introduce a remarkable linearity enhancement, with an IIP3 of 7.6 dBm. A current reuse feedback amplifier for Wake-Up-Receivers (WuRs) is introduced as well to demonstrate a sensitivity improvement from –63.2 dBm to –75 dBm, and area reduction from 36,800 μm^2 to only 700 μm^2 while power consumption is halved to 3.63 µA.

5G K-band LNA contributions are centered in GaAs and SOI technologies to achieve ultra-low-NF performance exploring the limits of the Process Design Kits (PDKs) employed. Major contributions include a design procedure to obtain a sub-1.4-dB NF GaAs LNA in a 100nm UMS technology node, and a sub-1-dB NF GaAs LNA in a 70nm OMMIC technology node, both with a gain of more than 25 dB in a four-stage approach. Both circuits follow a detailed design procedure that allows exploiting the maximum performance of the PDK to achieve a very competitive performance. We propose a combination of current-density and 50-Ω-S_{opt}-real-part oriented design approach combined with a custom high-Q gate inductor implementation to obtain the lowest NF possible. Then, we move to a SOI technology node to reduce power consumption, area and manufacturing costs. To further reduce power consumption and exploit MOSFET efficiency, we explore the application of the g_m/I_D methodology in a second version of the SOI cascode LNA, demonstrating significant power savings from 9 mW to less than 2 mW with a small sacrifice in the overall performance. The proposed LNA achieves the best performance trade-off of all the solutions identified in literature, furthermore, the design methodology is combined with the previously introduced approaches to provide a straightforward procedure, allowing mmWave low-power, high-performance LNA designs. In addition, a 0.38-V fully differential LNA implemented in 45nm CMOS SOI technology from GlobalFoundries is demonstrated using transformer based matching networks. The LNA reports, to the best of the author's knowledge, the lowest power consumption and NF of all the works available in the literature, and a remarkable trade-off between gain, bandwidth, NF, power consumption and area.

Ph.D
RFIC/MMIC Low Noise Amplifiers (LNAs) for Wireless Communications
David Galante

RFIC/MMIC

Low Noise Amplifiers (LNAs) for Wireless Communications

Universidad de Las Palmas de Gran Canaria
David Galante Sempere
PhD Thesis

Las Palmas de Gran Canaria
April 2024

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PROGRAMA DE DOCTORADO EN TECNOLOGÍAS DE TELECOMUNICACIÓN E INGENIERÍA COMPUTACIONAL

TESIS DOCTORAL

"RFIC/MMIC Low Noise Amplifiers (LNAs) for Wireless Communications"

Amplificadores de Bajo Ruido (LNAs) RFIC/MMIC para Comunicaciones Inalámbricas

David Galante Sempere

Las Palmas de Gran Canaria, April 2024

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UNIVERSIDAD DE LAS PALMAS DE GRAN CANARIA

RFIC/MMIC Low Noise Amplifiers (LNAs) for Wireless Communications

A dissertation submitted in partial satisfaction of the requirement for the degree Doctor of Philosophy

in

Telecommunication Technologies and Computational Engineering

by

David Galante Sempere

Committee in charge:

Professor F. Javier del Pino Suárez
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2024

The dissertation of David Galante Sempere is approved, and it is acceptable in quality and form for publication on microfilm and electronically:

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Amplificadores de Bajo Ruido (LNAs) RFIC/MMIC para Comunicaciones Inalámbricas

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DEDICATION

To my family

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Abstract of the Dissertation

RFIC/MMIC Low Noise Amplifiers (LNAs)

for Wireless Communications

by

David Galante Sempere

Doctor of Philosophy in Telecommunication Technologies and Computational Engineering

Universidad de Las Palmas de Gran Canaria, 2024

Professor Javier del Pino, Chair

The demanding requirements arising from electronic device users as well as next-generation Wireless Sensor Networks (WSNs), 5G technologies and Internet of Things (IoT) applications force integrated circuits designers to explore alternative topologies, techniques, and design procedures to be able to meet stringent latency, data rates, power consumption, gain, noise and area constraints. The thesis addresses these issues for Radiofrequency (RF) and mmWave circuits in CMOS, SOI and III-V compound technologies. Major contributions introduced are focused on Low Noise Amplifier (LNA) performance metrics and area reduction techniques both in RF and Microwave (MW) frequencies.

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Acronyms

ADC Analog-Digital Converter

ADS Advanced Design System

BLE Bluetooth Low Energy

CMFB Common-Mode Feedback

CMOS Complementary Metal-Oxide Semiconductor

CMRR Common-Mode Rejection Ratio

DAC Digital-Analog Converter

DRC Design Rule Check

EDA Electronic Design Automation

ESD Electrostatic Discharge

FET Field-Effect Transistor

GaAs Gallium Arsenide

g_m FET transconductance in Siemens (S = 1/A)

G_{max} Maximum Gain

GaN Gallium Nitride

GBW Gain Bandwidth

G_{min} Optimum Source Impedance for NF_{min} in Cadence and Spectre ($=S_{opt}$)

HVT High Voltage Threshold

IC Integrated Circuit

I_{DS} Drain-Source DC current in a FET in Amperes (A)

IEEE Institute of Electrical and Electronics Engineers

IoT Internet of Things

IoE Internet of Everything

IIP3 Third Order Intercept (input referred)

ISM Industrial, Scientific and Medical

LNA	Low-Noise Amplifier
LPF	Low-Pass Filter
LR-WPAN	Low-Rate WPAN
LVS	Layout vs Schematic
LVT	Low Voltage Threshold
MAC	Medium Access Control, referred to the layer with the same name in the OSI network model.
MCU	Microcontroller Unit
MIMCAP	Metal-Insulator-Metal CAPacitor
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NF	Noise Figure
NF_{min}	Minimum Noise Figure
NVT	Native Voltage Threshold
OA	Operational Amplifier (op-amp)
O-QPSK	Offset Quadrature Phase Shift Keying
OTA	Operational Transconductance Amplifier
PA	Power Amplifier
PAC	Peer-Aware Communications
PGA	Programmable-Gain Amplifier
PHY	Physical, referred to the physical layer of the OSI model
PLL	Phase-Locked Loop
PVT	Process-Voltage-Temperature
RF	Radio Frequency
RFID	Radio Frequency Identification
RVT	Regular Voltage Threshold
S11	Input return loss, input reflection coefficient or input matching

S22	Output return loss, output reflection coefficient or output matching
S21	Direct gain
S12	Reverse gain or isolation coefficient
S_{opt}	Optimum source impedance for NF_{min}
SIG	Special Interest Group
SOI	Silicon-On-Insulator
TLR	Topological Layout Rules
ULV	Ultra-Low Voltage
UMC	United Microelectronics Corporation
VCO	Voltage-Controlled Oscillator
VCVS	Voltage-Controlled Voltage Source
V_{DS}	Drain-Source DC voltage in a FET
VGA	Variable-Gain Amplifier
V_{GS}	Gate-Source DC voltage in a FET
WPAN	Wireless Personal Area Network
WSN	Wireless Sensor Network

THESIS

1. Introduction

1.1 Motivation

Radio Frequency Integrated Circuits (RFICs) and Monolithic Microwave Integrated Circuits (MMICs) are present in a wide range of advanced high technology applications, ranging from smartphones, wireless networks (such as Bluetooth or Wi-Fi), and millimeter-Wave (mmWave) systems to the deployment of radio and television satellites, Radiofrequency Identification (RFID), radiometry, spectroscopy, ultra-wideband radar systems, and remote environmental monitoring systems [1]. Even military and defense systems rely heavily on microwave technologies, not to mention consumer electronics, which is a growing field with very demanding specifications. For this reason, there is a growing demand for engineers who can tackle the challenges posed by current technologies and emerging applications. In fact, some of the challenges RFIC and MMIC designers are facing include achieving high performance, high efficiency, low power, low noise, compact area, low costs, high linearity, high level of integration, high speed, lower latency, and many others [2]. For instance, the market demands analog systems that are compatible with Complementary Metal-Oxide-Semiconductor (CMOS) processes and are capable of supporting multiple Internet of Things (IoT) device applications [2].

One of the fundamental enablers of IoT applications are Wireless Sensor Networks (WSNs), which are used for remote sensing and data monitoring. WSNs are one of the key enabling technologies for smart cities, as they are composed by low-cost, low-power nodes with a long lifespan capable of remote monitoring and sensing for many critical scenarios and hostile environments [3]. This is because, thanks to their limited size and to their communication capabilities, WSN nodes can be placed in areas humans can hardly reach. For this reason, WSNs are under extensive research and are especially interesting for harsh environments as well as for hazard areas, natural disasters, and polluted areas. One of the main components of a common WSN node is the Wake-up-Receiver (WuR), which enables very low-power consumption operation and a reduced

latency. The WuR can shut down the main Microcontroller Unit (MCU) of the node without losing the ability to listen to the communication channel, so that, when a certain sequence is received, the node knows it is being addressed and can resume normal operation [4]. However, due to this very low power consumption condition, the achievement of high-performance metrics such as high-sensitivity and low-latency are challenging and hardly met in practice. Therefore, both academic and industry researchers study different techniques and solutions to overcome the mentioned WuR limitations and improve their efficiency and performance while keeping low-power operation. Furthermore, improving WuR integrability and area entails cost reductions for the complete WSN node as RF circuits tend to be bulky because of the passive components used for impedance matching and filtering [5].

On the other hand, another IoT key enabling technology is the development of 5G networks [2]. The growing interest in providing faster connectivity to mobile devices resulted in the development of 5th Generation (5G) technologies, which leverage the available bandwidth in mmWave frequencies to offer data rates up to 10 Gbps. Furthermore, 5G technologies maintain extremely low latency and require high capacity from base stations [6]. As a result, users experience significantly better quality of service compared to 4G (4th Generation) LTE (Long-Term Evolution) networks. To achieve these goals, 5G networks operate both at low frequencies and bands in the tens of gigahertz range, including X, Ku, K, Ka, V, and W bands. For electronic devices to utilize 5G networks, it is necessary that the communication systems operate at these very high frequencies while maintaining a reasonably low power consumption and low costs. Additionally, these devices are intended to offer high-density communications, requiring systems to perform regularly in the presence of multiple interferers while maintaining low noise figures. Although 5G technologies define multiple frequency bands, the K-band is particularly interesting for the following reasons. The K-band ranges from 18 to 26.5 GHz, and is surrounded by Ku (K-under, ranging from 12 to 18 GHz) and Ka (K-above, ranging from 26.5 to 40 GHz) bands. The high-end of the K-band is generally used for high-resolution radar, satellite communications (SATCOMs), short range military aircraft radios and astronomical observations. Specifically, the 26-GHz frequency band was detected as a leading band for 5G new radio (NR) networks in Europe [6]. In fact, bands n257 (26.5-27.5 GHz) and n258 (24.25-27.5 GHz) have been defined for European communications in the 5G spectrum allocation. The n257 and n258 bands can provide

very high data rates and data capacity, which makes them perfectly suitable for hotspot coverage. Moreover, the USA, Japan and Korea identified the 27.5–28.35 GHz, 27.5–29.5 GHz and 26.5–29.5 GHz frequency bands, respectively, for the same purpose [6]. Note all these frequency bands are around 26~28 GHz, therefore, the implementation of an ultra-low noise figure (NF) low noise amplifier at this frequency is fundamental since 5G applications all over the world benefit from any advancements, improvements or new methodologies introduced.

As argued, wireless communications have become a fundamental feature of any electronic device, both in consumer electronics and industrial applications. Many different standards and technologies have arisen to cover the demanding performance required by contemporaneous applications. A wireless transceiver is responsible for transmitting and receiving RF signals, unlocking this wide range of advanced applications. Due to the nature of their task and the complexity involved, transceivers are frequently one of the most power-hungry components of any electronic device. The focus of this thesis is centered on one of the main components of a receiver radio interface: the Low-Noise Amplifier (LNA).

A transceiver integrates both a Transmitter (Tx) and a Receiver (Rx) on the same chip. In Fig. 1.1 a block diagram a transceiver with a traditional structure is shown. The LNA is placed in the receiver branch, which plays the role of amplifying the signal received by the RF antenna while contributing minimal noise and performing impedance matching to maximize the power transfer of the incoming signal [1], [7]. Depending on the architecture, the LNA can present a fixed gain or a variable gain, in the latter case it is also known as a Radiofrequency Variable Gain Amplifier (RF-VGA) or Variable Gain LNA (VG-LNA) [8]–[10]. Next in the Rx chain there is a mixer, which receives a tone of a specific frequency from the Local Oscillator (LO) to down convert the RF signal to intermediate frequencies (IF) or baseband (BB). After the mixer, there is a filter that allows channel selection, thereby rejecting interference or adjacent channels that interfere with the main signal. Finally, there is a variable gain amplifier (VGA) that allows for adjusting the signal level at the output of the Analog-to-Digital Converters (ADCs), optimizing the conversion process.

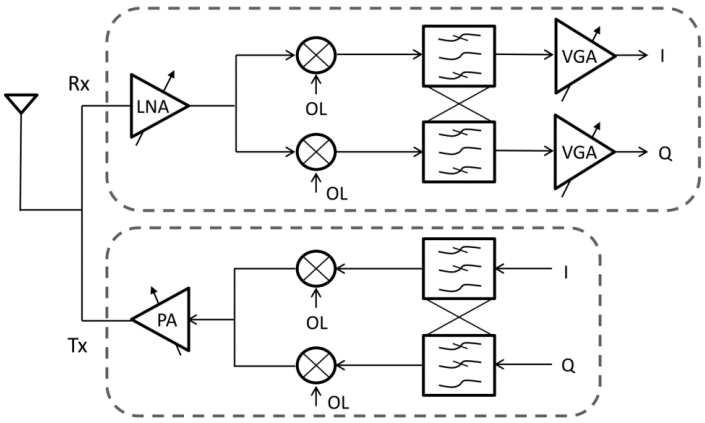

Fig. 1.1. Conventional transceiver scheme [11].

This thesis project focuses on the study of integrated LNAs for RF and MW frequencies (or, equivalently, LNAs for RFICs/MMICs) with the objective of developing techniques to improve their performance metrics, area and efficiency. These circuits constitute one of the critical blocks in wireless communication systems. As LNAs are the first element in the reception chain, their NF and gain (G) determine the performance of the entire receiver [4], [5], [12]. Therefore, the operation of the LNA is critical for wireless communication systems, and its study and improvement are necessary to meet the challenges outlined earlier.

The design of LNAs is not a straightforward procedure. Depending on the operating frequency, the designer can adopt different strategies. For instance, low frequency designs (RF is considered low frequency compared to MW and usually ranges from MHz to a couple GHz, i.e., 2 to 3 GHz) can employ a higher number of transistors since parasitic capacitances are not so critical for the circuit's operation as in a high frequency scenario (e.g., 28 GHz). In MW LNA designs the capacitances must be minimized because they severely limit the bandwidth of the circuit and the performance (the parasitic capacitances affect the transistor f_T, which is related to the NF and G parameters) [1], [12]–[14]. On the other hand, the size of passive components is also critical in RF designs since the lower the operating frequency, the bulkier the passive components needed. The opposite is also true, as the operating frequency rises, the more compact the passive components become [12], [15]. In addition, MW scenarios benefit from the use of distributed components such as transmission lines or stubs and can be combined with lumped components (e.g., inductors and capacitors). In contrast, distributed elements are avoided

in RF circuits due to their size. This can be easily explained by the relation between the wavelength (λ) and the passive component size [15].

A conventional LNA design procedure in MW frequencies involves careful selection of the device and its DC biasing conditions, proper choice of source and load impedances, DC biasing circuitry design and stability concerns [12]. Generally, to obtain certain specifications the designer selects the most suitable device, then chooses the impedances that yield maximum gain, minimum NF or a trade-off between the two. Then the matching networks required are implemented with as many passive components as needed. Nevertheless, current applications require a conscientious design procedure that caters power consumption as a critical parameter but ensuring the desired performance is achieved. This is why we delve into studying a design procedure that allows a very high performance LNA while we minimize power consumption. In addition, IC integration is also one of the most critical aspects that permit introducing as many circuits as possible in a reduced area, which is why we provide techniques focused on area reduction and compact LNAs, discussing the trade-offs involved in every design decision made.

When it comes to integrated LNA implementations, it is possible to use silicon-based technologies, Silicon-on-Insulator (SOI) processes or compound semiconductors (e.g., SiGe, GaAs, SiC, etc.). Silicon-based technologies, specifically conventional bulk-CMOS, offer a low-cost and high integration density solution. These characteristics make CMOS technologies accessible for a wide range of applications and facilitate integration between different applications. On the other hand, state-of-the-art III-V compound technologies provide significantly superior performance compared to conventional bulk-CMOS and SOI [7]. They offer lower NF, greater thermal and chemical stability, higher breakdown voltage, increased conductivity, and higher cutoff frequencies [16]. However, due to the challenges associated with processing these materials and manufacturing devices, the costs are much higher than those of silicon. For these reasons, III-V technologies are typically used in circuits where the performance of silicon processes is not sufficient to meet the required specifications. In any case, the fabrication of circuits using III-V technologies, as well as their presence in scientific publications, has increased dramatically in the last decade. SOI processes allow the achievement of remarkable results and the development of very high-performance circuits. In fact, SOI technologies are getting closer to the performance achieved with III-V processes [14], but III-V compounds –despite their higher price-per-mm^2– present numerous advantages and are

suitable for many applications with challenging specifications. For instance, gallium nitride (GaN) circuits are clearly superior in terms of power management, efficiency, and breakdown voltage, making them the favorite choice in power amplifier (PA) and high-power amplifier (HPA) design [17]. On the other hand, gallium arsenide (GaAs) technologies are more suitable in applications with challenging NF specifications at higher frequencies [4,5]. Such scenarios include mmWave applications, SATCOMs or 5G networks. In addition, MMIC processes, in contrast to conventional bulk-CMOS or SOI technologies, are particularly suitable to implement full radio interfaces in a single chip [15].

For all the aforementioned reasons, the study of LNAs is proposed in both silicon-based technologies (CMOS, SOI, etc.) and state-of-the-art technologies based on III-V compounds (SiGe and GaAs). This thesis project is part of the Research Program in Microelectronics Technology and Telecommunication Circuits, aligning with the objectives it pursues.

1.2 Thesis Overview

This thesis is focused on contributing to the state-of-the-art design of integrated high-performance, compact and low-power LNAs for next-generation wireless communication systems in SOI and III-V technologies for RF and MW frequencies. The thesis aims to contribute innovative techniques, combinations of techniques and design procedures to improve LNA performance, reduce area and power consumption, and optimize the performance trade-offs related to high-frequency IC design (shown in Fig. 1.2).

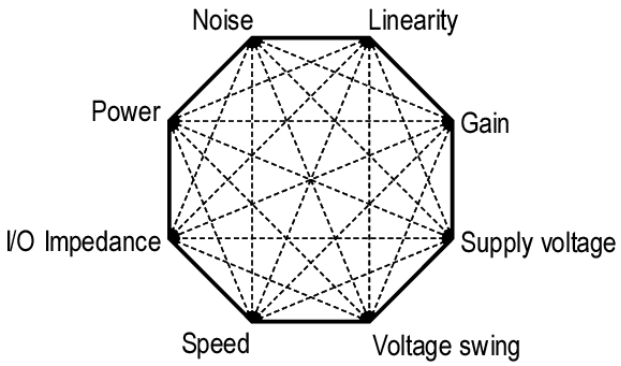

Fig. 1.2. Behzad Razavi's Analog Design Octagon of performance trade-offs [1].

The fundamental hypothesis for the development of the proposed dissertation is that there is a possibility to substantially improve the performance of state-of-the-art integrated LNAs in both RF and MW applications. Overcoming the actual limitations and exploiting the performance of LNA implementations in silicon-based technologies is of vital importance to facilitate their integration and accessibility in a wider range of applications and to improve state-of-the-art performance. We study CMOS LNAs for low-frequency WSN applications and move to SOI and III-V compounds for high-frequency MW scenarios. The development of LNAs in III-V and SOI technologies is particularly interesting due to their applications in multiple high-value sectors, such as the deployment of 5G base stations, spectroscopy, defense, and military applications. Similarly, SOI processes provide an intermediate solution between CMOS and III-V compounds in terms of manufacturing costs and performance. CMOS circuits have a lower price-per-area than SOI technologies, and SOI circuits have a lower price-per-area than III-V compound chips.

The main objective of this thesis is to study design techniques that can enhance LNA performance in current wireless communication systems. In particular, the focus is on improving parameters such as matching losses, power consumption, area, gain, and NF. The purpose of this study is to facilitate the implementation of these circuits and make a significant contribution to the current state of the art. The specific objectives of this thesis are as follows:

Obj. 1: Study the main performance improvement solutions. To make a relevant contribution to the state-of-the-art implementation and techniques for improving LNA performance, an in-depth study of the state of the art is conducted. Some of the most interesting techniques are Noise Cancelling, Current Conveyors, Current Reuse, and feedback techniques. Additionally, various design methodologies are discussed and explored which, in combination with the aforementioned techniques, can lead to optimal results. To cover the first objective, all the works presented are supported by a conscientious study of state-of-the-art solutions as well as the design techniques and procedures presented.

Obj. 2: Identification of the main limitations in the implementation of performance improvement techniques. After studying the techniques, the aim is to delve into their implementation in real communication systems. Specifically, during this

process, the goal is to identify the limitations and trade-offs encountered during the LNA design flow. To comply with this objective, all the works presented compare the state-of-the-art solutions and performance with the proposals introduced, giving relevant insights of the design procedure. We detail all the sizing information and design decisions as well as the technology nodes used to ensure that the results can be reproduced.

Obj. 3: Conducting tests and simulations with different performance improvement techniques. Based on the study of performance improvement techniques, the intention is to analyze circuits that combine different solutions. During the thesis, various experiments and prototypes with these techniques are developed, some of the works present post-layout simulations with Monte Carlo results and EM simulations, which is considered enough to provide a solid conclusion, whereas some others provide measurement results to support the hypotheses presented. As a result of these experiments, we present several enhancements of the performance of low-noise amplifiers and provide solutions to the challenges identified.

- Obj. 3.1: On one hand, the design effort is first focused on the development of techniques in RF circuits in SiGe and CMOS technologies, providing innovative solutions, techniques, combinations of techniques and design procedures to the state of the art.

- Obj. 3.2: On the other hand, tests with circuits operating in MW bands are explored in GaAs and SOI technology nodes, making a significant contribution to state-of-the-art K-band LNAs as well.

Obj. 4: Exploitation and dissemination of the results obtained. This objective includes presenting scientific articles in high-impact specialized journals, as well as international conferences and preparing and defending the PhD thesis. Essential results exploitation and dissemination include the development of design methodologies that can be exploited by the academy and industrial companies in the field of IC design. Another form of dissemination and exploitation is through the development and commercialization of innovative tools that facilitate the analysis of microwave integrated circuits, as well as knowledge transfer in the form of know-how commercialization.

Considering the previous discussion, the PhD thesis outline can be summarized as follows:

- The thesis contributions can be divided into two categories, RF and MW amplifiers. We first develop numerous LNAs for WSNs and RF applications centered in area reduction, lowering costs-per-node and reducing power consumption without significant performance penalties [20]. We develop a silicon-germanium (SiGe) BiCMOS (bipolar-CMOS) very compact, low-power, low-voltage wideband RF-VGA with the lowest area reported [5]. We then introduce improvements in the LNAs used in wake-up-receivers reporting a very compact, low-power and low-cost tuned-RF topology [21]. Finally, an inductor-less wideband CMOS noise-canceling, current conveyor-based LNA is proposed. The circuit achieves remarkable linearity, a very compact area, and a very high Figure of Merit (FoM) when compared to similar state-of-the-art contributions.
- The effort is then focused on MW LNA designs. In these works, the design of GaAs sub-1.4-dB NF LNAs are presented. To achieve such a challenge, the design of a very low NF LNA is explored first using commercial III-V compounds to reach a sub 1.4 dB NF [22] by introducing an efficient design procedure to achieve ultra-low-NF LNAs. Afterwards, the same LNA is moved to a high-performance OMMIC PDK to achieve an LNA with an NF lower than 1 dB [23]. Since III-V compounds present a very high price-per-area, we move the 1.4-dB NF LNA from GaAs to a GlobalFoundries (GF) SOI kit. A prototype cascode LNA with a 3.0-dB NF is demonstrated in a more affordable PDK. This paper has been already submitted and we are currently expecting the revisions and acceptance notification. Next, we explore power reduction techniques to maintain the achieved performance but improving power consumption. Two lines are born from this decision. On the one hand, a 0.9-V g_m/I_D-enabled 45RFSOI LNA is demonstrated. At this stage, the state-of-the-art study suggested a special interest is arising in fully differential circuits as the operating frequency increases, therefore, we move to a fully differential LNA. Also, we introduce transformed-based matching networks to improve circuit area significantly [24].

Related to these ideas we report the following results, which have been published in high impact magazines and journals indexed in the JCR (Journal Citation Report):

- A Compact Size Wideband RF-VGA Based on Second Generation Controlled Current Conveyors.
- Area-Efficient Integrated Current-Reuse Feedback Amplifier for Wake-Up Receivers in Wireless Sensor Network Applications.
- Miniature Wide-Band Noise-Cancelling CMOS LNA.
- A 2-V 1.4-dB NF GaAs MMIC LNA for K-Band Applications.
- A 1.2-V GaAs MMIC Ultra-Low-Noise Amplifier for K-band Applications.
- A g_m/I_D based Low-Power LNA for K-band Applications.
- A 0.38 V Fully Differential K-Band LNA with Transformer-Based Matching Networks.

In addition, the following paper has been submitted and we are awaiting review reports and acceptance:

- A 0.9-V 3.0-dB NF cascode LNA for Ku-band Applications in CMOS SOI.

1.3 Document Structure

The document structure is formed by 3 Sections and an Appendix with the following content:

- **Chapter 1 – Introduction**. The motivation of this thesis along with a detailed background is covered in this chapter. The main objectives and a brief introduction of each of the works developed are discussed.
- **Chapter 2 – Publications**. In this section, all the published works are collected, and are ordered as shown in the next sub-section.
- **Chapter 3 – Conclusions**. The main conclusions of the thesis are discussed here, giving a general overview of the theses and a detailed synthesis of each publication. Future lines of work are provided as well for each proposal.
- **Appendix 1 – Spanish abstract.** A complete Spanish summary containing the most relevant information of this PhD thesis is presented, with a brief introduction, thesis objectives, a highlight of the most relevant contributions and the conclusions drawn from each publication.

- **Appendix 2 – 0.9 V 3.0-dB NF cascode LNA in RFSOI.** An overview of the last paper submitted to a high impact journal is presented in this Appendix. The LNA was part of the GF University Partner Program, an brief introduction, design method and measurement results of the developed circuit are provided.

1.4 Justification and Overview of the Publications

1.4.1 A Compact Size Wideband RF-VGA Based on Second Generation Controlled Current Conveyors

A design procedure for wideband RF variable gain amplifiers using Second Generation Controlled Current Conveyors (CCII) is demonstrated in this contribution. Along the article a detailed analysis of the circuit and the CCIIs are discussed, providing the reader with valuable insights regarding the design decisions taken during the implementation and their consequences. The inductor-less RF-VGA is implemented, manufactured, and measured in a Silicon-Germanium (SiGe) low-cost Bipolar-CMOS (BiCMOS) process with a gate length of 0.35 µm, reporting a tunable gain in the range of 6.7 to 18 dB, an NF of 5.5 to 9.6 dB while drawing 1.7 mA from a ±1.5 V supply, and, to the authors' knowledge, the lowest area reported in the scientific literature (62 × 44 μm^2). The RF-VGA consists of two Class A amplifiers built with CCII to avoid the use of bulky inductors. Furthermore, thanks to the CCII approach, the input impedance is almost constant across the band and is fixed to 50 Ω to achieve wideband behavior. In this kind of RF circuits and WSN applications, the common approach consists of using external high-Q passives to achieve this task, which is avoided with the proposed approach, providing a significant area reduction and lower cost compared to similar state-of-the-art works. Moreover, due to the nature of the circuit, the higher the gain, the lower the current drawn by the amplifier. With maximum gain settings, the proposed circuit obtains a wideband behavior (DC up to 1 GHz) and is suitable for Software Defined Radios (SDNs), low frequency Industrial, Scientific, and Medical (ISM) and Medical Implant Communication System (MICS) applications. The proposed topology is very appropriate for wideband, low-power, and low-NF scenarios.

1.4.2 Miniature Wideband Noise-Cancelling CMOS LNA

The idea of the previous work is continued here to design a wideband CCII-based LNA with a noise canceling technique to reduce the NF of the circuit. To provide a solid approach, two implementations are compared in this publication: a CCII-based LNA and a CCII with noise canceling LNA. The wideband response is obtained by using the CCII to fix the input impedance in an inductor-less LNA, which brings the advantage of providing a broadband behavior with a very compact area. To implement the noise canceling technique, the noise contributed by the input transistor is canceled at the output terminal. The NC technique demonstrates an NF reduction of more than 1.5 dB, reporting a final NF of 3.2 dB. The circuit occupies a remarkable area of 160 × 80 μm^2 when implemented in a commercial UMC CMOS process with a gate length of 65 nm. Furthermore, the wideband response shows a stable performance from 0 up to 6.2 GHz, a 15.3-dB gain, Input Return Loss (IRL) better than 10 dB and a remarkable linearity (IIP3 = 7.6 dBm). The circuit is fed with a ±1.2 V DC supply and draws 18.6 mW. The circuit is compared to similar solutions available in the literature, proving the very high efficiency of the proposed approach, which benefits from a striking performance trade-off.

1.4.3 Area-Efficient Integrated Current-Reuse Feedback Amplifier for Wake-Up Receivers in Wireless Sensor Network Applications

In this paper, we commence by giving the reader a deep understanding of the state-of-the-art Wake-Up-Receiver (WuR) solutions and topologies available in the literature. We discuss the advantages and disadvantages of each approach and give examples of every single architecture to then move to a tuned-RF RFED (RF-Envelope-Detection) WuR with two different techniques. We first present a two-stage design with a feedback preamplifier to boost the receiver sensitivity and reduce power consumption and area. A sensitivity of –63.2 dBm and a power consumption of 6.77 µA in an area of only 398 × 266 μm^2 are achieved. However, in the second circuit, we maintain the performance and reduce power consumption by half (3.63 µA) by using a current reuse pre-amplifier which also benefits from a g_m-boosting technique. The circuit achieves a sensitivity of –75 dBm and the complete circuit shows an area of 262 × 262 μm^2. With this enhancement the preamplifier's area is reduced from 230 × 160 μm^2 to only 20 × 35 μm^2, i.e., the area is reduced from 36,800 μm^2 to 700 μm^2. The idea of this proposal is to provide a low-cost

solution for WSNs nodes and WuR designers, which are being extensively researched to provide device connectivity and new Internet of Things (IoT) solutions and applications. Also, WuRs are commonly implemented in WSN nodes when a low latency and very low power consumption are desired, and the node only needs to collect the data at certain time intervals. However, this low-latency very low-power scenario makes the achievement of high performance a very difficult challenge. The implementation of a low-power, high-data rate and high-sensitivity WuRs is not a simple procedure and is hardly achieved in practice. We give a design approach focused on the obtention of a low-cost solution with low power consumption, a reduced area, a high integrability and enhanced circuit sensitivity. Finally, a detailed discussion of some of the most important state-of-the-art proposals is shown to place the proposed circuits among similar works available in literature.

1.4.4 A 2-V 1.4-dB NF K-band GaAs MMIC LNA for K-band Applications

The design of a high-gain ultra-low-NF LNA is explored in this article in a commercially available GaAs process from UMS to demonstrate the achievement of a 1.4-dB NF LNA in a conventional GaAs process. Apart from cryogenic LNAs, a state-of-the-art review reveals a floor NF of ~1.4 dB in conventional K-band GaAs LNAs. The developed 28-GHz LNA can be fine-tuned to operate in a certain frequency range by slightly adjusting device geometry, DC biasing and matching networks. As previously introduced, the design of the LNA is critical since its NF directly affects the NF of the receiver. Hence, if a very low NF receiver is desired, careful attention must be paid to the implementation of the LNA. Also, the overall receiver sensitivity and linearity are affected by the performance of the LNA [2,7,8]. For instance, few works available in the literature demonstrate LNAs with a NF under 1.5 dB, a gain greater than 30 dB and low IRL [4,5,9–13]. The aim of the proposed circuit is to explore and push the limits of the PDK towards the achievement of the lowest NF possible. In this work, a comparison is made between a conventional design approach and a minimum-NF procedure. The effort is focused on replicating and then improving the conventional approach to introduce a detailed design procedure which allows the obtention of the desired ultra-low-NF LNA. After discussing the design procedure and decisions regarding device selection, impedance selection and biasing conditions, the circuit is laid out and simulated using EM analyses and yield estimations (Monte Carlo) to support the post-layout results

obtained. In this publication, a 4-stage LNA in a Gallium Arsenide (GaAs) pseudomorphic High Electron Mobility Transistor (pHEMT) process with a gate length of 100 nm covering the n258 (24.25–27.58 GHz) 5G New Radio (NR) frequency band is presented. The amplifier obtains a NF as low as 1.3 dB, a total gain of 34 dB, IRL better than 10 dB between 23 and 29 GHz, with a 1dB-compression point (P_{1dB}) of –18 dBm, and an output third-order intercept point (OIP3) of 24.5 dBm. The LNA in fed with a DC supply of 2 V and draws 59.1 mA, with an area of 3300 × 1800 μm^2 including pads. To support the post-layout results, electromagnetic (EM) simulations and Monte Carlo analysis are performed at room temperature, showing the LNA achieves 33 dB gain, a >1.4 dB NF, IRL better than 10 dB and confirm the linearity behavior previously mentioned. The paper concludes with a comparison between the proposed circuit and similar state-of-the-art LNAs, concluding the circuit is very competitive with recent solutions.

1.4.5 A 1.2-V GaAs MMIC Ultra-Low-Noise Amplifier for K-band Applications

Few works have been reported in the scientific literature achieving LNAs with under 1-dB NF whilst achieving a gain >25 dB and reduced IRL [31]–[33] with a reasonable power consumption. In the previous work, a 1.4-dB NF LNA in a commercial GaAs process is demonstrated, such a high performance is nevertheless limited by the technology characteristics (f_T and f_{max}). A 4-stage GaAs MMIC LNA with a NF under 1 dB and a 1.2 V supply is demonstrated in this work. In this case, we employ a very high-performance PDK from OMMIC, with a f_T = 300 GHz and f_{max} = 350 GHz. The LNA operates in the frequency range of 25.5 GHz up to 27 GHz –the upper end of the K-band– obtaining a maximum gain of 29.5 dB ±1 dB and an IRL of 12 dB at 26 GHz. To achieve such a low NF value, the layout of the input gate inductor is studied in depth [34]. By employing a custom tapered inductor, the quality factor is effectively increased and, hence, the NF is lowered, since the loss contributed by this element is minimized.

The focus of the circuit proposed in this work is to achieve an LNA with sub-1-dB NF and minimum IRL simultaneously, but the minimum NF is prioritized over the IRL. As previously mentioned, GaAs processes are suitable for high frequency LNA design since they are able to obtain a very low NF at K-band and mmWave frequencies. In this sense, the UMS PH10 GaAs pHEMT kit was tested in previous work to implement a

multistage LNA. With the best design effort, the LNA was able to achieve a NF as low as 1.4 dB @ 26 GHz, concluding, as expected, that the features of the PDK limit the achievable NF and do not allow under 1 dB NF. That is, the maximum active device f_T and the passives quality factors are fundamental parameters to consider at the technology selection stage after the specifications are determined, and even with the proposed minimum-NF methodology it is not possible to surpass the PDK limitations. Therefore, the high-performance OMMIC D007IH technology was selected to implement the LNA presented in this chapter. The process design kit (PDK) is characterized by providing depletion-mode InP-doped HEMT transistors with a fixed gate length of 70 nm. Additionally, the cutoff frequency f_T of the PDK is 300 GHz, and the maximum oscillation frequency f_{max} is 450 GHz, which allows very low-NF LNA designs. After a conscientious state-of-the-art revision of the most relevant commercially available LNAs in the market, the primary specifications for the circuit are determined to be: gain > 30 dB, NF < 1 dB, IRL and ORL above 15 dB and apparently no constraint related to power consumption in MMIC LNAs. That is, the commercially available GaAs LNAs studied consume as much DC power as needed. This fact highlights the difficulty of integrating commercially available LNAs in new applications and reveals they may not be prepared for hand-held devices and low-power applications such as IoT, WSN nodes or 5G mmWave chips.

A 4-stage MMIC LNA for K-band applications based on the previously introduced lowest-NF design procedure is demonstrated in this article. The implementation of this LNA is achieved using the components of a GaAs metamorphic HEMT (mHEMT) process from OMMIC with a gate length of 70 nm. The input matching network is formed by a high-Q single tapered octagonal inductor to further reduce the noise contribution. The LNA is fed from a 1.2-V DC supply with a total area of 2500µm×1750µm. EM simulation results at room temperature demonstrate the proposed circuit obtains a 29.5 dB gain with 1 dB ripple, a remarkable NF as low as 1 dB, IRL better than 10 dB and an ORL better than 20 dB across.

1.4.6 A g_m/I_D-based Low Power LNA for Ka-band Applications

The design of a Ka-band low-power cascode LNA operating with a 0.9 V DC power supply is presented in this chapter. The circuit is implemented in the 45nm SOI (45RFSOI) process from GF using a floating-body NMOS device (ADNFET). The design procedure is modified by following a g_m/I_D approach leading to a significant reduction in

power consumption in exchange for slightly lower gain and higher NF, but a greater figure of merit is demonstrated, thanks to the advantage of moderate inversion operation. The g_m/I_D methodology is combined with high frequency performance metrics, such as f_T, NF and gain to adapt the g_m/I_D to RF/MW environments providing an intuitive and straightforward procedure that yields an increased FoM to achieve a very efficient implementation.

The design procedure is divided as follows: first, the NFET performance is studied, and a database is built based on simulations of DC, AC and high-frequency metrics, following the g_m/I_D look-up-tables (LUTs) philosophy [37]–[39]. In this fashion the designer only needs to run the simulations once, which then can be used to analyze and design other circuits at the same frequency. Knowing the topology of the circuit and the equations defining its performance, the designer can obtain one or many versions of the circuit and select the one that better suits a given specification. Likewise, the designer can study a number of FoMs to determine the most efficient solution, depending on the most critical aspects considered. Then, ideal components are used to set up the circuit as a proof-of-concept, letting the designer verify the performance. During the design procedure discussion, we suggest the employment of a complex FET model, as supported by [13], [14], [36], built with: a combination of PDK components, an R+C+CC (resistance, capacitance and coupling capacitance) parasitic extraction and EM simulations to improve the design accuracy. Then the actual circuit with PDK components is implemented and a conventional approach is followed, i.e., iterative EM simulations and layout adjustments lead to the final circuit.

The ratio between the small-signal transconductance g_m of a MOSFET and the DC bias current I_D is known as the transistor efficiency and has been widely used in analog integrated circuit designs to obtain very low power circuits [37], [40]. The main advantage of the g_m/I_D methodology is that it provides a powerful sizing tool that allows the designer to take advantage of the subthreshold regions to obtain very low power consumption. As demonstrated by [37], [40], by studying the DC bias conditions and small-signal characteristics of the MOSFETs in a PDK one can generate a series of LUTs with all the information needed to design a circuit given a target specification. Although the g_m/I_D methodology was born in the field of low frequency analog IC design, efforts have been made to integrate this methodology with RF and MW circuit design, demonstrating the implementation of very low-power RFICs. For instance, sub-1-mW narrowband 2.4-GHz

LNAs as well as UWB LNAs (100 MHz up to 7 GHz) designed with the g_m/I_D methodology have been reported. In this work, we present and apply the g_m/I_D methodology adapted to RF/MW frequencies to obtain a Ka-band very low power LNA, thanks to the advantages introduced by the moderate inversion region.

1.4.7 A 0.38 V Fully Differential K-band LNA with Transformer-Based Matching Networks

Another possibility to reach challenging NF and gain specifications (imagine we wish to maintain NF ≈ 1.4 dB and G ≈ 15 dB) and saving power consumption simultaneously consists of using a strong-inversion coefficient with a low supply voltage. That is, one can bias the device with the required strong-inversion current density by lowering the supply voltage while compensating for this reduction in the drain current by other means (which depends on the circuit topology). Since the total power consumption is the product of the DC supply voltage and the amount of DC current drawn, lowering the supply voltage instead of the drain current is also a very effective way of saving power. Yet, this V_{DD} reduction comes at the expense of a somewhat lower linearity. Note that not every LNA topology is suitable for the application of this technique. Namely, the cascode amplifier consists of two stacked transistors, which limits the V_{DD} margin. That is why we use multistage common-source (CS) amplifier. As seen in both GaAs LNA designs, a multistage amplifier requires multiple matching networks, each of them with numerous passive components that increase the circuit area significantly. On the other hand, in contrast with single-ended circuits in a fully differential LNA the inductances needed to match each stage can be stacked as transformers, hence saving a very significant amount of space in the chip. Recently, many works delving with the design and modeling of integrated transformers for various applications have been published [11–13]. Apart from the multiple advantages the fully differential circuits provide (increased CMRR, supply noise resilience and $\Delta G = +3$ dB at the cost of twice the power consumption and number of components), many mixers operate in a fully differential fashion, and therefore the LNA interconnection with the mixer modules is easier, removing the need of a bulky and lossy passive balun. Furthermore, the transformer-based matching networks provide the following advantages [41]:

- Galvanic isolation between stages allows capacitor-less separation of DC domains and direct AC coupling.

- Input and output transformers can also operate as baluns.
- The fully differential topology allows symmetric transformers with a center-tap terminal, which can be used to bias the gates and drains without RF Chokes.
- The area needed for each matching network is equivalent to the area needed for a single inductance.

The design of a 0.38 V fully differential LNA with transformer based matching networks is demonstrated in this work. Still, despite the modifications added to the circuit topology, the principles developed throughout the paper can easily be adapted from the differential mode into a single-ended amplifier or from a CS into a cascode, always with limitations to some extent. The proposed circuit is a two-stage CS amplifier implemented in 45RFSOI process from GF. The circuit achieves a gain of 12.9 dB, a NF of 2.2 dB, IRL and ORL better than 10 dB, and an IIP3 of –4 dBm. The LNA consumes 11.7 mW when it is fed from a DC supply of 0.38 V and thanks to the transformer-based matching networks it achieves a very compact area of 0.15 mm^2. To the best of the author's knowledge, the reported NF and power consumption are the lowest among fully differential LNA proposals at the same frequency. Furthermore, a state-of-the-art impedance matching tool was replicated and used to implement the transformers by developing a MATLAB script to generate and equalize the inductances needed to perform impedance matching efficiently.

PUBLICATIONS

2.1. A Compact Size Wideband RF-VGA Based on Second Generation Controlled Current Conveyors

electronics

MDPI

Article

A Compact Size Wideband RF-VGA Based on Second Generation Controlled Current Conveyors

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Abstract: This paper presents a methodology to design a wideband radio frequency variable gain amplifier (RF-VGA) in a low-cost SiGe BiCMOS 0.35 µm process. The circuit uses two Class A amplifiers based on second-generation controlled current conveyors (CCCII). The main feature of this circuit is the wideband input match along with a reduced NF (5.5–9.6 dB) and, to the authors' knowledge, the lowest die footprint reported (62 × 44 µm^2 area). The implementation of the RF-VGA based on CCCII allows a wideband input match without the need of passive elements. Due to the nature of the circuit, when the gain is increased, the power consumption is reduced. The architecture is suitable for designing wideband, low-power, and low-noise amplifiers. The proposed design achieves a tunable gain of 6.7–18 dB and a power consumption of 1.7 mA with a ±1.5 V DC supply. At maximum gain, the proposed RF-VGA covers from DC up to 1 GHz and can find application in software design radios (SDRs), the low frequency medical implant communication system (MICS) or industrial, scientific, and medical (ISM) bands.

Keywords: radio frequency variable gain amplifier (RF-VGA); wideband amplifier; broadband amplifier; second-generation controlled current conveyor (CCCII); BiCMOS; ISM; MICS; SDR

1. Introduction

In radio frequency integrated circuits, the design of wideband amplifiers has been intensively discussed over the past few decades [1]. The most widely used wideband amplifier architecture is the distributed amplifier, which requires high power consumption and a large area due to the considerable number of stages and the extensive use of inductors [2–4].

Another commonly used technique is the use of feedback amplifiers [5–10]. This solution offers a good return loss, but, due to the feedback, it is difficult to achieve a low noise figure with a reasonable power consumption.

As an alternative to these two previous topologies, some authors have proposed the design of wideband circuits by converting narrowband circuits into broadband [11–13]. This is usually achieved by modifying the input matching network to act as a broadband filter and replacing the narrowband load (typically a tank circuit) with any of the wideband RC load implementations: series-peaking, shunt-peaking, shunt-series-peaking, etc. [14–16]. Again, as in the case of the distribute amplifier technique, the main limitation of this solution is the area as they use a large number of inductors. Note that the issues of large area and high power consumption are aggravated when variable gain is desired.

To reduce the area constraints, some authors have proposed the use of common-base or common-gate wideband amplifiers [14–16]. These topologies take advantage of the fact that, in such configurations, it is possible to obtain a broadband input impedance equal to 50 Ω by properly biasing the transistor. However, the gain and noise figure are determined by this biasing and consequently fixed to a certain value.

At system level, when implementing a wideband analog RF front-end, the most popular scheme includes a wideband low noise amplifier (LNA) followed by a variable gain amplifier (VGA). This maximizes the dynamic range of the upcoming stages and prevents the saturation of the receiver if a high-powered signal is received [17]. In these cases, the implementation of a wideband RF-VGA is of upmost interest.

This work addresses the design of a very compact, low power, low voltage, and high bandwidth RF-VGA using second generation controlled current conveyors. A CCCII is a four terminal device that can perform many useful analog signal processing functions when arranged with other electronic elements in specific circuit configurations [18]. CCCIIs have been successfully used in high frequency current mode applications such as filters [19] and LNAs [20]. The proposed radio frequency variable gain amplifier (RF-VGA) is based in the CCCII proposed in [21] and has been designed and fabricated in a low cost 0.35 µm SiGe BiCMOS technology. The rest of the paper goes as follows: Section 2 reviews the CCCII and describes the proposed RF-VGA topology and the design methodology, Section 3 focuses on the circuit performance and the analysis of the obtained results; finally, some conclusions are drawn in Section 4.

2. RF-VGA Based on the Current Conveyor

CCCIIs can be used to implement numerous functions, such as filtering, amplification, or impedance transformation. They also provide better performance than traditional OTAs, namely, improved power consumption and larger cut-off frequency [19].

A CCCII is a device with three ports (X, Y and Z) and a DC bias current (I_0). Each port is characterized by an impedance (Z_X, Z_Y and Z_Z) resulting from the implementation of the conveyor with non-ideal components. These impedances are defined by parasitic elements, which are highly dependent on the selected technology of fabrication and the bias current I_0. Thus, the concept of controlled current conveyor appears due to this dependence on I_0. The relationship that governs the interactions between the ports of the conveyor is defined as follows:

- between ports X and Z the device acts as a current follower,
- between ports Y and X it operates as a voltage follower,
- between ports Z and Y it behaves as a transconductor.

The matrix that defines these relationships is given by

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} Y_Y(I_0) & 0 & 0 \\ \beta(s) & Z_X(I_0) & 0 \\ 0 & \alpha(s) & Y_Z(I_0) \end{bmatrix} \cdot \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

where Y_Y is the conductance of port Y, and Y_Z, the conductance of port Z. In addition, the terms $\alpha(s)$ and $\beta(s)$ represent the unity current and voltage transfer functions. The resistive component of Z_X (defined as R_X) is particularly relevant since it can be used to define the interaction between ports.

Variable gain amplifiers can be implemented using CCCIIs [19–21], where the gain tuning is performed by means of adjusting the bias current of the conveyor. The dependence of R_X on the bias current I_0 can be exploited to provide wideband input matching without including a single passive component, resulting in a circuit with a very low input return loss. This situation is desirable in scenarios where the amplifier is the first integrated circuit in the reception path. For example, if a preceding LNA is added externally, the proposed RF-VGA facilitates impedance matching with

this element, and the signal coming from the LNA is received with a very low loss. In addition, the proposed design can potentially obtain a high cut-off frequency and low die footprint due to the reduced number of active devices needed to implement the conveyor.

To implement an RF-VGA, two CCCII blocks are connected as shown in Figure 1 [20]. Provided that the impedances Z_{X1} and Z_{X2} are entirely resistive, $V_{IN}(t)$ is transformed into a current $I_{IN}(t)$. This current is then converted into a voltage signal again thanks to Z_{X2}. Due to the relationship between R_X and the bias current I_0, it can be proved that the gain G of the amplifier reduces to:

$$G = \frac{V_{OUT}(t)}{V_{IN}(t)} = \frac{I_{01}}{I_{02}} \tag{2}$$

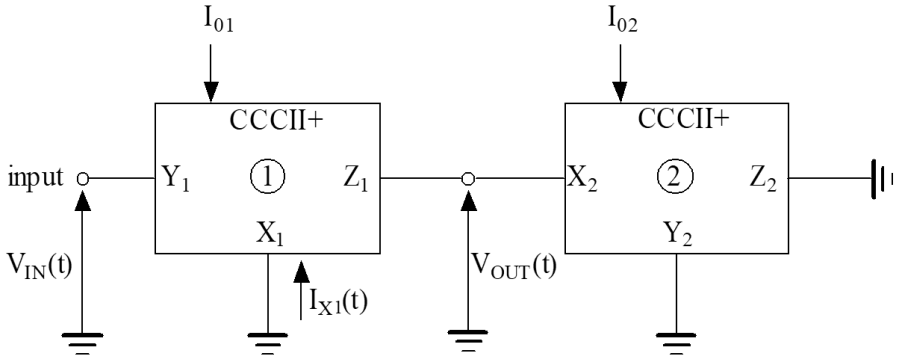

Figure 1. Connection of two CCCII blocks to provide voltage amplification.

Since the node Y_1 presents a high input impedance [19], the input signal is applied at node X_1. By doing so, the input impedance is reduced and can be controlled by the bias current I_{01}. Thus, the input impedance Z_{IN} of the RF-VGA can be adjusted by means of adjusting the value of the bias current I_{01}, which is fixed to obtain $|Z_{IN}| = 50\ \Omega$.

The value of the bias current I_{01} can be fixed to perform wideband input matching, and so the gain can be adjusted by setting the value of I_{02}. Due to the inversely proportional relationship given by (2), it is possible to increase the gain by reducing the bias current I_{02}. Therefore, higher gain settings lead to lower power consumption. A simple Class-A implementation scheme with CCCIIs is shown in Figure 2a. To obtain the structure depicted in Figure 1, nodes Z_1 and X_2 must be connected together, yielding the circuit depicted in Figure 2b. As mentioned above, the input signal is applied at node X_1 to facilitate input matching, allowing the elimination of transistor Q_{11}. The resulting scheme after simplification is presented in Figure 3. With this result, the number of BJTs is reduced as much as possible, yielding a higher cut-off frequency and a better noise performance [22]. The required values of the bias current I_{01} obtained in simulation to achieve a 50 Ω input impedance are plotted in Figure 4 for various transistor areas from the 0.35 μm SiGe design kit used.

The voltage gain and the bandwidth of the RF-VGA are plotted in Figure 5. The values between 100 μA and 250 μA present a trade-off between gain and bandwidth and can be used to determine the optimal combination of device area and bias current I_{02}. When I_{02} augments, the gain of the circuit drops while the bandwidth raises. The gain is not significantly affected by the variation in the transistor area, but, as expected, the bandwidth is increased if the area is reduced. Although the RF-VGA may be preceded by an LNA, its noise figure (NF) is one of the most relevant parameters in the design. If the LNA gain is low, the RF-VGA must provide a reduced NF and high gain to avoid degradation of the receiver performance.

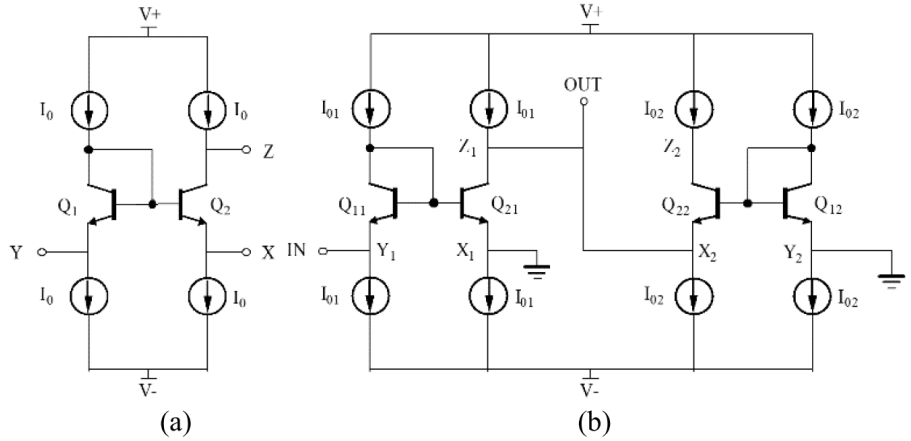

Figure 2. Class-A CCCII basic schematic (**a**) and topology of a voltage-mode amplifier using two basic class-A blocks (**b**).

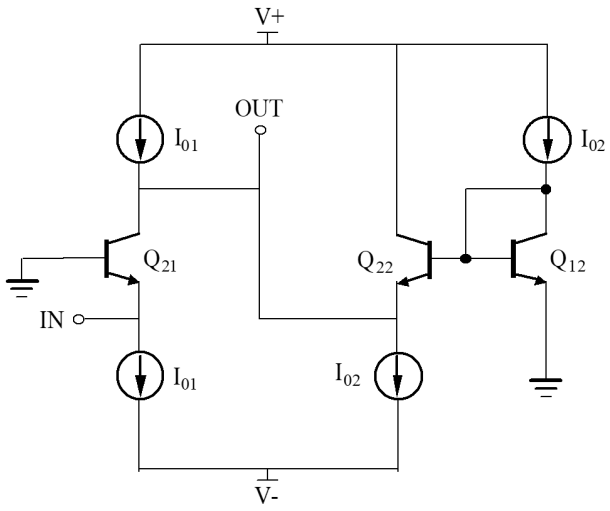

Figure 3. Schematic of the RF-VGA after simplification.

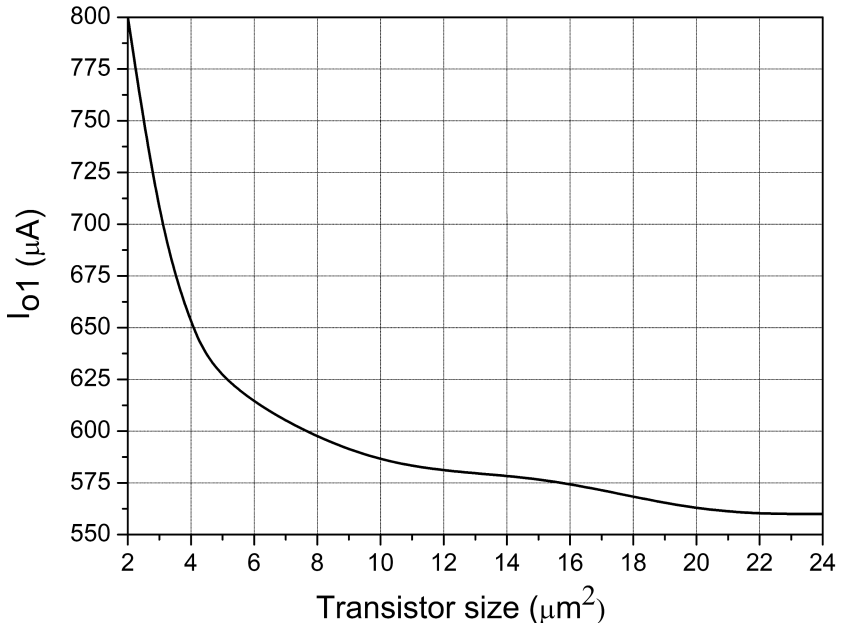

Figure 4. Bias current I_{01} vs. transistor size to obtain an input impedance of 50 Ω.

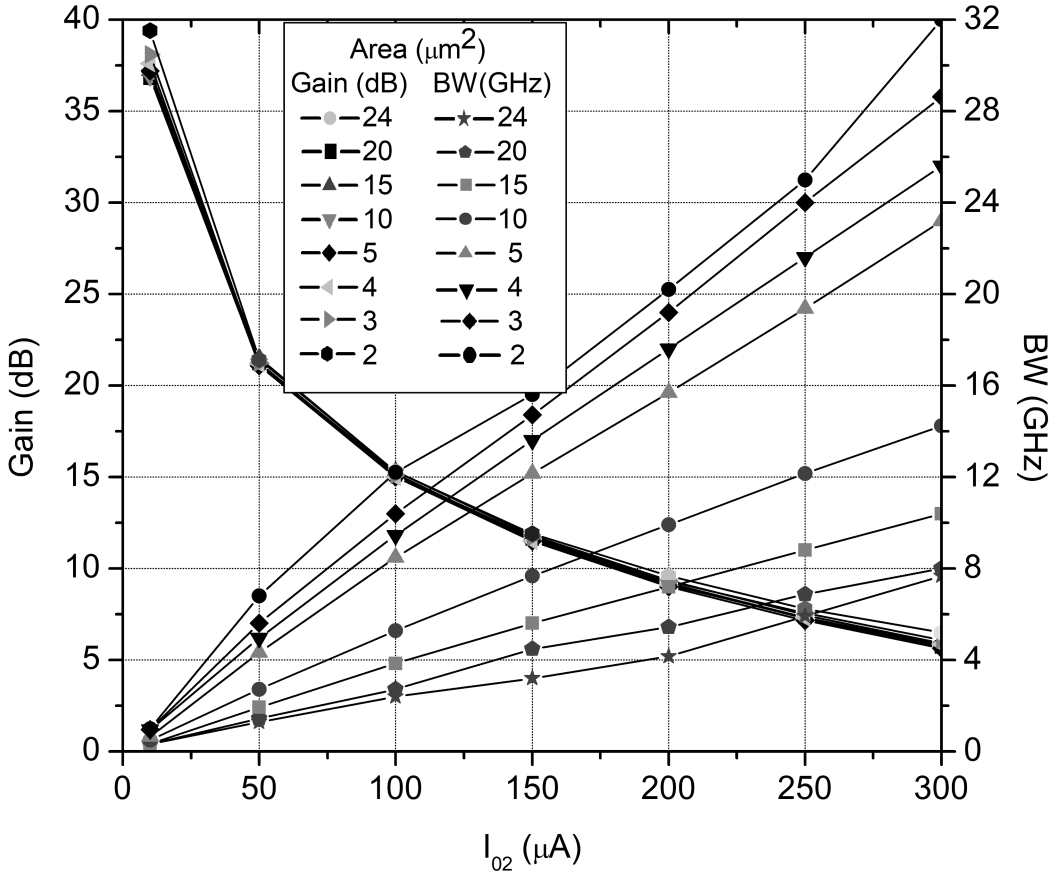

Figure 5. Simulated gain and bandwidth results of the RF-VGA at $V_{DC} = \pm 1.5$ V.

Depending on the application of interest, a trade-off between gain, noise, and bandwidth must be considered by the designer. In this implementation, the number of elements in the signal path is kept as low as possible (only tree BJTs), and there is a total absence of passive elements. Consequently, the noise introduced by spurious elements is minimized and the main noise contribution is due to the input transistor Q_{21}. Figure 6 depicts the simulated NF of the circuit for different transistor areas, where it is shown that the NF decreases when the device area is increased. The noise figure of the RF-VGA is also plotted against I_{02} in Figure 7 for a transistor area of 20 μm^2. Note that the noise figure is strongly dependent on the bias current, so that, when I_{02} increases, the gain is reduced and the NF augments. If a high gain and a low NF is desired, a lower I_{02} and a higher transistor area are required. However, this situation limits the achievable bandwidth since a low bias current combined with a high aspect ratio yields a reduced frequency performance (see Figure 5). As a result, a trade-off between noise figure, gain, and bandwidth is present and should be considered depending on the design specifications.

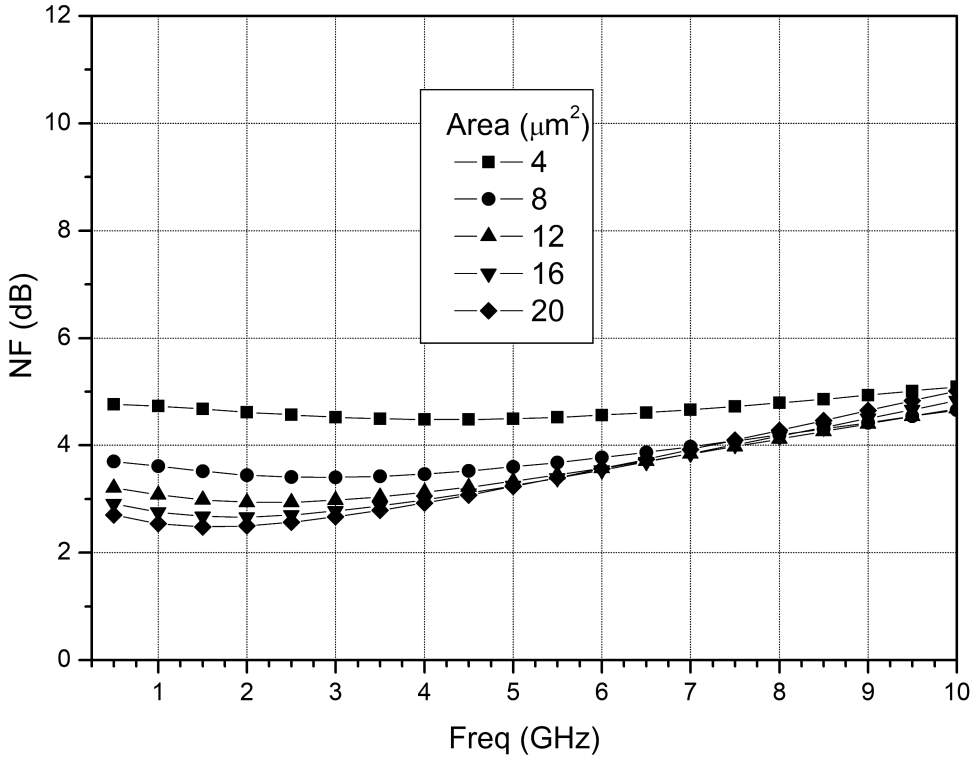

Figure 6. Noise figure vs. transistor area.

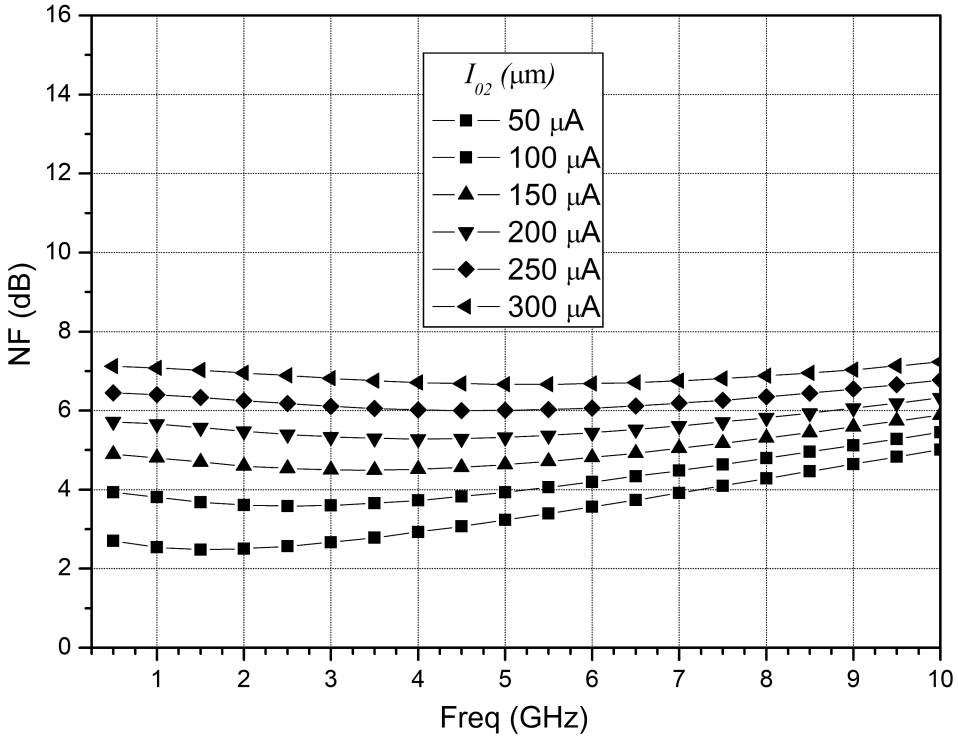

Figure 7. Noise figure vs. I_{02} for a transistor with 20 μm^2.

The final RF-VGA schematic is shown in Figure 8, where the current sources have been replaced with MOS transistors. The RF-VGA was designed and laid out in a BiCMOS SiGe 0.35 μm process with a DC supply of ±1.5 V. The layout of the circuit is presented in Figure 9. The layout was realized taking into account critical aspects of analog RFICs, such as circuit symmetry and transistor matching techniques to reduce PVT variations. The selected areas for each transistor were chosen to achieve a

maximum gain of 18 dB and a 900 MHz bandwidth with a total current consumption below 2 mA. The size of Q_{21} is 20 μm^2, which is twice the size of Q_{12} and Q_{22}, with 10 μm^2 each. The aspect ratio of the NMOS and PMOS transistors is 20/1 (μm/μm).

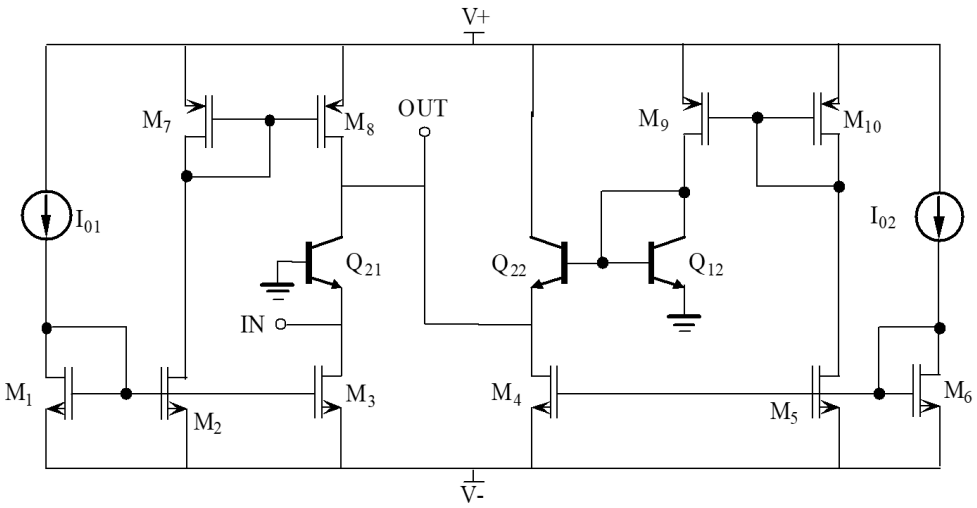

Figure 8. Schematic of the proposed RF-VGA.

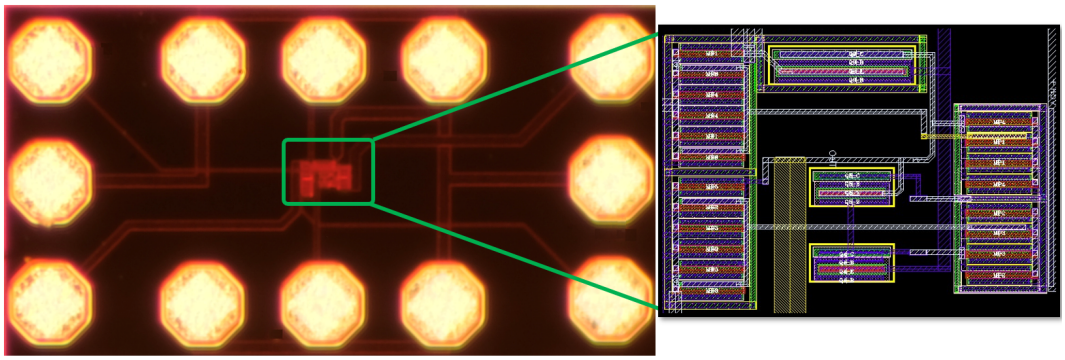

Figure 9. Die micro-photograph of the RF-VGA.

3. Measurements

Probe pads were added for on–wafer measurements. Two ground-signal-ground (GSG) and two signal-ground-signal (SGS) pads structures with 150 μm pitch were used. The DC supply is ±1.5 V and the amplifier draws a current of 1.7 mA. The total chip size of the RF-VGA including pads is 800 × 430 μm^2, but the core of the circuit occupies an area as low as 62 × 44 μm^2. The voltage gain of the RF-VGA is plotted in Figure 10 for a frequency range of DC–3 GHz vs. bias current I_{02}. A good agreement between measurement and simulation can be found with an error below ±1.1 dB in the entire band. As expected, when I_{02} is increased, the gain of the circuit decreases while the bandwidth raises. The simulation and measurement results of the NF of the proposed design are depicted in Figure 11. As can be seen, the NF increases with the bias current I_{02}. A reduced bias current (i.e., higher gain) is needed if a low noise figure is required. As mentioned above, the drawback is a reduction in the bandwidth of the amplifier. In many applications, it is desirable to extend the bandwidth thus a multistage approach or a bandwidth enhancement technique would be needed to obtain a high-gain and wide-band. For NF, the error between simulation and measurement is below 1.4 dB.

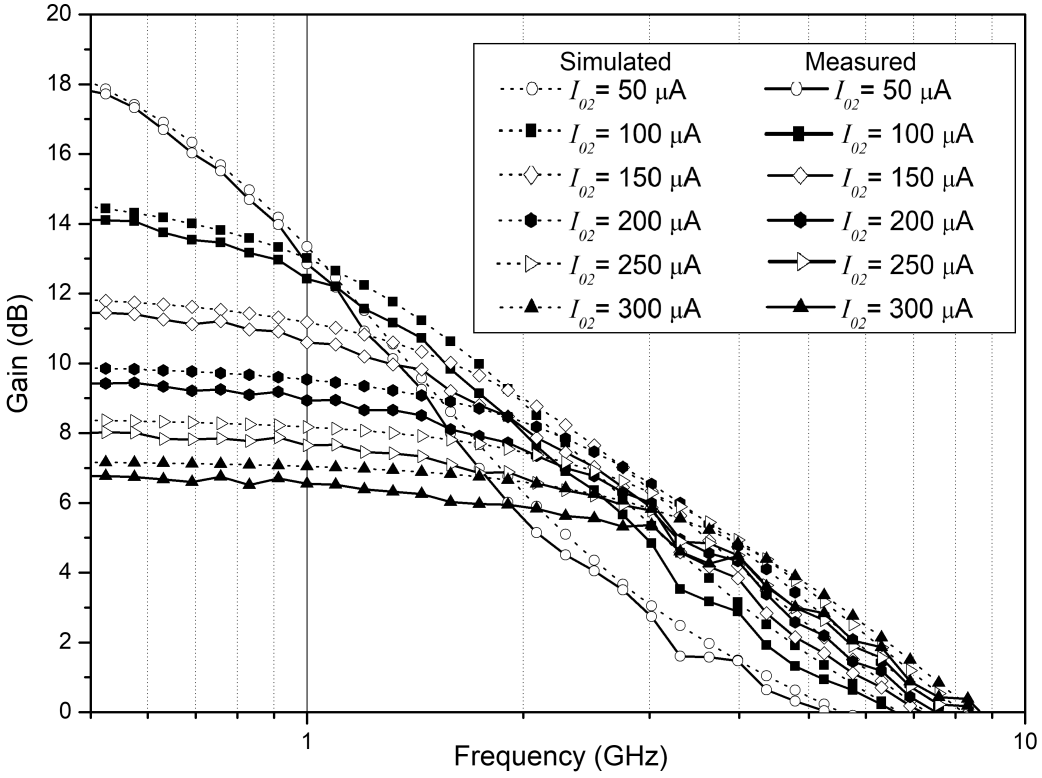

Figure 10. Measured and simulated gain of the RF-VGA for different bias currents I_{02}.

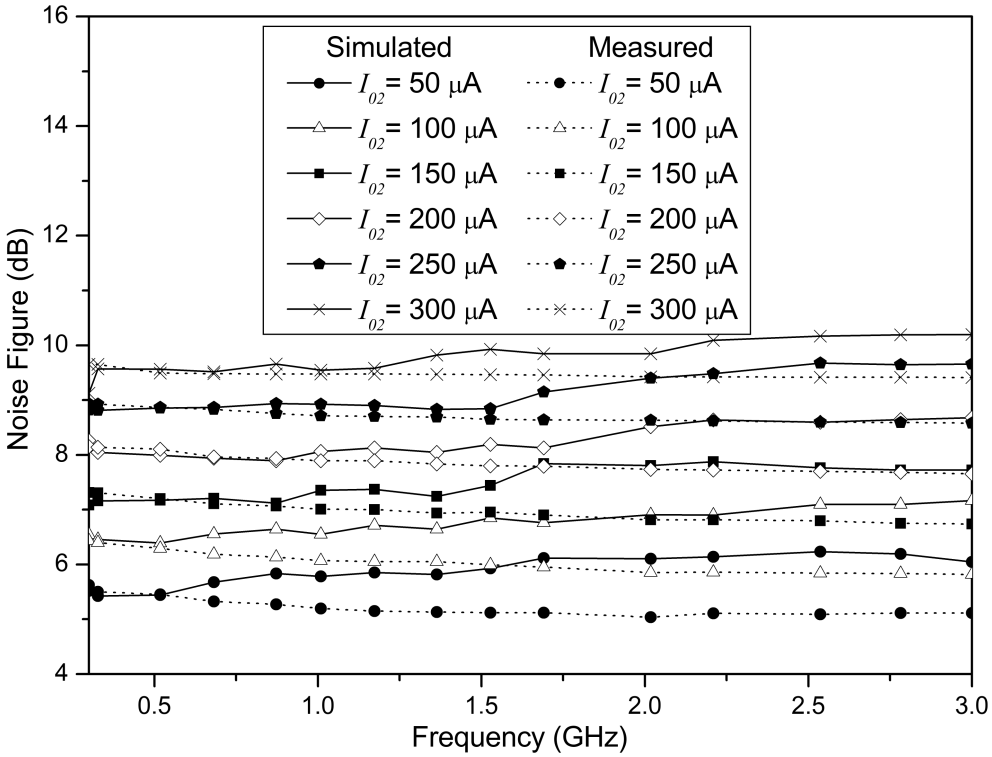

Figure 11. Measured and simulated NF of the RF-VGA for different bias currents I_{02}.

Another key parameter for the performance of the RF-VGA is the input return loss. When the LNA is implemented externally, the RF-VGA is the first integrated device in the receiver; thus, a broadband 50 Ω input match is required. The simulated and measured S_{11} are shown in Figure 12, where the measured magnitude for the S_{11} is better than 20 dB for frequencies up to 10 GHz.

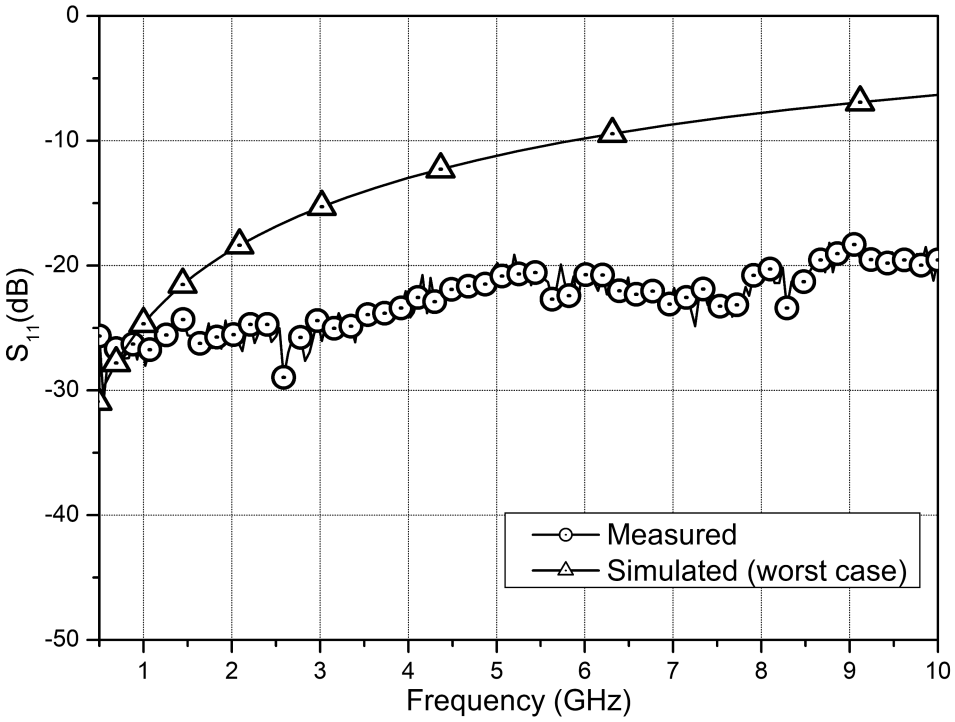

Figure 12. Measurement and simulation of the input return loss S_{11} for for $I_{01} = 600$ μA and $I_{02} = 50$ μA.

The linearity of the proposed RF-VGA was evaluated by measuring the input 1-dB compression point (P_{1dB}) using a test tone of 666 MHz. The measurement results for maximum gain settings (I_{01} = 600 μA and I_{02} = 50 μA) are plotted in Figure 13, obtaining a value of –20.18 dBm for the input P_{1dB}.

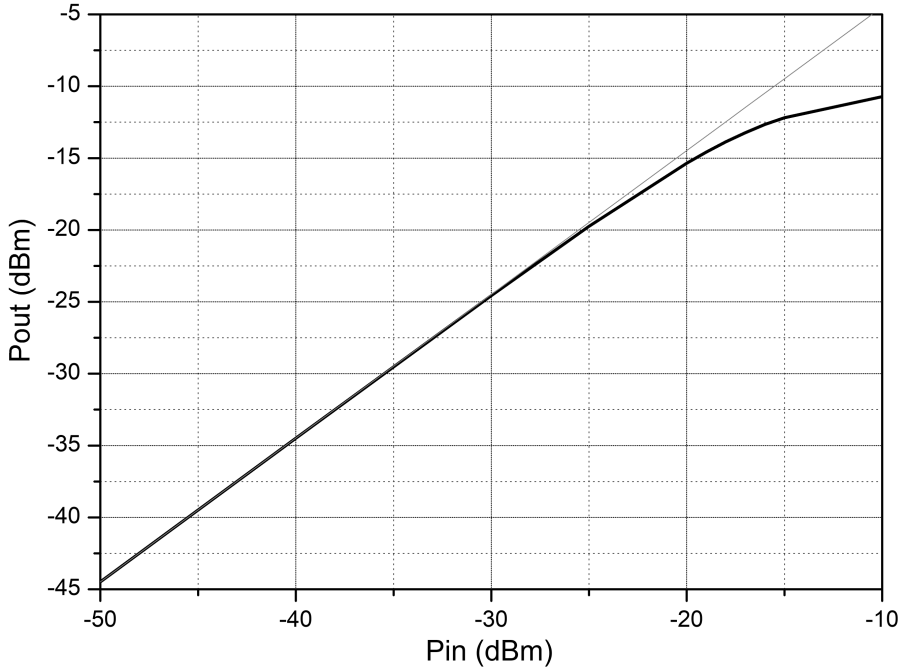

Figure 13. Measurement of the input 1-dB compression point for $I_{01} = 600$ μA and $I_{02} = 50$ μA.

A summary of the performance of the proposed RF-VGA versus I_{02} is presented in Table 1 for $I_{01} = 550$ μA and $V_{DC} = \pm 1.5$ V. A brief overview of similar works available in the literature is given in Table 2 [23–30]. With the exception of [26], which uses 40 nm technology, our work has better bandwidth. Compared with other authors, a good trade-off between gain and bandwidth is obtained. We have achieved a competitive noise figure, not exceeding 9.6 dB for the worst case. The power consumption is small, but not the lowest one, this is because the others authors have used more advanced technologies. To the best of the authors' knowledge, the present work achieves the lowest area occupation reported in the literature while showing competitive performances in terms of gain, NF and BW with a power consumption similar to that of other proposed solutions.

Table 1. Summary of measured results with $I_{01} = 550$ μA and $V_{DC} = \pm 1.5$ V.

I_{02} [μA]	50	100	150	200	250	300
Gain [dB]	18	14	11.4	9.4	8	6.7
BW [GHz]	0.85	1.3	1.9	2.7	3.26	4.3
NF [dB]	5.5	6.5	7.2	8	8.9	9.6
$\lvert Z_{out}\rvert[\Omega]$	500	256	175	133	105	90

Table 2. Performance comparison.

Reference	Gain [dB]	BW [GHz]	NF [dB]	Vdd [V]	Power [mW]	Area [mm^2]	Technology
[23]	−10–50	2	17–30	1.0	2.5	0.013	90 nm CMOS
[24]	−28–23	1	3.9–5.2	1.5	8.2	0.051	0.18 μm CMOS
[25]	2–24	2–2.2	24–29	1.2	3.5	0.010	65 nm CMOS
[26]	18.4–27.1	9.3	3.3–4.4	1.1	21.5–31.4	0.26	40 nm CMOS
[27]	−25–20	0.2–3.3	3.4–20	1.2	19	0.15	130 nm CMOS
[28]	−54–46	0.98–2.15	8–15	–	–	0.539	0.18 μm CMOS
[29]	4.6–12	0.4–4.5	3–9	1.5	22.5	1	28 nm FDSOI CMOS
[30]	−19–21	4	17–47	1.2	3.5	0.012	65 nm CMOS
This work	**6.7–18**	**0.85–4.3**	**5.5–9.6**	**±1.5**	**5.1**	**0.003**	**0.35 μm BiCMOS**

4. Conclusions

A very compact, low power, low voltage and high bandwidth RF-VGA based on the cascade connection of two CCCII blocks has been presented. The circuit was implemented in a standard low cost SiGe BiCMOS 0.35 μm process. A gain control from 6.7 to 18 dB is obtained varying the bias current of the circuit. The present work achieves, to the authors' knowledge, the lowest area occupation. For a polarization current I_{02} of 50 μA, the circuit achieves a power consumption of 1.7 mA with a ±1.5 V DC supply, an input return loss better than 20 dB from DC up to 10 GHz and a noise figure from 5.5 dB at maximum gain settings to 9.6 dB at minimum gain settings. Finally, the measured $P_{1\text{dB}}$ is −20.18 dBm. The RF-VGA achieves a very competitive trade-off between gain, noise figure, input return loss, power consumption, and die footprint, making this architecture suitable for the design of compact wide-band, low-power, and low-noise variable gain amplifiers.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

BW	bandwidth
CCII	second-generation current conveyor
CCCII	second-generation controlled current conveyor
ISM	industrial, scientific and medical
LNA	low noise amplifier
MICS	medical implant communication system
RF-VGA	radio frequency variable gain amplifier
SDR	software design radio
VGA	variable gain amplifier

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2.2. Area-Efficient Integrated Current-Reuse Feedback Amplifier forWake-Up Receivers in Wireless Sensor Network Applications

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Area-Efficient Integrated Current-Reuse Feedback Amplifier for Wake-Up Receivers in Wireless Sensor Network Applications

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Abstract: Wireless sensor network (WSN) applications are under extensive research and development due to the need to interconnect devices with each other. To reduce latency while keeping very low power consumption, the implementation of a wake-up receiver (WuR) is of particular interest. In WuR implementations, meeting high performance metrics is a design challenge, and the obtention of high-sensitivity, high data rate, low-power-consumption WuRs is not a straightforward procedure. The focus of our proposals is centered on power consumption and area reduction to provide high integrability and maintain a low cost-per-node, while we simultaneously improve circuit sensitivity. Firstly, we present a two-stage design based on a feedback technique and improve the area use, power consumption and sensitivity of the circuit by adding a current-reuse approach. The first solution is composed of a feedback amplifier, two op-amps plus a low-pass filter. The circuit achieves a sensitivity of –63.2 dBm with a power consumption of 6.77 µA and an area as low as 398 × 266 µm^2. With the current-reuse feedback amplifier, the power consumption is halved in the second circuit (resulting in 3.63 µA), and the resulting circuit area is as low as 262 × 262 µm^2. Thanks to the nature of the circuit, the sensitivity is improved to –75 dBm. This latter proposal is particularly suitable in applications where a fully integrated WuR is desired, providing a reasonable sensitivity with a low power consumption and a very low die footprint, therefore facilitating integration with other components of the WSN node. A thorough discussion of the most relevant state-of-the-art solutions is presented, too, and the two developed solutions are compared to the most relevant contributions available in the literature.

Keywords: wake-up receiver; radiofrequency envelope detector; tuned radiofrequency; low power; energy efficient; wireless sensor network; complementary metal-oxide semiconductor

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1. Introduction

WSN applications are under extensive research and development due to the need to interconnect devices with each other. Both industry and academia have shown an increasing interest in promoting internet of things (IoT) and internet of everything (IoE) devices to boost connectivity and enable complex, coordinated tasks. A WSN can be constructed by several low-cost, low-power wireless devices characterized by a simplistic structure. They also require a very low level of human interaction for maintenance. In this sense, a WSN node is designed with a long lifespan, as in many situations, the nodes are under critical environmental conditions and the batteries are hard to replace. Conventional radios play a crucial role in WSN nodes' operation since they are frequently one of the most expensive components in terms of power consumption [1]. A common solution to obtain significant power savings consists in duty cycling the radio interface [2]; this is applied by turning it off and on again to save power using hibernation or sleep modes, or using it only when necessary, as defined by the unscheduled IEEE 802.11 communications protocol. The

most severe drawback of such an approach is that the sensor node stays unreachable and unable to communicate during the times when its radio interface is in sleep mode, which may translate to a significant latency increment. However, depending on the network's activity, two different applications can be recognized: low-activity applications with a low-average throughput (such as WSNs for area monitoring, habitat monitoring, industrial monitoring, environmental sensing or threat detection, which consist of monitoring rare events and therefore do not require constant operation), and high-activity applications with a high-average throughput (such as multimedia and mobile WSNs, which require almost constant operation, high bandwidth, data processing and compressing techniques). In low-throughput applications, the sensor nodes' key metrics are sensitivity and power consumption, because the sensor is expected to be placed in a harsh environment and should present a wide lifespan but with reasonable sensitivity, or it would be unreachable. On the other hand, in high-throughput applications, the latency and data rate are critical, as the node is expected to exchange a high amount of information and should respond quickly to any queries the other nodes may produce. In this context, duty cycling the radio interface severely damages the overall network performance, and many applications may not support the associated delays.

A well-known approach to reduce latency while keeping a very low power consumption consists in the implementation of a WuR, so that the WSN node is listening to the communication channel and the main microcontroller unit (MCU), and conventional radio communication modules are in sleep mode. A block diagram of a WSN node containing a WuR is depicted in Figure 1 [3].

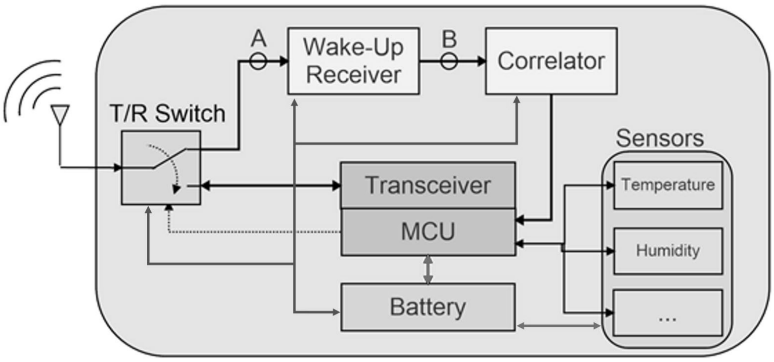


Figure 1. Block diagram of a sensor node integrating a WuR [3].

The MCU and the conventional radio interface are awakened when the sensor node is addressed, so that when a wake-up pattern is recognized, data exchange can occur. Of course, the WuR is always ready to detect and identify wake-up signals generated by the coordinating nodes in the WSN to maintain a low latency. To save power consumption and avoid waking up other nodes, the WuRs employ distinctive wake-up patterns and identifiers so that each node can be addressed individually. To perform this task, the WuRs are composed of an RF front-end and a digital baseband back-end, with a pattern recognizer or signal correlator used to identify the wake-up identifier. Power savings introduced by using WuRs are mostly observed in low-activity and low-average throughput applications, as the main radio interface is in sleep mode during a significant amount of time [4]. Due to its inherent simplicity, the on–off keying (OOK) modulation scheme is frequently the preferred option when designing a WuR. This scheme is equivalent to an amplitude-shift keying (ASK) of two levels, and it consists of a sinusoidal signal modulated with an on-and-off unipolar binary signal. Very simple architecture is needed to demodulate the OOK signal. At the same time, since very simple architecture is employed, meeting high performance metrics is a design challenge, and the design of high-sensitivity, high data rate, low-power-consumption WuRs is not a straightforward procedure. Although significant power savings are achieved with a low impact in latency, this advantage comes at the expense of somewhat higher system complexity, size and cost for the WSN node [5]. In

addition, the limited power consumption characterizing a WuR also limits the achievable sensitivity and selectivity, so conventional receivers are clearly superior to WuRs in these terms. This means that a higher transmitting power may be needed to reach a WuR when compared to the power needed to reach a conventional receiver for the same distance. However, in densely populated networks the priority is to reduce the cost-per-node as much as possible, so that the sensitivity/power consumption trade-off is not a design focus. Therefore, system integration, circuit area, assembly costs, bill of materials and calibration strategies are the main concern in these kinds of scenarios.

Nowadays, the integration of WuRs in commercial applications and consumer electronics is increasing, with industry and academia spending more, and more design effort in reducing the cost-per-node and power consumption and increasing sensitivity. This can be seen in several state-of-the-art works, since some authors have reported circuits achieving very high sensitivities while operating in the nW range. In this sense, the performance of some of the most relevant contributions in the literature are depicted in Figure 2; the *X*-axis refers to the sensitivity and the *Y*-axis covers the power consumption. In comparison with conventional receivers, in which the power consumption is frequently in the order of mW, a sub-nW power consumption is clearly remarkable. The advantage of these solutions is that the circuits can be powered by coin-sized batteries or even employ energy-harvesting strategies and are able to perform continuous channel listening for years. The approach adopted in [6] is an example of this idea, where a battery-less WuR with energy-harvesting techniques is implemented to produce a stable DC supply from the RF signals in the channel, to feed the different components of the system. Other works [1] define WuRs able to react to certain events or environmental conditions and awake the MCU as a consequence. Thanks to the implementation of low-power sensors for this task and because the systems are less prone to generating false wakeups, these solutions can result in a more efficient operation and a lower power consumption.

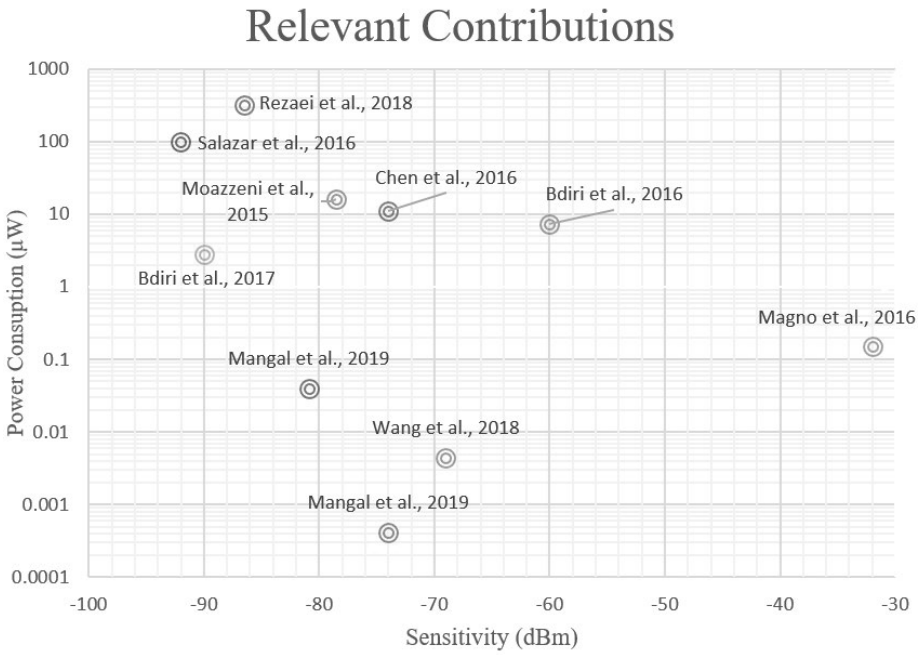


Figure 2. Representation of some of the most relevant state-of-the-art contributions in WuR design. Power consumption and sensitivity are the two most relevant parameters for WSN applications and, thus, the contributions are compared by means of these two metrics.

Many WuRs are based on the principle of envelope detection, consisting of a simple rectifier, and avoiding the use of local oscillators and phase-locked loops (PLLs), which leaves room for remarkable power savings at the cost of a limited sensitivity [1]. In Figure 2, it is clearly seen that a trade-off between power consumption and sensitivity

exists in WuR implementations. There is a frontier delimited by an imaginary line at the left-hand side of the figure, going from about 1 mW of power consumption to –75 dBm of sensitivity. Certainly, architecture selection plays a critical role when designing a WuR since some topologies lean toward higher power savings at the expense of sensitivity, and vice versa. One of the most significant differences lies in the use of active components such as amplifiers, mixers, or oscillators. When active RF components are used, the sensitivity is boosted, as well as the power consumption. On the other hand, it is possible to implement sub-nW WuRs if the power-hungry RF active components are kept to a minimum, or if they are carefully designed to present very low power consumption, thus improving the power consumption; however, the sensitivity is then limited to about –80 dBm.

In previous literature, different architectures provide sensitivity optimizations without major reductions in circuit area and costs-per-node, which are of utmost importance for system integration and low-cost densely populated networks. The aim of this work is to address these issues, presenting two different WuR implementations based on the tuned-RF architecture. The first circuit is based on [7], it employs a feedback amplifier and a band-pass filter to perform the envelope detection task. This circuit is developed as a proof-of-concept to replicate the results in [7]. The circuit achieves performance in line with most of the state-of-the-art solutions; however, it can be improved. Our main contribution is the introduction of the current-reuse feedback amplifier presented in [8] in the circuit proposed in [7], to improve the sensitivity, power consumption and area simultaneously. Therefore, in the second implementation of the WuR, the complex two-stage feedback amplifier is substituted by a feedback current-reuse topology. Both designs are presented from the schematic to the layout stage and are implemented in a low-cost standard CMOS process.

The remainder of this article is organized as follows: firstly, Section 2 offers a review of the existing WuR architectures and mentions some of the most relevant state-of-the-art contributions in each category. In Section 3, we present the development of two different WuRs in a low-cost CMOS commercial process. The performance of the proposed solutions and a comparison with the most relevant state-of-the-art solutions are shown in Section 4, and conclusions of this work are drawn in Section 5.

2. Wake-Up Receiver Architectures and State of the Art

A wide variety of topologies can be adopted when designing a WuR, as seen in 3. Although Zero- and Low-IF architectures are most frequently used in conventional receivers [9–13] they generally lead to high sensitivity, but have a power consumption that makes them unsuitable for low-power applications. Therefore, different solutions have been explored to reduce the power consumption of the receiver at the cost of reducing the sensitivity.

On the one hand, the simplest and most-used technique in the field of WuRs is radiofrequency envelope detection (RFED), shown in Figure 3a. With this approach the received signal is demodulated directly to base-band, avoiding the need for mixers and local oscillators (LOs), and potentially achieving very low power consumption [5]. Nevertheless, due to the inherent nonlinearity and wideband characteristics of the envelope detection process, RFED architectures are characterized by a high noise figure and low interference resilience when compared to other WuR architectures. Thus, the sensitivity these solutions can achieve is limited [13]. A common solution to improve the WuR's sensitivity consists of placing an LNA before the envelope detector to boost the signal-to-noise ratio (SNR), this architecture is known as tuned RF (TRF). A high gain is required from the LNA to reduce the contribution of the noise figure (NF) of the envelope detector, leading to a trade-off between sensitivity and power dissipation [4]. To improve the circuit's interference resilience, high-Q off-chip components can be used to implement the input filter [13]. Due to its simple architecture, and because many works prioritize power consumption over sensitivity, the RFED is one of the most frequent topologies in the literature [1,6,14–18]. In [6], a battery-less energy-harvesting WuR is demonstrated by implementing a passive RFED-based architecture. The front end uses no external power source since the receiver

converts the incident RF signal in a stable DC voltage to supply the different building blocks. In addition, various contributions [14–16] have reported RFED-based WuRs with very high sensitivities and a power consumption in the order of a few nW, by adding a large passive gain before the envelope detector. A sub-nW WuR achieving a sensitivity of −79 dBm is presented in [17], by implementing multi-stage passive energy detectors as well as a high-Q input matching network. However, these contributions exploit the latency–sensitivity trade-off by relaxing latency constraints to achieve such high WuR sensitivities [17].

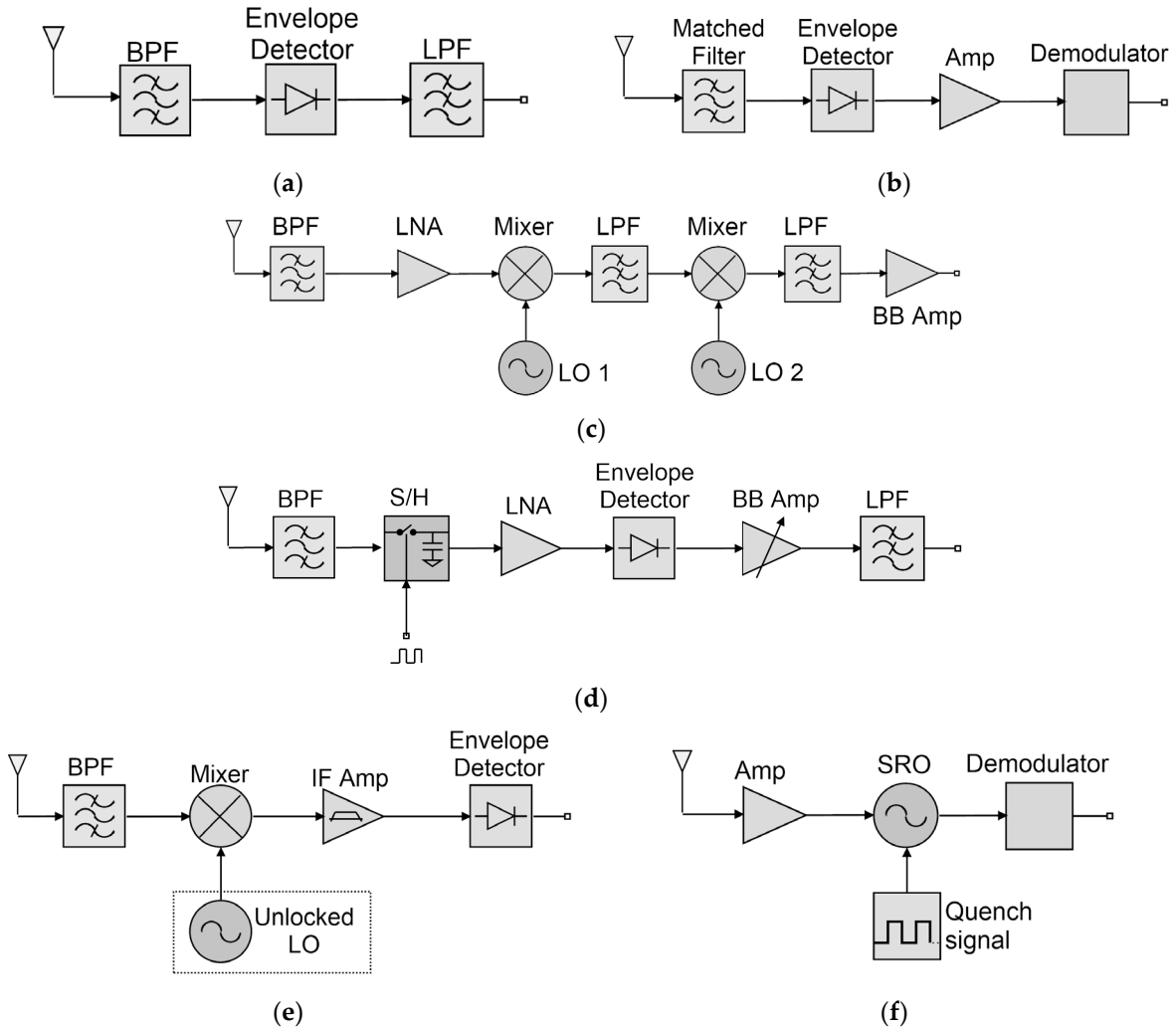


Figure 3. WuR topologies: envelope detector (**a**); matched-filter (**b**); superheterodyne (**c**); sub-sampling (**d**); uncertain-IF (**e**); and super-regenerative (**f**); and architectures.

A less common approach is the matched-filter architecture, employing widespread spectrum techniques to relax the dependence on the received signal strength and the issues related to in-band interferers. With the implementation of matched filters, the incoming signal spectrum is efficiently recovered in the receiver. A block diagram of this topology is presented in Figure 3b. These structures usually achieve low power consumption and high selectivity at the expense of sensitivity, caused by a high insertion loss due to the input matched filter [18]. An innovative code-domain matched filter is implemented in [19] to design a WuR with a sensitivity of –80.9 dBm and a power consumption of only 40 nW. The main receiver features a gate-biased envelope detector, followed by a current-reuse amplifier and an analog correlator. The analog correlator is composed of VCOs, delay lines and DACs, and a 4-phase filter is used to suppress VCO frequency and associated

harmonics. The output of the correlator is then fed to a comparator to identify the wake-up signal. The conventional superheterodyne (SH) architecture is a well-known, widely explored solution in the field of low-power receiver design. As shown in Figure 3c, the architecture employs an LNA and one or more mixers [20], followed by an IF amplifier to boost the SNR, and an ADC for digital base-band (DBB) signal processing. Since performing signal amplification at IF instead of RF is more power-efficient, such approaches often obviate the inclusion of an LNA to reduce power consumption at the expense of dealing with a higher NF. Following this approach can be advantageous in terms of sensitivity and interferer resilience, mainly because it is possible to design highly selective, low-power IF filters to reduce the impact of noise and blockers [13]. Generally, the SH receiver architecture yields a very high selectivity and overall performance compared to other solutions, but it presents a severe disadvantage. Due to the frequency synthesizers required to generate the mixing frequencies of the LO, the SH topology may present excessive power consumption, and thus, mixer-based architectures are only seen in applications where a power consumption over the range of tens of μW are acceptable. The superheterodyne architecture is possibly the most challenging approach to achieve an adequate performance in WuR design, mostly because of its complexity and the narrow margin to obtain power savings when compared to other architectures [4]. An example of an SH-based WuR is reported in [21], targeted for the band of 2.4-GHz with a high interference resilience. The receiver is designed for OOK-modulated signals, featuring a dual-IF N-path architecture with multiple inter-stage VGAs. The receiver provides a high sensitivity of –97 dBm at a data rate of 10 kbps, but the power consumption is as high as 99 μW.

The sub-sampling architecture is similar to the superheterodyne receiver, but in this case, the mixers are substituted by sample-and-hold (S/H) circuits [18], as depicted in Figure 3d. In this structure, the input signal is filtered and then converted to IF by the S/H circuit, which is followed by an IF amplifier and an envelope detector. In these receivers the RF LO is replaced by an accurate low-frequency LO, resulting in significant power savings [21]. Some works may include an RF LNA to improve receiver sensitivity, but then the power dissipation will be dominated by this element. One of the advantages of the sub-sampling architecture is that the designer has a certain degree of freedom when selecting the intermediate frequency (IF), since the sampling process results in the appearance of multiple signal replicas in the frequency domain [18]. Sub-sampling-based WuRs can achieve better sensitivity than RFED-based WuRs, but also at the cost of increased power consumption. A 2.4-GHz WuR based on the sub-sampling architecture can be found in [22]. The WuR is severely duty cycled to achieve the small power consumption of 7 μW, it achieves a remarkable sensitivity of –80 dBm and a reaction time of 30 ms. In [23], a dual-mode receiver with a sensitivity of –78.5 dBm and –75 dBm with a power consumption of 16.4 μW and 22.9 μW for the two modes (10 and 200 kbps data rates, respectively) is reported. The approach employs a two-stage differential S/H circuit followed by an LNA, an IF amplifier, and a conventional NMOS-based envelope detector.

One of the problems of having an LO is the need to include a PLL to generate the fixed, stable frequency required for signal down-conversion, which is a very expensive element in terms of power consumption. Similarly, as previously mentioned, the power overhead attributed to front-end LNAs can be quite significant. The uncertain-IF architecture, shown in Figure 3e, is aimed to address these two issues. This receiver structure implements no LNA and presents an IF that can vary in a delimited range, which is defined by an LO without PLL [18]. By doing so, the power consumption needed to amplify the signal at IF is reduced, too. In this case, since the signal down-conversion process covers a wide frequency range, uncertain-IF receivers are very vulnerable to interferers and, therefore, they usually require an external high-Q input filter [24]. In addition, this architecture can present high sensitivity, but it is limited due to the wide IF range the receiver must cover to be able to manage LO uncertainty, and the associated noise [21]. Nevertheless, the uncertain-IF architecture can be exploited to obtain sensitivities close to the SH architectures, while consuming less power. An example of an uncertain-IF based WuR for the UHF 408-MHz

frequency band can be found in [25]. The receiver achieves a sensitivity of –55 dBm at 50 kbps with a power consumption of 100 μW. The architecture employs a SAW filter at the input to improve selectivity, a mixer, and a multistage IF amplifier, followed by an envelope detection stage.

A unique solution to avoid the need to include PLLs is to use a tuned oscillator as a frequency-to-amplitude conversion block to extract FSK-modulated data from the incoming signal [26]. This is the principle behind the injection-lock architecture [27–29]. If the carrier frequency of the input signal is close to the LO frequency, coupling between both signals occurs and a single frequency appears at the output. This effect is called injection locking. However, if the carrier frequency of the incoming signal is not close enough to the LO frequency, the LO is perturbed, but there is no coupling between the signals, and the system generates two different tones. This is the effect of injection pulling. One of the drawbacks of using this technique is that the injection-lock receiver relies significantly on the input signal strength, and a trade-off between receiver sensitivity and power dissipation in RF amplifiers has to be considered by the designer [29]. A differential injection-lock-based receiver front-end incorporating an external loop antenna is developed in [29], operating at 433 MHz with a power consumption of 54 μW and a low-power of 11 μW. The receiver shows a sensitivity of –80/–78/–77 dBm under OOK/FSK/PSK modulation schemes at a data rate of 200 kbps. Additionally, an injection-locking digitally controlled oscillator is introduced in [28], reporting a sensitivity of –62 dBm for a data rate of 312 kbps, operating at 80 MHz with a power consumption of 45 μW.

As in the injection-lock topology, the super-regenerative oscillator (SRO) idea is another approach in which the generated oscillations are dependent on the input signal strength. The architecture, as shown in Figure 3f, is characterized by an RF oscillator changing periodically between stable and unstable states, and it is controlled by a low-frequency quench oscillator [30]. When the main oscillator is in stable-mode operation, the generated output signal amplitude is linearly proportional to the input signal amplitude. One distinctive characteristic of SRO-based WuRs is that the bias current of the oscillator is dynamically modulated to change between the two states. This can lead to a more selective bandpass filter than in injection-lock receivers, where an oscillator with a constant bias current is used [24]. It is, therefore, theoretically possible to achieve a better performance with an SRO-based WuR than with an injection-lock architecture in similar conditions. In contrast to the injection-lock and uncertain-IF architectures, an SRO-based WuR can receive OOK-, FSK- and ASK-modulated signals. Additionally, SRO-based WuRs are generally superior to SH-based WuRs due to the existence of positive feedback, which enhances receiver sensitivity and reduces power consumption [24]. The limitations of the SRO architecture are the excessive spurious emissions that do not meet some standard regulations, and the distortion introduced to the output signal. The latter, however, is less of a concern for amplitude modulation schemes. Hence, although the SRO-based WuRs often suffer from poor selectivity, the topology is employed in scenarios such as key-less remote transmitters and AM receivers [24]. While the SRO architecture can provide decent performance even at a sub-100 μW range, it suffers from some fundamental challenges. The SRO architecture presents the great disadvantage of requiring multiple calibration schemes to guarantee proper performance [24]. In addition, unknown frequency offsets between the desired channel and its operating frequency can be produced by the amplitude variation at the SRO's output. Finally, during the implementation of an SRO-based receiver, the designer must consider the existing trade-offs between sensitivity and power consumption, and back-radiated signal power. In [31], the authors propose an SRO-based WuR with a self-quench circuit and a technique to prevent oscillations when no carrier is present. This solution employs PWM wake-up codes and low-power decoding, achieving a sensitivity of –63.8 dBm and a power consumption of 20 μW, operating at the 28-MHz human-body communications (HBC) frequency band. A binary search algorithm is used in [24] for calibration of the quench signal and the receiver's operating frequency. A sensitivity of –86.5 dBm and –101.5 dBm is reported for data rates of 1000 kbps and 31.25 kbps, respec-

tively. The system operates in the 902–928 MHz ISM band with a power consumption of 320 μW. In addition, a high-performance SRO-based WuR with a power consumption of only 1 μW and a sensitivity of –90 dBm has been reported [32].

Considering all the alternatives presented, the envelope detection approach is the architecture that achieves the lowest power consumption [5,19]. This feature comes at the cost of limited sensitivity, making the RFED technique suitable in WSNs where the nodes are close to each other. In applications with scattered nodes, alternative structures may produce more appropriate results due to the need for higher sensitivity. Otherwise, an increment in transmitted signal power would be required to reach the nodes and overcome the poor sensitivity characterizing the sensors' RF interface. The tuned-RF strategy can solve this issue by introducing better sensitivity at the expense of slightly higher power consumption. Since many works include off-chip components to improve receiver performance, namely power consumption, sensitivity and selectivity, WuR integration is another challenge [21]. Many of these contributions show high power efficiency, but they usually suffer from a poor selectivity and high power dissipation, making them less suitable for densely populated WSN scenarios and applications requiring a power consumption under 100 μW [21]. As mentioned before, some WuR implementations use high-Q external resonators for narrowband filtering at RF, or to serve as accurate time-base references for the LO [21]. Nevertheless, the inclusion of these bulky and costly elements yields a more expensive bill of materials and assembly costs per device, which may be incompatible with low-cost WSNs [21]. Therefore, we avoid the use of this external circuitry to maintain a high level of integrability.

3. CMOS-Integrated WuR Design with a Feedback Configuration and Current-Reuse Technique

The implementation of the WuR is depicted schematically in Figure 1, with a target frequency of 868 MHz corresponding to the European definition of the industrial, scientific, and medical (ISM) band. Since the tuned-RF architecture is selected to implement the WuR, the OOK scheme is better suited as a modulation scheme for the wake-up signal. In the block diagram shown in Figure 1, the wake-up signal is received by the sensor while it is listening to the ISM channel. Node A represents the OOK signal at the WuR's input, whereas at node B the wake-up signal's envelope is obtained. The signal at node B contains the wake-up pattern or signature to be demodulated by the signal correlator. This element operates in the frequency range of 15 kHz to 150 kHz, and its main purpose is to recognize the wake-up pattern. If it is recognized, then an interruption is generated so that the main MCU is awakened, and conventional communications can occur. The T/R switch is set by the MCU and allows two possible paths for the input signal: a path to receive the wake-up signal when the sensor is in low-power mode, and a path for the conventional radio communications.

The wake-up signal used in this configuration is obtained from a low frequency sequence (0.5 to 4 kbit/s) modulated with a high frequency carrier (15 kHz to 150 kHz), which is then modulated again with a carrier of 868 MHz [3]. With this approach, the same antenna can be used for conventional communications and wake-up signaling. With this approach, a circuit as low-cost and low-power as the AS3933 can be employed as a signal correlator [13].

3.1. Tuned RFED WuR with a Feedback Pre-Amplifier

The architecture employed to implement the WuR is based on the tuned-RF topology, so that the circuit is composed of an input matching network, a rectifier, and a low-pass filter. Some improvements can be applied to the basic RFED WuR scheme by adding a two-stage pre-amplifier to increase the sensitivity of the circuit, at the expense of slightly higher power consumption. This is the principle behind the tuned-RF architecture presented in Section 2. Moreover, this element can be implemented in a feedback configuration, as introduced by [7], boosting the WuR's sensitivity with very low power consumption. The

circuit implementation is shown in Figure 4, based on the work proposed by [7]. The design consists of two different blocks: the first stage is formed by an input-matching network, a low-power amplifier, a band-pass filter and a second ultra-low power amplifier; the second stage is composed of two base-band amplifiers and a low-pass filter.

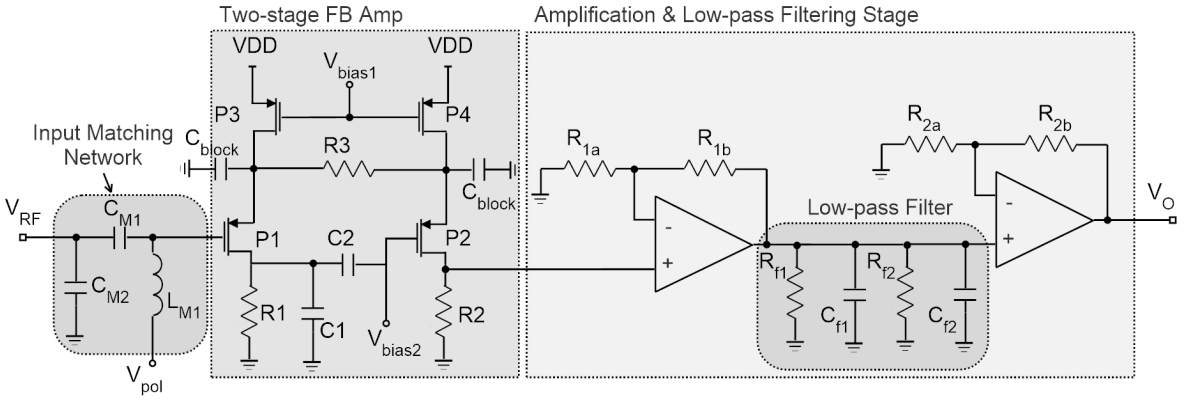


Figure 4. RFED WuR with a feedback amplifier stage [7].

The feedback amplifier used in the first stage is composed by PMOS transistors, since they present lower flicker noise than NMOS transistors. The first amplification is performed by the common-source transistor P1, biased in weak inversion and drawing a current of 2.95 µA, which simultaneously performs as an RF detector and baseband LNA [7]. An RF suppression filter is formed by R1 and C1, and the MOS transistor P2 enhances the low frequency gain thanks to the feedback path opened through R3. The capacitor C_{block} sets the low cut-off frequency, whilst R1 and C1 adjust the upper cut-off frequency. This combination has a band-pass effect, performing the first step of the envelope detection task. The second common-source amplifier is formed by the PMOS transistor P2, biased with a drain current of 2.02 µA. The PMOS transistor P3, acts as the load of P1, and the same applies to P4 and P2. The amplifiers operate with a V_{DD} = 1 V, V_{bias1} = 0.01 V, V_{bias2} = 0.57 V and V_{pol} = 0.05 V, to maintain low power consumption. The second stage is composed by two operational amplifiers in a feedback non-inverting configuration, with a gain of 25 dB per stage and a second-order low-pass filter. The bandwidth of this stage has been designed to cover from 100 kHz to 1 MHz to obtain the OOK input signal's envelope, as shown in Figure 5.

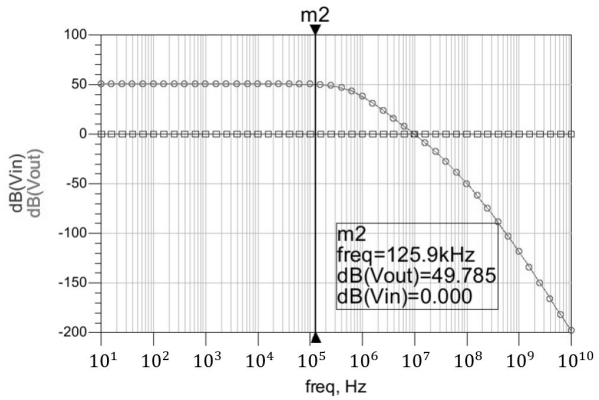


Figure 5. Simulation results of the pre-amplifier and the filter.

The results regarding the input matching of the full circuit are shown in Figure 6a, showing that an Input Return Loss better than 20 dB is obtained at 868 MHz in simulations. To determine the WuR's sensitivity, a harmonic balance simulation is needed to verify the output power of the WuR. The harmonic balance simulation results of the complete WuR are depicted in Figure 6b,c, where we are using an AM input signal of –71.6 dBm and

868 MHz plus two tones (868.875 MHz and 868.125 MHz) of –75 dBm each. Considering that the AS3933 needs at least 113.15 μV_p to be able to recognize the pattern, a minimum input power of –63.2 dBm is required to be able to detect the WuR signal.

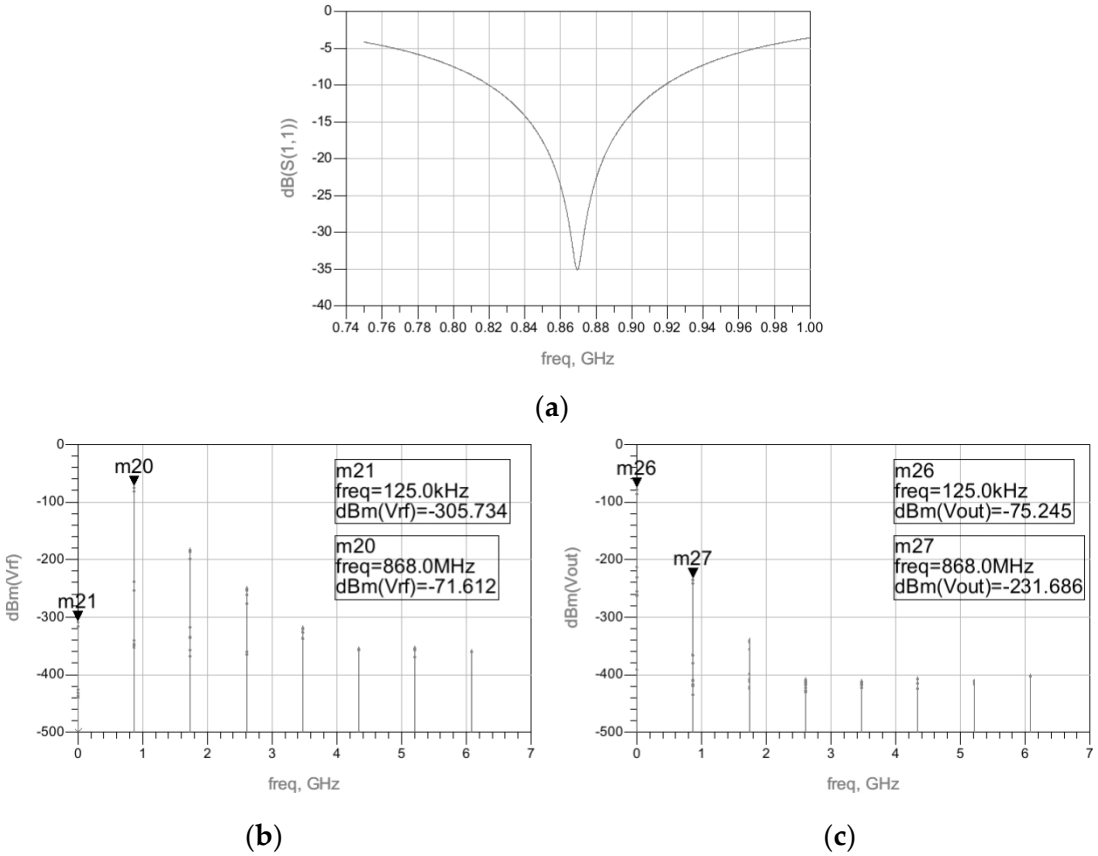


Figure 6. Input Return Loss simulation results of the feedback WuR with amplification and low-pass filtering stages (**a**) and harmonic balance simulation results of the WuR for the RF input signal (**b**) and the WuR's output (**c**).

Finally, a time-domain simulation is presented in Figure 7, showing the AM input signal (V_{rf}), the output of the first stage (V_{in}), and the output of the second stage (V_{out}). As shown, the signal at the first stage's output contains the unfiltered envelope of the wake-up pattern, and after the second-stage filtering the output is completely clean. The value of the feedback resistors, as well as the components of the low-pass filter used, are given in Table 1. The complete stage presents a gain of 50 dB in simulations, with a power consumption of only 1.8 µW. The simulation results show a sensitivity of –63.2 dBm for the complete WuR, with a power consumption of 6.77 µW, concluding that this circuit achieves improved sensitivity and power consumption in comparison with the previously developed solutions.

This design is implemented to operate from a 1-V DC supply with all the values given in Table 1. The layout of the first stage is presented in Figure 8, with a total size of 230 × 160 μm^2. As seen, the two DC block capacitors are the bulkiest components in this implementation. The total size of the complete layout, including the op-amps and the second-stage low-pass filters, is 398 × 266 μm^2.

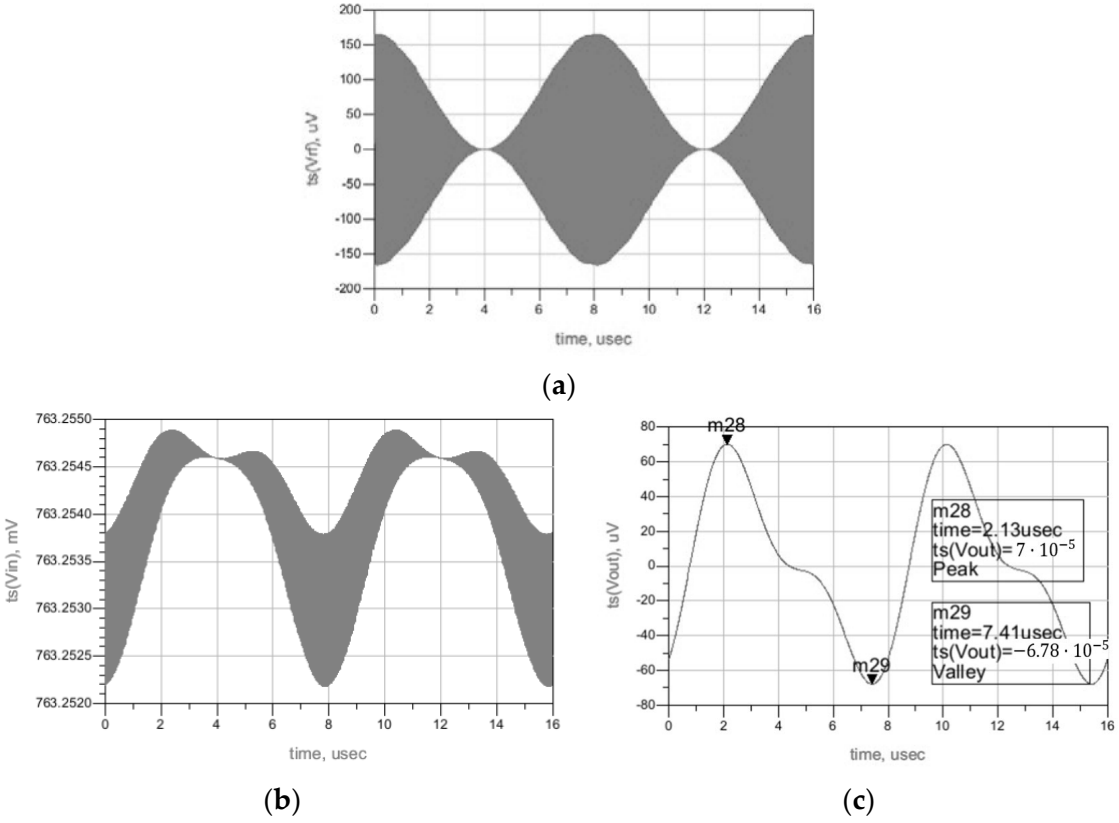


Figure 7. Time-domain simulation results of the WuR with amplification and low-pass filtering stages. AM input signal (V_{rf}) (**a**), the output of the first stage (V_{in}) (**b**), and the output of the second stage (V_{out}) (**c**).

Table 1. Summary of component values for the tuned RFED with feedback amplifier WuR.

Parameter	Value	Parameter	Value
P1	(200 µm/3 µm)	L_{M1}	6.7 nH
P2	(1.6 µm/0.4 µm)	R1	90 kΩ
P3	(1 µm/3 µm)	R2	799 kΩ
P4	(2 µm/2 µm)	R3	250 kΩ
C1	1.4 pF	R_{1a}, R_{1b}	1 kΩ
C2	300 fF	R_{2a}, R_{2b}	17 kΩ
C_{block}	250 nF	R_{f1}, R_{f2}	100 Ω
C_{block2}	400 pF	V_{bias1}	0.01 V
C_{f1}, C_{f2}	10 pF	V_{bias2}	0.57 V
C_{M1}	1.9 pF	V_{pol}	0.05 V
C_{M2}	840 fF	V_{DD}	1 V

3.2. Tuned RFED WuR with Current-Reuse Pre-Amplifier

A possible improvement of the circuit presented in Figure 4 is to adopt a current-reuse approach to reduce the power consumption in the feedback amplifier of the first stage. In addition, by adopting the current-reuse technique, the current mirror formed by P3 and P4 can be eliminated and all the passives (R1 to R3 and C1, C2 and C_{block}) can be simplified. The first-stage feedback amplifier with current-reuse is an inverter in a feeback configuration, and is depicted in Figure 9 [8].

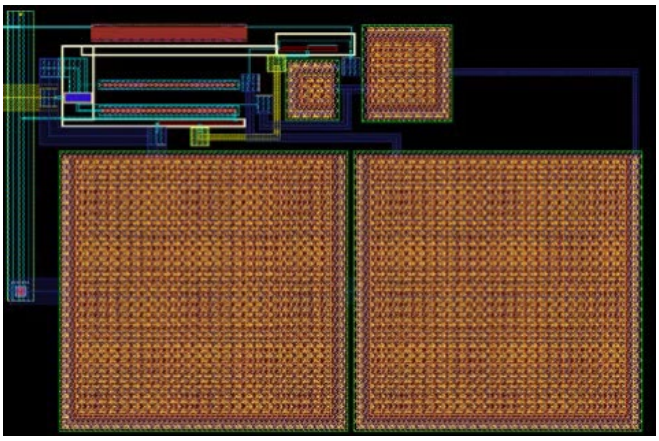


Figure 8. Layout of the two-stage feedback amplifier, total size of 230 × 160 μm^2.

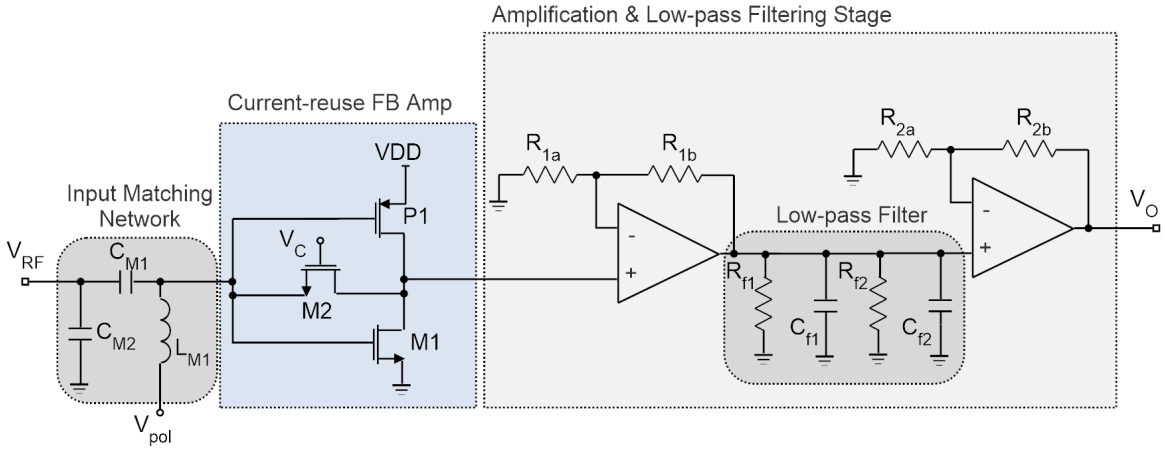


Figure 9. RFED WuR with current-reuse amplifier [8].

The enhancement introduced by this topology is mainly due to the addition of the PMOS transistor's transconductance to the equivalent g_m of the circuit, as shown in (1), where g_{mN} and g_{mP} are the NMOS and PMOS transconductances, respectively, and R_F is the value of the feedback resistor. The PMOS P1 reuses the biasing current of the NMOS transistor M1, with a value of 1.83 μA from a 1-V DC supply. Transistor M2 is used in the feedback path since a high resistance is required to maintain a low NF, also achieving high g_m-boosting for improved AC gain and a reasonable power consumption [8]. By using M2 instead of a conventional resistor the circuit avoids the large footprint and resistance tolerances associated with integrated resistors, while achieving a very small area. The only drawback of this approach is the need for an additional DC control voltage (V_C), which is set to 0.72 V. Likewise, V_{pol} is set to 0.45 V to bias the gate of M1 and P1 with a reasonable performance. To obtain high resistance, transistor M2 is a long-length, narrow device with a size of (80 nm/3 μm). Since it presents a feedback configuration, the input impedance of the circuit is given by (2), where A_v represents the circuit AC gain. The AC gain increment ensures a high bandwidth, given as (3), since it relaxes the contribution of the parasitic capacitances due to M1 and P1. In this equation, C_{gsN} and C_{gsP} refer to the NMOS and PMOS gate-source capacitance, respectively. In this case, the band-pass filter in the feeback amplifier is eliminated, as the filter in the second stage is enough to obtain the input signal's envelope. The advantage of this topology is the compact size and low power consumption achievable thanks to the implementation with only three MOSFETs.

$$|A_v| \approx (g_{mN} + g_{mP}) \cdot R_F \tag{1}$$

$$Z_{in} \approx \frac{R_F}{1 + |A_v|} \tag{2}$$

$$BW_{3\text{dB}} \approx \frac{1 + |A_v|}{R_F\left(C_{gsN} + C_{gsP}\right)} \tag{3}$$

As shown in Figure 10a, an Input Return Loss better than 20 dB is obtained at 868 MHz in simulations for the full circuit including the second-stage amplifier and filter. In addition, the harmonic balance simulation is presented in Figure 10c. In this case, we are using an AM input signal of –90 dBm and 868 MHz, plus two tones of –95 dBm each, resulting in a sensitivity of –75 dBm.

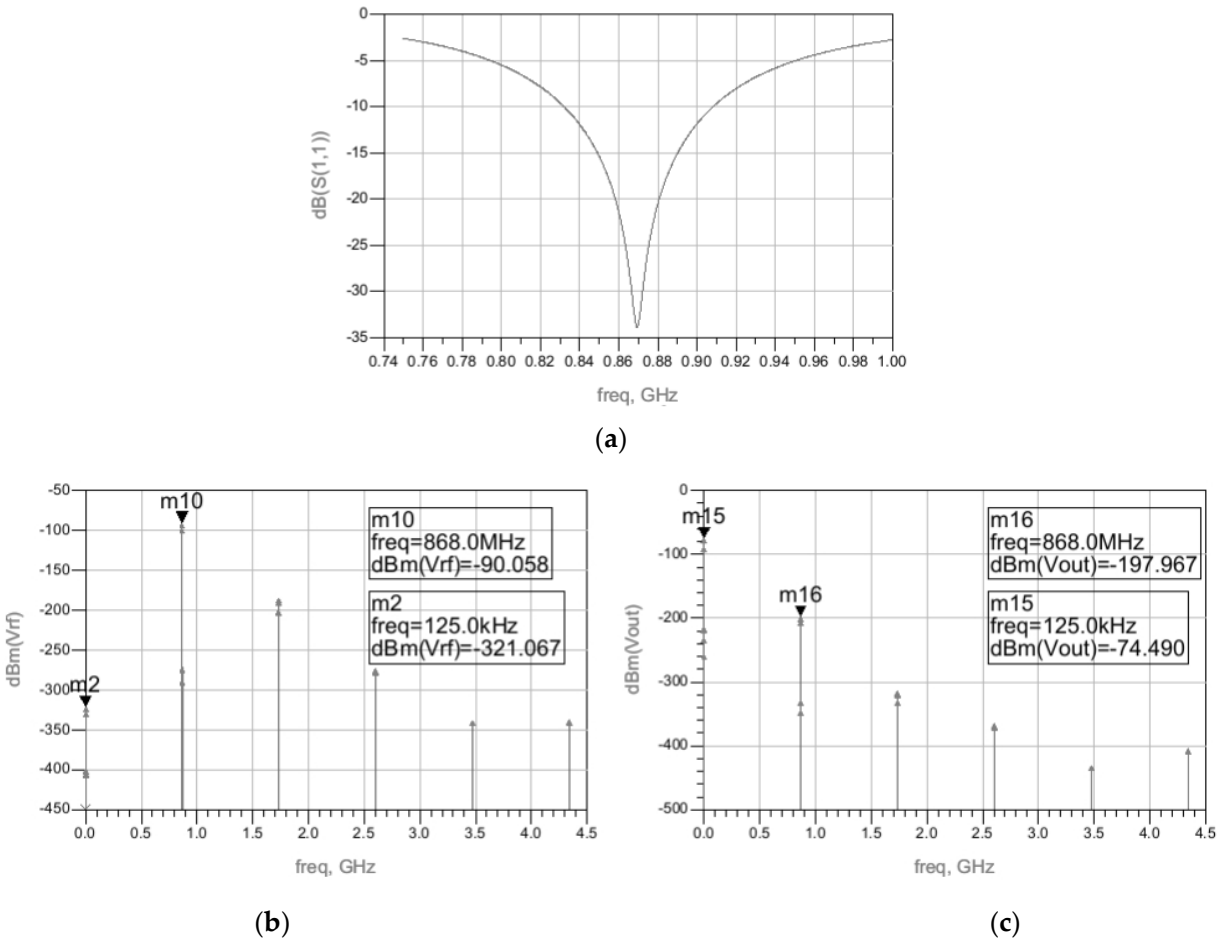
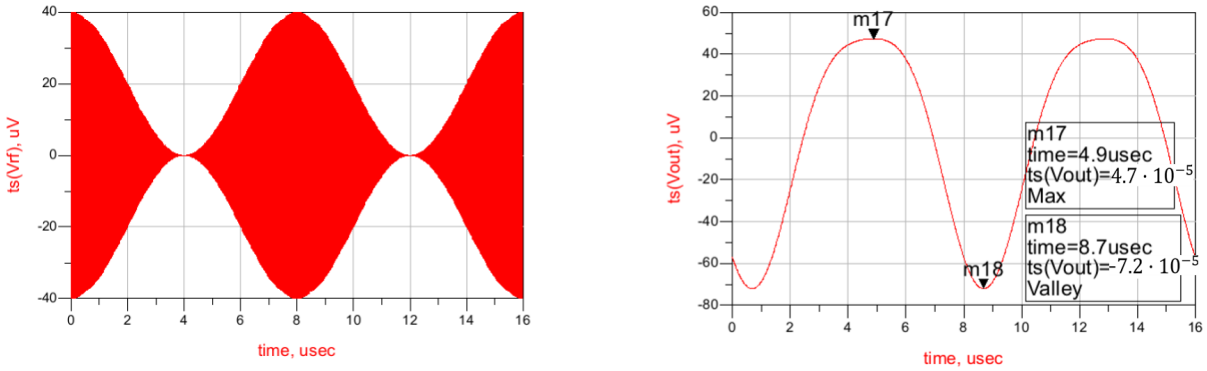


Figure 10. Input Return Loss simulation results of the current-reuse feedback WuR with amplification and low-pass filtering stages and harmonic balance simulation results. Input Return Loss of the circuit (**a**), harmonic balance AM input signal (**b**), and WuR's output signal (**c**).

The results regarding the time-domain simulation are shown in Figure 11. As seen, the signal is effectively filtered, and at the output of the WuR signal is completely clean.

The layout of the current-reuse feedback amplifier, shown in Figure 12, occupies an area of only 20 × 35 μm^2 with a power consumption of 1.83 μW. The complete layout, including the op-amps and low-pass filters, results in a size of 262 × 262 μm^2. The circuit is almost ten times smaller than the previously developed feedback amplifier, since there are no passive elements in the structure. All the elements forming the second stage have their values presented in Table 2. The full circuit simulations reveal an input return loss of 32.5 dB, with a sensitivity of –75 dBm and a power consumption of only 3.63 μW.



(**a**) (**b**)

Figure 11. Time-domain simulation results of the current-reuse feedback WuR with amplification and low-pass filtering stages. Input (**a**) and output signals (**b**).

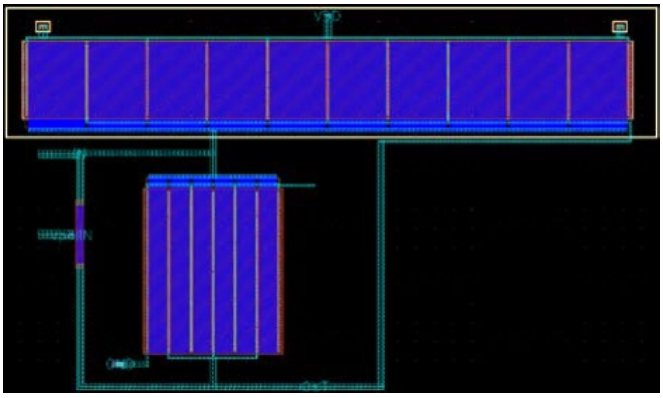


Figure 12. Layout of the current-reuse feedback amplifier used in the WuR.

Table 2. Summary of component values for the tuned RFED with feedback amplifier WuR.

Parameter	Value	Parameter	Value
M1	(51 µm/0.97 µm)	R_{1a}, R_{1b}	1 kΩ
M2	(0.08 µm/3 µm)	R_{2a}, R_{2b}	17 kΩ
P1	(1 µm/3 µm)	R_{f1}, R_{f2}	100 Ω
C_{f1}, C_{f2}	10 pF	V_C	0.72 V
C_{M1}	1.1 pF	V_{pol}	0.45 V
C_{M2}	1.02 pF	V_{DD}	1 V
L_{M1}	4.26 nH		

4. Overview and Discussion

Two structures based on the tuned-RF principle have been explored. To improve the WuR's sensitivity and power consumption simultaneously, a structure formed by a feedback amplifier and a band-pass filter, followed by two op-amps and a low-pass filter, is studied. This circuit obtains a sensitivity of –63.2 dBm, with a power consumption of only 6.77 µW and a total size of 398 × 266 µm^2, of which only 230 × 160 µm^2 are occupied by the feedback pre-amplifier. Thus, with this approach, the sensitivity and power consumption of the WuR are simultaneously improved. The second design presented utilizes a current-reuse feedback amplifier to further reduce the power consumption and die footprint. This approach gives a remarkable sensitivity of –75 dBm in simulations with a power consumption of only 3.63 µW and a die footprint as low as 262 × 262 µm^2, of which only 20 × 35 µm^2 are occupied by the current-reuse feedback amplifier in the first stage. That is, the area of the first stage is reduced from 36,800 µm^2 to 700 µm^2, simultaneously improving the WuR's sensitivity and power consumption. The tuned-RF WuR with current-reuse

pre-amplifier achieves one of the best trade-offs between performance and die footprint of all the explored solutions. A visual comparison between our main contributions and some of the most relevant state-of-the-art solutions in the field of WuR design, in terms of power consumption and sensitivity, is presented in Figure 13. The acronym RFED-FB refers to the tuned-RF WuR with a feedback topology, and RFED-Curr refers to the current-reuse circuit presented in this work. Note that only sensitivity and power consumption are considered in the figure, and the die footprint is not included. A comparison of circuit performance is given in Table 3 with a higher level of detail. In the table, the value used for the figure of merit (FoM_{LAT}) is obtained from [13], and is defined in Equation (4). Again, in this equation, only sensitivity and power consumption are considered as the two most relevant performance parameters in WSN nodes. However, this definition of the FoM may not be as suitable for applications where the nodes present a high throughput. That is why we used the FoM_{ARE} in Equation (5) [3], to include the circuit area. As seen in Table 3 and in Figure 13, the RFED WuR with current-reuse feedback amplifier presents a better trade-off that the other proposed circuits.

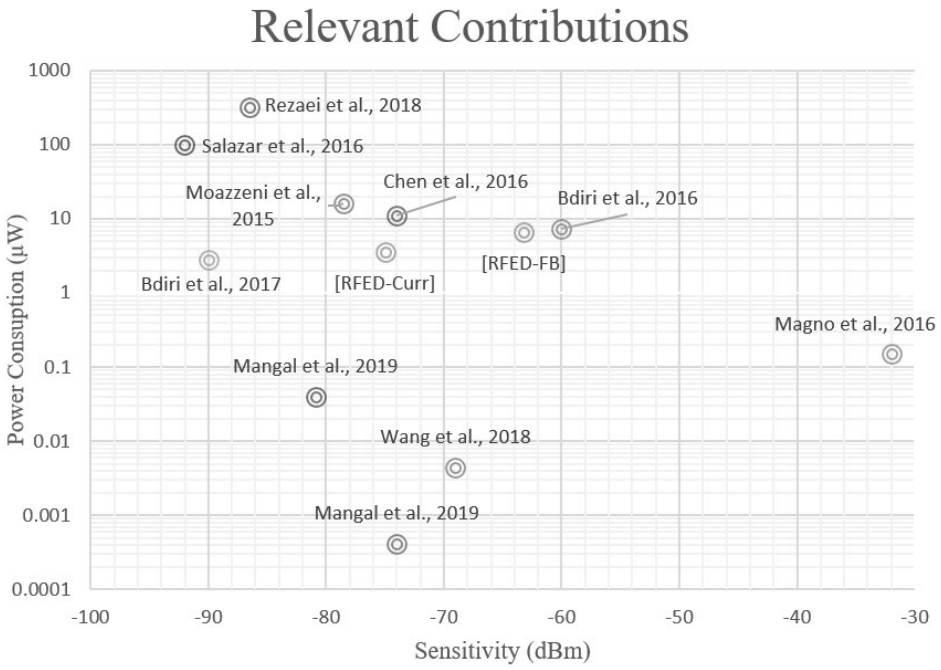


Figure 13. Representation of the performance of the proposed contributions along with some of the most relevant state-of-the-art works involving WuR design.

The authors in [4] also adopt a tuned-RF architecture in the implementation of a WuR, with a remarkable performance. To reduce power consumption with low latency, a modified MAC protocol, along with enhanced duty-cycled listening, are used. In [13], an integrated transformer is used within an RFED WuR to obtain a passive gain of 25 dB achieving a very high sensitivity with a power consumption of only 4.5 nW. On the other hand, the work in [21] is an example of an uncertain-IF WuR. In this proposal, the power consumption is 99 µW while achieving an outstanding sensitivity of –97 dBm. An example of the injection-lock architecture can be found in [29]. In this article, an external loop antenna is presented, and two operation modes are implemented to obtain high sensitivity and low power consumption. The WuR shown in [24] is based on the SRO strategy, and therefore, is characterized by the highest power consumption of all the explored solutions. A fully integrated WuR is proposed in [17]. The circuit is composed of 40-stage gate-biased self-mixers and matched filters with DC offset cancellation, achieving a power consumption of about 1 nW and sensitivity of –74 dBm. The authors of [19] present a WuR based on a code-domain matched-filtering strategy, where a continuous time analog correlator is

employed as pattern recognizer, reporting a very high performance WuR. The work in [2] proposes the implementation of an RFED WuR with off-chip components; the envelope detector is composed by Schottky diodes and the AS3933 circuit is used as correlator. Finally, another RFED WuR in a PCB fashion is presented in [33] using the TI CC430F5147 SoC, which implements an MCU and a transceiver. This solution employs two antennas to improve the accuracy instead of sharing the path by using a T/R Switch, as we did. It is seen that the developed WuR with a current-reuse feedback amplifier is superior to the proposals in [2,23,24,29,33] in terms of the sensitivity and power consumption trade-off. If we include the area efficiency in the FoM as indicated by Equation (5), the current-reuse feedback amplifier is clearly superior to all the explored solutions but [17,19], which are superior both in sensitivity and power consumption. Thus, we can conclude that the current-reuse feedback WuR presented in this work shows a performance in line with most of the state-of-the-art contributions and is superior in terms of area use. This fact makes the circuit especially suitable for circuits and application scenarios where a high integrability is required.

Table 3. Performance summary of the explored RFED-based solutions.

WuR Topology	Frequency (GHz)	Sensitivity (dBm)	Power Consumption (μW)	Area (μm^2)	FoM_{LAT} (dB)	FoM_{ARE} (dB)
RFED w/feedback amp.	0.868	–63.2	6.77	398 × 266	84.9	34.6
RFED w/current reuse	0.868	–75	3.63	262 × 262	99.4	51
[2] RFED	0.868	–60	7.5	37,000 × 22,000	81.2	−7.9
[33] RFED	0.868	–32/–55	0.152/1.2	–	70.2/84.2	–/–
[4] Tuned-RF	0.868	–90	2.8	46,300 × 24,500	115.5	25
[23] Sub-sampling	0.915	–78.5	16.4	1000 × 200	96.4	43.3
[13] RFED w/transformer	0.1135	–69	0.0045	(PCB)	122.5	–
[21] Uncertain-IF	2.4	–97/–92	99	360 × 160	107.0/102.0	54.4
[29] Injection-Lock	0.433	–80/–74	54/11	900 × 500	91.4/93.6	37.1
[24] SRO	0.915	−86.5	320	900 × 500	91.4	34.9
[17] Self-mixer + DLL	0.151/0.434/1.016	–79/–79.2/ –74	~0.00042	370 × 250	142.8/143/137.8	93.1/93.3/88.1
[19] CT-Analog Correlator	0.4508	–80.9	0.04	500 × 480	124.9	71

$$\mathrm{FoM_{LAT}(dB)} = -P_{SEN}(\mathrm{dBm}) - P_{DC}(\mathrm{dBm}) - 60 \quad (4)$$

$$\mathrm{FoM_{ARE}(dB)} = -P_{SEN}(\mathrm{dBm}) - P_{DC}(\mathrm{dBm}) - 10 * \log\left(area\left(\mu\mathrm{m}^2\right)\right) \quad (5)$$

5. Conclusions

The design of two WuRs based on the tuned-RF principle operating in the 868-MHz ISM band has been presented. The focus of our proposals is centered on area reduction to provide high integrability and maintain a low cost-per-node. In particular, we have presented a design based on [7] and improved the area use of the circuit by adding a current-reuse approach as in [8]. These characteristics result in an easier implementation of sensor nodes in low-cost IoT applications. The discussed alternatives show a performance in line with most of the state-of-the-art contributions, with a very low die footprint, making the topologies attractive in situations where a high integrability and low cost-per-node is pursued. The first solution is composed of a feedback amplifier, two op-amps plus a low-pass filter. The circuit achieves a sensitivity of –63.2 dBm with a power consumption of 6.77 μA and an area as low as 398 × 266 μm^2. The second design is aimed at improving the power consumption and area simultaneously by using a current-reuse feedback amplifier. With this technique the power consumption is halved (resulting in 3.63 μA) and the resulting circuit area is as low as 262 × 262 μm^2. Thanks to the nature of the circuit, the sensitivity is improved to –75 dBm. This latter proposal is particularly suitable in applications where a fully integrated WuR is desired, providing a reasonable sensitivity with low power consumption and a very low die footprint, therefore facilitating the integration with other components of the WSN node. A thorough discussion of the most relevant state-of-the-art solutions has been presented, too, and the two developed solutions are compared to the

most relevant contributions available in the literature. Two different definitions of the FoM are presented, with one valuing mainly the sensitivity and power consumption, and another considering the circuit's area as well. In this sense, it is shown that the current-reuse feedback WuR is superior to most of the explored solutions and achieves one of the best trade-offs between area and performance.

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Abbreviations

ADC	Analog-to-Digital Converter
ASK	Amplitude-Shift Keying
CMOS	Complementary Metal-Oxide Semiconductor
DAC	Digital-to-Analog Converter
DBB	Digital Baseband
DC	Direct Current
FoM_{ARE}	Figure of Merit (Area)
FoM_{LAT}	Figure of Merit (Latency)
FSK	Frequency-Shift Keying
HBC	Human-Body Communications
IF	Intermediate Frequency
IoE	Internet of Everything
IoT	Internet of Things
ISM	Industrial, Scientific, and Medical
LNA	Low-Noise Amplifier
LO	Local Oscillator
MAC	Medium-Access Control
MCU	Microcontroller Unit
MOSFET	Metal-Oxide Semiconductor Field-Effect Transistor
NF	Noise Figure
OOK	On–Off Keying
PLL	Phase-Locked Loop
PSK	Phase-Shift Keying
PWM	Pulse-Width Modulation
RF	Radiofrequency
RFED	Radiofrequency-Envelope Detection
SH	Superheterodyne
S/H	Sample-and-Hold
SoC	System-on-Chip
SRO	Super-regenerative Oscillator
SNR	Signal-to-Noise Ratio
T/R	Transmitter/Receiver
TRF	Tuned-RF
VCO	Voltage-Controlled Oscillator
VGA	Variable-Gain Amplifier
WuR	Wake-up Receiver
WSN	Wireless Sensor Network

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2.3. Miniature Wide-Band Noise-Canceling CMOS LNA

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Communication

Miniature Wide-Band Noise-Canceling CMOS LNA †

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Abstract: In this paper, a wide-band noise-canceling (NC) current conveyor (CC)-based CMOS low-noise amplifier (LNA) is presented. The circuit employs a CC-based approach to obtain wide-band input matching without the need for bulky inductances, allowing broadband performance with a very small area used. The NC technique is applied by subtracting the input transistor's noise contribution to the output and achieves a noise figure (NF) reduction from 4.8 dB to 3.2 dB. The NC LNA is implemented in a UMC 65-nm CMOS process and occupies an area of only 160 × 80 μm^2. It achieves a stable frequency response from 0 to 6.2 GHz, a maximum gain of 15.3 dB, an input return loss (S11) < −10 dB, and a remarkable *IIP*3 of 7.6 dBm, while consuming 18.6 mW from a ±1.2 V DC supply. Comparisons with similar works prove the effectiveness of this new implementation, showing that the circuit obtains a noteworthy performance trade-off.

Keywords: RFIC; wide-band; low noise amplifier; current conveyor; noise canceling; CMOS

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1. Introduction

A low-noise amplifier (LNA) is one of the key elements in a wide-band receiver. As the first element in the receiving chain, its noise figure (NF) and gain have a greater impact than other modules on the overall performance. Source impedance matching is also required to limit reflections. Conventional broadband LNA designs, such as resistive-loaded common source (CS) or common gate (CG) amplifiers, have proven difficult to meet the above requirements [1]. On the other hand, amplifiers employing a global negative feedback can achieve low NF with good input matching, but they are prone to becoming unstable [2]. Other alternatives, such as distributed amplifiers (DAs) [3] or cascode amplifiers with LC broadband input-matching networks [4–6], provide good impedance matching and high gain in a larger frequency range, but they need several inductors. Another topology used to design broadband LNAs is based on the use of current conveyors (CC) [7–9]. Although they have many advantages, such as good input matching, high linearity, and low power consumption, they suffer from the drawback of having a relatively high NF. In this paper we explore the use of noise-canceling techniques [10–12] to obtain a significant reduction in the NF of CC-based broadband LNAs. The goal is to present an amplifier topology that combines the advantages of a CC-based circuit with the possibility of reducing the NF at the output of the circuit.

The organization of the paper is as follows. In Section 2, a wide-band amplifier based on CC is discussed. In Section 3, the noise-canceling technique of a CG amplifier is presented. The CC-based amplifier with noise cancelation is introduced in Section 4.

Section 5 reports the simulation results of the proposed LNA implemented in a UMC 65-nm CMOS process. Finally, conclusions of this work are drawn in Section 6.

2. CMOS Current Conveyor Based LNA

The basic topology of a CC-based amplifier using CMOS technology is shown in Figure 1. It consists of an input CG gain stage (M1), followed by a source follower stage (M2) [8].

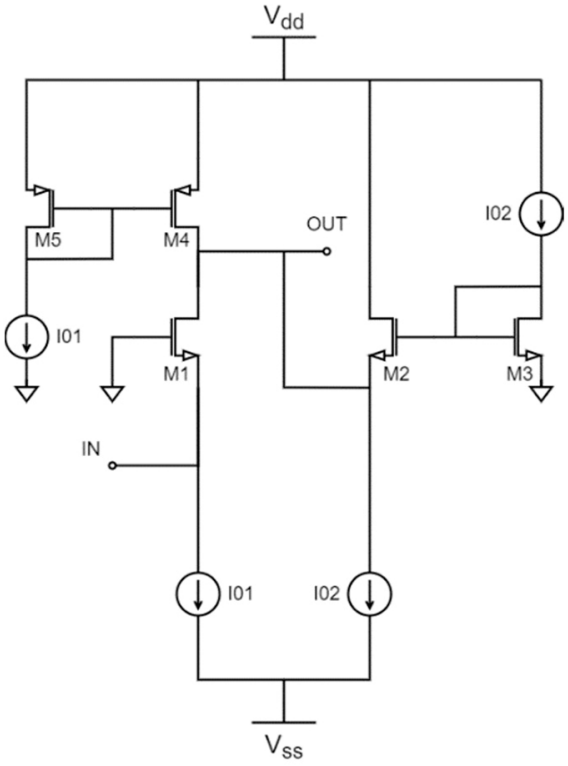


Figure 1. CMOS LNA based on current conveyors with ideal current sources.

The DC gain (G), bandwidth ($f_{-3\text{dB}}$), and noise factor (F) can be calculated as shown by (1), (2), and (3), respectively, where g_{m1} and g_{m2} are the M1 and M2 transconductances, C_T represents the total parasitic capacitance at the output node, and γ is the excess noise factor, which is a constant that depends on the transistor size.

$$G = \frac{g_{m1}}{g_{m2}} \tag{1}$$

$$f_{-3\text{dB}} = \frac{g_{m2}}{2\pi C_T} \tag{2}$$

$$F = 1 + \gamma\left(1 + \frac{g_{m2}}{g_{m1}} + \frac{g_{m4}}{g_{m1}}\right) \tag{3}$$

The circuit's input and output impedances can be easily computed as

$$Z_{in} = \frac{1}{g_{m1}}, \tag{4}$$

$$Z_{out} = \frac{1}{g_{m2}}. \tag{5}$$

There is a trade-off between g_{m1} and g_{m2} and, consequently, between the transistor sizes and bias currents. Current I_{01} affects the gain through g_{m1}, but has no effect on the bandwidth, while I_{02} controls the gain and bandwidth through g_{m2} (if I_{02} is increased, the

bandwidth increases, but the gain is decreased). On the other hand, when g_{m1} increases, F decreases, as shown in (3). This can be done by increasing the size of M1 or the current I_{01}. Likewise, if M2 and M4 are either smaller or biased with a lower I_{02}, F decreases. Finally, the input and output impedances are directly related to their associated transistors and bias currents. For example, through I_{01}, Z_{in} can be matched to the source impedance without resorting to matching networks, allowing for a much smaller circuit when compared to conventional topologies. This is one of the main advantages of this approach. Following this discussion, the bias currents I_{01} and I_{02} are selected as 1 mA and 200 µA, respectively, to maintain a reasonable power consumption.

The complete implementation of the circuit schematic is shown in Figure 2, where the ideal current sources have been replaced by current mirrors. The high number of transistors certainly affects the performance of the circuit, especially bandwidth, noise, and power consumption. Due to the low output conductance of transistors in deep submicron technologies, the input impedance also deviates from the conventional $1/g_m$ value. This, rather than being a problem, can be useful to isolate the input-matching condition from the noise-canceling one, providing a degree of freedom in the input-matching design [12].

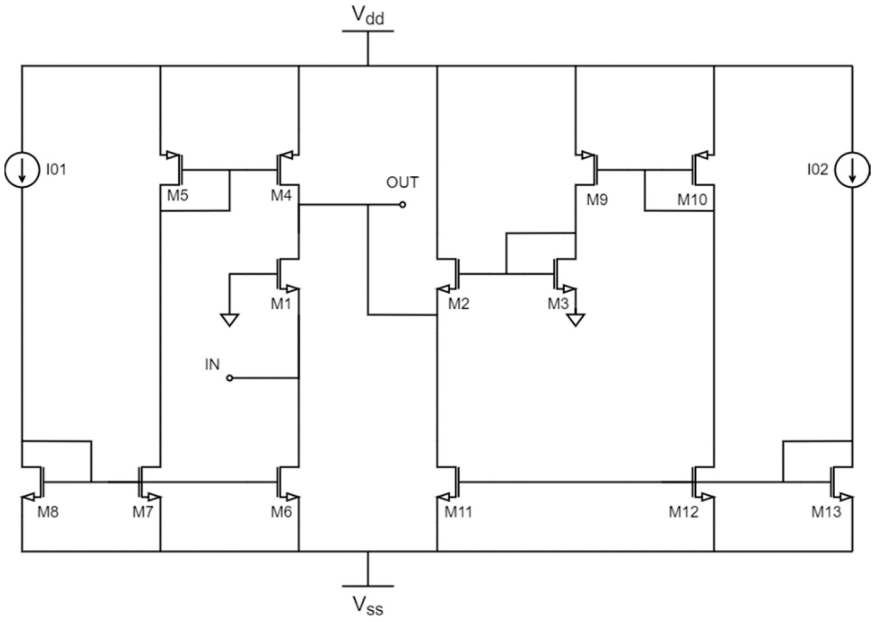


Figure 2. CMOS LNA based on current conveyors with current mirrors as current sources.

3. Noise-Canceling Technique Applied to a CG Stage

Equation (3) shows that the input common-gate transistor (M1) is the main noise contributor. Various architectures can be found in the literature to cancel the noise of this topology [10–12]. The simplified diagram of a common-gate stage with noise cancelation is depicted in Figure 3. With this technique, the noise of the input transistor passes through two different paths (transistors MX and MY), and is canceled at the output, while the input signal is boosted. This can be seen better in the inset of Figure 4, where the noise and the signals are plotted on the schematic. Transistor M1 is the main noise contributor, and a noise source (i_{noise}) represents its contribution in the circuit. This source generates a voltage at the source of M1 and a fully correlated voltage at the drain with the same magnitude and opposite sign. The noise reaches the output through two different paths, and thanks to the CS inverting stages composed by transistors MX and MY, it is canceled at the output. In contrast, the input signal is amplified through the same paths thanks to the CS-CG inverting amplifier (transistors M1 and MY) and the CS inverting amplifier (MX) and is amplified at the output instead of being canceled.

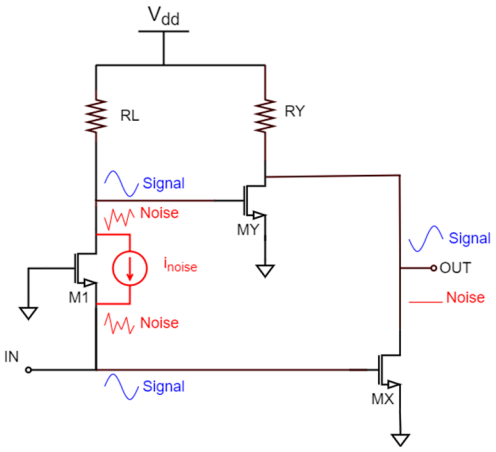


Figure 3. Common-gate amplifier with noise canceling.

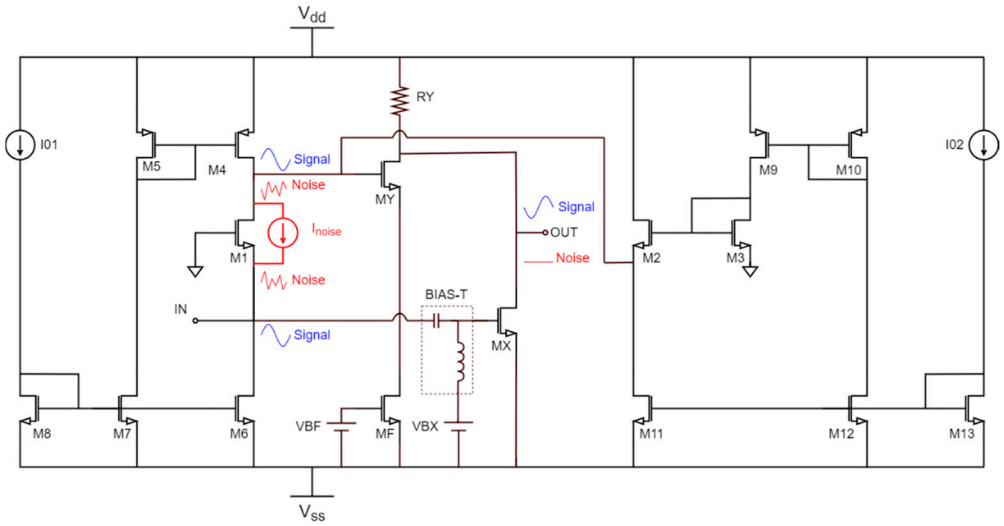


Figure 4. Proposed LNA based on current conveyors with noise canceling.

To achieve perfect noise cancelation, the two noise paths should have the same gain. Therefore, transistors MX and MY must be independently biased. It is important to note that transistors MX and MY also introduce noise into the circuit, so they must be carefully designed. Thus, the key to achieve a low overall NF has now shifted to a low noise implementation in the noise-canceling stage.

4. LNA Based on CC with Noise Canceling

To better understand the improvements introduced by the noise-canceling technique, two different implementations were developed with the same sizing and bias currents. On the one hand, a current conveyor-based LNA is implemented following the schematic depicted in Figure 2. On the other hand, a second implementation of the LNA applying the noise cancelation technique is developed following the schematic shown in Figure 4.

The circuits are developed using UMC 65-nm CMOS technology with a $\pm$1.2 V DC supply voltage. A summary of the device sizing information is given in Table 1, where the length of all the MOSFETs is fixed to the minimum allowed value of 65 nm. Note that the bias currents I_{01} and I_{02} are selected as 1 mA and 200 µA, respectively, and the DC voltages V_{BF} and V_{BX} are 0.35 V each. In addition, the resistor R_Y is selected as 220 ohms. The schematic of the proposed noise-canceling LNA based on CC is presented in Figure 4. This circuit combines the CC-based approach shown in Figure 2 with the noise-canceling technique presented in Section 3. As explained above, the input transistor generates a noise contribution of equal magnitude but opposite phase at its drain and source terminals.

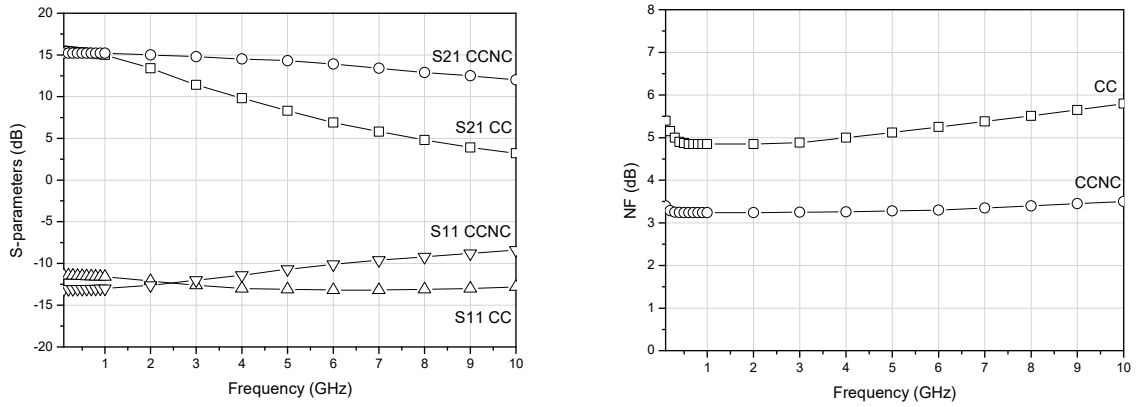
These two noise signals pass through two inverting paths and are canceled at the output. On the contrary, the input signal has the same sign on the drain and source terminals of the input transistor, so it passes through the two inverting paths, and it is added at the output. In the design of this circuit, the size of the input stage should be determined to obtain a good broadband input impedance match. The noise-canceling stage must be designed to achieve broadband noise cancelation while introducing as little noise as possible and degrading gain, bandwidth, power consumption, and input matching as little as possible. Using a CC-based LNA as the input stage instead of a simple CG stage gives a degree of freedom in satisfying the input-matching conditions.

Table 1. Device sizes summary of the implemented LNAs.

M1	**M2**	**M3**	**M4**	**M5**	**M6**	**M7**	**M8**
20 × 5 µm	5 × 5 µm	2 × 0.5 µm	2 × 0.5 µm	2 × 0.5 µm	2 × 0.5 µm	2 × 0.5 µm	2 × 0.5µm
M9	**M10**	**M11**	**M12**	**M13**	**MX**	**MY**	**MF**
2 × 0.5 µm	2 × 0.5 µm	2 × 0.5 µm	2 × 0.5 µm	2 × 0.5 µm	30 × 4 µm	2 × 0.5 µm	2 × 0.5 µm

5. Simulation Results and Analysis

The simulated performance comparison of the LNA based on CC (CC) and the proposed LNA based on CC with noise cancelation (CCNC) is shown in Figure 5. The proposed technique reduces the noise figure from 4.85 dB to 3.25 dB at 1 GHz. At frequencies below 6 GHz, both circuits present a reasonable input matching, with an input return loss (S11) < −10 dB. However, at higher frequencies the input matching deteriorates slightly. This can be solved by simply increasing the bias current I_{02}, but at the expense of increasing the power consumption.



(**a**) (**b**)

Figure 5. Simulation results of (**a**) the S–parameters and (**b**) the NF of the LNA based on current conveyors (CC) and the proposed LNA based on current conveyors with noise cancelation (CCNC).

The layout of the proposed LNA is shown in Figure 6. To reduce the circuit area, the BIAS-T inductor needed to bias the MX transistor is replaced by a large resistor, which is implemented in practice by the large leakage resistance of a reverse-biased p-n junction of a diode-connected MOS transistor operating in the cutoff region (2 × 0.5 µm). Note that the exact value of this resistance or its temperature and voltage dependence are not relevant, provided that it remains large enough not to influence the circuit operation at the lowest frequency required. As no inductor is present, the LNA core occupies an area of only 160 × 80 μm^2, which is among the smallest designs available in the literature.

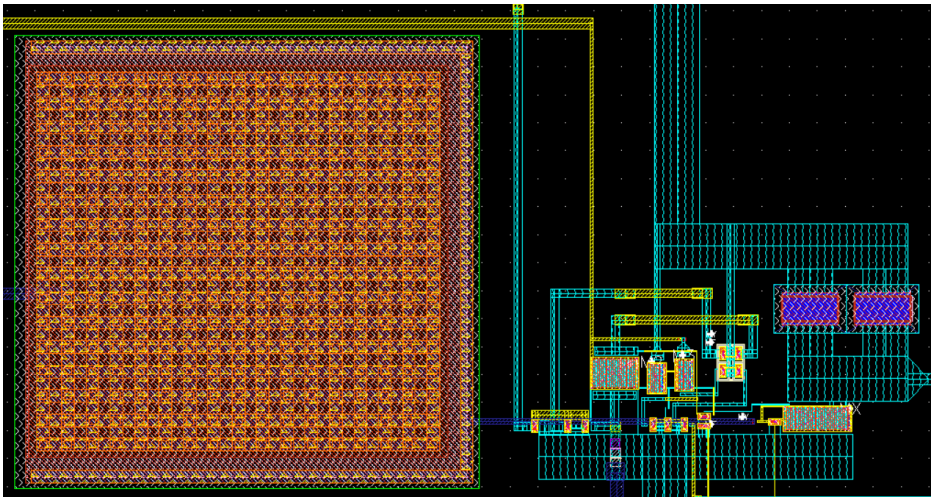


Figure 6. Physical chip layout of the proposed LNA based on current conveyors with noise cancelation (occupied area: 160 × 80 μm^2).

Linearity is a very important feature of an LNA since a higher 1-dB compression point means a larger capability of receiving weak signals in the presence of strong ones. This technique presents the advantage of significantly boosting the circuit's linearity, since the same mechanism leading to noise cancelation can also cancel partially the nonlinear distortions [13]. The simulation results shown in Figure 7 demonstrate an input 1-dB compression point of –2 dBm. Finally, the power dissipation of the circuit is 18.57 mW, with a DC supply of ±1.2 V.

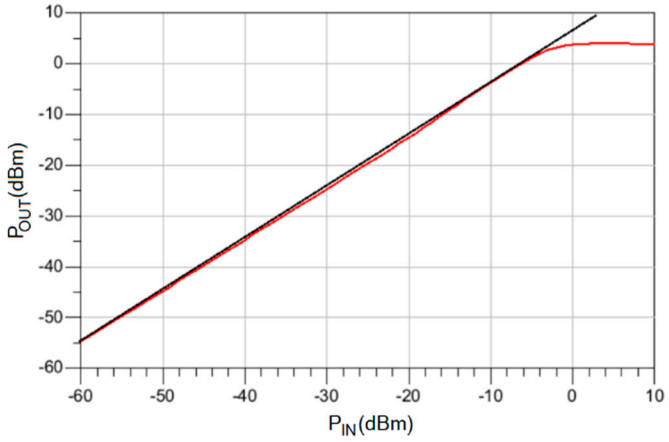


Figure 7. Simulated output power (red line) as a function of the input power to calculate the 1-dB compression point. The black line represents the ideal response without distortion.

The performance of the proposed LNA is compared in Table 2 with recently reported LNAs available in the literature. To fairly compare the proposed CCNC LNA with the other designs, we have defined the following figure of merit (*FoM*), which considers a positive contribution of amplifier gain, bandwidth, and *IIP3*, and a negative contribution of power consumption, noise factor, and active area:

$$FoM = \frac{Gain(\text{abs}) \times BW(\text{GHz}) \times IIP3(\text{mW})}{P_{DC}(\text{mW}) \times (F-1) \times area(\text{mm}^2)}. \quad (6)$$

Table 2. Performance summary of the proposed LNA and similar works available in the literature.

Parameter	Soleymani [14]	Iji [15]	Baumgratz [16]	Wang [17]	Liu [18]	Baumgratz [19]	Hsieh [20]	Farzaneh [21]	Farzaneh [21]	This Work CCNC	This Work CC
Year	2020	2012	2017	2017	2016	2019	2020	2020	2021	2022	2022
Tech. (nm)	180	250	130	180	65	130	180	180	90	65	65
S_{11} (dB)	<−21	<−10	<−10	N/A	N/A	<−10	<−10	<−10	<−10	<−10	<−10
BW (GHz)	1.1	1.1	2.9	0.3875	2	3.1	0.1	3.8	4.7	6.2	6
Gain (dB)	20.2	13.8	10	15	24	20	10	22	21	15.3	15.3
*IIP*3 (dBm)	−9.5	−12	−10	32 *	11.6	−11.1	0	−4	−4	7.6	7.6
Power (mW)	8	1.8	15.6	43	3.48	19	0.6	13	8.8	18.6	18.6
NFmin HG (dB)	1.68	2.3	4.9	15	24	3.4	4	3.25	3.2	3.2	4.8
Area (mm^2)	0.0158	1	0.15	0.1	0.01	0.15	0.9	0.0258	0.014	0.0128	0.0128
FoM	21.16	0.27	0.19	26.23	52.62	0.71	0.39	51.00	156.44	797.27	415.99
Sim./Meas.	Sim.	Sim.	Meas.	Sim.	Meas.	Meas.	Meas.	Sim.	Sim.	Sim.	Sim.

N/A, Not Available; * OIP3.

The proposed CCNC LNA presents the highest *FoM* value among the reported designs. This is because the proposed technique achieves a high bandwidth and *IIP*3 values using a very small area, while the gain and NF are within the average. The price to pay is a slightly higher power consumption than most of the other designs in the comparison.

6. Conclusions

A wide-band CMOS noise-canceling current conveyor-based LNA is proposed in this paper and is implemented in a standard 65-nm CMOS process. The design exploits a noise-canceling technique consisting of an amplifying stage based on a CC that provides input impedance matching, and a noise-canceling stage composed of two transistors in CS configuration that subtracts the input transistor noise contribution while adding the signal contributions. The simulation results show that the proposed CCNC LNA achieves wide-band input impedance matching (0–6.2 GHz), with high gain (15.3 dB) and low noise (4.8 dB), in a very small area (160×80 μm^2). The circuit presents a power dissipation of 18.57 mW from a DC supply of $\pm$1.2 V. In addition, the proposed noise-canceling technique also improves the linearity because it is capable of partially canceling nonlinear distortions. The proposed circuit achieves a remarkable *IIP*3 of 7.6 dB and an input P_{1dB} of –2 dBm. The price to pay with this approach is the additional power dissipation introduced by the auxiliary amplifier in the noise-canceling path. As shown in the comparison with similar works, the proposed circuit presents the highest *FoM* value among the reported designs.

Author Contributions: Investigation, H.G.-V.; supervision, S.L.K. and J.d.P.; writing—original draft, D.G.-S. and J.d.P. All authors have read and agreed to the published version of the manuscript.

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2.4. A 2-V 1.4-dB NF GaAs MMIC LNA for K-Band Applications

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A 2-V 1.4-dB NF GaAs MMIC LNA for K-Band Applications

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Abstract: A 1.4-dB Noise Figure (NF) four-stage K-band Monolithic Microwave Integrated Circuit (MMIC) Low-Noise Amplifier (LNA) in UMS 100 nm GaAs pHEMT technology is presented. The proposed circuit is designed to cover the 5G New Release n258 frequency band (24.25–27.58 GHz). Momentum EM post-layout simulations reveal the circuit achieves a minimum NF of 1.3 dB, a maximum gain of 34 dB, $|S_{11}|$ better than –10 dB from 23 GHz to 29 GHz, a P_{1dB} of –18 dBm and an OIP3 of 24.5 dBm. The LNA draws a total current of 59.1 mA from a 2 V DC supply and results in a chip size of 3300 × 1800 μm^2 including pads. We present a design methodology focused on the selection of the active device size and DC bias conditions to obtain the lowest NF when source degeneration is applied. The design procedure ensures a minimum NF design by selecting a device which facilitates a simple input matching network implementation and obtains a reasonable input return loss thanks to the application of source degeneration. With this approach the input matching network is implemented with a shunt stub and a transmission line, therefore minimizing the contribution to the NF achieved by the first stage. Comparisons with similar works demonstrate the developed circuit is very competitive with most of the state-of-the-art solutions.

Keywords: low noise amplifier; noise figure; monolithic microwave integrated circuit; gallium arsenide; electromagnetic simulation; input return loss; K-band; 5G

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1. Introduction

Although SOI technologies achieve remarkable results and are closing the gap with existing III-V processes [1], the latter still show a superior performance and are attracting the attention of many integrated circuit designers. Moreover, monolithic microwave integrated circuit (MMIC) processes provide an efficient solution for implementing discrete components and full radio interfaces in a single chip [2]. In this sense, gallium nitride (GaN)-based circuits provide many advantages, mainly in terms of power management, efficiency, and breakdown voltage [3]. In contrast, gallium arsenide (GaAs) technologies are the preferred option when a lower noise figure (NF) is pursued at greater frequencies [4,5]. Therefore, GaAs technologies are most appropriate in high-frequency scenarios requiring a very low NF, such as mmWave applications, SATCOMs or 5G networks. These technologies are utilized in high-resolution radar, including short range military aircraft radios and astronomical observations, all of them operating in the K-band. Particularly, the 26 GHz frequency band is of great interest since it has been identified as a pioneer band for the European Union's 5G new radio (NR) networks [6]. There are two mm-Wave bands, designated as n258 and n257 in 3GPP NR, ranging from 24.25 to 27.5 GHz and 27.5 to 29.5 GHz, respectively. They enable very high data rates and data capacity, making them suitable for hotspot coverage. Similarly, the US identified the 27.5–28.35 GHz band for the same purpose, whereas the 27.5–29.5 GHz and 26.5–29.5 GHz frequency bands are considered for Japan and Korea, respectively [6].

To implement a very low noise receiver, special attention must be paid to the design of the low-noise amplifier (LNA) since its noise contribution is critical to the NF of the system.

Thus, the LNA performance affects the overall receiver sensitivity and linearity [2,7,8]. Not many works are available in the literature that report LNA implementations achieving a NF below 1.5 dB with a gain above 30 dB and low Input Return Loss (IRL or $|S_{11}|$) [4,5,9–13].

In this article, a 2-V 1.4-dB NF four-stage GaAs MMIC LNA from 24.25 to 27.5 GHz is presented. We introduce a design methodology focused on the selection of the active device geometry and DC bias conditions to obtain the lowest NF possible in a common-source (CS) amplifier with source degeneration. The LNA operates in the K-band (from 23 to 29 GHz), achieving a maximum gain of 34 dB at 24.5 GHz, a minimum NF of 1.3 dB at 26.5 GHz, an $|S_{11}|$ better than 10 dB, a P_{1dB} of –18 dBm and an OIP3 of 24.5 dBm. In Section 2, a detailed description of the proposed circuit is presented, and particular aspects regarding the design implementation with the selected Process Design Kit (PDK) are provided in Section 3. Electromagnetic (EM) post-layout simulation results of the four-stage GaAs LNA are shown in Section 4, and a comparison is made with the most relevant proposals available in the literature. Conclusions are drawn in Section 5.

2. Circuit Design

According to the Friis formula [2,7], the overall noise figure (NF_{tot}) of a cascaded system with n stages is given as (1), where NF_n and G_n represent the NF and gain of the n-th stage, respectively. As seen, the first element contributes the most to NF_{tot}, and the NF of the upcoming stages is attenuated by the gain of the first stage (G_1) and all the preceding stages. Hence, the implementation of the LNA must be thoroughly carried out since its performance is critical for the receiver [2,7].

$$NF_{tot} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{G_1} + \ldots + \frac{NF_n - 1}{G_1 \cdots G_{n-1}} \quad (1)$$

The LNA is composed of four cascaded CS stages with source degeneration to achieve a minimum NF design. The Friis formula can be applied to the whole system but it can be applied locally too, as shown in (2).

$$NF_{LNA} = 1 + (NF_{s1} - 1) + \frac{NF_{s2} - 1}{G_{s1}} + \frac{NF_{s3} - 1}{G_{s1} \cdot G_{s2}} + \frac{NF_{s4} - 1}{G_{s1} \cdot G_{s2} \cdot G_{s3}} \quad (2)$$

If the LNA is divided into four CS amplifiers, the first stage (characterized by NF_{s1}, G_{s1}) is again the main contributor to the overall LNA NF (NF_{LNA}). Applying (2), one can calculate the requirements of each stage to achieve a certain value of NF_{LNA}. We assume the designer is interested in NF_{LNA} = 1.4 dB and G_{tot} = 33 dB. If the first stage presents NF_{s1} = 1 dB and G_{s1} = 6.5 dB (which is constrained by the selected process and the active device selection), assuming $NF_{s2} = NF_{s3} = NF_{s4} = NF_{s234}$ and $G_{s2} = G_{s3} = G_{s4} = G_{s234}$ for simplicity, then to achieve the desired performance, the NF_{s234} and G_{s234} should be:

$$\begin{cases} NF_{s234} < 1.7\ (\text{dB}) \\ G_{s234} \geq 9\ (\text{dB}) \end{cases}, \quad (3)$$

In this sense, the first stage should introduce the lowest NF possible and a high gain in order to allow a more flexible design of the upcoming stages. Additionally, to achieve NF_{s1} = 1 dB and G_{s1} = 6.5 dB, the implementation of the input matching network with a single inductor is desired to minimize the number of elements in the signal path and to minimize the noise contribution of the input matching network. Otherwise, obtaining an LNA with an NF under 1.4 dB is not possible without lowering the NF of stages 2, 3 and 4. However, as explained in the following section, lowering NF_{s234} is only possible at the expense of a gain reduction, which means an additional stage may be needed to reach G_{tot} = 33 dB.

The performance of the active device used in the CS amplifier is mainly defined by three parameters: the minimum NF it provides (NF_{min}), the maximum stable gain (G_{max}) and Rollet's stability factor (k). The value of these three parameters depends on

several factors, namely, the device geometry, physical parameters of the selected process, impedance matching or DC bias conditions, among others. The value of NF_{min} is given as (4), where g_m is the device transconductance (obtained from the device's DC operating point), R_G and R_S are the gate and source resistances, f is the frequency of operation and f_T is the transit frequency [1]. Similarly, G_{max} is defined as (5), and Rollet's stability factor k is given by (6).

$$NF_{min} = 1 + K\sqrt{g_m \cdot (R_G + R_S)} \cdot \frac{f}{f_t} \tag{4}$$

$$G_{max} = \left|\frac{S_{21}}{S_{12}}\right| \cdot \left(k - \sqrt{k^2 - 1}\right) \tag{5}$$

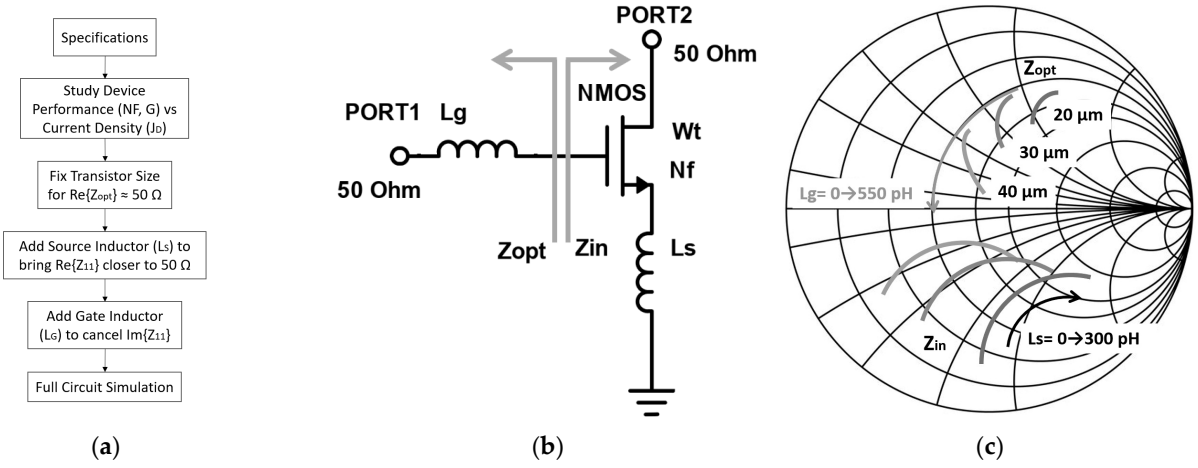
$$k = \frac{1 - |S_{11}|^2 - |S_{22}|^2 + |S_{11}S_{22} - S_{12}S_{21}|^2}{2|S_{21}S_{12}|} > 1 \tag{6}$$

Impedance matching selection plays a critical role in the design of each stage of the LNA. To obtain an amplifier that yields the maximum gain, one must match the input of the LNA to $(S_{11})^*$, whereas to obtain a minimum NF design, one must match the input to the conjugate of the optimum source impedance $(S_{opt})^*$. Nevertheless, these two values (S_{11} and S_{opt}) are generally different, so that simultaneously matching the circuit for NF_{min} and G_{max} is not possible. Therefore, source degeneration is often applied to the CS amplifier to bring these two impedances close together. To be able to use a single inductance to implement the input matching network, the selected source impedance should present a real part close to 50 Ω so that a single gate inductor is enough to cancel the capacitive component [1]. The main problem is that most designs use fixed transistor sizes, so their S_{opt} may not present a real part close to 50 Ω, resulting in a non-minimum NF design. To address this issue, multiple iterations of the design process are performed to find a combination of device size and input matching network that meets the appropriate NF specifications.

Design Approach

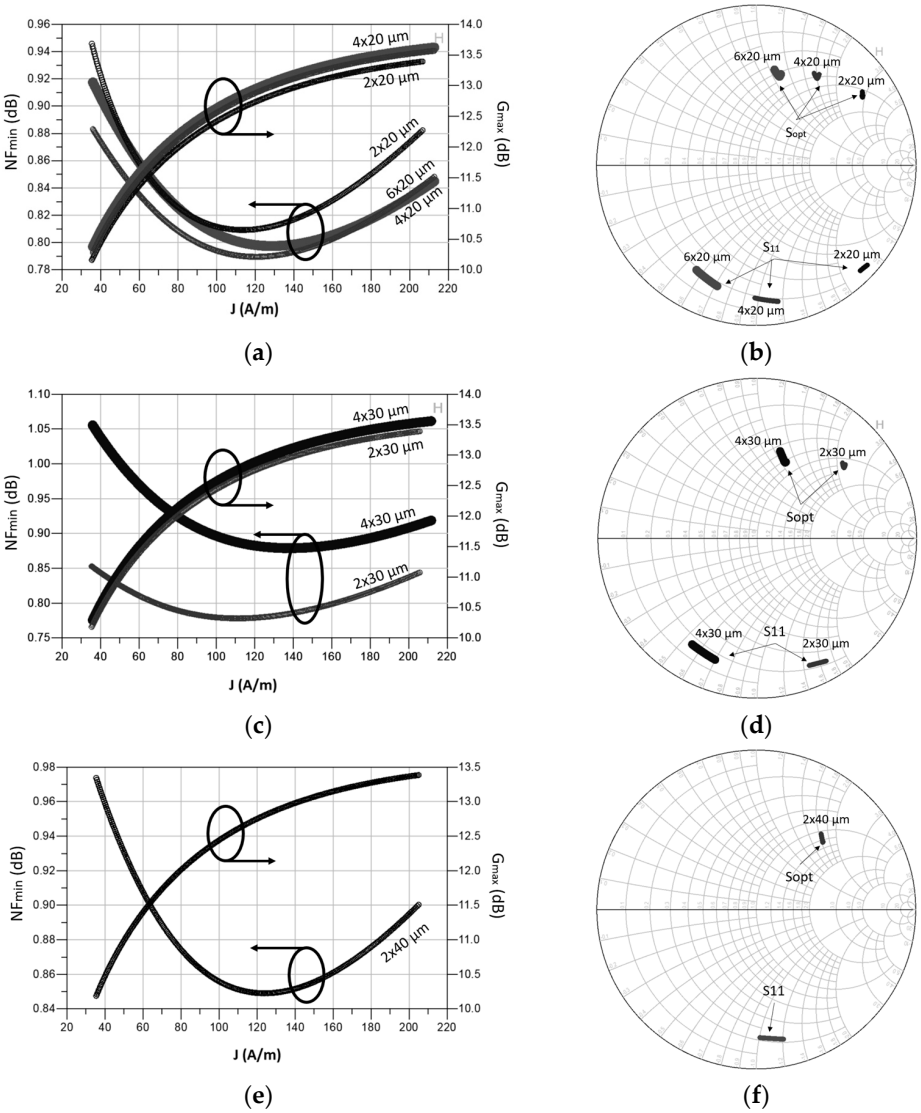
In this paper, we present a design methodology focused on how to choose the active device geometry and DC bias conditions to obtain the lowest NF possible when source degeneration is applied. A simplified overview of the design procedure is given in Figure 1a. First, to select the device size, the CS amplifier with the source degeneration depicted in Figure 1b is employed. Note that all the ports are matched to 50 Ω and the DC biasing circuitry is not shown for simplicity. The device geometry is defined by the total width (W_t), which is the product of the unitary finger width (W_u) and the number of fingers (N_f). Z_{opt} is the impedance seen looking away from the gate and Z_{in} is the impedance seen looking into the gate of the active device. The effect of increasing W_t, the value of the source inductor (L_s) and the gate inductor (L_g) are shown in Figure 1c.

In Figure 1b, the source degeneration inductance L_s is swept from 0 to 300 pH. Source degeneration helps reduce the NF at the expense of a gain reduction, improving the amplifier's stability. A value of approximately 150 pH for L_s is enough to bring the S_{11} and S_{opt} closer to the unity circle, i.e., to achieve a real part of about 50 Ω. A gate inductor is then used to bring both S_{11} and S_{opt} to the center of the Smith chart, obtaining a maximum gain and minimum NF amplifier. To select the size and biasing of the LNA first stage device, its performance (NF_{min} and G_{max}) against its current density (J) is studied, keeping close attention to the S_{11} and S_{opt}, as shown in Figure 2, for different device sizes. In these figures, only device geometries that provide S_{11} and S_{opt} close to 50 Ω are included.



(**a**) (**b**) (**c**)

Figure 1. Simplified overview of the design procedure (**a**), schematic diagram used for device selection (**b**) and Smith Chart representation of the influence of varying the transistor width (W_t), the source inductor (L_s) and the gate inductor (L_g) on the input impedance (Z_{in}) and the optimum source impedance (Z_{opt}) (**c**).



(**a**) (**b**) (**c**) (**d**) (**e**) (**f**)

Figure 2. Current density and S_{11}, S_{opt} of the first stage transistor for a finger width of 20 µm (**a**,**b**), 30 µm (**c**,**d**) and 40 µm (**e**,**f**).

A finger width of 20 µm is explored in Figure 2a,b. In Figure 2a, the NF_{min} and G_{max} are plotted as a function of the current density. As seen, a device of 4 fingers and 20 µm biased with a current density of 0.12 mA/µm results in a G_{max} of 12.7 dB and 0.79 dB of NF_{min}, which is the lowest NF_{min} possible. As shown in Figure 2b, a device of 2 fingers × 20 µm would require a very high value of L_g to be matched. It presents a real part higher than 50 Ω and would be increased further after applying source degeneration, so this choice is discarded. However, 6 and 4 finger devices present a real part lower than 50 Ω and would be suitable for the first stage design. In fact, both options could be matched to the input with a single gate inductor with a very similar value. Nevertheless, since the 4 × 20 µm transistor presents a S_{opt} closer to the unitary circle, a lower value of L_s can be employed. This situation is highly desirable since a very high L_s decreases the NF, but it also decreases the gain significantly. In Figure 2c,d, a finger width of 30 µm is explored. Note that a 2 × 30 µm transistor results in an even lower NF_{min} than the 4 × 20 µm device. Still, this device presents a real part higher than 50 Ω, so it is discarded for the same reason as the 2 × 20 µm transistor. The 4 × 30 µm transistor would be a better option, but its NF_{min} is higher than the 4 × 20 µm device. Finally, a 2 × 40 µm transistor is studied in Figure 2e,f. Further geometries are discarded directly since their Re{S_{opt}} are significantly lower than 50 Ω, making them unsuitable for the design. In addition, a higher total width yields a higher power consumption for the same current density.

From this analysis the designer can determine the optimal device and current density for minimum NF, maximum gain, or a reasonable trade-off between NF, gain and power consumption. Note that, as previously discussed, a 4 × 20 µm transistor with a current density of 0.12 mA/µm (120 A/m) is required for minimum NF, which results in a G_{max} of about 12.8 dB and NF_{min} of ~0.8 dB. However, after applying source degeneration, the value of G_{max} is greatly reduced. A drain current (I_D) of 4 (fingers) × 20 (µm) × 0.12 (mA/µm) = 9.6 (mA) is needed to bias the active device. In this step, it is critical to fix a device size and current density which facilitate the input matching considering the discussion of Figure 1b [1]. Once the components of the first stage are selected, the same procedure is followed to determine the device size and biasing of the upcoming stages to define their optimum source and load impedances to meet (3). When they are known, the interstage matching network can be designed. The last step is the design of the DC bias lines to feed the devices of each stage. In our circuit, quarter-wavelength lines with bypass capacitors were used to bias the gate and drain of each transistor. The transmission lines (TLs) used in the bias paths show high impedance in the LNA's operating frequency band, and therefore, they do not contribute to impedance matching significantly.

3. Proposed Circuit

The amplifier is implemented using the models of the 100-nm UMS PH10 GaAs pHEMT process, characterized by a 130-GHz transit frequency (f_T) and 1-dB NF @ 30 GHz. The schematic implementation of the proposed circuit is depicted in Figure 3, and the corresponding layout is shown in Figure 4.

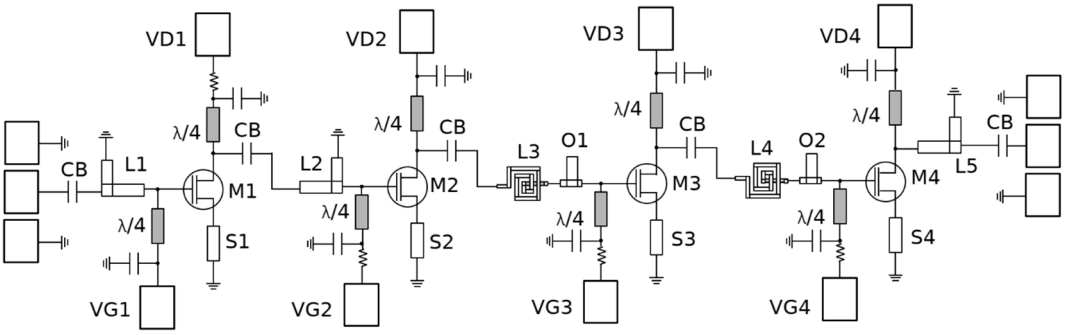


Figure 3. Proposed four-stage GaAs LNA detailed schematic.

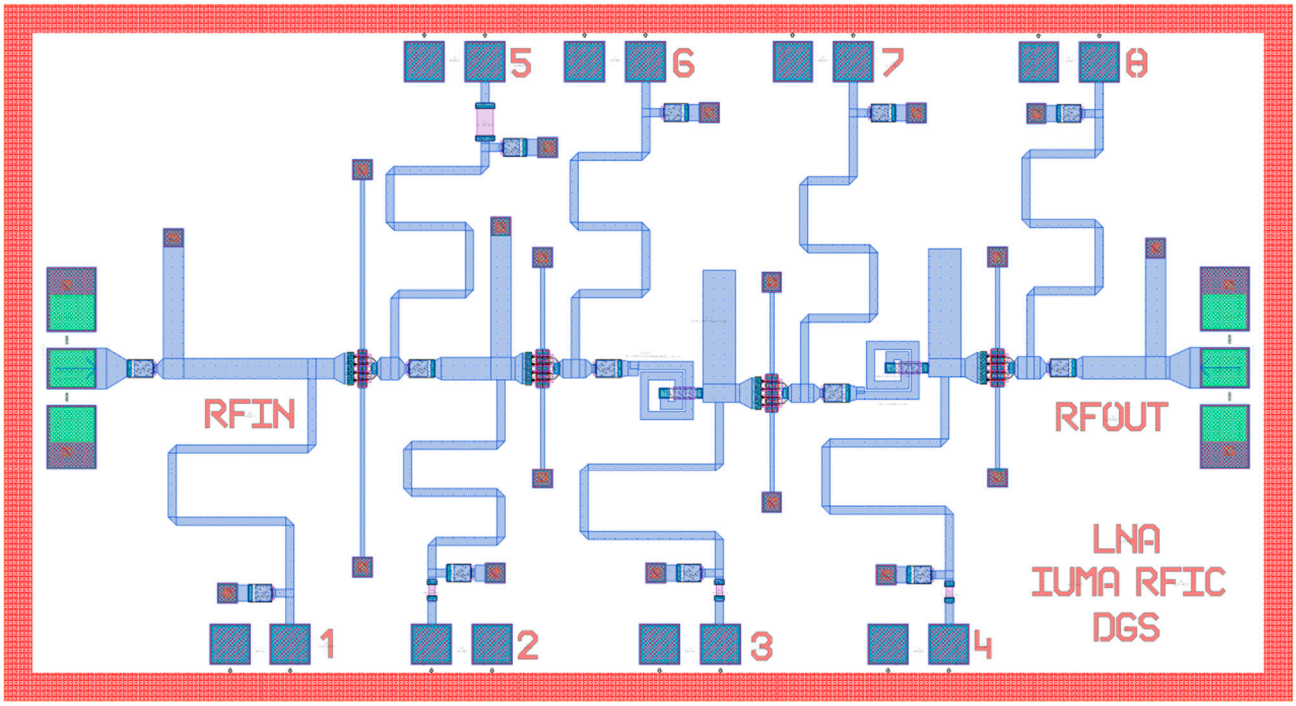


Figure 4. Layout of the Low-Noise Amplifier. Pads 1, 2, 3 and 4 represent the terminals VG1, VG2, VG3, and VG4, respectively. Also, pads 5, 6, 7 and 8 represent the terminals VD1, VD2, VD3, and VD4, respectively.

Ground-signal-ground (GSG) pads with 150-µm pitch are used for the input and output RF signals. The gate voltages of each stage are provided through DC pads VG1, VG2, VG3, and VG4. Similarly, DC pads VD1, VD2, VD3 and VD4 are used to bias the drain voltage of each stage with 2 V. Instead of relying on inductors to bias the active devices as RF chokes, we use quarter-wavelength ($\lambda/4$) TLs with a length of 1 mm and a shunt capacitor of 0.53 pF. These bias lines are oversized to comply with the maximum ratings defined by the process design kit (PDK) to avoid electro-migration and aging issues. The main advantage of using $\lambda/4$ TLs is that, if designed correctly, they barely affect the matching networks and result in an almost negligible impact on the LNA's overall NF and gain. Additionally, in order to provide DC isolation, a 0.58-pF DC block capacitor (CB) is used in the interstage matching networks as an additional component.

Since a very low NF is pursued, the designer must carefully choose the bias currents and inductances for each stage. Therefore, the first stage employs a device of four fingers with 5 µm each, resulting in a total width of 20 µm, and is biased with a current density of 0.47 mA/µm for minimum NF and low-power operation. Since the first stage achieves a very low NF (about 1 dB @ 26 GHz) but a limited gain (about 6.5 dB for the same frequency), the next stages are biased with a higher current density of 0.53 mA/µm to obtain a 9-dB gain-per-stage at the expense of a slightly higher NF. The device geometry selected for stages 2, 3 and 4 is 4 × 7.5 µm. Note that a V_G and a V_D of 0 V and 2 V are used to bias to all the transistors, respectively. Source degeneration is applied to all the CS stages since it prevents instability, reduces the NF, brings the S_{11} and S_{opt} closer together and increases the circuit resilience to process, voltage, and temperature (PVT) variations. The source transmission line (S1 in Figure 3) adds a small inductance which brings the S_{11} of the input transistor closer to $S_{opt,}$ as discussed in Figure 2b. The size of S1 is 420 × 10 µm^2, which is enough to ensure stability and a low NF for the first stage. The transmission lines S2, S3 and S4 are sized 200 × 10 µm^2, providing a lower inductance for a higher gain than the first stage. The selected source impedance for the first stage is equivalent to the device's S_{opt} and is given by (7). As seen, thanks to careful device sizing plus source degeneration, the real part of Z_{s1} is very close to 50 Ω. From the selected source impedance, one can obtain the

source reflection coefficient (Γ_S) and then the corresponding load reflection coefficient (Γ_L) by applying expression (8). After translating Γ_L into the load impedance Z_{L1}, Equation (9) is obtained. Following this methodology, the source and load impedances for stages 2, 3 and 4 are obtained as (10) and (11), respectively. Since the interstage matching does not require any intermediate 50 Ω termination, the stages are directly matched to each other.

$$Z_{S1} = (Z_{in})^* = 50 \cdot (1.043 + j \cdot 1.399)\ (\Omega) \tag{7}$$

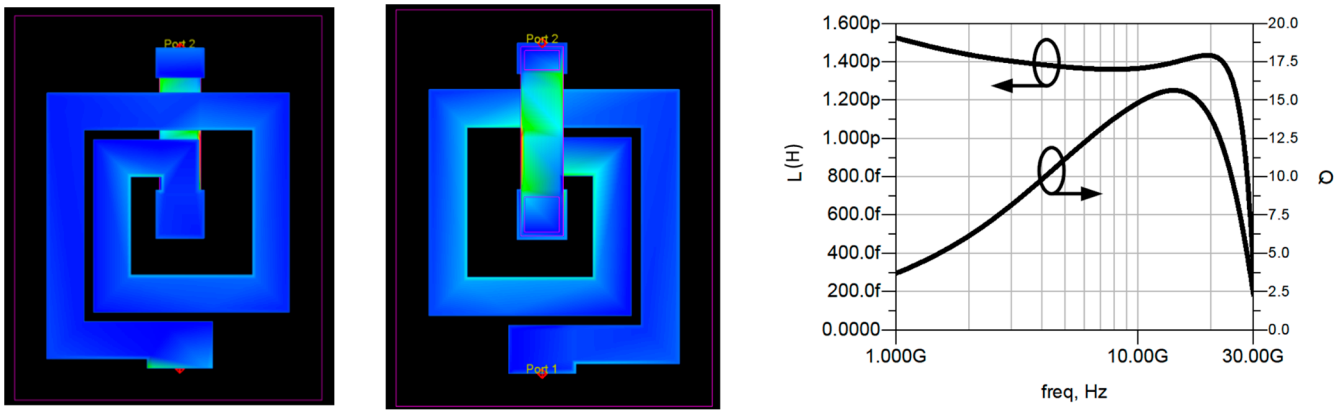
$$\Gamma_L = \left(S_{22} + \frac{S_{12} S_{21} \Gamma_S}{1 - S_{11} \Gamma_S} \right)^* \tag{8}$$

$$Z_{L1} = (Z_{out})^* = 50 \cdot (1.366 + j \cdot 1.261)\ (\Omega) \tag{9}$$

$$Z_{S2,3,4} = 50 \cdot (0.329 + j \cdot 0.709)\ (\Omega) \tag{10}$$

$$Z_{L2,3,4} = 50 \cdot (0.537 + j \cdot 0.955)\ (\Omega) \tag{11}$$

The input matching network can be implemented by a very low-inductance, high-Q inductor since it is critical that it presents a very high Q to avoid a significant degradation of the NF [14,15]. However, in practice, the inductance required is so small that it can be easily implemented with a series TL and a shunt stub. The same applies to the inductor between stages 1 and 2, which has been replaced with a series TL and a shunt stub. The matching networks between stages 2 and 3 and 3 and 4 were implemented using two inductors (520 pH and 510 pH, Q ≈ 15) and two open stubs (O1, O2) in series. The layout of these inductors, the current density distribution and the inductance and Q values obtained from the EM simulations are shown in Figure 5. The open stubs O1 and O2 are sized 80 × 280 μm^2 and 80 × 270 μm^2, respectively, and they provide an extra capacitance required for proper matching. Finally, a series TL, a shunt stub, and a DC Block capacitor of 0.58 pF form the output matching network. The layout of the circuit is depicted in Figure 4, with a total size of 3300 × 1800 μm^2 including pads.

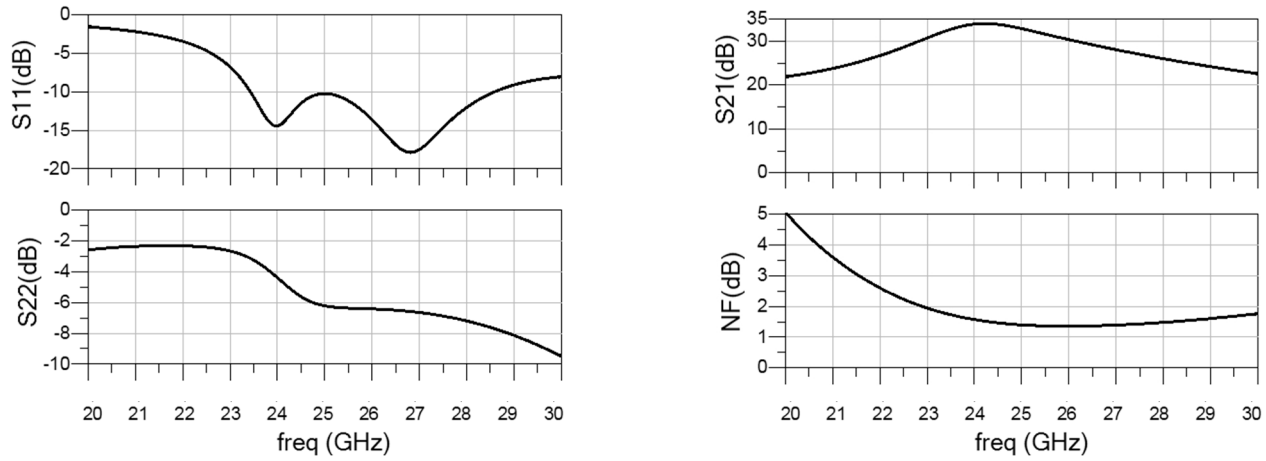


(**a**) (**b**)

Figure 5. Layout and current distribution (**a**), and inductance, and quality factor (**b**) for the inductors employed in stages 3 and 4.

4. Simulation Results

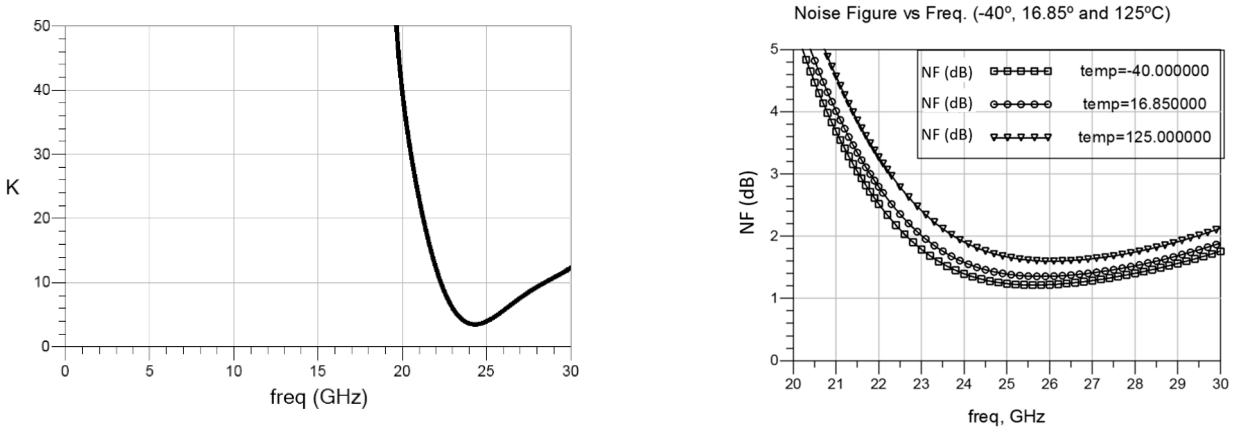
Post-layout scattering (S-parameters) and noise parameters were simulated using Keysight's Advanced Design System software and the Momentum EM simulator at room temperature. The resulting $|S_{11}|$ and $|S_{22}|$ as well as the gain and NF are depicted in Figure 6a,b. The proposed LNA presents an IRL better than 10 dB from 23.5 to 28.5 GHz and an output return loss better than 5 dB. A maximum gain of 34 dB is obtained at 24 GHz, and an NF below 1.4 dB is obtained from 24 GHz to 28 GHz with a minimum value of 1.3 dB at 26.5 GHz.



(**a**) (**b**)

Figure 6. Input and output return loss (**a**), and gain and NF (**b**) of the proposed LNA from 20 to 30 GHz.

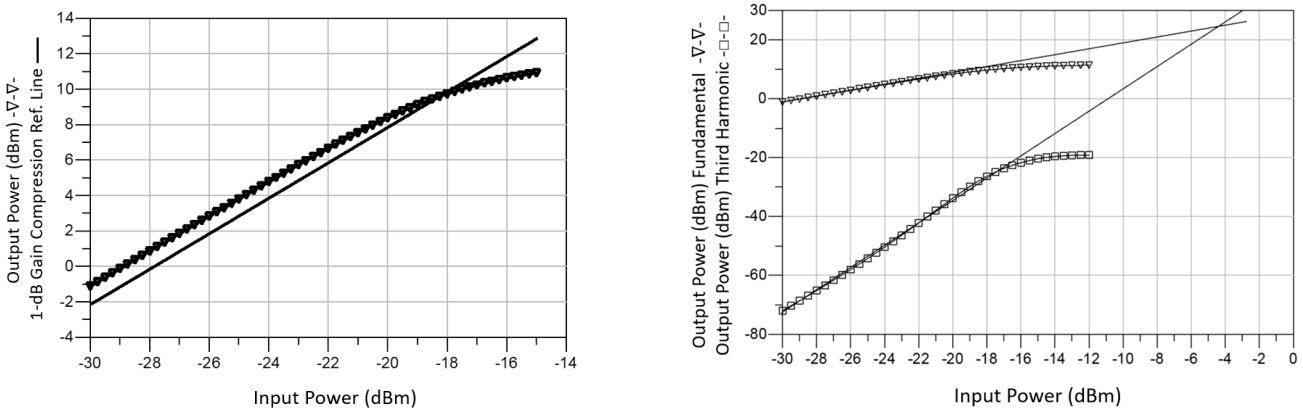
The value of the Rollet's stability factor k is shown in Figure 7a. As seen, the k-factor is above one from 0 to 30 GHz, with a minimum of 3.5 at a frequency of 24.3 GHz. Individual stability was also checked for each stage and for the whole four-stage amplifier, concluding that the LNA is unconditionally stable. The NF of the LNA was simulated for different temperature values (–40 °C, 16.85 °C and 125 °C), as shown in Figure 7b. As expected, the best results are observed at the lowest temperature, with a minimum NF as good as 1.2 dB at 25.5 GHz. On the other hand, at 125 °C the LNA presents a minimum NF of 1.6 dB at 26 GHz.



(**a**) (**b**)

Figure 7. Stability factor (**a**), and NF for –40 °C, 16.85 °C and 125 °C (**b**) of the proposed GaAs LNA.

The results of the single- and two-tone non-linear simulations for the proposed 4-stage GaAs LNA are shown in Figure 8. The gain compression of the LNA at 26 GHz is presented in Figure 8a, and the input and output third order intercept points (IIP3 and OIP3) are shown in Figure 8b, where two tones with 200 MHz spacing from a central frequency of 26 GHz were used. The GaAs LNA achieves an output power 1 dB-compression point (P_{1dB}) of −18 dBm, an IIP3 of −4.5 dBm and an OIP3 of 24.5 dBm.



(**a**) (**b**)

Figure 8. Output 1-dB compression point (P_{1dB}) (**a**), and output third order intercept (OIP3) (**b**) of the proposed GaAs LNA.

A Monte Carlo analysis with 250 samples was also carried out to verify the results vary within an acceptable range. The histograms representing the input return loss, output return loss, gain and NF of the circuit are shown in Figure 9. As seen, the input return loss is better than 10 dB for all the samples, the output return loss is better than 5 dB for most of the samples, the gain is between 32 and 33 dB, and the NF is better than 1.4 dB for most of the samples.

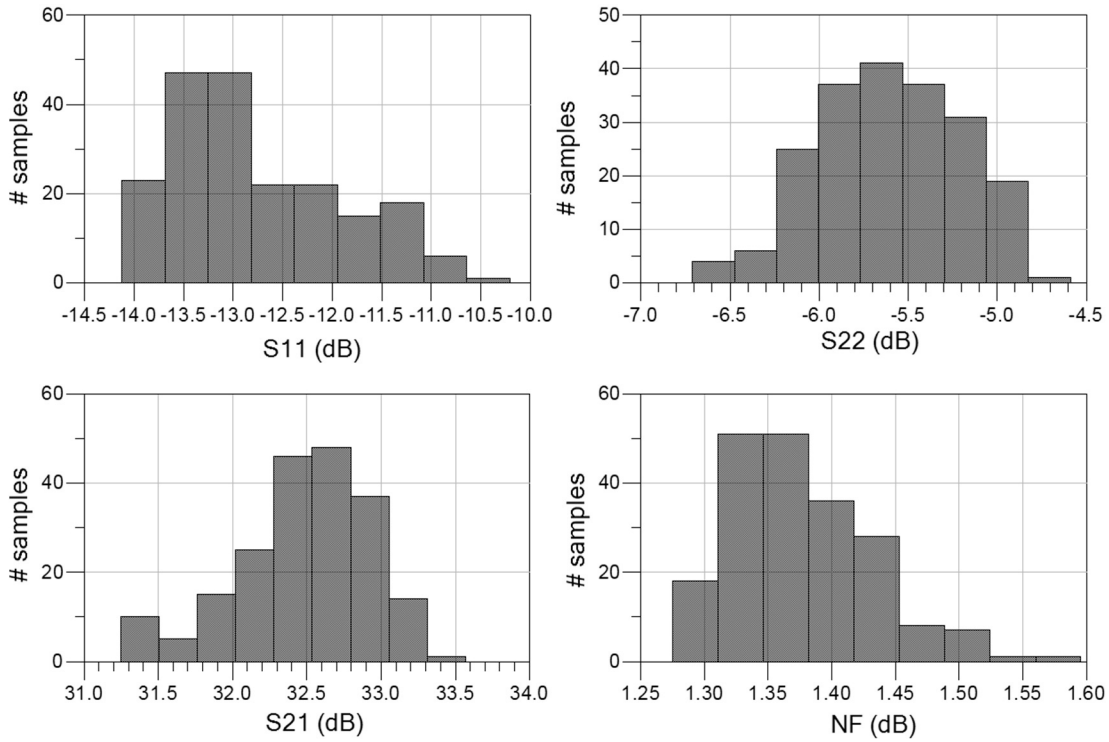


Figure 9. Monte Carlo results for 250 samples of the proposed 4-stage GaAs LNA.

To better understand how the proposed circuit performs in contrast to other works available in the literature, the small-signal figure of merit (FoM_{SS}) defined in (12) is introduced [5]. A concise comparison with similar works available in the literature along with the main results of the proposed LNA are given in Table 1. The results of the proposed circuit are superior to most of the GaAs LNAs reported in the literature and are superior to the SOI LNA proposed in [16]. As seen in Table 1, although the 4-stage LNA presents a

power consumption and area in line with most of the proposals available in the literature, it achieves one of the highest gains and lowest NFs reported, this combination results in the best FoM_{SS} compared with the other proposals.

$$FoM_{SS} = \frac{G}{NF - 1} \tag{12}$$

Table 1. Comparison of similar works available in literature.

Parameter	[17]	[18]	[16]	[19]	[4]	This Work
Data	**Simulated**	**Measured**	**Measured**	**Measured**	**Measured**	**Simulated**
Freq. range (GHz)	26–36	15–25	23–30	17.5–22.5	24–30	23–29
Gain (dB)	33	30	12.8	23.9	25	33
Noise figure (dB)	1.8	1.5	1.5	1.3	1.5	1.4
$\lvert S_{11} \rvert$ (dB)	12	10	6	12	10	10
$\lvert S_{22} \rvert$ (dB)	12	10	6	5	10	5
Power consumption (mW)	-	212	15	66	150	118.2
Publication year	2015	2017	2018	2020	2022	2023
FoM_{SS}	41.25	60	25.6	79.67	50	82.5
Process	GaAs 100 nm	GaAs 150 nm	SOI 45 nm	GaAs 90 nm	GaAs 70 nm	GaAs 100 nm
Area (mm^2)	3.64	1.87	0.3021	2.6	-	5.94

5. Conclusions

This paper presents a four-stage LNA using a 100 nm GaAs pHEMT process that covers the 5G New Release n258 frequency band (24.25–27.58 GHz). The proposed LNA achieves a maximum gain of 34 dB, a minimum NF as low as 1.3 dB, an input return loss better than −10 dB from 23 to 29 GHz, a P_{1dB} of −18 dBm, and an OIP3 of 24.5 dBm. The LNA draws a total current od 59.1 mA from a 2V DC supply, resulting in a chip size of 3300 × 1800 μm^2 including pads. Electromagnetic simulations as well as a Monte Carlo analysis results at room temperature demonstrate a final gain of 33 dB, a 1.4 dB NF, an $\lvert S_{11} \rvert$ better than 10 dB, an $\lvert S_{22} \rvert$ better than 5 dB, a P_{1dB} of −18 dBm and an OIP3 of 24.5 dBm in the band of interest. The paper also presents a design methodology focused on the selection of the active device size and DC bias conditions to obtain the lowest NF when source degeneration is applied. The design procedure ensures a minimum NF design by selecting a device that facilitates a simple input matching network implementation and obtains a reasonable input return loss thanks to the application of source degeneration. This approach minimizes the number of elements in the input matching network. Comparisons with similar works demonstrate the developed circuit is competitive with state-of-the-art solutions.

Author Contributions: Methodology, D.G.-S., S.L.K. and J.d.P.; Investigation, D.G.-S., S.L.K. and J.d.P.; Supervision, S.L.K. and J.d.P.; Writing—original draft, D.G.-S.; Writing—review and editing, S.L.K. and J.d.P.; Visualization, D.G.-S., S.L.K. and J.d.P.; Project administration, D.G.-S., S.L.K. and J.d.P.; Funding acquisition, D.G.-S., S.L.K. and J.d.P. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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2.5. A 1.2-V GaAs MMIC Ultra-Low-Noise Amplifier for K-band Applications

A 1.2-V GaAs MMIC Ultra-Low-Noise Amplifier for K-band Applications

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***A*bstract— A four-stage K-band MMIC Low-Noise Amplifier (LNA) is designed using a 70 nm GaAs mHEMT OMMIC process (D007IH). Based on Momentum EM simulation results, the four-stage LNA achieves a gain of 29.5 dB ±1 dB, a Noise Figure (NF) as low as 1 dB and an Input Return Loss better than -10 dB across the band. The LNA chip size is 2500µmx1750µm. The design work flow allows the improvement of the NF and the Input Return Loss of the LNA since the source impedance is selected to minimize the number of elements required to implement the input matching network. The input matching network of the proposed circuit consists of a single tapered octagonal inductor in series with the gate of the active device, resulting in a low impact for the NF achieved by the first stage and a remarkable improvement of the Input Return Loss of the LNA.**

Index terms: Low Noise Amplifier (LNA), Monolithic Microwave Integrated Circuit (MMIC), Noise Figure (NF), Input Return Loss, Electromagnetic Simulation, Gallium Arsenide (GaAs), K-band.

I. Introduction

III-V semiconductor compounds have attracted the attention of integrated circuit designers in the latest years. For instance, gallium nitride (GaN) devices exhibit numerous advantages in terms of power management and efficiency, and they possess the ability to withstand high input signal levels [1]. On the other hand, gallium arsenide (GaAs) technologies provide a very low noise figure (NF) at higher frequencies. Thus, GaAs devices are suitable for systems with very restrictive noise requirements and high frequency scenarios such as mmWave applications, radio satellites, TV broadcast and 5G networks. The K-band, operating from 18 to 27 GHz, is of particular interest since it is typically utilised for satellite communications and high-resolution radar, as well as short range military aircraft radios and astronomical observations. In addition, Monolithic Microwave Integrated Circuit (MMIC) processes offer a compact solution to implement discrete components as well as complete radio interfaces [2]. One of the main components of wireless transceivers is the Low-Noise Amplifier (LNA). The NF contributed by this element directly adds to that of the receiver, affecting its overall sensitivity and linearity [2], [3]. Few works have been reported demonstrating LNAs with a NF below 2 dB while achieving a high gain and reduced Input Return Loss [4]–[6]. In this work, a four-stage GaAs MMIC Low-Noise Amplifier with a NF below 1 dB and a DC Supply of 1.2 V is presented. The LNA operates in the upper end of the K-band (25.5 GHz up to 27 GHz), achieving a total gain of 29.5 dB with 1 dB ripple and an Input Return Loss as low as -12 dB at a centre frequency of 26 GHz. In Section II, the design approach for this circuit is explained, while Section III provides key details regarding the proposed design. Section IV shows the simulation results of the final LNA design and some conclusions are drawn in Section V.

II. Design Approach

The implementation of the first stage of the LNA is vital for the overall performance of the amplifier. The most common approach to design this stage is to select a source impedance that leads to the minimum NF possible. This solution requires a large number of elements to implement the input matching network, which yields a poor NF. In order to avoid this situation, the first stage of the LNA can be designed for minimum Input Return Loss and the active device can be selected so that its optimum source impedance (S_{opt}) presents a real part of approximately 50 Ω. To achieve maximum power transfer, the conjugate match must be achieved at the input. Since the real part of the S_{opt} is 50 Ω, the matching network must only cancel the imaginary part of this impedance. By following this approach, the number of elements needed in the input signal's path is minimized.

To prove the validity of the above statement, two single stage amplifiers were simulated. The first amplifier was designed for minimum NF (NF_{min}) while the second one was designed following the approach described above. Since the contribution of the first stage to the overall NF is critical, once it is successfully implemented the requirements for subsequent stages can be relaxed.

The value of V_G and V_D for both amplifiers is fixed to -0.1 V and 1.2 V, respectively. The device size selected for minimum NF is 8x28 µm, obtaining an ideal NF_{min} of 0.432 dB and a maximum gain of 6.8 dB. To approximate the real part of the S_{opt} to 50 Ω, a device size of 6x25.5µm is selected, obtaining a slightly higher NF_{min} (0.436 dB) and a maximum gain of 8.1 dB. The selected source impedance for the minimum NF amplifier is given by equation (1) and the load impedance is given by equation (2). The selected source and load impedances for the second amplifier are given by expressions (3) and (4), respectively. Note that source and load impedances are very close to each other for the latter case.

$$Z_{S1} = 38.6 + j \cdot 8.6\ (\Omega) \quad (1)$$

$$Z_{L1} = 47.75 + j \cdot 17.65\ (\Omega) \quad (2)$$

$$Z_{S2} = 49.95 + j \cdot 19.7\ (\Omega) \quad (3)$$

$$Z_{L2} = 52.2 + j \cdot 21.7\ (\Omega) \quad (4)$$

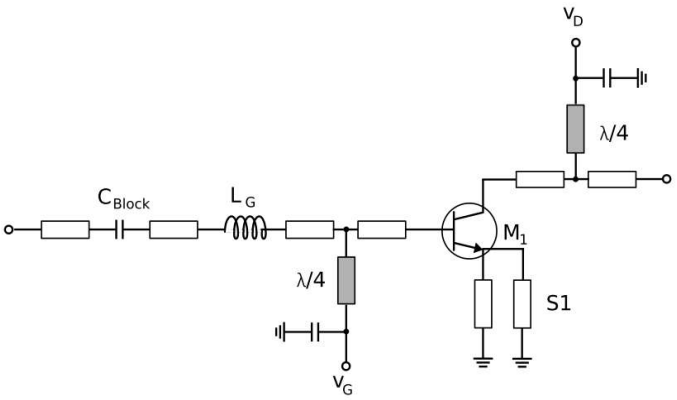


Fig. 1. Simplified schematic of the single stage Low-Noise Amplifier.

Simulations were performed using the Advanced Design System (ADS) software and OMMIC's D007IH process models. Simulation results reveal that the NF_{min} amplifier requires a shunt inductor of 0.557 nH and a series capacitor of 0.39 pF, yielding a noise figure of 0.61 dB and a gain of 6.621 dB. On the other hand, the second approach needs a single series inductor with a value of 0.184 nH, resulting in a NF of 0.554 dB and a gain of 7.98 dB. These results show that our proposal provides better results than the traditional approach. However, the noise performance of the input matching network can be further improved by minimizing the series resistance (loss) of the inductor, which results in a higher quality factor at the frequency of interest [3].

III. Proposed Design

The OMMIC D007IH GaAs process is selected for the proposed design. The technology is characterized by a 70 nm gate length, a f_T of 300 GHz and a NF of 0.5 dB @ 30 GHz. Each stage of the LNA is implemented with the topology shown in Fig. 1. Each stage is designed with 6x25.5 µm, 6x23.5 µm, 6x23.5 µm and 6x23.5 µm transistors, respectively. A V_G of -0.1 V and a V_D of 1.2 V are applied to all the transistors in order to obtain a DC drain current of 30.2 mA for M1 and 28.7 mA for M2-M4. A simplified schematic of the four-stage LNA is shown in Fig. 2 and the layout of the circuit is depicted in Fig. 3. The die size of the full amplifier is 2500µmx1750µm.

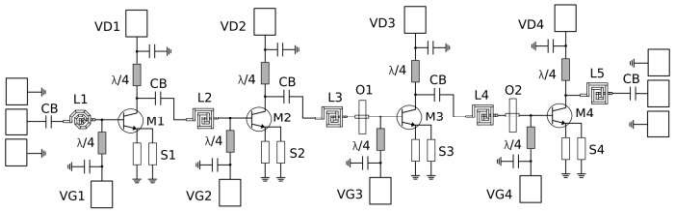


Fig. 2. Schematic of the proposed four-stage Low-Noise Amplifier.

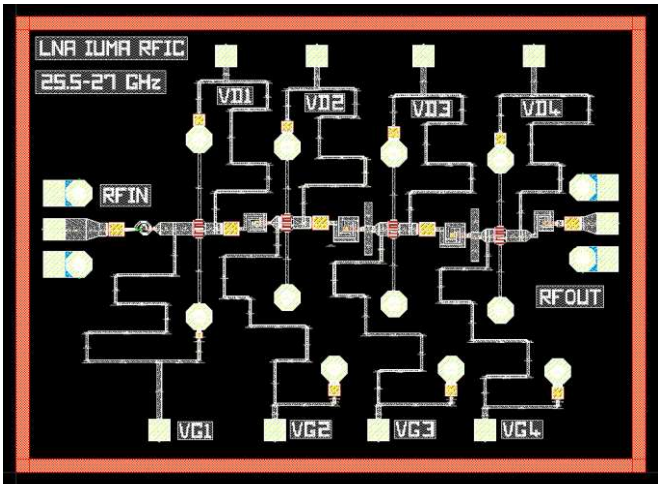
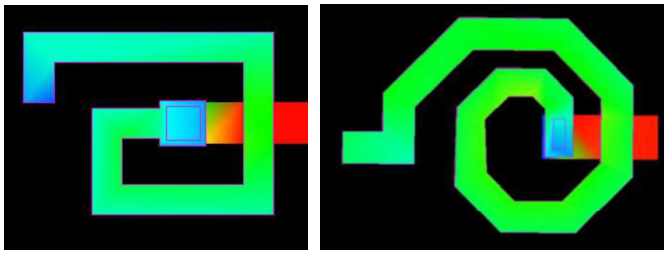


Fig. 3. Layout of the Low-Noise Amplifier.

Source feedback is applied to all the transistors due to the multiple advantages it provides [6]. Namely, it prevents instability and improves the Process-Voltage-Temperature (PVT) variations of the circuit. The inductance arising from the two source transmission lines (S1 in Fig. 1 and 2) allows the input impedance of the transistor to approximate to the optimum source impedance (S_{opt}). Thus, source feedback can improve the Input Return Loss of the LNA. The size of S1 is 250µmx10µm in order to achieve stability and a reduced NF for the first stage. Transmission lines S2, S3 and S4 have a size of 200µmx10µm, which is enough to stabilize the transistors and obtain a slightly higher gain than that of the first stage. Quarter wavelength transmission lines (λ/4) with a length of approximately 1 mm and a shunt capacitor (0.74 pF) are used as RF Chokes to bias the active devices [7]. The main advantage of this approach is that it barely affects the matching networks and it has a low impact on the overall NF of the LNA. Finally, a DC Block capacitor (CB in Fig. 2) of 1.18 pF is placed between stages to provide DC isolation.

As previously mentioned, the quality factor (Q) of the input matching network has a great impact in the NF of the first stage of the LNA. Therefore, the implementation of the inductor included in the input matching network is a key parameter. For the proposed design, a square inductor provided by the PDK was tested using EM simulations (Fig. 4(a)). Fig. 5 shows that the inductance and quality factor of this inductor are adequate. However, to minimize the series resistance of the inductor, a custom octagonal tapered inductor [8], [9] with a tapering of 1µm per turn, shown in Fig. 4 (b), was tested. Its EM simulation results are also presented in Fig. 5.



(a) (b)

Fig. 4. Simulated current density of the (a) square and (b) octagonal tapered inductor at 26 GHz.

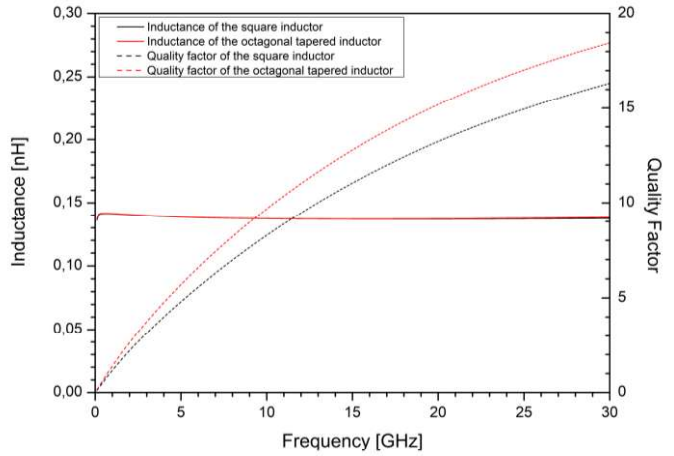


Fig. 5. Inductance and quality factor of the implemented inductor.

As shown in Fig. 5, the inductance of both elements is similar (the goal was to provide an inductance of 0.138 nH at 26 GHz), although the quality factor of the octagonal inductor is larger (17.34 @ 26 GHz for the octagonal inductor vs 15.2 @ 26 GHz for the square one). These results can be explained in terms of two mechanisms. Firstly, it is widely known that the quality factor of a rectangular inductor can be increased by approximating its geometry to that of an ideal spiral inductor. This approach improves the current circulation and, therefore, reduces the losses across the inductor's geometry. The quality factor can be further improved if the number of sides or the number of turns is increased while the inductance value is maintained [3]. Secondly, the skin and proximity effects may produce severe current crowding at the inner turns of the inductor, limiting its quality factor [8], [10]. As presented in [8], a higher Q can be obtained if the strip widths of the inner turns are reduced. Therefore, a tapered inductor can achieve a higher Q than a regular inductor. For this reason, the octagonal tapered inductor was selected to implement the input matching network of the LNA, as depicted in Fig. 2.

Once the first stage is successfully designed with a NF of 0.9 dB and a gain of 7.2 dB, the requirements for the next stages can be relaxed so they can be designed to provide a higher gain. As depicted in Figs. 2 and 3, the impedance matching network between stages 1-2 is achieved by means of a single square inductor (L2) with a value of approximately 0.37 nH. To implement the matching networks between stages 2-3 and 3-4, inductors L3, L4 (0.36 nH each) and two double open stubs (O1, O2) were used. The double open stubs O1 and O2 have a size of 30µmx90µm and 30µmx100µm, respectively. Finally, the output matching network is implemented with a single series inductor L5 of 0.24 nH.

IV. Simulation Results

Scattering and noise parameters were simulated at room temperature with ADS software and Momentum EM simulator. The resulting Input and Output Return Losses are depicted in Fig. 6, and the gain and NF are presented in Fig. 7. The simulated LNA presents an Input Return Loss of -12 dB at 26.25 GHz and an Output Return Loss of -23 dB at the same frequency. A gain of 29.5 dB ± 1 dB across the band of interest, and a NF of 1 dB are obtained. The device isolation coefficient (S_{12} parameter) is lower than -47 dB in the band of 25.5 GHz to 27 GHz. As shown in Fig. 8, the value of the stability factor *k* is above unity for all frequencies, and presents a minimum value of 2.760 at a frequency of 13.2 GHz. Individual stability was ensured as well, concluding that the amplifier is unconditionally stable.

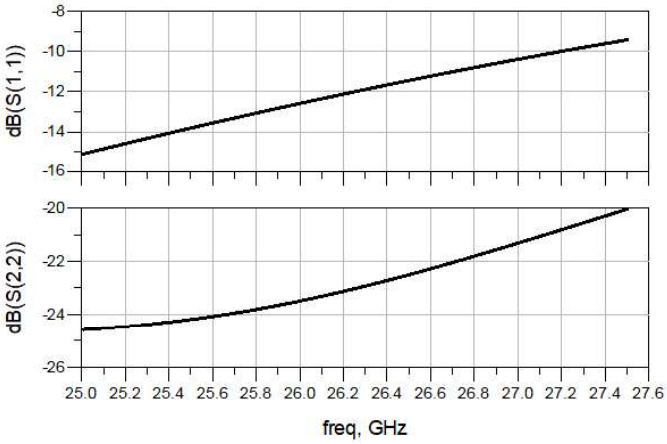


Fig. 6. Input and Output Return Loss of the proposed LNA.

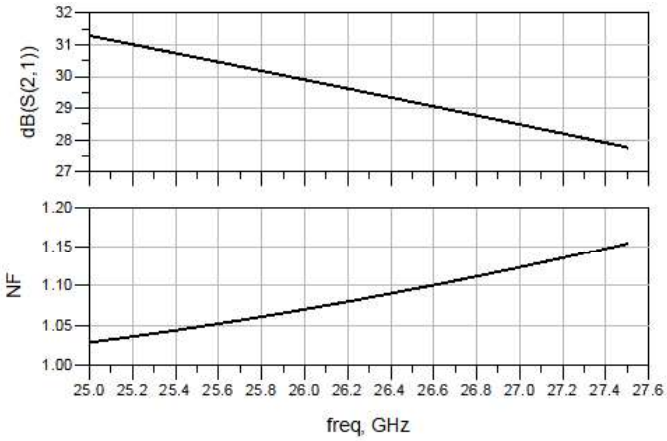


Fig. 7. Gain and Noise Figure of the proposed LNA.

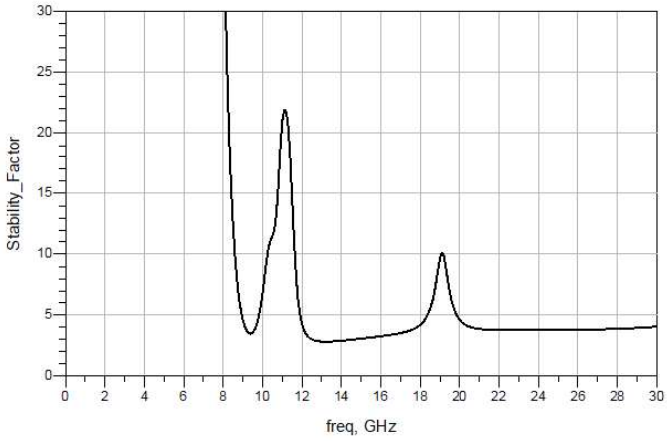


Fig. 8. Stability factor of the proposed LNA.

The main results of the proposed design and a brief overview of similar works are given in Table 1. To the authors' knowledge, the results presented in this work are expected to deviate from the simulations to some extent. However, the

overall performance of the circuit is expected to stay within the requisites. The performance of the proposed LNA is similar to other GaAs LNAs so far reported in the same frequency band at room temperature.

Table 1. Results summary and overview of similar works.

	[4]	[5]	[6]	*This Work*
Freq. Range (GHz)	*26-36*	*25-31*	*18-31*	*25.5-27*
Gain (dB)	*33 ±0.7*	*22*	*22*	*29.5 ±1*
Noise Figure (dB)	*1.5*	*1.7*	*1.7*	*1*
Input Return Loss (dB)	*-12*	*-12*	*<-30*	*-12*
Output Return Loss (dB)	*-12*	*-20*	*<-20*	*-20*
Supply (V)	-	*3.5*	*3.5*	*1.2*
Process	*GaAs 100 nm*	*GaAs 90 nm*	*GaN 100 nm*	*GaAs 70 nm*
Area (μm^2)	*2800x1300*	*2400x1000*	*2300x1000*	*2500x1750*

V. Conclusions

An approach to enhance the NF and Input Return Losses of MMIC LNAs is presented in this paper. The design work flow allows the improvement of the NF and the Input Return Loss of the LNA since the source impedance is selected to minimize the number of elements required to implement the input matching network. Two single stage amplifiers are designed and simulated at room temperature to compare the performance with the traditional approach, showing remarkable improvements in the Noise Figure and Input Return Loss of the amplifier.

A four-stage K-band MMIC Low-Noise Amplifier based on the previous approach is also presented. The LNA is designed using the models of the 70 nm GaAs mHEMT OMMIC process. The input matching network of the first stage consists of a single tapered octagonal inductor in series with the gate of the active device. The LNA is DC-biased with 1.2 V and the chip size is 2500µmx1750µm. Electro-magnetic simulation results at room temperature prove that the four-stage LNA achieves a total gain of 29.5 dB with 1 dB ripple, a Noise Figure as low as 1 dB, an Input Return Loss better than -10 dB and an Output Return Loss better than -20 dB across the band of interest.

VI. Acknowlegments

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2.6. A g_m/I_D-based Low-Power LNA for Ka-band Applications

sensors

MDPI

Article

A g_m/I_D-Based Low-Power LNA for Ka-Band Applications

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Abstract: This article presents the design of a low-power low noise amplifier (LNA) implemented in 45 nm silicon-on-insulator (SOI) technology using the g_m/I_D methodology. The Ka-band LNA achieves a very low power consumption of only 1.98 mW andis the first time the g_m/I_D approach is applied at such a high frequency. The circuit is suitable for Ka-band applications with a central frequency of 28 GHz, as the circuit is intended to operate in the n257 frequency band defined by the 3GPP 5G new radio (NR) specification. The proposed cascode LNA uses the g_m/I_D methodology in an RF/MW scenario to exploit the advantages of moderate inversion region operation. The circuit occupies a total area of 1.23 mm^2 excluding pads and draws 1.98 mW from a DC supply of 0.9 V. Post-layout simulation results reveal a total gain of 11.4 dB, a noise figure (NF) of 3.8 dB, and an input return loss (IRL) better than 12 dB. Compared to conventional circuits, this design obtains a remarkable figure of merit (FoM) as the LNA reports a gain and NF in line with other approaches with very low power consumption.

Keywords: low noise amplifier; cascode; low-power; g_m/I_D; Ka band; 45 nm; silicon-on-insulator

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1. Introduction

Low noise amplifiers (LNAs) are the first active components in the analog front end of any conventional receiver and are generally considered one of the most power-hungry blocks, as their performance is critical for the overall system. The LNA dictates the receiver's noise figure (NF) and sensitivity [1–3]. The LNA's high power consumption stems from the fact that it must provide adequate input matching, high gain, low noise, and high linearity simultaneously, all of which require high power as well as high supply voltages. These combined specifications have made the design of low-power and low-voltage LNAs a challenging research topic [4–10]. Given a certain circuit topology, the conventional LNA design approach consists of finding the optimal current density for minimum NF, maximum gain, or covering the application requirements. It requires several iterations to obtain a successful design covering the desired specifications and relies heavily on the designer's expertise and intuition. A very attractive methodology to exploit the advantages of subthreshold MOSFET operation, reduce the time-consuming design flow, and efficiently explore the LNA design space is the g_m/I_D methodology [11–14]. It explores the ratio between the small-signal transconductance (g_m) of a MOSFET and the DC drain current (I_D), known as the MOSFET efficiency. The g_m/I_D methodology has been widely used in analog integrated circuit designs to obtain very-low-power circuits for relatively low-frequency applications [4,6,15–19]. The main advantage of the methodology is that it provides a powerful sizing tool that allows the designer to take advantage of all the subthreshold regions to obtain very low power consumption circuits with very few iterations and significant time reduction in the design flow. As demonstrated by [11,12], by studying the DC bias conditions and small-signal characteristics of the MOSFETs in a PDK, circuit designers can generate a series of look-up tables (LUTs) with all the information needed

to obtain a circuit given a target specification. The main principle of the methodology is the use of a device-independent parameter (frequently, a figure of merit such as the inversion coefficient or the g_m/I_D ratio) as the main design parameter to explore the design space or determine the optimal operation region. Thanks to the generated LUTs, the need for iterative simulations is removed and near-first-time success can be achieved to cover the design requirements. Although the g_m/I_D methodology was born in the field of low-frequency analog integrated circuit design, significant efforts have been made to integrate this methodology with radiofrequency (RF) and microwave (MW) circuit design [14,20–23], demonstrating the implementation of very-low-power RFICs. However, these proposals are limited to operating frequencies of only 2.4 GHz, with no g_m/I_D-based LNA designs above an operating frequency of 5 GHz reported.

In contrast to traditional bulk silicon (Si) complementary metal-oxide-semiconductor (CMOS) processes, silicon-on-insulator (SOI) technologies present multiple advantages, such as reduced parasitic capacitances, higher quality factor (Q, figure of merit related to passive components' narrow-band response and insertion loss), improvement of device performance and speed, downsizing to nanometer dimensions, reduction in device operating voltage, lower power consumption, and reduced leakage currents, among others [24]. Although III–V compounds such as gallium arsenide (GaAs) technologies are generally employed in very-high-frequency scenarios with demanding NF requirements such as mm-wave applications, 5G networks, or satellite communications (SATCOMs), SOI technologies provide a comparable performance while facilitating system integration with lower production costs. Both III–V and SOI technologies can find application in high-resolution radar, short-range military aircraft radios, and astronomical observations, which operate at Ka-band frequencies [25–29]. For instance, the 28 GHz frequency band is identified as a pioneer band to host 5G new radio (NR) networks worldwide. It provides a very high data rate and capacity, making it a convenient choice for hotspot coverage. In this sense, the European Union designated the n258 and n257 frequency bands, which extend from 24.25 to 27.5 GHz and 27.5 to 29.5 GHz, respectively, the US identified the 27.5–28.35 GHz band, and Japan and Korea considered the 27.5–29.5 GHz and 26.5–29.5 GHz bands, respectively, for the same purpose [30]. Therefore, the developments introduced in Ka-band LNAs greatly benefit 5G mm-wave systems and applications all over the world.

In this work, we apply the g_m/I_D methodology, adapted to an RF/MW environment, to obtain a Ka-band very-low-power LNA with a remarkable performance thanks to the advantages introduced by exploiting the moderate inversion region of a MOSFET. The proposed LNA achieves a very low power consumption of only 1.98 mW and is the first time the g_m/I_D approach is applied at such a high frequency. The 28 GHz cascode LNA is implemented in GlobalFoundries 45nm RFSOI and occupies an area of 1.23 mm^2 excluding pads. The circuit achieves a gain of 11.4 dB with an NF of 3.8 dB and input return loss (IRL) better than 12 dB when fed from a 0.9 V DC supply, drawing only 1.98 mW. The organization of this paper is the following. Section 2 presents the circuit design of the proposed g_m/I_D-enabled LNA. Section 3 shows the post-layout simulation results and Section 4 concludes this paper.

2. Design Procedure

The g_m/I_D design procedure is a powerful sizing and biasing tool for MOSFET-based circuits [11,12]. The methodology exploits the ratio between the transconductance and the drain current as they are both width-dependent parameters to obtain a width-independent design variable. Since this ratio gives the ability of a MOSFET to generate a small-signal current gain from a DC bias current, the g_m/I_D ratio is often referred to as the MOSFET efficiency. The characterization of a MOSFET in terms of g_m/I_D ratio allows the derivation of the main performance metrics of a circuit to provide a width-independent sizing tool, allowing fast optimization and near-first-time successful design. A series of LUTs can be generated to avoid conventional SPICE iterative simulations, and designers can apply optimization algorithms to find optimal sizing and operating points or simply explore the

design space more efficiently [31]. The first step consists of simulating several devices to fully characterize their behavior and build the LUTs with fundamental DC, AC, and noise parameters. These values can then be used to design LNAs given the specifications and circuit topology. The floating-body (FB) transistors of the GlobalFoundries 45RFSOI process design kit (PDK) are chosen to design the LNA. Since they are FB transistors, they do not possess substrate contact. To analyze their behavior, several geometries are simulated to fully characterize the behavior of the FETs in the selected kit. The total width (W) is varied from 20 to 120 µm in steps of 5 µm; the length (L) comes in discrete values of 32, 40, and 48 nm; and the unit finger width (w_f) is varied from 0.5 to 2 µm, which is the maximum range available in the PDK. In addition, the DC voltage V_{GS} is varied from 0 V to 1 V in steps of 25 mV and V_{DS} is varied from 0 V to 1 V in steps of 25 mV, using the schematic shown in Figure 1a, which is used to simulate all the parameters analyzed in this section.

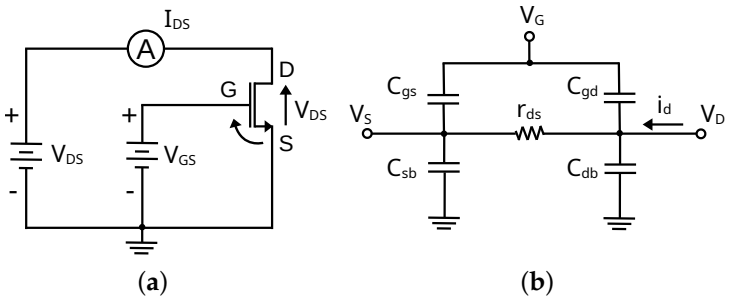


Figure 1. Schematic diagram of the setup used to obtain the I−V curves of the FB−FET from GlobalFoundries 45RFSOI PDK (**a**) and representation of the device capacitances (**b**).

The DC parameters observed include the drain current I_{DS}, the threshold voltage V_{TH}, the gate-drain current I_{GD}, and the gate-source current I_{GS}. On the other hand, the AC parameters obtained are regular transconductance g_m, gate-bulk transconductance g_{mb}, drain-source transconductance g_{ds}, and all FET capacitances (shown in Figure 1b, gate-source C_{gs}, gate-drain C_{gd}, source-bulk C_{sb}, drain-bulk C_{db}). Finally, the noise of the FET is characterized using two main parameters: STH and SFL (thermal and flicker noise, respectively).

To automate the sweeps and generate the LUTs efficiently, the simulations are automated using a single MATLAB script that performs the following tasks:

- Generates DC sweeps for all corners. These corners are generated by considering all possible combinations of process, temperature, and noise variations and depend on the PDK used. In this case, the combinations include typical (T), slow (S), and fast (F) devices with −40 °C, 16 °C, 125 °C and high-, nominal-, and low-noise corners.
- Maps the FET's operating point parameters into the desired output variables to build a multidimensional MATLAB matrix from the Cadence database results.
- Generates the Spectre simulation netlists with the desired geometries and sweeps.
- Sequentially runs all the previously generated simulations.
- Generates a .mat file with the multidimensional data for each corner as a result.

The original code provided by [11,12] is adapted to accommodate the 45RFSOI PDK and the mentioned sweeps. A simple *lookUp()* function is then used to recover the desired values and plot the desired parameters. More information about this process can be found in [11,12].

Since the Ka-band frequency range spans from 26.5 GHz to 40 GHz and the n257 frequency band (26.5 to 29.5 GHz) defined in the 3GPP 5G NR specification is particularly interesting for European mm-mave communications, a central frequency of 28 GHz is considered for the LNA design. To achieve high gain with a low NF and reasonable power consumption, a cascode topology, as shown in Figure 2, is selected [32–36]. It provides a high output impedance and higher input/output isolation compared to common-source and common-gate amplifiers, which allows the designer to cascade several stages if a higher gain is needed.

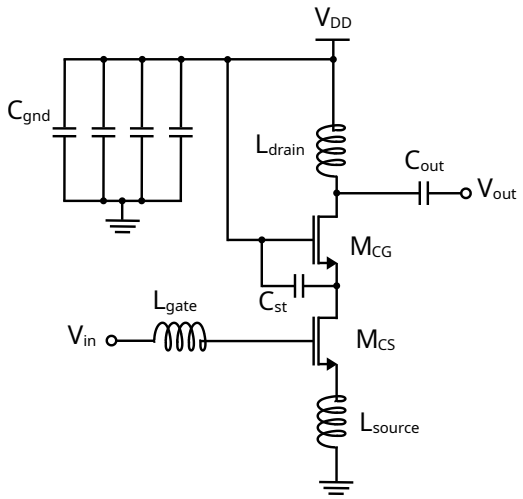


Figure 2. Schematic diagram of the cascode LNA developed.

The inversion coefficient (IC) is used to identify the sub-threshold operation region of a MOSFET and is expressed using Equation (1), with W/L being the MOSFT aspect ratio and $I_{spec\square}$, the specific current defined as (2) [37]. Details regarding the obtaining of $I_{spec\square}$ for a given process can be found in [37]. The definition of IC results in the definition of three inversion regions: weak inversion (for $IC \leq 0.1$), moderate inversion (for $0.1 < IC \leq 10$), and strong inversion ($10 < IC$).

$$IC = \frac{I_{DS}}{I_{spec\square} \cdot W/L} \tag{1}$$

$$I_{spec\square} = 2n\mu_0 C_{ox} U_T^2 \tag{2}$$

Following [14], a figure of merit for RF performance (FoM_{RF}) can be defined, as shown in Expression (3), which can be employed to find the optimal inversion coefficient IC value for a given transistor in a high-frequency design.

$$FoM_{RF} = (g_m/I_D) \cdot f_T \tag{3}$$

The values of g_m/I_D, f_T, and FoM_{RF} are presented in Figures 3a, 3b and 3c, respectively. Note that, as seen in Figure 3a, g_m/I_D is maximal in the weak inversion region and it decreases as IC moves toward the strong inversion region. On the other hand, the f_T value (Figure 3b) is remarkably low in weak inversion and it rises as IC moves towards strong inversion. The result, as expressed in (3) and presented in Figure 3c, is that the moderate inversion region achieves the optimal trade-off and it benefits from the best combination of transistor efficiency g_m/I_D and high-frequency performance (f_T). However, with this approach, the value of the input impedance (Z_{11}) and optimal NF impedance (Z_{opt}) are not known yet. Impedance selection is critical in the design process, as the input matching network implementation severely affects the gain and noise performance of the LNA.

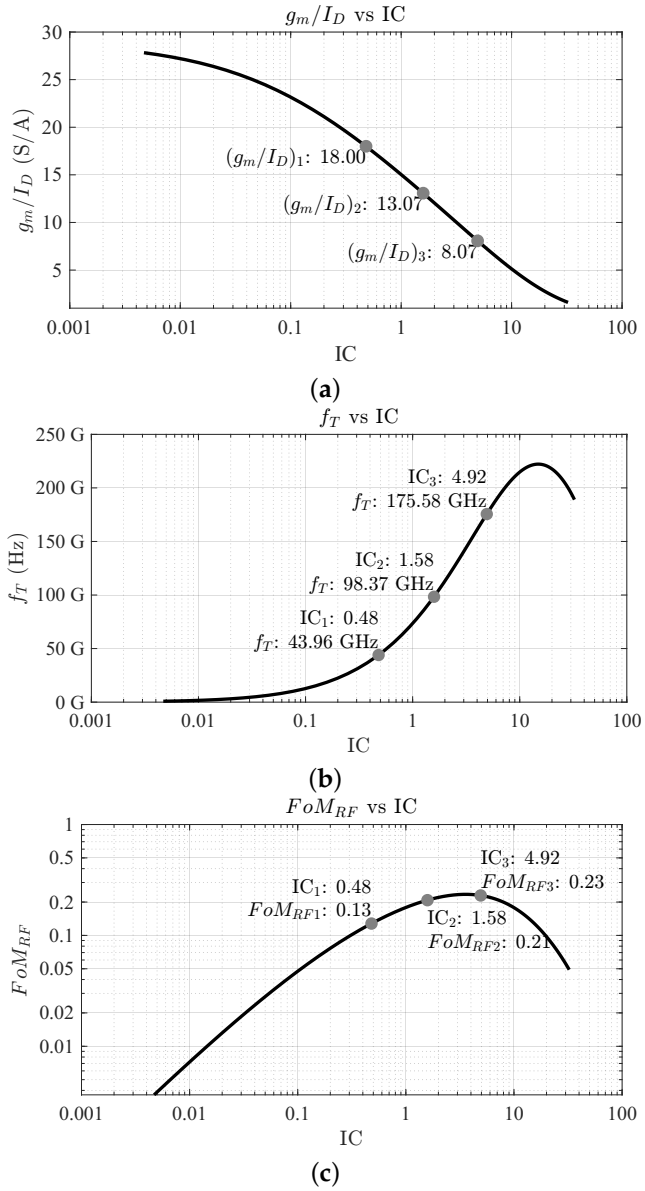


Figure 3. Representation of g_m/I_D (**a**), f_T (**b**), and FoM_{RF} (**c**) as functions of the inversion coefficient IC.

In conventional cascode amplifier design, where a common-source and a common-gate amplifier are used in series, simultaneous minimum NF and maximum gain matching can be achieved if source degeneration (L_S) is applied. Generally, the drain current density and transistor width are increased to move Z_{opt} to the 50 Ω circle, and then a single gate inductance (L_G) can be employed to match the circuit [38]. Therefore, a Z_{opt} with a real part close to 50 Ω is desired to facilitate impedance matching with a single gate inductor. To consider device geometries that allow this condition, assume the input impedance of a CS amplifier is given as (4) and the real part of the optimum source impedance is (5) [38,39]. From the state of the art, at Ka-band frequencies, an L_G under 500 pH and an L_S between 50 and 250 pH are conventionally used. Notice the parameters in (5) are known, and thus, the required width for Z_{opt} = 50 Ω can be obtained.

$$Z_{in} = r_g + s(L_G + L_S) + \frac{1}{sC_g s} + \frac{g_m L_S}{C_g s} \tag{4}$$

$$Re[Z_{opt}] \approx \sqrt{\frac{r_g}{2g_m}} \times \frac{f_T}{f} \tag{5}$$

A total device width close to 50 µm is determined to satisfy the condition of an Z_{opt} with a real part close to 50 Ω. To provide some insights into the impedances defined in (4) and (5), a graphical representation is more clearly reflected in Figure 4. Proper choice of the source inductor value can ensure that Z_{opt} and Z_{in}* are approximately equal for maximum power transfer. Then, a single gate inductor can be used to cancel the capacitive component at the gate of M_{CS} in Equation (4).

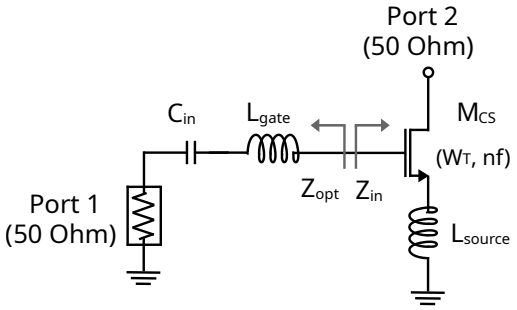


Figure 4. Schematic used to obtain the input and optimal NF impedances.

For the selected technology and the transistor employed, the total width value is determined to be 50 µm. The design approach consists of selecting a certain IC value that accommodates the specifications of the LNA. To decide which IC should be used, consider the following discussion. The transit frequency f_T limits the frequency of operation and factors such as the achievable gain and NF [38]. The f_T is closely related to the IC, as shown in Figure 3b. If the transistor's f_T is too close to 28 GHz, the LNA may not achieve a reasonable performance (low gain and high NF), but it may have low power consumption, as the lower the IC, the lower the drain current needed to bias the device. On the other hand, if the f_T is very high (n times the operating frequency), the LNA will offer very high performance (high gain and low NF), but with high power consumption.

The advantage of using the g_m/I_D methodology is that the designer can access the LUTs and produce several sets of values to perform several designs. As an example to carry on with the design, consider three values: $f_{T1} = 44$ GHz, $f_{T2} = 98$ GHz, and $f_{T3} = 175$ GHz. Since the value of f_T is approximately given by (6) for a MOSFET and g_m increases as does I_{DS}, the f_T increases as the IC is augmented. The moderate inversion region is targeted for 44 GHz, the moderate-strong inversion region for 98 GHz, and the strong inversion region for 175 GHz. Operation in weak inversion results in a very high aspect ratio (W/L), and, therefore, the device presents significant capacitance with low drain current, resulting in poor high-frequency operation. The proof-of-concept design process is conducted for these f_T values to make a comparison and select the best performance compromise. From Figure 3b, the value of IC is deduced, which is needed to obtain the DC operating point from the LUTs. In the case of the 44 GHz frequency, the corresponding IC_1 value is 0.48. For 98 GHz, IC_2 has a value of 1.58, and for 175 GHz, IC_3 has a value of 4.92. The next step is to calculate the values of threshold voltage (V_{TH}) and effective gate-source voltage or overdrive voltage (V_{GSeff} or V_{ov}) to properly bias the MOSFET. These parameters are plotted as a function of IC, as illustrated in Figure 5a,b.

$$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})} \tag{6}$$

The required V_{GS} voltage for the transistor to operate with the desired IC can be deduced from the previous figures and is given by Equation (7). V_{GS} sets the desired current flowing through the FETs, and thus, the higher the IC, the higher the V_{GS} needed to bias the device with the desired drain current. For the 44 GHz f_T case, V_{GS1} has a value of 182.41 mV to obtain a drain current of 0.67 mA; for the 98 GHz case, V_{GS2} is 255 mV for I_D = 2.2 mA; and for the 175 GHz case, $V_{GS3} = 360$ mV to set an I_D of 6.8 mA.

$$V_{ov} = V_{GS} - V_{TH} \tag{7}$$

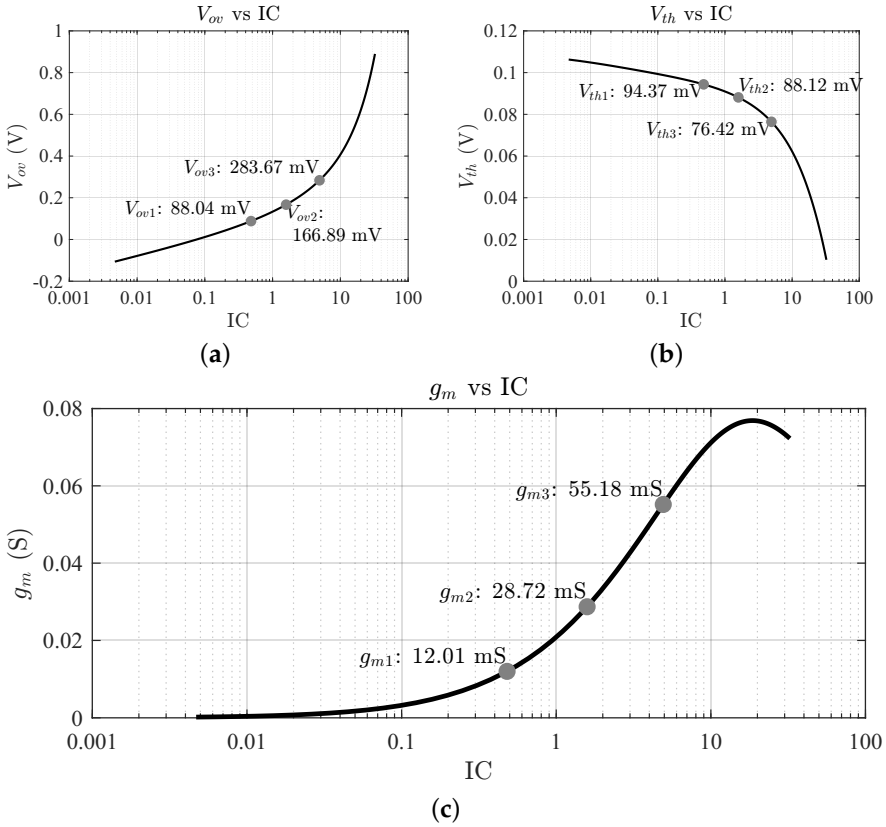


Figure 5. Simulation results of the overdrive voltage V_{ov} (**a**), threshold voltage V_{TH} (**b**), and transconductance (**c**) as functions of IC.

To fully characterize the FETs, the transconductances g_m for each IC are collected, which determine the transistor capability to produce a drain current change from an increment in V_{GS}. As shown in Figure 5c, an IC_1 of 0.48 yields a g_{m1} of 12 mS; for IC_2 = 1.58, g_{m2} is 28.72 mS; and for IC_3 = 4.9, g_{m3} is 55.18 mS. As expected, the transconductance increases as does the drain current and is maximal in the strong inversion region. Similarly, the transistor efficiency (g_m/I_D) versus IC is sought, as shown in Figure 3a. As opposed to the transconductance, the transistor efficiency is usually maximal in weak inversion and it decreases as the operation region moves towards strong inversion; hence, for IC_1, $(g_m/I_D)_1$ is 18 S/A; for IC_2, $(g_m/I_D)_2$ is reduced to 13.07 S/A; and for IC_3, $(g_m/I_D)_3$ is only 8.07 S/A. With the values of g_m/I_D and g_m available, the drain current I_D can be solved from Equation (8).

$$I_D = \frac{g_m}{g_m/I_D} \tag{8}$$

At this point, the designer may wonder about the actual devices' high-frequency performance for the selected IC values. Therefore, the G_{max} and NF_{min} can be calculated, as shown in Figure 6. The case of IC_1 suffers from a limited G_{max1} of 6.78 dB due to the lower f_T and g_m, as well as an increased NF_{min1} of 1.37 dB for the same reason. Note these are ideal values assuming ideal matching networks are used and are expected to deviate to some extent once real components are added to the circuit. That means the actual circuit implementation with PDK components results in a higher NF and a lower gain due to finite Q factors and parasitic components. For the case of IC_2, the G_{max2} is significantly improved to 10.34 dB because of the increase in both f_T and g_m, and NF_{min2} in this case is 1 dB. Finally, for the case of IC_3, the G_{max3} obtained is 13.08 dB and NF_{min3} is as low as 0.86 dB. Since the

original setup collects data from a single transistor, e.g., a common-source amplifier, both a higher gain and NF are expected when the cascode is set up.

The advantage of using this methodology is that LNAs can be designed by optimizing the power consumption for given specifications without the need for iterative simulations. Instead, a database with transistor parameters for a specific technology is available. In summary, Table 1 presents the values of the calculated parameters for the three IC values of 0.48, 1.58, and 4.92.

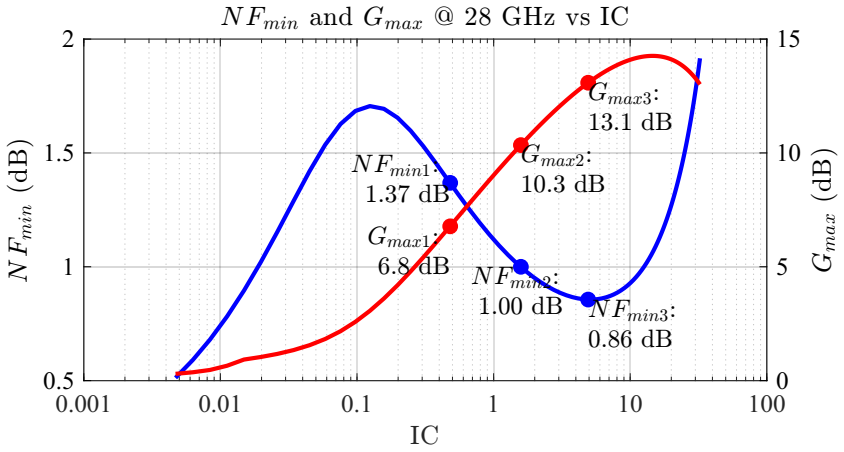


Figure 6. Maximum gain G_{max} and NF_{min} as a function of the inversion coefficient.

Table 1 illustrates the design trade-offs mentioned earlier. The most favorable among the three cases can be determined through the analysis of power consumption and a figure of merit (FoM_{IC}), as defined by Equation (9). Depending on the desired characteristics, the corresponding FoM definition and inversion region should be chosen. For instance, for our definition of FoM_{IC}, if low power consumption is desired, the weak inversion region should be selected. However, this choice comes with the flaw of increased NF_{min} and a lower G_{max} compared to the other cases. On the other hand, if a high gain with a lower minimum noise figure is sought, it should be noted that the required I_D increases, leading to higher power consumption. In contrast to low-frequency designs, in this case, the transistor area is not particularly relevant, as the impedance-matching components (inductors) occupy most of the space. Their area could be included in the definition of the FoM if the designer wants to account for them in a fairer comparison. These parameters enable us to assess and compare the quality of the different cases.

As shown in Table 1, in the case of IC_1, a high value of the FoM_{IC} is achieved with very low power consumption, but with unfavorable results, the NF is significantly high and the gain is under 10 dB. However, the FoM_{IC1} = 5.7 indicates that the LNA is more efficient in generating a high gain and low NF performance from the current drawn. For IC_1, the LNA shows a maximum gain of 8.6 dB and an NF_{min} of 3.9 dB, but it draws only 0.67 mA. Whereas the power consumption of solution IC_1 is remarkable, the gain and NF values are not in line with state-of-the-art K-band LNA designs. A gain above 10 dB and NF under 3 dB with ∼10 mA are considered state-of-the-art results. Notice the results for IC_2, with a G_{max} increment of more than 5.5 dB compared to IC_1 (to 14.2 dB) and NF_{min} reduction of 2 dB (to 1.9 dB), with a three-times-higher drain current (2.2 mA) required compared to IC_1. Considering similar works available in the literature, these values of G_{max} and NF_{min} are closer to state-of-the-art K-band LNAs. As seen for IC_3, the values of G_{max} and NF_{min} are improved further to 17 dB and 1.4 dB, respectively, but the current drawn increases as well. The required I_D is three times that required to bias the IC_2 LNA, yet the NF_{min} is only improved by 0.5 dB, and the maximum gain, by less than 3 dB. In the case of IC_2, slightly inferior results are obtained compared to IC_3, but with a much higher FoM_{IC} value and better power consumption. On the other hand, comparing IC_1 to IC_2, the improvement in FoM_{IC} or power consumption is not as significant, meaning IC_2 is not as efficient as IC_1,

yet the results are inferior to state-of-the-art K-band LNAs. In the case of IC_3, the results can be further improved, but with a strong impact on the LNA's power consumption with small gains in performance. Ultimately, the decision is to proceed with the layout design for IC_2 = 1.76 µA, as it provides enough gain and NF to be in line with state-of-the-art solutions with the best trade-off between performance and power consumption, which will be explained in more detail in the following section.

Table 1. Values of the DC and AC parameters of the three selected ICs.

Parameter	IC_1 = 0.48	IC_2 = 1.58	IC_3 = 4.92
V_{GS} (mV)	182	255	360
V_{TH} (mV)	94	88	76
I_D (mA)	0.67	2.2	6.8
g_m (mS)	12	28.7	55.2
g_m/I_D (S/A)	18	13	8
W/L	1.25 k	1.25 k	1.25 k
NF_{min} (dB)	3.9	1.9	1.4
G_{max} (dB)	8.6	14.2	17
P_{DC} (mW)	0.6	1.98	6.2
L_{source} (pH)	180	135	104
L_{gate} (pH)	458	408	352
L_{drain} (pH)	500	500	500
FoM_{IC}	5.7	4.2	2

$$FoM_{IC} = \frac{2 \cdot S_{21}[dB]}{NF[dB] \cdot P_{DC}[mW]} \tag{9}$$

After assembling the schematic, the DC operating point of the circuit is analyzed to verify the previously calculated values. There is an expected deviation in the DC parameters, since the FETs were simulated in a common-source configuration with a V_{DS} of 0.9 V. However, in the cascode the effective V_{DS} for each FET is reduced to ∼0.45 V, and due to the nature of short-channel devices, there is a drain current mismatch. Therefore, V_{GS} must be adjusted to ensure the drain current targeted value. Now, the LNAs' matching components can be calculated. To bring the Z_{11} and Z_{opt} to the center of the Smith chart, the values of L_{source}, L_{gate}, and L_{drain} inductors (see Figure 2) are calculated. Additionally, a C_{out} value of 50 fF has been established for all three cases to improve the S_{22}.

3. MOSFET Characterization and Simulation Results

To include the effect of metal interconnections on FET performance early in the design process, the layout of the cascode is developed first [40]. The new component consists of the raw PDK FET device, an RCC (resistance, capacitance, and coupled capacitance) parasitic extraction of the low-level, thin metal layers, and an EM characterization of the high-level, thick metal layers to account for parasitic inductance. As indicated in expression (10), the value of NF_{min} can be optimized [38]. Note that R_G is the gate resistance, R_S is the source resistance, f is the working frequency, and f_T is the unity current gain frequency.

$$NF_{min} = 1 + K \cdot \sqrt{(g_m \cdot (R_G + R_S))} \cdot \frac{f}{f_T} \tag{10}$$

The circuit is implemented using the GlobalFoundries 45 nm RFSOI PDK. The technology has seven copper (Cu) layers (M1-M3, C1, UA, OA, OB) and one aluminum (Al) layer with a thickness of 4.125 µm. The RCC extraction is obtained using Calibre xRC extraction,

and the EM characterization is obtained from EMX Planar 3D software. A staircase configuration is used to optimize the NF (NF_{min}) of this device by reducing parasitic capacitances and gate and source resistances. To facilitate DRC rules compliance and current flow, the FETs are divided into four instances. In addition, a C_{GS} capacitor (C_{st} in Figure 2) is added in metal layer C1 to improve device stability. The 3D view of the developed layout is presented in Figure 7.

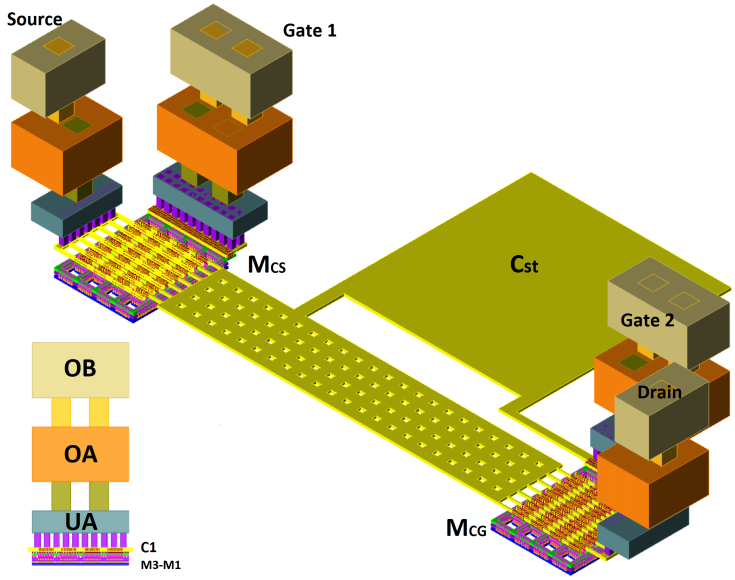


Figure 7. 3D view of the two MOSFETs used to design the cascode LNA.

Once the MOSFET characterization is availablem the schematic in Figure 2 is set up and the values of the inductors needed are adjusted to compensate for the deviations introduced by the new RCC + EM characterization of the cascode MOSFETs. The gate inductor is adjusted to 409 pH to achieve input impedance matching, L_{drain} is reduced to 313 pH, L_{source} is reduced to 130 pH and substituted by a transmission line, and C_{out} is adjusted to 24 fF to improve S_{22}. In addition, for proper AC grounding, a number of 1 pF shunt capacitors are added at the gate of M_{CG}. The final cascode layout is shown in Figure 8.

A post-layout extraction of the S-parameters after EM simulation with all the passive components in the final circuit is performed to verify the LNA. The simulation results are presented in Figure 9, showing a gain of 11.4 dB and a NF of 3.8 dB at a central frequency of 28 GHz. Regarding the input and output return losses, an $|S_{11}|$ of 12.7 dB and an $|S_{22}|$ better than 10 dB are obtained. The LNA draws a total of 1.98 mW from a 0.9 V DC supply and occupies a core area of 0.723×0.598 mm^2. As shown in Figure 9b, a two-tone simulation with 100 MHz spacing is conducted to verify the LNA's linearity, demonstrating a P-1 dB of 1.8 dBm and an IIP3 of -1 dBm.

Table 2 presents a comparison with some of the most relevant state-of-the-art solutions. In [41], the authors develop a mm-wave multi-band LNA in 45 nm CMOS SOI using a three-stage differential cascode with interstage transformer-based matching networks to save area. It achieves a notable gain of 19.5 dB with an NF of 4.7 dB, but at the cost of high power consumption (59 mW). A single-ended-input, differential-output tunable K/Ka-band LNA operating at 28 and 39 GHz is demonstrated in a 65 nm CMOS in [42], maintaining a very low NF of 2.8 dB with a gain of 17.2 dB, yet with a very high power consumption of 28.5 mW. In [43], a 22 nm CMOS fully depleted-SOI low-power LNA with a single-stage cascode configuration is presented. It achieves a remarkable power consumption of only 4.6 mW, a gain of 7 dB, and an NF of 5 dB. A dual-band LNA in 22 nm CMOS FDSOI for 5G wireless systems is demonstrated in [44]; the authors report a high gain (19.3 dB) and a minimum NF of 5.2 dB with a power consumption of 11.4 mW in

0.27 mm^2. The LNA achieves simultaneous dual-band operation by employing a two-stage single-ended cascode topology with carefully optimized transmission lines and capacitor-based matching networks. In [29], a wideband (14 and 31 GHz) LNA in 54 nm CMOS SOI is demonstrated, providing a low NF of only 1.4 dB with 12.8 dB gain. However, this LNA draws as much as 15 mW and occupies an area of 0.3 mm^2. In contrast, we propose a low-power LNA that achieves a gain of 11.4 dB with only 1.98 mW power consumption, while maintaining an NF within the average range of the other state-of-the-art designs. The developed work demonstrates the g_m/I_D methodology can effectively be used to obtain an LNA with a gain above 10 dB with a low NF. We report a very low power consumption with remarkably high performance at Ka-band frequencies.

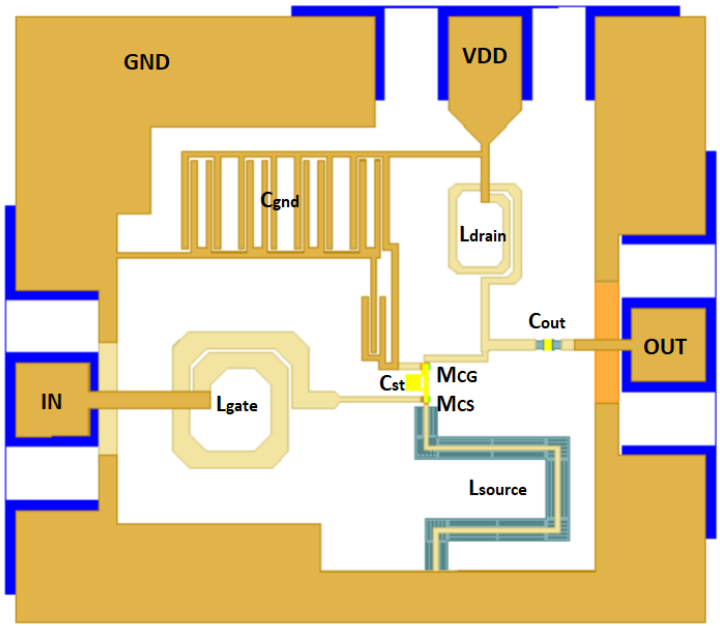
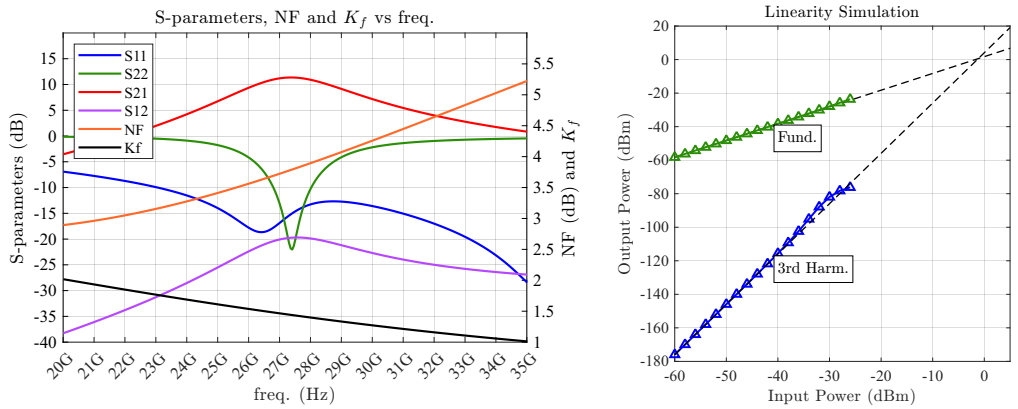


Figure 8. Simplified frontal view of the cascode LNA final layout.



(**a**) (**b**)

Figure 9. Simulation results of the proposed LNA with the EM characterization of each passive component (**a**) and two-tone linearity simulation for the obtainment of the IIP3 (**b**).

Table 2. Overview of similar state-of-art LNAs with the proposed circuit.

Reference	This Work	[41]	[42]	[43]	[44]	[29]
Tech.	45 nm SOI	45 nm SOI	65 nm CMOS	22 nm SOI	22 nm SOI	45 nm SOI
BW (GHz)	25.5–29.5	21–28	23.5–32.5	24–28	26.6–31.6	14–31
Centre Freq. (GHz)	27.5	24.5	27.5	26	29.1	22.5
Supply (V)	0.9	1	1	0.8	1.6	1.5
Max Gain (dB)	11.4	19.5	17.2	7	19.3	12.8
Threshold Gain (dB)	8.4	16.5	14.2	4	16.3	9.8
NF (dB)	3.5–3.8	4.7	2.8–3	5	5.2	1.4
IRL (dB)	12.7	–	25	6	10	10
ORL (dB)	10	–	–	–	10	10
P_{DC} (mW)	1.98	59	28.5	4.6	11.4	15
Meas./Sim.	Sim	Meas.	Meas.	Meas.	Meas.	Meas.
FoM_{IC}	3.03	0.14	0.4	0.608	0.65	2.08
Core area (mm^2)	0.43	0.42	0.157	0.1	0.27	0.3

4. Conclusions

The design of a low-power Ka-band cascode LNA using the g_m/I_D methodology is discussed in this work. The proposed circuit achieves a very low power consumption of only 1.98 mW. In addition, it is the first time the g_m/I_D approach is applied at Ka-band frequencies. The proposed circuit is developed with the 45 nm SOI PDK components. The LNA has a central frequency of 28 GHz as the circuit operates in the n257 frequency band defined by 3GPP NR for European mm-wave communications. The design approach presented involves the g_m/I_D methodology to exploit the advantages of sub-threshold operation in a high-frequency scenario, biasing devices in the moderate inversion region for a remarkable performance trade-off. A single MATLAB script is used to generate all the sweeps and the simulation netlists, to run the SPECTRE simulations, and to map the desired parameters in a multidimensional .MAT file containing all the LUTs needed to perform automated circuit design. We explore the procedure by providing a design example, from scratch to post-layout simulations, of a Ka-band cascode LNA obtaining a very-low-power, high-performance amplifier. The final circuit draws 1.98 mW from a DC supply of 0.9 V with a chip size of 0.43 mm^2 excluding pads. After post-layout parasitic extraction and EM analyses, the circuit exhibits a gain of 11.4 dB, an NF of 3.8 dB, and an IRL better than 12 dB across the band of interest. Finally, a comparison is made with similar works available in the literature. The proposed circuit shows a very high performance, since the amplifier obtains a gain and NF in line with other works and a very low power consumption of only 1.98 mW.

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Abbreviations

The following abbreviations are used in this manuscript:

C_{gs}	Gate-Source Capacitance
C_{gd}	Gate-Drain Capacitance
C_{sb}	Source-Drain Capacitance
C_{db}	Drain-Bulk Capacitance
CMOS	Complementary Metal Oxide Semiconductor
IC	Inversion coefficient
I_D	Drain current
I_{GD}	Gate-Drain Current
I_{GS}	Gate-Source Current
IRL	Input Return Loss
FB	Floating-Body
FoM	Figure of Merit
g_{ds}	Drain-Source Transconductance
g_m	Regular Transconductance
g_{mb}	Gate-Bulk Transconductance
LNA	Low-Noise Amplifier
MMIC	Monolithic Microwave Integrated Circuit
MW	Microwave
NF	Noise figure
ORL	Output Return Loss
PDK	Process Design Kit
RF	Radiofrequency
RFIC	RF Integrated Circuit
UWB	Ultrawide Band
VDS	Drain-Source Voltage
VGA	Variable Gain Amplifier
VGS	Gate-Source Voltage
VTH	Threshold Voltage
SATCOM	Satellite Communications
SOI	Silicon-on-insulator
STH	Thermal Noise coefficient
SFL	Flicker Noise Coefficient
w_f	Unit Finger Width

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2.7. A 0.38 V Fully Differential K-Band LNA with Transformer-Based Matching Networks

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A 0.38 V Fully Differential K-Band LNA with Transformer-Based Matching Networks

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Abstract: The implementation of a 0.38 V K-band low-power fully differential low-noise amplifier (LNA) in a 45 nm silicon-on-insulator (SOI) process is presented. The proposed architecture employs a two-stage approach with transformer-based interstage matching networks to minimize circuit area. The proposed LNA covers the frequency range from 20.3 to 24.1 GHz, it achieves a noise figure (*NF*) as low as 2.2 dB, and a gain of 12.9 dB, with a power consumption of 11.7 mW from a 0.38 V DC supply in a very compact area (0.15 mm^2) excluding pads. Non-linearity simulations show the proposed circuit achieves a P_{o1dB} of −7.3 dBm, and an OIP3 (Output Third Order Intercept) of 7 dBm. The transformers allow improved area use since they are simultaneously used as matching networks, RF chokes to bias the active devices, baluns at the input and output terminals to convert the single-ended signal into differential mode, and vice versa, and facilitates the interconnection with the upcoming stages. We used a state-of-the-art tool that generates the desired inductances to perform impedance matching for a given frequency and coupling factor value. A comparison with similar works proves the proposed LNA achieves a very low *NF* and the lowest power consumption reported in a differential circuit.

Keywords: silicon on insulator; fully differential; low noise amplifier; transformer-based matching networks; electromagnetic analysis; K-band

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1. Introduction

The role of the LNA is vital in radio frequency (RF) and microwave (MW) receivers. Its performance directly affects the receiver sensitivity as it is generally the first active element to process the received signal. The main function of the LNA is to perform proper impedance matching with the antenna while providing a noise figure (*NF*) as low as possible and sufficiently high gain to attenuate the noise contribution of the upcoming stages. However, usually the LNA consumes most of the power available to provide such high performance, leaving the other components in the system with a small DC power budget [1]. A feasible solution, as seen in [1–3], consists of reducing the supply voltage so that the power budget available for the rest of the components in the receiver is relaxed. By adopting this approach, circuit integration is improved as the LNA can be introduced in a wide range of devices and systems since it can be biased with a very low voltage. Another concern in LNA design is the area needed for the final circuit since conventional LNA design involves the use of bulky inductors to perform impedance matching, source degeneration, inductive neutralization, gain peaking or resonate internal transistor capacitances, among other techniques [4,5]. Although the inductor size is reduced as the operating frequency increases, the area use can be further improved if a transformer-based approach is introduced, bringing multiple advantages to the designer as it allows higher gain and bandwidth and lower noise as well [6].

The differential architecture presents advantages such as a high common mode rejection ratio (CMRR), better ground plane quality, lower parasitic effects of chip interconnections, wider dynamic range and easier coupling between stages, among others. Differential circuits allow direct coupling between stages, avoiding the need for DC isolation capacitors and complex interstage matching networks. As a result, it reduces the area of the integrated circuit and, therefore, its manufacturing costs. Numerous works available in the scientific literature introduce differential LNAs to facilitate system-on-chip integration since they provide high resilience to power supply and common-mode noise [7–10]. However, in differential circuits, the number of components and the power consumption are doubled. In addition, the use of a balun (BALanced-to-UNbalanced) is necessary to transform the single-ended (SE) input signal into a differential signal. Integrated transformer design is gaining prominence in mm-Wave circuit design. Several works have been published recently regarding the design and modeling of integrated transformers for various applications [11–13]. Nevertheless, this element produces extra losses in the signal path due to the limited values of the magnetic coupling coefficient (k) and quality factor (Q) achievable in integrated technologies, which can negatively impact the *NF* of the LNA.

In contrast to traditional bulk silicon (Si) complementary metal-oxide-semiconductor (CMOS) processes, SOI technologies present multiple advantages, such as reduction of parasitic capacitances, improvement of device performance and speed, downsizing to nanometer dimensions, reduction of device operating voltage and lower power consumption, among others [14]. Therefore, the proposed circuit is implemented using an SOI process design kit (PDK) from Global Foundries.

In this work, a fully differential LNA with transformer-based interstage matching networks for K-band applications is presented. The LNA is based on a two-stage CS (common source) topology and is developed in a 45 nm SOI (45RFSOI) process from Global Foundries. The main features of the proposed circuit are a *NF* as low as 2.2 dB, a gain of 12.9 dB, input and output return losses (IRL and ORL) above 10 dB, an IIP3 of -4 dBm, and power consumption of 11.7 mW from a 0.38 V DC supply in a very compact area (0.15 mm^2). This is possible thanks to the transformer-based approach, which allows improved area use as they simultaneously act as RF chokes to bias the active devices, and as baluns at the input and output terminals to convert the SE signal into differential mode, and vice versa. To implement the transformers we replicated a state-of-the-art tool into a MATLAB script that generates and equalizes the desired inductances to perform impedance matching for a given frequency and coupling factor value. The content of this paper is organized as follows: the circuit design is discussed in Section 2, and the implementation of the interstage transformers is discussed in Section 3. Then, in Section 4, the simulated S-parameters, *NF*, and non-linearity results are shown, along with a comparison with state-of-the-art LNAs. Finally, in Section 5, the conclusions of this work are drawn.

2. Circuit Design

The main concern in LNA design is the achievement of the lowest *NF* possible because it is critical for the overall *NF* of the system. In this work, the LNA is divided into two fully differential CS stages with source degeneration, as shown in Figure 1. All the values of the passive components used in the circuit are described in Table 1. The advantage of using a CS topology with inductive degeneration is the possibility of simultaneously achieving impedance matching for minimum *NF* and maximum gain (G_{max}) [15]. This topology is widely used in applications with very low *NF*. In comparison to CS amplifiers, the common gate (CG) topology is frequently used in wideband applications, because of its potential to achieve a higher gain. However, the *NF* obtained is usually higher in comparison with CS amplifiers. On the other hand, a higher gain can be obtained with a cascode architecture as well, but at the expense of higher power consumption, since the supply voltage cannot be reduced due to the presence of two transistors in the same branch. Transistors M1 and M2 in Figure 1 are the core of the first stage, and are biased with the DC voltage V_G. Transistors M3 and M4 are the core of the second stage, and they are sized and biased exactly as M1

and M2. The degeneration inductances L_s are used to improve the noise and IRL of both stages. The input matching network of the circuit is efficiently implemented by the input transformer T1, which is characterized by the coupling factor k_1, primary inductance L_{p1} , and secondary inductance L_{s1} . The same applies to transformers T2 (k_2, L_{p2}, L_{s2}) and T3 (k_3, L_{p3}, L_{s3}). Transformer T1 performs three tasks simultaneously: translation from SE to differential mode, impedance matching, and efficient DC biasing of transistors M1 and M2 through the center tap connection of the secondary. In the same way, transformer T3 has the same task at the output node, but it converts the differential mode signal into SE mode in order to facilitate the measurement procedure of the amplifier. Transformer T2 is used to couple stages 1 and 2 and is also efficiently used to bias the drains of M1 and M2, and the gates of M3 and M4 at the same time, while performing interstage impedance matching. An integrated transformer occupies the same space as a single inductor but performs three tasks simultaneously, therefore, we are able to save a significant amount of area. Finally, capacitors C_m of 195 fF are used at the gates of M3 and M4 to improve impedance matching without significantly compromising the performance and area of the resulting circuit.

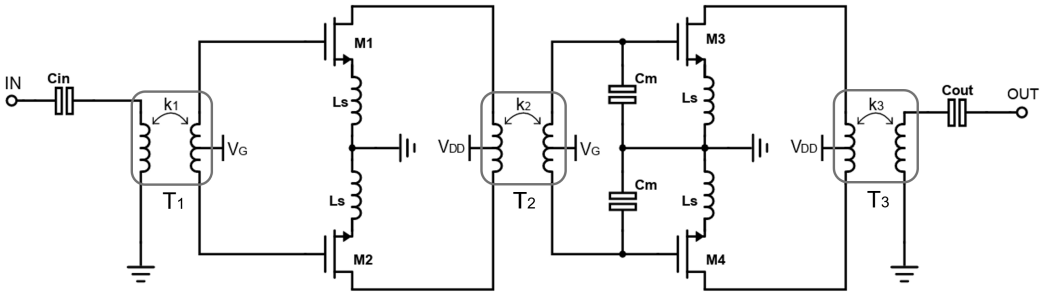


Figure 1. Schematic of the proposed fully differential 2-stage LNA with transformer-based interstage matching networks.

Table 1. Component values used in the proposed LNA.

L_{eq1}	k_1	C_{in}	L_{eq2}	k_2
751 pH	0.73	57 fF	312 pH	0.66
C_m	L_{eq3}	k_3	C_{out}	L_s
195 fF	475 pH	0.81	79 fF	161 pH

To perform device sizing, we inspect the most relevant performance metrics (i.e., the minimum *NF* and G_{max}) in relation to the current density J_{DS} for a number of device geometries. As depicted in Figure 2, for a device geometry of 60 µm with 120 fingers (0.5 µm per finger), a minimum *NF* of 1.17 dB is obtained when the device is biased with a J_{DS} of 0.1286 mA/µm. Thus, a drain current I_{DS} of 0.1286 mA/µm × 60 µm = 7.71 mA is required. To achieve this current density, a gate voltage V_G of 0.38 V is employed. Therefore, we choose this size and biasing conditions for the CS transistors M1 and M2. Once the device is biased with a DC drain current of 7.71 mA, the resulting optimum source impedance S_{opt} required at the gate of M1 and M2 is calculated to achieve the minimum *NF*. In a conventional design, a complex input matching network would be needed to match the S_{opt} to the 50 Ohms of the input antenna, but thanks to the differential approach, we are able to efficiently use transformers for this task.

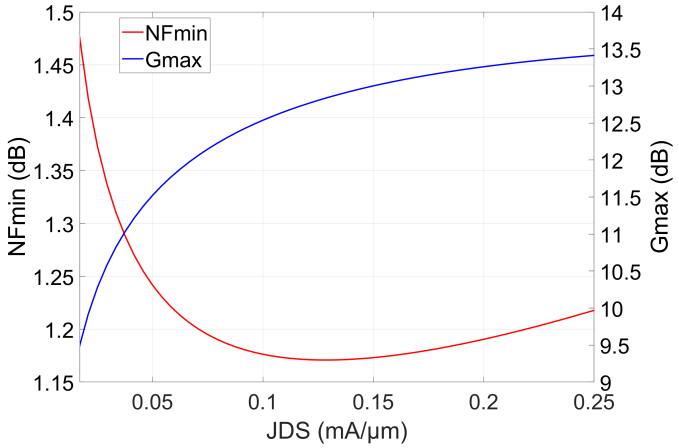
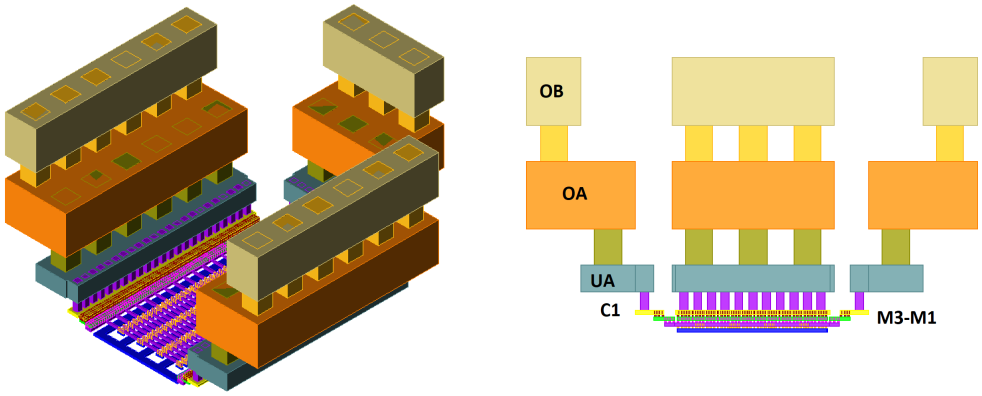


Figure 2. Simulated NF_{min} and G_{max} as a function of the device current density J_{DS} at 22.5 GHz.

The Global Foundries 45-nm RFSOI PDK is used to design the layout of the transformers. The design kit offers 7 copper (Cu) layers (M1-M3, C1, UA, OA, OB) and a 4.125-µm thick aluminum (Al) layer. The OB and OA metal layers are used to implement all the inductors since they are composed of copper lines with the same thickness (3 µm), which facilitates the equalization of inductors. That is, it facilitates the obtention of the same inductance and quality factors of the windings of the primary and secondary inductors [16]. Since the transistors are placed on the substrate and the passive components are generally implemented in the top metal layers to obtain the highest quality factor (Q) possible, a number of vias and interconnections have to be added to bring the connections of the gate, source, and drain terminals from the low, thin metal layers to the top, thick layers. So as to account for the effect of these metal interconnections on the LNA performance, we developed the layout of the selected transistor early in the design procedure to consider these effects [17]. The 3D view of the developed layout is presented in Figure 3a and the front view of the same layout is shown in Figure 3b. To prepare the layout of the active device, we sliced it down to 4 instances of 15 µm with 30 fingers each, which allows gate, drain, and source interconnections complying with the design kit physical rules, since low metal layers have very restrictive constraints related to their maximum width and area. To minimize parasitic capacitances at the gate, drain, and source nodes we employed a staircase configuration. This implementation also caters to the reduction of the gate resistance and parasitic capacitances to optimize the achievable minimum noise figure (NF_{min}) of this device. In this sense, the NF_{min} for a MOS device can be expressed as (1), where K is a constant value, g_m is the transconductance of the device, R_G is the gate resistance, R_S is the source resistance, f is the working frequency and f_T is the unity current gain frequency [4]. Hence, maximizing f_T (by minimizing parasitic capacitances) and minimizing R_G and R_S allows the reduction of NF_{min}.

$$NF_{min} = 1 + K \cdot \sqrt{(g_m \cdot (R_G + R_S))} \cdot \frac{f}{f_T} \quad (1)$$

The new, complex model of the FET is composed of the intrinsic PDK FET device, an RC parasitic extraction of the interconnections from M1 to C1 layers using Calibre xRC, and an EM simulation model generated with EMX of the interconnections from UA to OB metal layers.



(**a**) (**b**)

Figure 3. The 3D representation of the active device layout (**a**), and front view of the same device (**b**).

The design of the 0.38 V low-power LNA is possible thanks to the CS current density design approach, which is detailed as follows. The active device provides an excellent noise performance at J_{Dopt} = 0.1286 mA/µm. Hence, the device provides optimal noise performance when it is biased with I_{DS} of 7.71 mA. We can then search for a combination of V_D and V_G that yields the desired I_{DS}. Since the LNA is formed by two cascaded CS stages, we can reduce the nominal 0.9 V drain DC voltage required by the PDK and increase the gate DC voltage accordingly to maintain the same J_{DS}, which results in a severe reduction in power consumption without significantly compromising the LNA performance. This would not be possible if a cascode topology had been used. The DC supply voltage is reduced from 0.9 V to 0.38 V and the gate voltage V_G is increased to 0.38 V as well. With these values, the drain current I_{DS} is 7.71 mA as desired, ensuring minimum *NF* performance with little deviation in gain and impedance matching of the LNA.

3. Transformers Implementation

A transformer is a passive structure composed of primary and secondary inductors (L_p and L_s), with a certain magnetic coupling coefficient k between them. In a transformer, k determines the strength of the magnetic coupling between the windings and is given by (2), where M is the mutual inductance between the primary and the secondary.

$$k = \frac{M}{\sqrt{L_p \cdot L_s}} \tag{2}$$

Due to the overlapping, the proximity of the windings, and the dielectric constant of the substrate material, designers have to deal with a finite parasitic capacitance (C_{par}) which can give rise to a low value of the self-resonant frequency (SRF). The SRF is the frequency at which the transformer resonates, determined by (3), and it limits the range of use of the transformer. This is because C_{par} is proportional to the inductance value (L). In electronic circuit design, it is desirable for the operating frequency to be a fraction of SRF in order to attain the maximum possible inductance for a given operating frequency. However, as the frequency increases, the utilization of large inductances becomes increasingly challenging due to the corresponding increase in C_{par} with frequency. Since we are dealing with the design of a K-band LNA, the transformers need to be designed to present an SRF in the order of 50 GHz, which is achieved by means of layout techniques.

$$\omega_{srf} = \frac{1}{\sqrt{L \cdot C_{par}}} \tag{3}$$

To size the transformers defining the values of k, L_p, and L_s, the designer must obtain the desired source and load impedances (Z_S and Z_L, respectively). The impedance Z_S

refers to the impedance seen at the input terminal of the transformer (the primary), while impedance Z_L is the impedance at the output node of the transformer (the secondary), which is equivalent to the conjugate value of the desired S_{opt}. This situation is reflected in Figure 4.

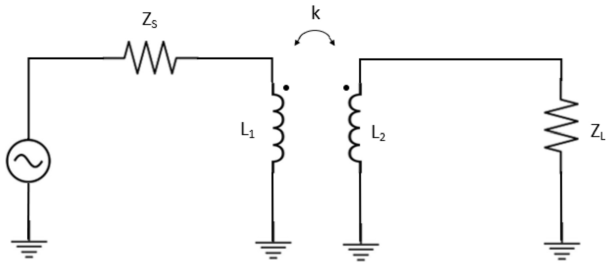


Figure 4. Equivalent circuit of a transformer-based impedance matching network.

Instead of using a discrete analytical solution as an approximation to the final values of k, L_p, and L_s, the transformer-based impedance matching tool proposed in [12] is replicated in MATLAB for transformer sizing and inductance equalization. The developed tool receives the working frequency f, the magnetic coupling coefficient k, the source impedance Z_S, and the load impedance Z_L as inputs, and it produces the inductance values of a transformer that matches the given impedances at the operating frequency.

The MATLAB script generates the values of inductances L_p and L_s to match the two impedances at the given frequency and magnetic coupling coefficient. In addition, an equalization process is implemented, following [12], to adjust the inductors to present the same inductance value, L_{eq}. As a result of the equalization process, an additional passive element has to be added to the source or load of the transformer to perform impedance matching. This is the reason why the capacitors C_{in}, C_m, and C_{out} are added to the schematic in Figure 1.

Due to the nature of integrated technologies, achieving a k greater than 0.8~0.9 can be challenging. The EMX full-wave electromagnetic (EM) solver has been used to explore the k values that can be achieved in the 45RFSOI technology (~0.7). The MATLAB tool is then used to calculate the inductances needed to match Z_S with Z_L for this k value. Obtaining the desired inductances depends on the geometry and physical properties of the metals and layers used, so obtaining them is an iterative process, highly dependent on the physical structure used. The final design of the transformers is shown in Figure 5. The layout design has been based on the proposal in [18]. The design of T1 is the most challenging due to its high L_{eq} value (751 pH), and as the first element in the circuit, it is crucial to minimize its losses. As studied in [16], there are several ways to design an integrated transformer. One option is a stacked layout, which allows for a high magnetic coupling (k = 0.6~0.8) but also leads to a large parasitic capacitance between the primary and secondary inductors since they are completely overlapped. In the case of transformer T1, it is designed using a stacked layout with interwound windings to obtain a high SRF. The transformer's primary and secondary inductors are implemented with two turns, with the secondary being larger in size compared to the primary. However, this inductance difference is compensated by extending the connection of the primary to the ground, which adds a small inductance to compensate for the difference.

For the other two transformers, the goal is to maximize k and minimize the area at the expense of decreasing the SRF. To achieve this, the primary and secondary metals were stacked. Transformer T2 has only one turn as the required L_{eq2} is 312 pH, while the L_{eq3} needed in T3 is 475 pH, which is why it was implemented with two turns. Table 1 shows the values of all the elements used in the design of the LNA.

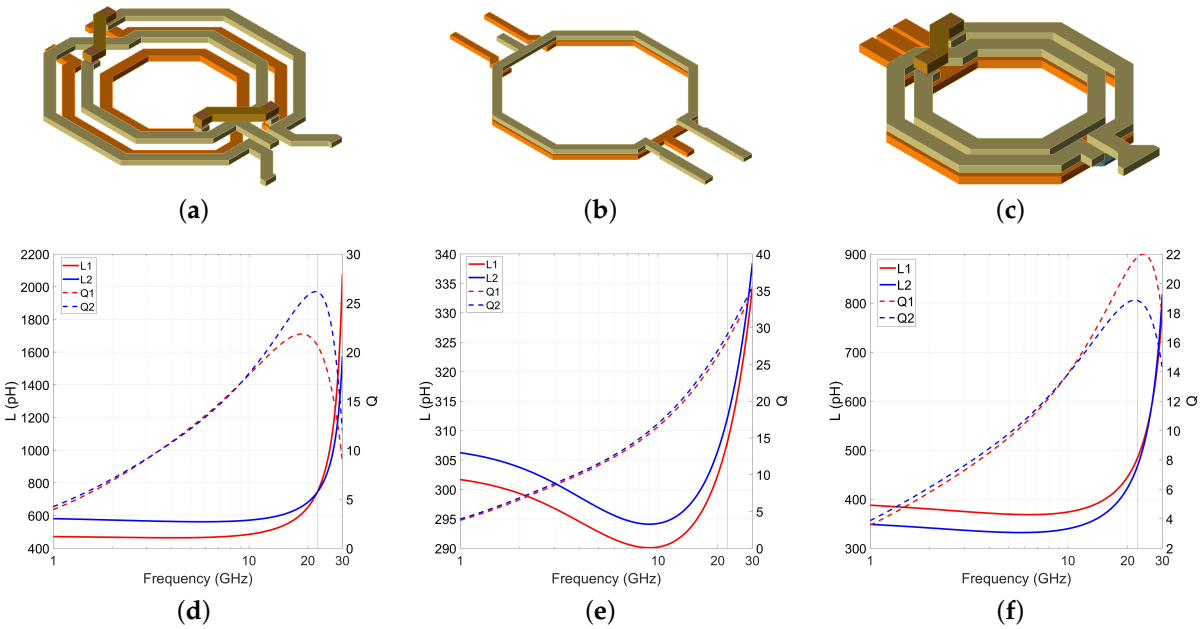


Figure 5. Layout of the input transformer T1 (**a**), the second transformer T2 (**b**), and the output transformer T3 (**c**), and inductance, and quality factor of transformers T1 (**d**), T2 (**e**), and T3 (**f**).

4. Simulation Results and Comparative

The performance of the proposed LNA was obtained with Spectre RF Simulator after performing the post-layout parasitic extraction in Cadence Virtuoso using Calibre PEX tools. The LNA consumes a DC current of 30.7 mA, resulting in a power consumption of 11.7 mW. The simulation results of the S-parameters are shown in Figure 6a. A maximum gain of 12.9 dB is obtained at 21.2 GHz, with a 3 dB bandwidth ranging from 20.3 to 24.1 GHz. The $|S_{11}|$ and $|S_{22}|$ are lower than 10 dB from 20.7 to 21.7 GHz and from 21.4 to 24.6 GHz, respectively. The $|S_{12}|$ is less than 19.5 dB over the whole band. The simulated results of *NF* and Rollet stability factor (k-Rollet) are shown in Figure 6b. The *NF* has a minimum value at 22.4 GHz and varies between 2.2 and 3.5 dB within the 3 dB bandwidth. Note the amplifier is unconditionally stable as long as the value of k-Rollet is above one. The layout of the proposed LNA is shown in Figure 7.

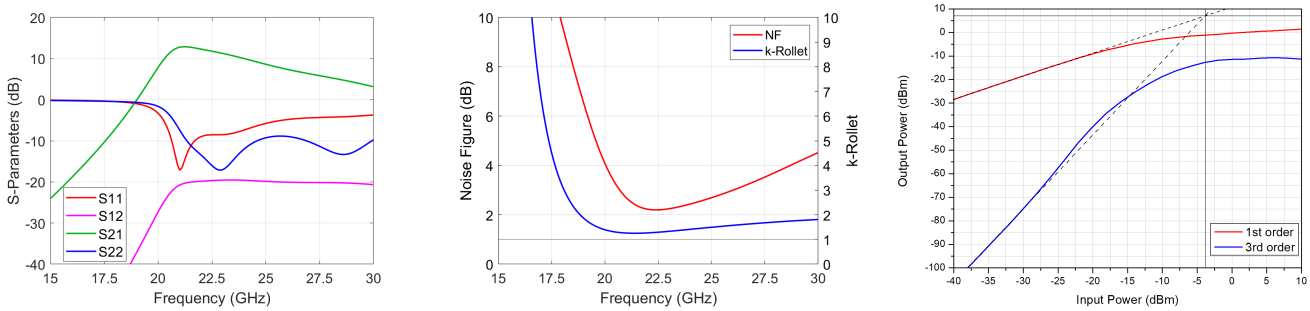


Figure 6. Simulated S-parameters (**a**) and *NF* and Rollet stability factor (**b**), and input and output third-order intercept of the developed LNA (**c**).

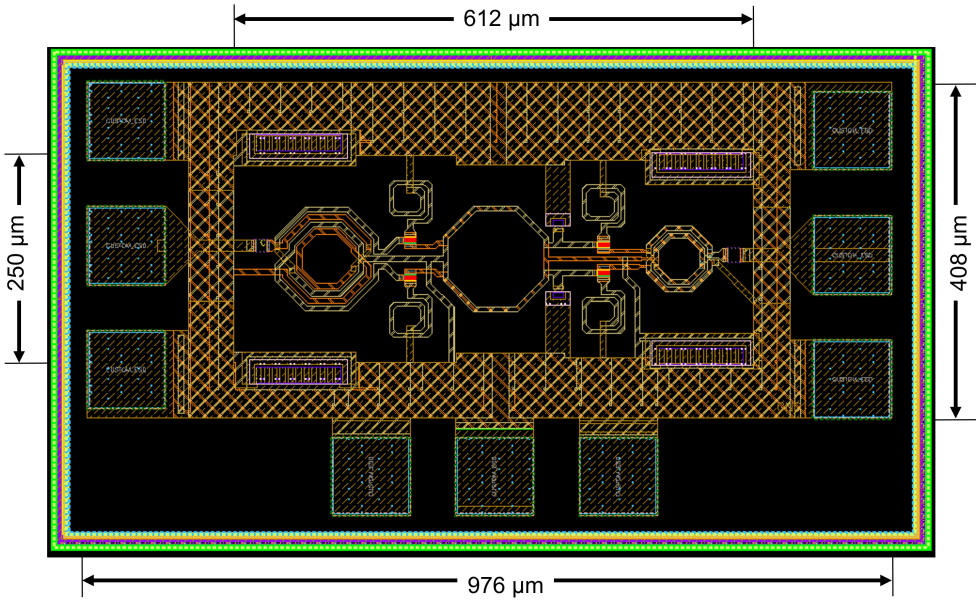


Figure 7. Layout of the proposed LNA.

The simulation results of the non-linearity analysis are shown in Figure 6c, concluding that the proposed LNA achieves a P_{o1dB} of −7.3 dBm, and an OIP3 of 7 dBm. To validate the results, a 250-occurrences Monte Carlo run is performed to determine if the performance meets the specifications under all conditions. The histograms containing the information of this analysis are presented in Figure 8a–d. As shown, the IRL (Figure 8a) is better than 8 dB and the ORL (Figure 8b) is better than 15 dB. The gain and *NF* of the LNA are depicted in Figure 8c,d, respectively, concluding the LNA achieves a gain above 11.5 dB and an *NF* of 2.2 dB at 22 GHz.

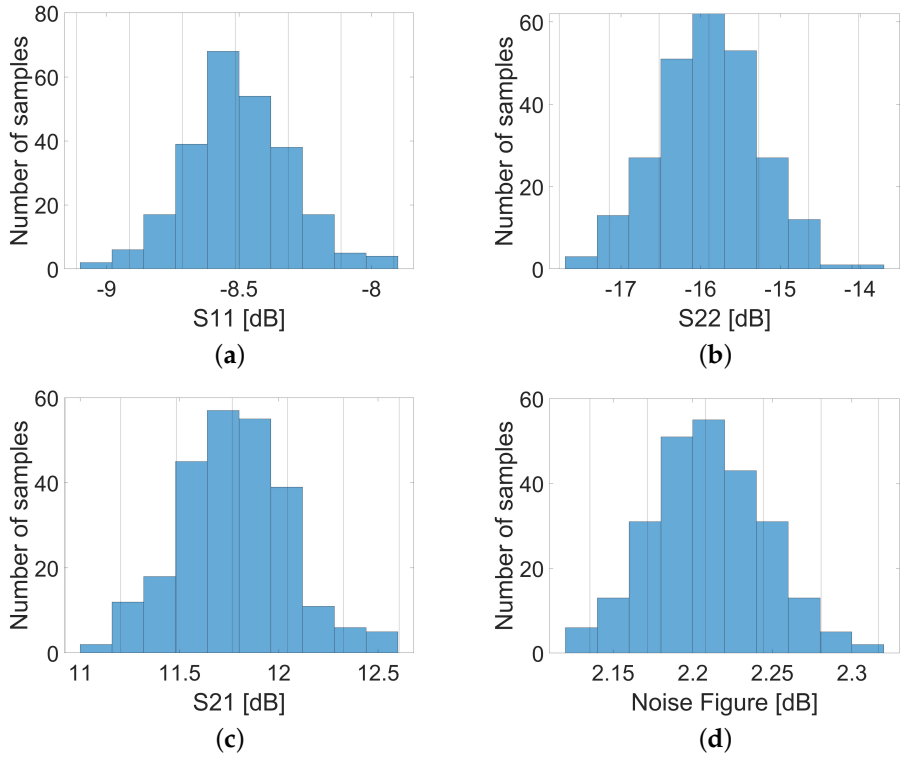


Figure 8. Monte Carlo analysis results of the IRL (**a**), ORL (**b**), gain (**c**), and *NF* (**d**) of the proposed LNA at 22 GHz.

The performance of the proposed LNA is compared with recent publications in Table 2, Refs. [7–10]. Only differential LNAs are considered. In order to provide a fair comparison with similar works, the figure of merit (*FoM*) defined in (4) is used in the table, where g is the linear gain of the LNA, BW is the bandwidth in Hz, F is the noise factor, P_{DC} represents the power consumption, and *area* is the total circuit area. A similar definition of this (*FoM*) can be found in [10,15,19].

$$FoM = \frac{g \cdot BW}{(F-1) \cdot P_{DC} \cdot area} \tag{4}$$

The work proposed in [7] demonstrates the design of a low-phase noise, source degenerated K-band cascode LNA with transformer-based matching networks and current steering to achieve a variable gain. The amplifier obtains a gain of 18.5 dB, with 4.1 dB *NF* and a 14.5 dBm OIP3. However, this high-performance circuit results in significant power consumption (67.2 mW from a 1.2 V DC power supply), which is reflected in the low value of the *FoM* (1.71). In [8] , the authors present a variable gain LNA as well, employing a split-common gate transistor technique in a two-stage cascode LNA. The authors report a very high gain of 25 dB and a low *NF* (3.4 dB) at 22 GHz, drawing 25.2 mW from a 1.2 V DC supply. Nevertheless, the LNA operates in a narrow bandwidth of 2 GHz. A very compact (0.11 mm^2) 45 nm RFSOI 28-GHz LNA is introduced in [9] , based on a source degenerated cascode with integrated baluns. The circuit achieves a gain of 9 dB, a *NF* of 3.1 dB, and very high linearity (IIP3 = 10 dBm), over a bandwidth of 4.5 GHz, with a total power consumption of 34 mW from a 1.8 V DC power supply. This performance trade-off results in a significant improvement of the *FoM* (9.63). Another 45 nm RFSOI LNA is introduced in [10] , based on a 3-stage cascode amplifier with baluns and switched capacitors to achieve multiband operation. The LNA presents a gain of 19.5 dB, a *NF* of 4.7 dB, but at the expense of a total power consumption of 59 mW and an area of 0.32 mm^2, thus lowering the value of the *FoM* obtained with this solution.

As shown in Table 2, the proposed LNA achieves the highest *FoM* value (14.5) of all the solutions considered, since circuit performance is a result of an excellent trade-off between the gain, BW, NF, P_{DC} and area. Note that the gain of other contributions is higher at the expense of a significant increase in power consumption. The developed LNA presents the lowest power consumption and *NF* reported in a differential LNA, to the best of the authors' knowledge. In fact, the power consumption in this work is less than half the one used in [8], which reports the lowest power consumption and highest gain of all the state-of-the-art solutions considered. In addition, we reported a very low *NF*, high gain, and high bandwidth in a very compact area.

Table 2. Performance comparison of the designed LNA with state-of-the-art differential LNAs.

Reference	**[7]**	**[8]**	**[9]**	**[10]**	**This Work ***
Technology	65 nm CMOS	65 nm CMOS	45 nm SOI	45 nm SOI	45 nm SOI
Topology	2-stage CAS	2-stage CAS CG	1-stage CAS	3-stage CAS	2-stage CS
BW_{3dB} [GHz]	4 (19–23)	2 (21–23)	4.5 (25.5–30)	8 (20–28)	3.8 (20.3–24.1)
Gain [dB]	18.5	25	9	19.5	12.9
NF [dB]	4.1	3.2	3.1	4.7	2.2
IIP3 [1] [dBm]	−4	-	10	-	−4
DC Supply [V]	1.2	1.2	1.8	1	0.38
Power [mW]	67.2	25.2	34	59	11.7
Area [mm^2]	0.19	0.2	0.11	0.32	0.15
FoM	1.71	6.48	9.63	3.26	14.5

[1] Input Third Order Intercept. * Post-layout simulation results.

5. Discussion

A fully differential LNA with transformer-based interstage matching networks for the K band in a 45 nm SOI process is presented. The methodology addresses the improvement of critical design trade-offs, allowing the design of a high-performance, low-power, and very compact LNA. This is accomplished thanks to the transformer-based matching network approach , which allows improved area use, as the transformers simultaneously act as RF chokes and as baluns at the input and output terminals to convert the SE signal into differential mode, and vice versa. In order to generate and equalize the desired transformer inductances a state-of-the-art tool was used following the proposal in [12]. In addition, a low-power LNA based on optimal current density selection is obtained, allowing the reduction of the nominal DC power supply from 0.9 V to 0.38 V, which results in a significant reduction in power consumption (which is more than halved). The circuit consumes a total power of 11.7 mW from a 0.38 V DC supply, and occupies an area of 0.15 mm^2 excluding pads. The LNA obtains a gain of 12.9 dB, a *NF* of 2.2 dB with an IRL higher than 10 dB. Non-linearity simulations show the proposed circuit achieves a P_{o1dB} of -7.3 dBm, and an OIP3 of 7 dBm. To validate the circuit, EM simulations, and Monte Carlo analysis results are presented as well. Compared to similar works available in the scientific literature, the results of the developed circuit achieve an excellent trade-off between gain, bandwidth, NF, power consumption, and area. In particular, the circuit presents a remarkably low power consumption and NF, obtaining the lowest values reported in a differential LNA compared to the state-of-the-art solutions. Although the reported results of our study demonstrate excellent performance there is room for further improvement. In this sense, future lines of work include the fabrication and measurement of the proposed circuit to validate the results, optimization of the second stage amplifier to improve gain and linearity, integration of the proposed LNA in a complete receiver or a real system, and improvement of the circuit PVT (Process–Voltage–Temperature) resilience.

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Abbreviations

The following abbreviations are used in this manuscript:

Balun	Balanced to Unbalanced
BW	Bandwidth
CAS	Cascode
CMOS	Complementary Metal Oxide Semiconductor
CMRR	Common Mode Rejection Ratio
CG	Common Gate
CS	Common Source
EM	Electromagnetic
FoM	Figure of Merit

G_{max}	Maximum Gain
IIP3	Input Third Order Intercept
IRL	Input Return Loss
LNA	Low Noise Amplifier
mm-Wave	Millimeter Wave
MW	Microwave
NF	Noise Figure
NF_{min}	Minimum Noise Figure
OIP3	Output Third Order Intercept
ORL	Output Return Loss
P_{o1dB}	Output 1-dB Compression Point
PVT	Process-Voltage-Temperature
Q	Quality Factor
RF	Radiofrequency
SE	Single Ended
SOI	Silicon on Insulator
SRF	Self Resonant Frequency

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CONCLUSIONS

3. Conclusions

The published works demonstrate a clear line of development in the design of high-performance low noise amplifiers, both in RF and MW frequencies. Although these two scenarios differ in their requirements, we adapted the topologies, techniques, and design procedures to achieve very competitive performance trade-offs.

On the one hand, we developed LNAs for WSNs and IoT devices using CCIIs to achieve wideband input matching without using any bulky passive components for this task, resulting in significant savings in area and, therefore, reducing the costs-per-node greatly. The proposed circuit achieves the lowest area reported in the scientific literature. Since WSNs benefit from low power and low-cost nodes, we identified this gap and produced numerous solutions to ensure a high performance with area and power savings. Following the CCII implementation we introduced a combination of the CCII topology with a noise canceling technique to further reduce the NF at the expense of a slightly higher power consumption added due to the NC path, achieving very promising results. We also studied wake-up receivers, which also contain LNAs with very restrictive power and performance constraints. After a conscientious and profound study of the state-of-the-art architectures and implementations, we decided to introduce an RFED tuned-RF topology with a feedback current reuse LNA to introduce sensitivity and power consumption improvements while reducing circuit area as well.

On the other hand, we moved to the implementation of LNAs for 5G networks and devices, which are key IoT enablers. We identified the K-band as a pioneer band defined for Europe, USA, Japan and Korea as a 5G potential frequency band. Therefore, the implementation of two single ended multistage LNAs with an ultra-low-NF were presented. We delve into the detailed design procedure to achieve ultra-low-NF behavior exploiting the design kit to the best performance possible. As a result, we report a 1.4-dB NF LNA in UMS GaAs and a sub-1-dB NF LNA using OMMICs D007IH process. The LNA proposed achieves the lowest NF reported in scientific literature. Furthermore, we

then move to a SOI process to introduce a fully differential low-voltage, low-power LNA using transformer based matching networks to provide an efficient and compact approach. The proposed fully differential LNA achieves the lowest NF and power consumption reported in the literature.

We detail the contributions, future lines of work and conclusions of each of the works presented in the following subsections.

3.1 A Compact Size Wideband RF-VGA Based on Second Generation Controlled Current Conveyors

The implementation and measurement results of a very compact, low power wideband RF-VGA are presented in this contribution. We discussed relevant design decisions and how different parameters affect circuit performance. The structure is based on the use of two CCII blocks, allowing an inductor-less approach that permits wideband behavior. The proposed RF-VGA is manufactured in a conventional SiGe BiCMOS 0.35 µm low-cost process. Gain settings allow 6.7–18 dB tuning by setting the value of the DC bias current of the circuit. For a biasing DC current I_{02} of 50 µA, the circuit draws 1.7 mA from a ±1.5 V DC supply. With these conditions, the RF-VGA presents IRL better than 20 dB from 0 to 10 GHz, a NF ranging from 5.5 dB (maximum gain) to 9.6 dB at (minimum gain). In addition, measured P_{1dB} is −20.2 dBm. The circuit obtains a remarkable and very competitive trade-off between gain, NF, IRL, power consumption, and area. The topology presented is very suitable for low-power, wide-band, compact and low-noise VGAs. Finally, to the best of the authors' knowledge, the circuit achieves the lowest chip size reported in the state-of-the-art.

Although the circuit shows a remarkable performance, there is room for further improvements. Some of the future lines of work derived from this proposal include the following:

- Introducing the manufactured prototype in a real WSN node to test the performance in a real-life scenario.
- Removing the external DC biasing current generation to use an on-chip dynamic gain regulation circuit.

- Applying the g_m/I_D methodology to further reduce power consumption and optimize the device performance, taking advantage of moderate inversion operation.
- Using a common-centroid layout to enhance PVT tolerances.

3.2 Miniature Wide-Band Noise-Cancelling CMOS LNA

In this publication, the implementation in a commercial 65nm CMOS process of a wideband noise canceling CCII-based LNA is demonstrated. The circuit achieves wideband input matching in an inductor-less approach thanks to the use of CCII, and a noise reduction is obtained by canceling the noise contributed by the input transistor at the output terminal using two CS transistors. Post-layout simulation results prove the proposed amplifier obtains a gain of 15.3 dB, a NF of only 3.2 dB and wide input impedance matching from DC to 6.2 GHz in a very compact area of 160 × 80 μm^2. The circuit obtains the largest bandwidth among all the solutions considered in the state-of-the-art. The CCNC LNA consumes 18.57 mW from a DC supply of ±1.2 V. Moreover, the proposed LNA enhances linearity as well, as it can partially cancel nonlinear distortions. The circuit obtains a very high IIP3 of 7.6 dB and an input P_{1dB} of –2 dBm. The only drawback is the additional power consumption required to bias the noise canceling path. Finally, the circuit presents the highest FoM of all the works available in literature.

Some future lines of work derived from this work include the following:

- The topology of the CCNC LNA can be moved to a higher frequency band to test if a high frequency LNA would benefit from CCII and NC techniques.
- Applying the g_m/I_D methodology to further reduce power consumption and optimize the device performance, taking advantage of moderate inversion operation. This would improve even further the FoM.
- The layout of the circuit would benefit from a common-centroid approach to relax PVT tolerances.

3.3 Area-Efficient Integrated Current-Reuse Feedback Amplifier for Wake-Up Receivers in Wireless Sensor Network Applications

In this paper, two ISM-band wake-up-receivers with an RFED tuned-RF topology are presented. The aim of these two circuits is to reduce the circuit area to ensure high integration and a lower cost-per-node. The proposed approach makes use of a feedback current-reuse approach, which results in a simpler implementation with a better performance. This is reflected in the achievement of a power consumption reduction by half and an increase in the circuit sensitivity from –63.2 dBm (circuit 1) to –75 dBm (circuit 2). Additionally, the circuits present a very low area, what makes them appropriate for high-integration and low-cost scenarios. On the one hand, the first circuit (circuit 1) proposed utilizes a feedback amplifier and a low-pass filter, reporting 6.77 µA current consumption and a size of 398 × 266 μm^2. The power consumption (of circuit 2) improves thanks to the current-reuse topology when compared to the first proposal, with 3.63 µA of current consumption, and also reduces the area to only 262 × 262 μm^2. This second implementation is perfectly suitable for fully integrated WuR designs, as it provides a very high sensitivity with low power consumption and area, which improves integrability with the rest of the components of a WSN node. It is worth noting that, in this work, an in-depth analysis of some of the most relevant state-of-the-art solutions is provided along with the available architectures for WuR design. Furthermore, the two proposed circuits are compared and placed in context by using two different FoMs, one focused on sensitivity and overall performance, and the other accounting for chip size as well. In conclusion, it is demonstrated that the feedback current-reuse proposal shows a higher performance than most of the approaches available in literature and obtains one of the most efficient trade-offs between area and performance of all the works considered.

Some future lines of work derived from this contribution include the following:

- The implementation of the operational amplifiers used in the filtering stage can be improved. Low power techniques such as g_m/I_D can be applied to reduce power consumption without significant performance degradation.
- Supply voltage reduction techniques can lead to lower power consumption as well.

- The layout of the circuit would benefit from a common-centroid approach to relax PVT tolerances too.

3.4 A 2-V 1.4-dB NF GaAs MMIC LNA for K-band Applications

A four-stage GaAs LNA in a 100nm pHEMT process for K-band applications is presented in this article. The circuit operates in the n258 frequency band, from 24.25 to 27.58 GHz, and it obtains a very high gain of 34 dB and an ultra-low noise figure of 1.3 dB. In addition, the circuit achieves an IRL of –10 dB, a P_{1dB} of –18 dBm and an OIP3 of 24.5 dBm when it is fed from a 2 V DC supply, drawing a total current of 59.1 mA. The complete circuit occupies 3300 × 1800 μm^2 including pads. To validate the results obtained with this implementation EM and Monte Carlo simulations at room temperature are presented in this work. To reach the desired ultra-low NF, we provide a design methodology centered on careful device sizing, selection of the adequate DC bias conditions and source and load impedances that permit efficient impedance matching and the obtention of the lowest NF possible. The design method explains how to select the device size paying close attention to the value of the real part of S_{opt}, so that the input matching network simplifies to a single inductance and the minimum NF can be obtained. With this solution, the input matching network is simplified and introduces minimal loss. Finally, a comparison with similar works available in literature demonstrates the circuit achieves a very competitive performance with the rest of the state-of-the-art circuits.

Some future lines of work derived from this article include the following:

- Instead of using a conventional CS with source degeneration, many strategies can be followed to move from a narrowband LNA to a wideband response, such as frequency staggering, RC-feedback or using a wideband LRC tank.
- Dynamic biasing techniques could also be employed to ensure a stable DC biasing, or a self-biasing approach could be added to give the circuit an added value.
- A custom input matching inductor can be used to further reduce the NF and improve the performance of the circuit.

3.5 A 1.2-V GaAs MMIC Ultra-Low Noise Amplifier for K-band Applications

The design flow presented in the previous work is used in this work with a high-performance PDK to lower the NF of the GaAs LNA from 1.4 to 1 dB. The design of two simple amplifiers is shown to give the reader valuable insights on the differences between a conventional design approach and the proposed minimum NF procedure. A four-stage LNA for K-band applications is then presented in a 70nm GaAs mHEMT process from OMMIC following the previously introduced method. To further reduce the circuit NF a full-custom single tapered octagonal inductor is used in the input matching network. The inductor layout improves current circulation and, therefore, boosts the Q-factor to lower the loss introduced by this element. The LNA is biased with a DC supply of 1.2 V and has a total area of (2500 µm × 1750 µm). To validate the results, EM simulations at room temperature are carried out, showing a gain of 29.5 dB with a ripple of 1 dB, a NF of only 1 dB, an IRL above 10 dB and an ORL above –20 dB. To the best of the author's knowledge, this LNA achieves the lowest NF reported of all the GaAs LNAs identified in literature.

Some of the future lines of work derived from this work include the following:

- The future lines of work included in the previous design can also be applied to this design.
- The circuit could be moved to a SOI technology node to reduce costs without significant performance degradation.
- A self-biased approach can be used to eliminate the need for external DC bias voltages for the gate of the transistors.

3.6 A g_m/I_D-based Low Power LNA for Ka-band Applications

A SOI version of the previous LNA using the g_m/I_D methodology is presented in this work. A combined methodology for high-frequency LNA designs is proposed, demonstrating a very low-power, high performance Ka-band LNA. The approach leads to a significant power consumption reduction in exchange for a slightly lower gain and higher NF, but a greater FoM is obtained. The g_m/I_D methodology is combined with high frequency performance metrics, such as f_T, NF and gain to adapt the g_m/I_D to RF/MW

environments providing an intuitive and straight forward procedure that yields an increased FoM. The design procedure can be summarized as follows: device performance is studied, and a database is built based on simulations of key performance metrics, so that the designer needs to run the simulations once, which then can be used to analyze and design other circuits at the same frequency. Given the topology of the circuit and the background equations, the designer can obtain one or many versions of the circuit and select the one that better suits a certain specification.

To provide a solid background, three different inversion coefficients are chosen and developed in the schematic design phase. The advantages and disadvantages of each version are analyzed to select the most efficient one and carry on the layout of the selected version. The developed g_m/I_D LNA achieves a power consumption of only 1.98 mW from a DC supply of 0.9 V. With these DC biasing conditions, the LNA obtains a gain above 11 dB, a NF of 3.8 dB and, IRL and ORL better than 10 dB. Comparisons with similar works available in literature demonstrate the proposed LNA achieves the lowest power consumption and best performance trade-off of all the solutions studied in the state-of-the-art.

Some of the future lines of work derived from this work include the following:

- Apart from the future lines provided for the 0.9 V Ka-band cascode LNA presented in the previous section, this circuit would benefit from further and deeper development of the application of the g_m/I_D methodology. We believe the LNA design procedure can be enhanced further.
- Since the g_m/I_D methodology has been applied successfully to the LNA design, we propose adapting this procedure in other LNA topologies and circuits such as PAs, HPAs, mixers and phase shifters, which would benefit greatly of the advantages of using all inversion regions.

3.7 A 0.38 V Fully Differential K-band LNA with Transformer-Based Matching Networks

In this work, a K-band fully differential LNA with a DC supply of 0.38 V and transformer-based matching networks is presented in a GF 45nm SOI process. The design procedure and the selected topology allow the obtention of a very low-NF, low-power, and compact LNA. The circuit area benefits from the use of transformer based matching

networks, which can be efficiently used for multiple tasks: single-ended to differential conversion and vice versa, DC biasing of each node without RF Chokes, efficient impedance conversion for impedance matching and AC coupling with galvanic isolation between stages. Note the transformer allows inductor stacking, which means gate and drain inductors can be implemented in the same area. To obtain the parameters of the required transformers, a state-of-the-art tool was replicated in a MATLAB script that generates the required inductances for a given coupling factor and frequency. Moreover, to reduce the power consumption of the circuit, we select the optimal current density and then reduce the DC supply voltage from 0.9 to 0.38 V while keeping the desired current. Since the power consumption is the product of the DC current and the supply voltage, power consumption is reduced by the same factor the DC voltage is decreased. The circuit obtains the lowest power consumption reported in literature, to the best of the author's knowledge. The two-stage LNA draws a power of 11.7 mW from a 0.38 V DC supply and obtains a total area of 0.15 mm^2 excluding pads. The circuit is validated through EM analysis and Monte Carlo simulation, achieving a 12.9 dB gain, the lowest NF reported in literature in a fully differential LNA at K-band frequencies, to the best of the author's knowledge, with a value of 2.2 dB. The IRL is better than 10 dB, and non-linearity simulations demonstrate an output P_{1dB} of −7.3 dBm, and an OIP3 of 7 dBm. In comparison with similar works available in literature, the proposed circuit reports the lowest NF and power consumption in a fully differential K-band LNA, and an excellent compromise between gain, NF, bandwidth, linearity, power consumption and area is reached.

Although the proposed circuit shows remarkable results, there is room for further development. Some future lines of work include the fabrication and measurement of the proposed LNA to verify simulation results, performing optimization of the second stage to enhance gain and linearity simultaneously, integration of the circuit in a real receiver, and studying and enhancing PVT (Process–Voltage–Temperature) resilience. Also, the LNA could benefit from the g_m/I_D methodology to further reduce power consumption with small sacrifices in performance.

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APPENDICES

References

Appendix 1 – Resumen Completo de la Tesis en Español

Amplificadores de Bajo Ruido (LNAs)

RFIC/MMIC para Comunicaciones Inalámbricas

por

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Introducción

Las necesidades de los usuarios de dispositivos electrónicos comerciales y de las aplicaciones finales tales como las Redes Inalámbricas de Sensores (WSN), las tecnologías 5G (*5th Generation*) o el Internet de las Cosas (IoT) son cada vez más exigentes. Tanto es así que los diseñadores de circuitos integrados se ven obligados a explorar topologías, técnicas y procedimientos de diseño alternativos para poder cumplir con las rigurosas restricciones de latencia, tasa de datos, consumo de energía, ganancia, ruido y área. Esta tesis aborda estos problemas para el ámbito del diseño de circuitos de Radiofrecuencia (RF) y Microondas (*Microwave* o MW) en tecnologías *Complementary Metal-Oxide Semiconductor* (CMOS), *Silicon-On-Insulator* (SOI) y compuestos III-V. Las principales contribuciones se centran en el desarrollo de técnicas de reducción de área, mejora de las prestaciones y compromisos de diseño de los amplificadores de bajo ruido (*Low Noise Amplifier* o LNA) para sistemas de comunicación inalámbrica de última generación de RF y MW en tecnologías CMOS, SOI y III-V. La tesis tiene como objetivo aportar técnicas innovadoras, combinaciones de técnicas y procedimientos de diseño para mejorar el rendimiento de los LNAs actuales, reducir el área y el consumo de energía, y optimizar los compromisos de diseño relacionados con los circuitos integrados de alta frecuencia (entre ruido, linealidad, ganancia, consumo, adaptación de impedancias, tensión de alimentación, velocidad…).

La hipótesis fundamental para el desarrollo de la disertación propuesta consiste en que es posible mejorar sustancialmente el rendimiento de los LNAs identificados en el estado del arte tanto en bandas de RF como de MW. Se comienza por estudiar el diseño

de LNAs en tecnologías CMOS y BiCMOS para aplicaciones de WSN de RF y posteriormente en tecnologías SOI y III-V para escenarios de MW de alta frecuencia. Por un lado, superar las limitaciones actuales y aprovechar el rendimiento de las implementaciones de LNA en tecnologías basadas en silicio es de vital importancia para facilitar su integración, reducción de costes y accesibilidad en un rango más amplio de aplicaciones. Por otro lado, el desarrollo de LNAs en tecnologías III-V y SOI es particularmente interesante debido a sus aplicaciones en múltiples sectores de alto valor, como el despliegue de estaciones base 5G, espectroscopía, comunicaciones satelitales, aplicaciones militares y de defensa. De manera similar, los procesos SOI proporcionan una solución intermedia entre los circuitos CMOS y los compuestos III-V en términos de costes de fabricación y rendimiento. Los circuitos CMOS tienen un precio por área más bajo que las tecnologías SOI, y los circuitos SOI tienen un precio por área más bajo que los chips de compuestos III-V.

Objetivos

El objetivo principal de esta tesis consiste en estudiar técnicas de diseño que puedan mejorar el rendimiento de los LNAs en sistemas actuales de comunicación inalámbrica. En particular, las contribuciones se centran en mejorar parámetros como las pérdidas de retorno por adaptación de impedancias, el consumo de energía, el área, la linealidad, la ganancia y la Figura de Ruido (NF). El propósito de este estudio es facilitar la implementación de estos circuitos y realizar una contribución significativa al estado del arte. Los objetivos específicos son los siguientes:

- Estudiar las principales soluciones y técnicas de diseño de los LNAs del estado del arte. Para hacer contribuciones relevantes primero es necesario realizar una profunda revisión de las publicaciones recientes y de las técnicas más novedosas y con más presencia en el área.

- Identificar y analizar las principales limitaciones y compromisos de las técnicas de diseño de LNAs actuales. Una vez realizado el estudio del estado del arte, se trata de identificar fortalezas y debilidades, así como oportunidades de mejora en el proceso de diseño de LNAs.

- Conducir tests y simulaciones con las técnicas estudiadas en diseños de LNAs. Este objetivo se subdivide, por un lado, en la aplicación de técnicas en escenarios de RF y, por otro, en el dominio de bandas de frecuencia de MW.

- Explotación y diseminación de los resultados obtenidos. Cumpliendo con los requisitos del Programa de Doctorado en Tecnologías de Telecomunicación e Ingeniería Computacional (T2IC), uno de los objetivos fundamentales consiste en la presentación de artículos científicos de alto impacto en revistas especializadas, así como la diseminación de conocimiento realizando ponencias en congresos internacionales.

Considerando la discusión anterior, la tesis doctoral puede ser resumida de la siguiente forma. Las contribuciones se dividen en dos categorías: LNAs de radiofrecuencia y LNAs de microondas. En primer lugar, se desarrollan numerosos LNAs para WSNs, centrando la atención en la reducción de área, la disminución de costes por nodo y la reducción del consumo de energía sin penalizaciones significativas en el rendimiento. Se desarrolla un Amplificador de Ganancia Variable de RF (RF-VGA) de banda ancha muy compacto, de bajo consumo, y baja tensión basado en silicio-germanio (SiGe) BiCMOS (Bipolar-CMOS) que presenta el área más baja de los trabajos publicados hasta la fecha. A continuación, se introducen mejoras en los LNAs utilizados en Receptores de Activación (*Wake-Up Receivers* o WuRs), presentando una topología *tuned-RF* muy compacta, de bajo consumo y bajo coste. Finalmente, se propone un LNA CMOS de banda ancha sin inductores y con cancelación de ruido basado en convertidores de corriente. El circuito logra una linealidad notable, un área muy compacta y una elevada Figura de Mérito (FoM) en comparación con contribuciones similares del estado del arte.

El esfuerzo se centra después en el diseño de LNAs para frecuencias de MW. En estos trabajos, se comienza por el diseño de LNAs con una NF inferior a 1.4 dB utilizando GaAs. Para lograr este desafío, se explora primero el diseño de un LNA con compuestos III-V comerciales para alcanzar un NF inferior a 1.4 dB, introduciendo un procedimiento de diseño eficiente para lograr una NF ultra baja. Posteriormente, el mismo LNA se traslada a un Kit de Diseño (PDK) de OMMIC de altas prestaciones para lograr un LNA con una NF inferior a 1 dB. Dado que los compuestos III-V presentan un costo muy alto por área, se traslada el LNA de 1.4 dB NF de GaAs a un kit GlobalFoundries (GF) SOI. Se demuestra un prototipo de un LNA en cascodo con una NF de 1.6 dB en un PDK más asequible. A continuación, se exploran técnicas de reducción de consumo para mantener el rendimiento logrado, pero mejorando el consumo de energía. A partir de esta decisión, surgen dos líneas. Por un lado, se demuestra un LNA 45RFSOI diseñado con g_m/I_D alimentado a 0.9 V. Por otro, el estudio del estado del arte sugiere un interés especial en los circuitos totalmente diferenciales a medida que aumenta la frecuencia de operación, por lo que se decide pasar a un LNA totalmente diferencial de ultra bajo consumo. También se introducen redes de adaptación basadas en transformadores para mejorar significativamente el área del circuito.

A continuación, se desglosan las contribuciones realizadas detallando el trabajo realizado en cada publicación.

A Compact Size Wideband RF-VGA Based on Second Generation Controlled Current Conveyors

El trabajo a frecuencias de RF, que se centra en LNAs para nodos de WSNs, resulta en el diseño, fabricación y medida de un RF-VGA basado en Convertidores de Corriente Controlados de Segunda Generación (CCII). Gracias al uso de CCIIs, se logra una respuesta de banda ancha en un circuito sin bobinas, que resulta en la huella de chip más pequeña de todas las soluciones disponibles en la literatura. Además, debido a la

naturaleza de los CCIIs utilizados, cuanto mayor es la ganancia, menor es el consumo de potencia del circuito. El RF-VGA propuesto se implementa en un proceso SiGe BiCMOS de bajo coste de 0.35 µm de longitud de puerta. La ganancia del RF-VGA se puede ajustar entre 6.7 y 18 dB configurando la corriente de polarización en continua del circuito. A su vez, bajo el conocimiento de los autores, el circuito logra el tamaño de chip más reducido de todas las propuestas identificadas en la literatura científica. Para una corriente de polarización I02 de 50 µA, el circuito consume 1.7 mA de una fuente de alimentación de ±1.5 V DC. Con estas condiciones, el RF-VGA presenta unas Pérdidas de Retorno a la Entrada (IRL) mejores que 20 dB desde DC hasta 10 GHz y una NF que varía desde 5.5 dB (en ganancia máxima) hasta 9.6 dB (en ganancia mínima). Además, el Punto de Compresión a 1-dB (P_{1dB}) medido es de –20.2 dBm. El circuito propuesto logra un compromiso notable y muy competitivo entre ganancia, NF, IRL, consumo de energía y área. La topología presentada es particularmente adecuada para amplificadores de ganancia variable muy compactos, de banda ancha, bajo consumo y bajo ruido.

Miniature Wide-Band Noise-Canceling CMOS LNA

La técnica de Cancelación de Ruido (NC) se explota en una segunda versión del amplificador presentado en la contribución anterior para reducir aún más la NF del circuito (en más de 1.5 dB) y mejorar la linealidad, obteniendo un Punto de Intercepción de Tercer Orden (IIP3) de 7.6 dBm. En este trabajo se demuestra la implementación en un proceso CMOS comercial de 65 nm de un LNA con cancelación de ruido de banda ancha basado en CCII. En línea con la propuesta anterior, se logra una adaptación de entrada de banda ancha en una topología sin bobinas, y se obtiene una reducción de ruido significativa al cancelar la contribución del ruido del transistor de entrada utilizando dos amplificadores en *common-source*. Los resultados de simulación *post-layout* del circuito demuestran que el amplificador propuesto logra una ganancia de 15.3 dB, una NF de solo 3.2 dB y una adaptación de impedancias de entrada desde DC hasta 6.2 GHz, en un área extremadamente compacta (160 × 80 μm^2). Bajo el conocimiento del autor, el circuito obtiene el ancho de banda más elevado de entre todas las soluciones consideradas en el estado del arte. Asimismo, el LNA consume 18.57 mW de una fuente de alimentación de ±1.2 V. A su vez, el LNA propuesto mejora la linealidad final frente a la propuesta anterior, ya que puede cancelar parte de las distorsiones no lineales. El circuito obtiene un destacado IIP3 de 7.6 dBm y un P_{1dB} de entrada de –2 dBm. La única desventaja que presenta la solución es el consumo de energía adicional necesario para polarizar la ruta de cancelación de ruido. Finalmente, la comparativa con el estado del arte revela que el circuito logra la mayor figura de mérito de todas las soluciones disponibles.

Area-Efficient Integrated Current-Reuse Feedback Amplifier for Wake-Up Receivers in Wireless Sensor Network Applications

Continuando con el desarrollo de LNAs para RF, en este trabajo se introduce un amplificador realimentado con reutilización de corriente para un receptor *wake-up* con el que se demuestra una mejora de la sensibilidad de –63.2 dBm a –75 dBm y una reducción

de área de 36,800 μm^2 a solo 700 μm^2. Igualmente, se demuestra una reducción del consumo de potencia a la mitad, con un total de 3.63 µA. En este artículo se estudian dos circuitos para proponer una técnica de reutilización de corriente con realimentación, lo que resulta en una implementación más simple y unas prestaciones mejoradas. Además, los amplificadores presentan un área muy reducida, lo que los hace adecuados para escenarios y aplicaciones que requieren una elevada capacidad de integración y muy bajo coste. Por su parte, el primer circuito propuesto utiliza un amplificador realimentado y un filtro paso bajo, con un consumo de potencia total de 6.77 µA y un área de 398 × 266 µm². El segundo circuito, que introduce la técnica de reutilización de corriente, mejora el consumo de energía en comparación con el anterior, resultando en 3.63 µA, y consigue reducir el área a solo 262 × 262 µm² al simplificar la topología del amplificador. Esta segunda implementación es muy adecuada para diseños totalmente integrados de receptores de *wake-up*, ya que proporciona una sensibilidad muy alta con bajo consumo y un área muy reducida, lo que mejora la capacidad de integrar el amplificador en un sistema completo con el resto de los componentes de un nodo de WSNs. En este trabajo también se presenta un profundo análisis de las soluciones más relevantes en el estado del arte, junto con las arquitecturas disponibles a la hora de implementar receptores *wake-up*. Asimismo, se comparan los dos circuitos propuestos y se sitúan en contexto mediante el uso de dos FoMs diferentes, una centrada en la sensibilidad y las prestaciones en general, y otra que también incluye el área del circuito. Se demuestra que la propuesta de reutilización de corriente con realimentación es superior a la mayoría de los enfoques disponibles en la literatura y obtiene uno de los mejores compromisos entre área y prestaciones de todas las obras consideradas.

A 2-V 1.4-dB NF GaAs MMIC LNA for K-Band Applications

Las contribuciones al diseño de LNAs para 5G en banda K, Ku y Ka se centran en implementaciones basadas en tecnologías GaAs y SOI para lograr una NF ultra reducida, explorando los límites de los PDKs empleados.

La principal contribución de este trabajo incluye un procedimiento de diseño completo para obtener un LNA con una NF por debajo de 1.4 dB. En este trabajo se presenta un LNA de cuatro etapas para alcanzar una ganancia de 34 dBs, implementado en un proceso GaAs pHEMT de 100 nm de UMS. El circuito propuesto opera en la banda n258, desde 24.25 hasta 27.58 GHz, logrando una NF mínima de 1.3 dB. Además, el circuito logra un IRL de 10 dB, un P_{1dB} de –18 dBm y un Punto de Intercepción de Tercer Orden de Salida (OIP3) de 24.5 dBm cuando se alimenta a 2 V, consumiendo una corriente total de 59.1 mA. Asimismo, el circuito completo ocupa 3300 × 1800 µm², incluyendo los pads. Para validar los resultados obtenidos con esta implementación, se presentan simulaciones electromagnéticas y de Monte Carlo a temperatura ambiente para considerar las variaciones debidas al proceso de fabricación. Para alcanzar una NF ultra reducida se proporciona una metodología de diseño completa. Se estudia el dimensionamiento de los transistores, la selección de las condiciones adecuadas de polarización, la selección óptima de las impedancias de fuente y carga que permitan una

adaptación de impedancias eficiente y el diseño de las redes de alimentación de cada etapa. El método de diseño presenta cómo seleccionar el tamaño del dispositivo prestando especial atención al valor de la parte real de S_{opt} (impedancia óptima para mínimo ruido), de modo que la red de adaptación de entrada se simplifica a una sola bobina. Dado que se minimiza la contribución de la red de adaptación de entrada al ruido del LNA, se puede obtener una NF lo más reducida posible. Finalmente, la comparativa con trabajos similares disponibles en la literatura científica demuestra que el circuito logra un rendimiento muy competitivo con el resto de los circuitos de última generación.

A 1.2-V GaAs MMIC Ultra-Low-Noise Amplifier for K-band Applications

El trabajo a frecuencias de MW continúa con una reducción de la NF de los LNAs en banda K, tratando de superar la barrera de 1 dB de NF. Como resultado, se logra diseñar un LNA en GaAs con una NF inferior a 1 dB en tecnología de 70 nm de OMMIC. El flujo de diseño presentado en el trabajo anterior se utiliza en este trabajo con un PDK de altas prestaciones para reducir la NF del LNA en GaAs de 1.4 dB a 1 dB. Primero, se muestra el diseño de dos amplificadores simples para proporcionar al lector información valiosa sobre las diferencias entre un procedimiento de diseño convencional y el método propuesto para una NF mínima. Posteriormente, se desarrolla un LNA de cuatro etapas para aplicaciones en banda K, siguiendo el método introducido. Para reducir aún más la NF del circuito, en la red de adaptación de entrada se utiliza una sola bobina octagonal de anchura variable (*tapered*) cuyo *layout* se realiza totalmente a medida. El diseño de la bobina mejora la circulación de corriente y, por lo tanto, aumenta su Factor de Calidad (Q) para reducir las pérdidas que introduce este elemento. El LNA resultante se polariza con 1.2 V de continua y tiene un área total de 2500 µm × 1750 µm. Para validar los resultados, se realizan simulaciones electromagnéticas a temperatura ambiente, mostrando una ganancia de 29.5 dB con una variación de 1 dB, una NF de tan solo 1 dB, un IRL superior a 10 dB y un ORL por encima de 20 dB. Según el conocimiento del autor, este LNA logra la menor NF de todos los LNAs de GaAs identificados en la literatura.

A g_m/I_D-based Low-Power LNA for Ka-band Applications

El estudio de LNAs de altas prestaciones a frecuencias de MW se traslada de compuestos III-V a una tecnología SOI para reducir costes, área y consumo de potencia. Además, para reducir aún más el consumo y aprovechar la eficiencia de los MOSFET, se explora la aplicación de la metodología g_m/I_D en un LNA en configuracióncascodo. El circuito propuesto logra el mejor compromiso de prestaciones de todos los LNAs presentes en la literatura. De hecho, la metodología se combina con las propuestas anteriores para ofrecer un procedimiento de diseño que permite obtener LNAs de MW de altas prestaciones con un menor consumo. Se consigue demonstrar un LNA en banda K con un consumo por debajo de los 2 mW, ofreciendo más de 10 dB de ganancia y menos de 4 dB de NF. El método empleado conduce a una reducción significativa del consumo de potencia a cambio de una ganancia ligeramente menor y una NF más alta, pero se obtiene una mayor figura de mérito. La metodología g_m/I_D se combina con métricas de

rendimiento de alta frecuencia, como la f_T, la NF y la ganancia, para adaptar el método g_m/I_D a entornos de RF/MW, proporcionando un procedimiento intuitivo y directo que resulta en un rendimiento mejorado. El procedimiento se puede resumir de la siguiente manera: acorde con los principios de la metodología g_m/I_D, se estudia el rendimiento del dispositivo y se construye una base de datos con una caracterización completa de los transistores, de modo que el diseñador solo necesita ejecutar las simulaciones una vez, lo que luego se puede utilizar para analizar y diseñar otros circuitos a la misma frecuencia. Dada la topología del circuito y las ecuaciones características, el diseñador puede obtener una o varias versiones del circuito para explorar el espacio de diseño, o ir a unas especificaciones determinadas y seleccionar la opción que mejor se adapte a sus necesidades. Para demostrar la efectividad y el potencial de la metodología, se eligen y desarrollan tres coeficientes de inversión diferentes en la fase de diseño sobre esquemático. Se analizan las ventajas y desventajas de cada versión para seleccionar la más eficiente y continuar con la implementación de la mejor solución. El LNA desarrollado con la metodología g_m/I_D logra un consumo de energía de tan solo 1.98 mW a partir de una alimentación de 0.9 V. Con estas condiciones de polarización, el LNA obtiene una ganancia superior a 11 dB, una NF de 3.8 dB y unas pérdidas IRL y ORL superiores a 10 dB. Comparaciones con trabajos similares disponibles en la literatura demuestran que el LNA propuesto logra el menor consumo de energía y el mejor compromiso de prestaciones de todas las soluciones estudiadas en el estado del arte.

0.38 V Fully Differential Multistage K-band LNA with Transformer-Based Matching Networks

Finalmente, se demuestra un LNA diferencial en tecnología SOI de 45 nm con una tensión de alimentación de 0.38 V utilizando redes de adaptación basadas en transformadores. El procedimiento de diseño y la topología seleccionada permiten obtener un LNA con una NF muy reducida, bajo consumo de energía y un área compacta. A diferencia del circuito anterior, en este LNA en lugar de reducir la densidad de corriente, se reduce la tensión de alimentación para reducir el consumo. A su vez, el área del circuito se beneficia del uso de redes de adaptación basadas en transformadores, que pueden utilizarse eficientemente para múltiples tareas: conversión de modo asimétrico a diferencial y viceversa, polarización de continua de cada etapa, conversión eficiente de impedancias para realizar la adaptación entre etapas y acoplamiento en corriente alterna con aislamiento galvánico entre etapas. Cabe destacar que el transformador permite el apilamiento de inductancias, es decir, que las inductancias de puerta y drenador pueden implementarse en la misma área que se emplearía para una sola bobina. Además, para obtener los parámetros de los transformadores requeridos, se replicó una herramienta del estado del arte en un script de MATLAB que genera las inductancias necesarias para un factor de acoplamiento y frecuencia de trabajo dados. Para reducir el consumo de potencia del circuito, se selecciona la densidad de corriente óptima y luego se reduce la tensión de alimentación de 0.9 a 0.38 V manteniendo la corriente deseada. Dado que el consumo de energía es el producto de la corriente y la tensión de continua, el consumo se reduce en el mismo factor por el cual se disminuye la tensión de alimentación. El LNA de dos etapas

consume 11.7 mW para una fuente de 0.38 V y obtiene un área total de 0.15 mm^2 excluyendo los pads. El circuito se valida mediante análisis electromagnético y simulación de Monte Carlo, logrando una ganancia de 12.9 dB y la menor NF de la literatura en un LNA completamente diferencial en frecuencias de banda K, según el conocimiento del autor, con un valor de 2.2 dB. Las pérdidas de retorno son mejores de 10 dB, y las simulaciones de linealidad demuestran un P_{1dB} de –7.3 dBm y un OIP3 de 7 dBm. En comparación con trabajos similares disponibles en la literatura, el circuito propuesto demuestra la menor NF y el menor consumo de energía en un LNA completamente diferencial en la banda K, y se alcanza un excelente compromiso entre ganancia, ancho de banda, NF, consumo de energía, linealidad y área.

Las obras publicadas demuestran una clara línea de desarrollo en el diseño de amplificadores de bajo ruido de altas prestaciones, tanto en frecuencias de RF como en MW. Aunque estos dos escenarios difieren en sus requisitos, adaptamos las topologías, técnicas y procedimientos de diseño a las particularidades de cada escenario para lograr compromisos de prestaciones muy competitivos y mejorar los resultados del estado del arte.

Appendix 2 – A 0.9-V 3.0-dB NF Cascode LNA for Ku-band Applications in CMOS SOI

In this Appendix, a summary of a recent work developed in line with this PhD thesis as part of the study of MW frequency SOI LNAs is presented. In this sense, the following paper has been submitted to the journal TCAS II:

- **D. Galante-Sempere**, S. L. Khemchandani, and J. del Pino, "A 0.9-V 3.0-dB NF Cascode LNA for Ku-band Applications in CMOS SOI," Transactions on Circuits And Systems II: Express Briefs, submitted Apr. **2024**.

The design of a Ku-band low-power cascode LNA operating with a 0.9 V DC power supply is presented in this section. The circuit is implemented in the 45nm SOI (45RFSOI) process from Global Foundries (GF) using a floating-body FET. The manufacturing costs of this circuit were sponsored by the GF University Partner Program, and we would like to specially thank Mr. Ned Cahoon and Mr. Nogel Stoneman for their support in the development of this circuit.

In this thesis, the work on MW frequencies results in ultra-low-NF LNAs which were developed using III-V compounds. First in a conventional UMS GaAs process and then in a high-performance OMMIC GaAs process. However, here the focus is moved from III-V compounds to a SOI technology, and from a multistage topology to a single-stage cascode to demonstrate measurement results of a 3.0-dB NF LNA with a significant reduction in power and aera. Since III-V compounds price-per-area is significantly higher than bulk-CMOS and SOI technologies, the obtention of a SOI LNA with comparable performance is particularly interesting to reduce manufacturing costs. Furthermore, instead of using a multistage approach, the topology is modified into a single stage cascode LNA to ensure a reasonable power consumption with a very high gain. In this manner, one can increase the number of stages to increase the gain further as desired with very little impact in the NF of the overall amplifier at the expense of a higher power

consumption and chip area. The LNA is a fundamental component of the wireless receivers, and it dominates its overall NF. In the scientific literature, cutting edge Ku-band LNAs report a NF as low as 1.4 dB with a power consumption of ~10 mW and 10-dB gain [35]. Note that in phased-array systems, the LNA gain should be above 10 dB in order to maintain a low overall NF, because the phase shifter generally presents an NF as high as 10-16 dB [36].

The design procedure is divided into the following stages. First, the circuit schematic is presented along with an overview of the main performance metrics of the active devices available in the selected PDK. A deep study of the transistors' characterization and performance is shown to give the reader valuable insights in transistor selection. The results of different combinations of floating body devices in a cascode LNA are studied from 10 to 20 GHz to identify the optimal choice. Then, the cascode layout is developed to account for device geometry and losses due to metal interconnections and parasitic resistance, capacitance, and inductance at an early stage. The performance of the gate inductor, which is critical for LNA performance, is studied in detail. We focus on the most relevant aspects of laying out a LNA for mmWave frequencies [36]. After the obtention of the complete layout of the LNA, an EM simulation of all the passive components is presented to account for deviations due to parasitic inductance and EM interactions. At this point, measurement results of the manufactured chips are introduced along with a comparative with similar works available in the literature. We provide S-parameter data, NF measurements and linearity results for the proposed LNA, demonstrating an IIP3 of 5 dBm, an minimum NF of 3.0 dB and a maximum gain of 12.9 dB at 20 GHz for a power consumption of 9 mW from a 0.9 V DC supply.

Conclusions

The design and measurement results of a 0.9 V Ku-band cascode LNA are reported in this chapter. The proposed circuit is developed as part of GF University Partner Program, which covers the manufacturing costs of the circuit. The LNA achieves a comparable performance to the previously developed UMS GaAs LNA with significant power consumption and area savings. We demonstrate the feasibility of achieving a 2.9-dB-NF LNA in 45RFSOI technology with a gain as high as 12.9 dB in a single stage cascode approach. The measurement reports demonstrate the LNA operates in the 28 GHz frequency band reaching a NF of 2.9 dB, IRL and ORL better than 10 across the band and

an IIP3 of 5 dBm. The circuit occupies 0.14 mm^2 and is fed from a 0.9 V DC supply, drawing less than 10 mW of power consumption. Comparisons with similar works available in literature prove the proposed circuit is very competitive with state-of-the-art LNAs and achieves a remarkable performance when compared to commercially available GaAs LNAs. To obtain such results, the complete design procedure is presented including the best floating body device combination, optimal current density selection, device sizing, impedance matching selection and the most relevant aspects of the circuit layout.

Some of the future lines of work derived from this work include the following:

- Introducing RC feedback to transform the narrow-band operation of the LNA into a wideband response.
- Modification of the drain inductor into an LRC tank to improve circuit bandwidth.
- Introduction of the body-bias technique to reduce the LNA DC supply voltage and, hence, reduce power consumption.
- Introduction of the bulk-driven technique to improve LNA linearity.
- Combine body-bias and bulk-driven techniques to reduce power consumption and compensate the linearity reduction of the LNA.

Resumen en Español

El estudio de LNAs de altas prestaciones a frecuencias de MW se traslada de compuestos III-V a una tecnología SOI para reducir costes, área y consumo de potencia, presentando resultados de medida de un LNA en cascodo para la banda Ku con una NF medida de 3.0 dB. Cabe destacar que los costes de fabricación del circuito fueron esponsorizados por el programa University Partner Program de GlobalFoundries. En este trabajo se presentan los resultados de diseño y medidas de un LNA en cascodo para la banda Ku alimentado a 0.9 V. El LNA ocupa 0.14 mm2 y logra un rendimiento comparable al LNA de GaAs previamente desarrollado con tecnología de UMS, con ahorros significativos en consumo de energía y área. Se demuestra la viabilidad de lograr un LNA de 3 dB de NF en tecnología 45RFSOI con una ganancia de hasta 12.9 dB en una topología de cascodo de una sola etapa. Las medidas demuestran que el LNA opera en la banda de frecuencias de 20 GHz, alcanzando una NF de 3.0 a 3.2 dB, con IRL y ORL superiores a 10 en toda la banda y un IIP3 destacable de 5 dBm. Asimismo, el

circuito consume un total de 9 mW de energía. La comparativa con trabajos similares de la literatura científica demuestra que el circuito propuesto es muy competitivo con los LNAs del estado del arte y logra un rendimiento elevado si se compara con los LNAs de GaAs disponibles. Para obtener tales resultados, se estudian en profundidad los dispositivos activos más adecuados tras probar diferentes combinaciones, encontrando la densidad de corriente óptima para mínimo ruido a la frecuencia de interés, al igual que las dimensiones y las impedancias óptimas. Tras discutir los aspectos más relevantes del diseño del circuito, se realiza un análisis EM completo de todos los componentes del LNA.